Control and Status Register

CSR

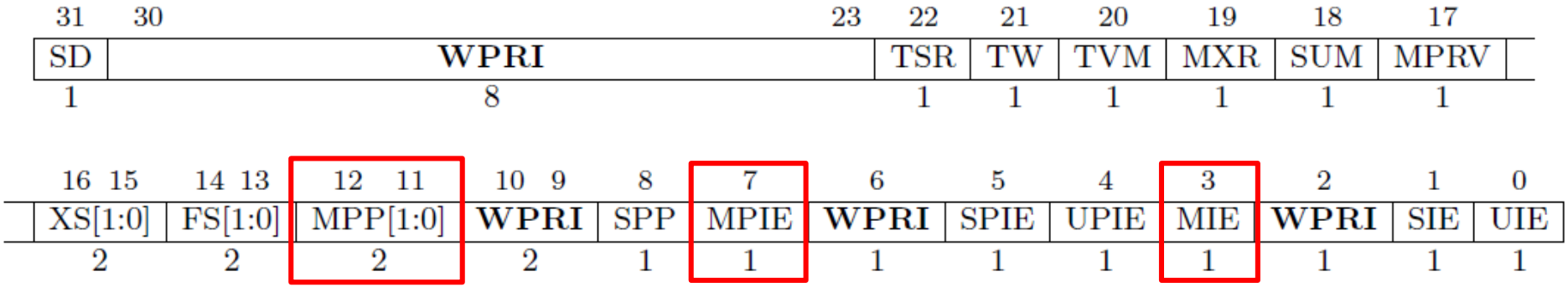
- Three level
  - User-level
  - Supervisor-level
  - Machine-level

Address	Privilege	Name	Description
0x300	M	mstatus	Machine status register
0x304	M	mie	Machine interrupt-enable register
0x305	M	mtvec	Machine Trap-Vector Base-Address register
0x341	M	mepc	Machine exception program counter
0x344	M	mip	Machine interrupt pending register

Table 1-4: CSR in machine-level

CSR - mstatus

- Machine status register
- Keep track of and controls the current operating state.

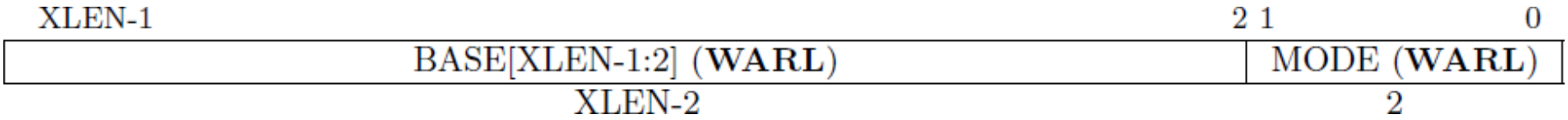


- MIE: Global Interrupt-enable bits
- MPIE: Holds the value of the interrupt-enable bit active prior to the trap
- MPP: Holds the previous privilege mode
- Other bits can hardwire to 0
- MIE will be written by instruction initially
- WFI should be unaffected by MIE

- When interrupt is taken
  - MPIE <= MIE
  - MIE <= 0
  - MPP <= 2'b11(machine mode)
- When interrupt is return
  - MPIE <= 1
  - MIE <= MPIE
  - MPP <= 2'b11(machine mode)

CSR - mtvec

- Machine Trap-Vector Base-Address Register
- Store the address where ISR start(Trap)



- Mode
  - 0: Direct: The pc to be set to the address in the BASE field.
  - 1: Vectored: The pc to be set to the address in the BASE field plus 4*the interrupt cause number
- In this homework, only implement the Direct mode, so
  - PC <= { mtvec[31:2],2'b00 }
- mtvec is hardwire to 0x0001_0000
  - The address where the trap is set.

CSR – mip & mie

Machine Interrupt Registers

mip: Machine interrupt-pending register

XLEN-1 12	11	10	9	8	7	6	5	4	3	2	1	0
WIRI	MEIP	**WIRI**	SEIP	UEIP	MTIP	**WIRI**	STIP	UTIP	MSIP	**WIRI**	SSIP	USIP
XLEN-12	1	1	1	1	1	1	1	1	1	1	1	1

- MEIP/MTIP: Indicates a machine-mode external/timer interrupt is pending
  - Connect to the external/timer interrupt signal
  - Need check MEIE/MTIE value
- Other bits hardwire to 0

mie: Machine interrupt-enable register

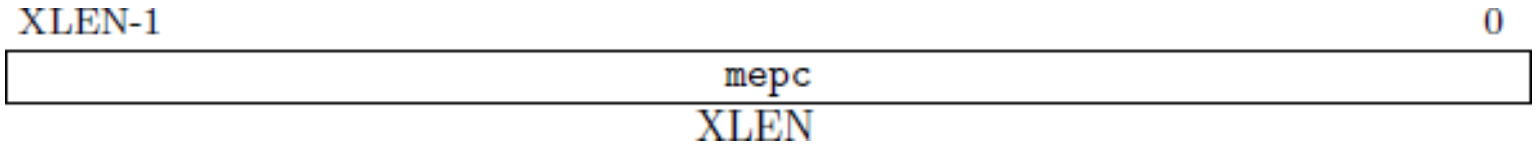
XLEN-1 12	11	10	9	8	7	6	5	4	3	2	1	0
WPRI	MEIE	**WPRI**	SEIE	UEIE	MTIE	**WPRI**	STIE	UTIE	MSIE	**WPRI**	SSIE	USIE
XLEN-12	1	1	1	1	1	1	1	1	1	1	1	1

- MEIE/MTIE: External/timer interrupt enable
  - MEIE is set by CSR instructions
- Other bits hardwire to 0

- WFI shouldn't ignore the MEIE/MTIE

CSR - mepc

Machine Exception Program Counter

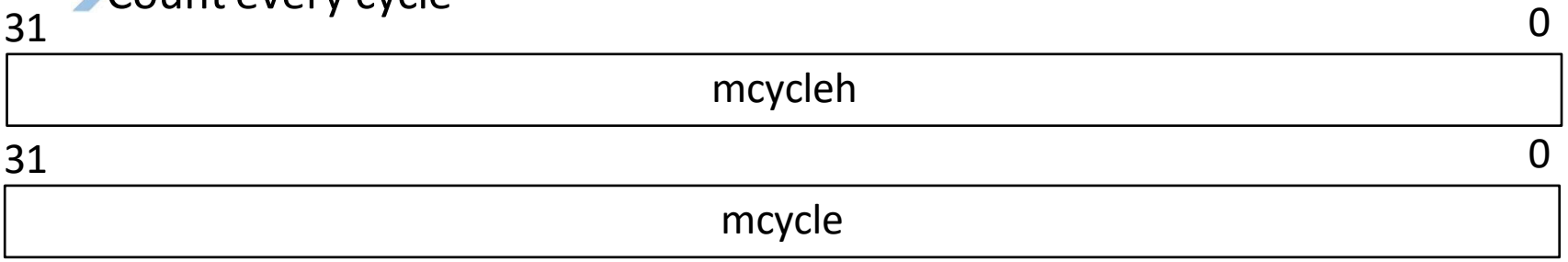


- When interrupt is taken
  - If the interrupt is taken when WFI is currently executed, store the following instruction
    - mepc <= pc+4
  - Otherwise, store the address of the instruction that encountered the interrupt
    - mepc <= pc
- When interrupt return
  - pc <= mepc

CSR – Hardware Performance Monitor

mcycleh & mcycle

- Holds the number of cycles that hardware has executed
- Divide **64-bit mcycle** into mcycleh and mcycle
- Count every cycle



minstreth & minstret

- Holds the number of instructions that CPU has completed
- Divide **64-bit minstret** into minstreth and minstret
- Count when instruction retired