ARM ISA

Friday, March 23, 2018 3:27 AM

1. **LDUR**
   I. Instruction - D Format

00111000010 (11)	9bit-Addr	00	5bit-BaseReg#	5bit-Reg#

   II. Action: RegFile[Reg#] <= DM[9bit-Addr + RegFile[BaseReg#]]
2. **STUR**
   I. Instruction - D Format

00111000000 (11)	9bit-Addr	00	5bit-BaseReg#	5bit-Reg#

   II. Action: DM[9bit-Addr + RegFile[BaseReg#]] <= RegFile[Reg#]
3. **ADD**
   I. Instruction - R Format

10001011000 (11)	5bit-Reg1#	000000	5bit-Reg2#	5bit-DestReg#

   II. Action: RegFile[DestReg#] <= RegFile[Reg1] + RegFile[Reg2]
4. **ADDI**
   I. Instruction - I Format

1001000100 (10)	12bit-Immed#	5bit-Reg1#	5bit-DestReg#

   II. Action: RegFile[DestReg#] <= RegFile[Reg1] + Immed#
5. **SUB**
   I. Instruction - R Format

11001011000 (11)	5bit-Reg1#	000000	5bit-Reg2#	5bit-DestReg#

   II. Action: RegFile[DestReg#] <= RegFile[Reg1] - RegFile[Reg2]
6. **AND**
   I. Instruction - R Format

10001010000 (11)	5bit-Reg1#	000000	5bit-Reg2#	5bit-DestReg#

   II. Action: RegFile[DestReg#] <= RegFile[Reg1] & RegFile[Reg2]
7. **ORR**
   I. Instruction - R Format

10101010000 (11)	5bit-Reg1#	000000	5bit-Reg2#	5bit-DestReg#

   II. Action: RegFile[DestReg#] <= RegFile[Reg1] | RegFile[Reg2]
8. **CBZ**
   I. Instruction - CB Format

10110100 (8)	19-bitAddr	5bit-CheckReg#

   II. Action: PC <= (RegFile[CheckReg#]) ? PC+4 : PC+Addr
9. **CBNZ**
   I. Instruction - CB Format

10110101 (8)	19-bitAddr	5bit-CheckReg#

   II. Action: PC <= (RegFile[CheckReg#]) ? PC+Addr : PC+4
10. **B**
   I. Instruction - B Format

000101 (6)	26bit-Addr

   II. Action: PC <= PC+Addr
11. **TRAP**
   I. Instruction - TRAP Format

11111111111 (11)	00000000000000000000

   II. Action: Halt (End Program/ Stop Machine)