CHAPTER 4: MEMORY SYSTEM ARCHITECTURE

1. Explain **FOUR (4)** types of memory access method. Give **ONE (1)** example for each of the access method.

   a) Sequential access
   -Memory is organized into units of data called records. Access must be made in a specific linear sequence. Access time is variable.
   -Magnetic tapes

   b) Direct access
   -Involves a shared read-write mechanism. Individual blocks or records have a unique address based on physical location. Access time is variable.
   -Magnetic disks

   c) Random access
   -Each addressable location in memory has a unique, physically wired-in addressing mechanism. The time to access a given location is independent of the sequence of prior accesses and is constant. -Main memory and some cache systems

   d) Associative
   -A word is retrieved based on a portion of its contents rather than its address. Each location has its own addressing mechanism and retrieval time is constant independent of location or prior access patterns.
   -Cache memories

2. Differentiate between Dynamic RAM (DRAM) and Static RAM (SRAM).

Dynamic RAM (DRAM)	**Static RAM (SRAM)**
Made with cells that store data as charge on capacitors	Digital device that uses the same logic elements used in the processor
Presence or absence of charge in a capacitor is interpreted as a binary 1 or 0	Binary values are stored using traditional flip-flop logic gate configurations
Requires periodic charge refreshing to maintain data storage	Will hold its data as long as power is supplied to it

3. Once the cache has been filled, when a new block is brought into the cache, one of the existing blocks must be replaced. List and explain **THREE (3)** most common replacement algorithms.

- Least recently used (LRU) Replace that block in the set that has been in the cache longest with no reference to it.

- First-in-first-out (FIFO) Replace that block in the set that has been in the cache longest.

- Least frequently used (LFU) Replace that block in the set that has experienced the fewest references.

4. Levels of Redundant Array of Independent Disks (RAID) do not imply a hierarchical relationship but designate different design architectures that share three common characteristics. State the **THREE (3)** common characteristics of RAID scheme.

- Set of physical disk drives viewed by the operating system as a single logical drive.
- Data is distributed across the physical drives of an array in a scheme known as striping.
- Redundant disk capacity is used to store parity information, which guarantees data recoverability in case of a disk failure.

5. A computer system has a memory architecture made up of a main memory of **1024 MB** and a cache of **320 KB**. In order to perform an efficient mapping function, the main memory is arranged in block of **16 bytes**. Draw the address structure for the different mapping functions as below (Indicate the fields and the number of bits required for each field.)

(a) Direct Mapping
(b) Associative Mapping
(c) Two-Way Set Associative Mapping

a) Main memory : 1024 MB =2^30 = 30 bits of address length
Cache : 320 kb / 16b = 20k = 2 ^15 = 15 bits of line
Block = 16b = 2^4 = 4 bits of word

Tag = 30 – 15 – 4 = 11

Line = 15
Word = 4

b) Main memory : 1024 MB =2^30 = 30 bits of address length
Block = 16b = 2^4 = 4 bits of word
Tag = 30 –4 = 26
Word = 4

c) Main memory : 1024 MB =2^30 = 30 bits of address length
Cache : 320 kb / 16b = 20k/2 = 10k = 2^14 = 14 bits
Block = 16B =2^4 = 4 bits of word
Tag = 30 – 14 -4 =12
Set : 14
Word : 4

6. A computer system has a memory architecture made up of a main memory of **450 MB** and a cache of **80 KB**. In order to perform an efficient mapping function, the main memory is arranged in block of **32 bytes**. Draw the address structure for the different mapping functions as below (Indicate the fields and the number of bits required for each field.)
   (a) Direct Mapping
   (b) Four-Way Set Associative Mapping

a) Main memory : 450 MB =2^29 = 29 bits of address length
Cache : 80 kb / 32b = 2.5k = 2 ^12 = 12bits of line
Block = 32b = 2^5 = 5 bits of word

Tag = 29 – 12 – 5 = 12
Line = 12
Word = 5

b) Main memory : 450 MB =2^29 = 29 bits of address length
Cache : 80 kb / 32b = 2.5k/4 = 0.625k = 2^10 =10bits of line
Block = 32b = 2^5 = 5 bits of word
Tag = 29 – 10- 5 = 14
Line = 30
Word = 5

7. A computer system has a memory architecture made up of a main memory of **40 MB** and a cache of **48 KB**. In order to perform an efficient mapping function, the main memory is arranged in block of **8 bytes**. Draw the address structure for the different mapping functions as below (Indicate the fields and the number of bits required for each field.)

   (a) Direct Mapping
   (b) Associative Mapping
   (c) Two-Way Set Associative Mapping

a) Main memory: 40 MB = 2^26 = 26 bits of address length Cache: 48kb / 8b = 6k = 2^13 = 13 bits of line Block 32b = 2^5 = 3 bits of word Tag: 26-13-3=10 Line: 13 Word: 3

b)
Main memory: 40 MB = 2^26 = 26 bits of address length Block 32b = 2^5 = 3 bits of word Tag: 26-3=23 Word: 3

c)
Main memory: 40 MB = 2^26 = 26 bits of address length Cache: 48kb / 8b = 6k/2 = 3k = 2^12 = 12 bits of set Block 32b = 2^5 = 3 bits of word Tag: 26-12-3=10 Line: 12 Word: 3

8. A computer system has a memory architecture made up of a main memory of **4 GB** and a

cache of **128 KB**. In order to perform an efficient mapping function, the main memory is arranged in block of **64 bytes**. Draw the address structure for the different mapping functions as below (Indicate the fields and the number of bits required for each field.)

   (a) Direct Mapping
   (b) Eight-Way Set Associative Mapping

(a) Direct Mapping Main memory: 4GB = 2^32 = 32 bits of address length Cache: 128KB / 64B = 2K = 2^11 = 11 bits of line Block: 64B = 2^6 = 6 bits of word Tag: 32 – 11 – 6 = 15 Line: 11 Word: 6

(b) Eight-Way Set Associative Mapping Main memory: 4GB = 2^32 = 32 bits of address length Cache: 128KB / 64B = 2K/8 = 0.25K = 2^8 = 8 bits of set Block: 64B = 2^6 = 6 bits of word Tag: 32 – 8 – 6 = 18 Set: 8 Word: 6

EXTRA QUESTION

1. A computer system has a memory architecture made up of a main memory of **9 GB** and a cache of **8192 KB**. In order to perform an efficient mapping function, the main memory is arranged in block of **1024 bytes**. Draw the address structure for the different mapping functions as below (Indicate the fields and the number of bits required for each field.)
   (a) Direct Mapping
   (b) Associative Mapping
   (c) Eight-Way Set Associative Mapping

(a) Direct Mapping Main memory : 9GB = 2^34 = 34 bits of address length ITECTURE Cache: 8192KB / 1024B = 8K = 2^13 = 13 bits of line Block: 1024B = 2^10 = 10 bits of word Tag: 34 – 13 – 10 = 11 Set: 13 Word: 10

(b) Associative Mapping Main memory: 9GB = 2^34 = 34 bits of address length Block: 1024B = 2^10 = 10 bits of word Tag: 34 – 10 = 24 Word: 10

(c) Eight-Way Set Associative Mapping Main memory: 9GB = 2^34 = 34 bits of address length Cache: 8192KB / 1024B = 8K/8 = 1k = 2^10 = 10 bits of set Block: 1024B = 2^10 = 10 bits of word Tag: 34 – 10 – 10 = 14 Set: 10 Word: 10