**实验3**

课程名称:数字逻辑

实验教学学时：

学时 ；

年级/班级： 6

分组学生人数： 2

专业：软件工程

姓名：汪良应

1. **实验目的**
2. This tutorial guides you through the design flow using Xilinx Vivado software to create a simple digital circuit using Verilog HDL. A typical design flow consists of creating model(s), creating user constraint file(s), creating a Vivado project, importing the created models, assigning created constraint file(s), optionally running behavioral simulation, synthesizing the design, implementing the design, generating the bitstream, and finally verifying the functionality in the hardware by downloading the generated bitstream file.
3. Verfying whether the code we design can work well.

**二、实验原理或预习内容**

（1）Operating the inputs logcially according to the digital circuit’s rules.The switch is one(true)when it is on and the LED is light when the output is one(right).We can observe the LEDs to test our circuit.

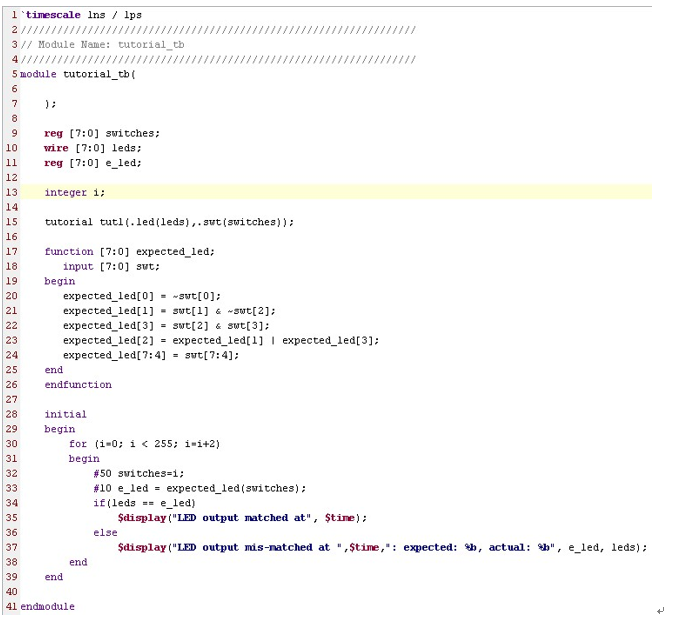
**三、实验环境**

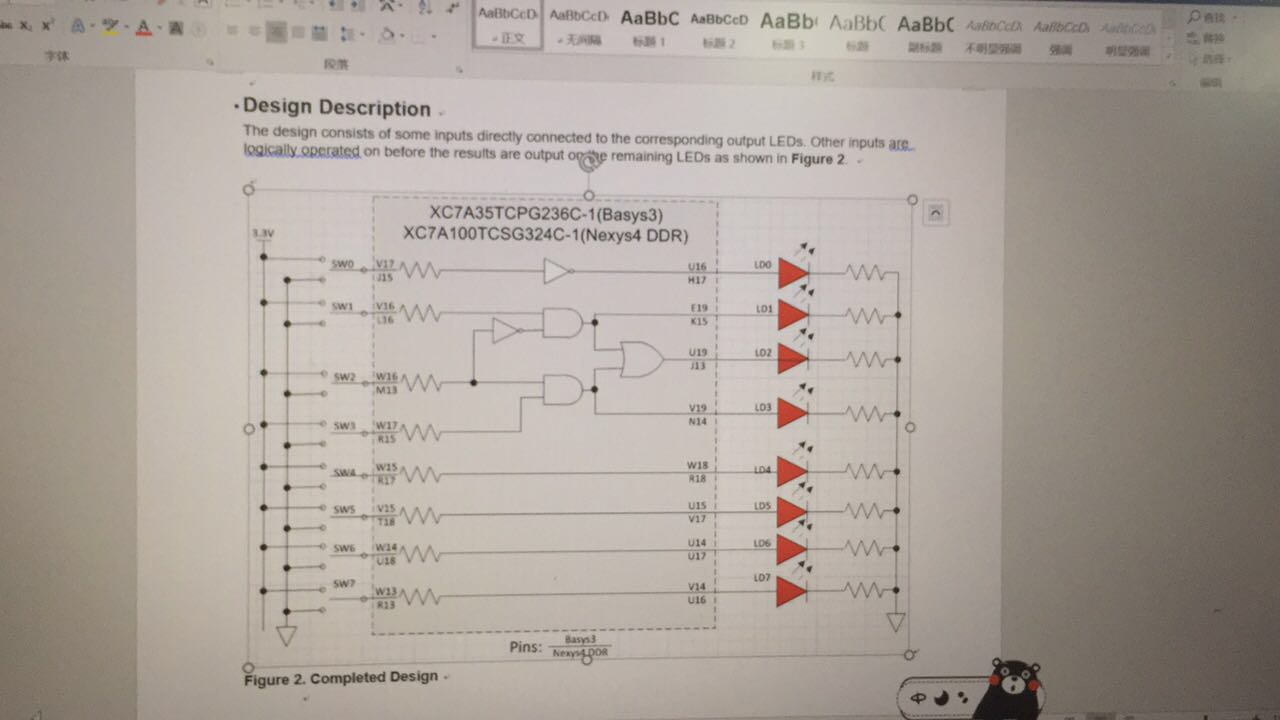
（1）Basys3 board

（2）Vivado

**四、实验内容**

**The following HDL code shows that it creat a logic circuit which is shown by another picture.**

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The truth tables are listed as follows.

SW0 LD0 SW1 SW2 SW3 LD1 LD2 LD3

**0 1**   **0 0 0 0 0 0**

**1 0**   **0 0 1 0 0 0**

**0 1 0 0 0 0**

**0 1 1 1 1 1**

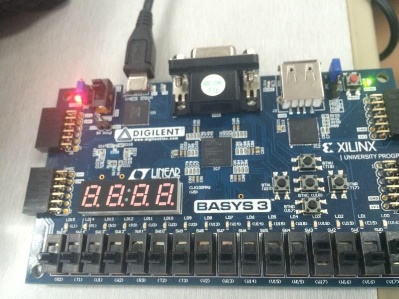
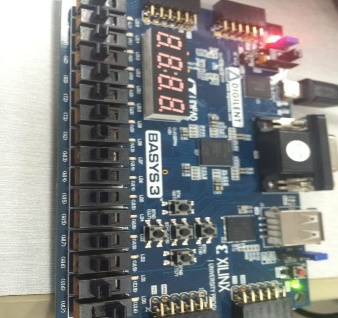
**1 0 0 1 1 0**

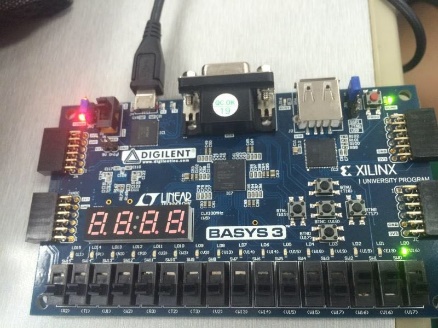
**1 0 1 1 1 0**

**1 1 0 0 0 0**

**1 1 1 0 1 1**

**The following pictures show us the outputs.**

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**五、实验结论及思考题**

（1）According to the outputs of Basys3 board,we can draw a conclusion that the code we designed is perfect and we have successed in creating a Vivado project targeting a specific FPGA device located on the Basys3 board,which revealed that The Vivado software tool can be used to perform a complete design flow.

（2）The perfect outputs show that the digital circuit we design can work well and we have successed in getting the right outputs.