NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2018-2019

EE6402 – REAL-TIME DSP DESIGN AND APPLICATIONS

November/December 2018 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 6 pages.
2. Answer all 5 questions.
3. All questions carry equal marks.
4. This is a closed-book examination.

---

1. (a) Consider an infinite precision signal $w(n)$ being truncated to the binary fixed point representation $[w(n)]$ in Q3.4 format.

   (i) What is the probability density function of the truncation error $e(n) = [w(n)] - w(n)$ in the above representation?

   (ii) What is the mean value (or, average value) of $e(n)$?

   (iii) How many bits are needed to represent a number in Q3.4 format?

   (iv) What is the dynamic range of Q3.4 format?

   (v) What is the precision of Q3.4 format?

   (11 Marks)

   (b) An input $x(n)$ passes through a bandpass filter with frequency response

$$H(e^{j\omega}) = \begin{cases} 1, & \frac{\pi}{4} \le |\omega| \le \frac{\pi}{2} \\ 0, & otherwise \end{cases}$$

   to give an output $y(n)$.

Note: Question No. 1 continues on page 2

The effect of finite precision representation of $x(n)$ is modelled as a noise $u(n)$ added to the input, such that the output is now $y(n) + v(n)$, as shown in Figure 1.

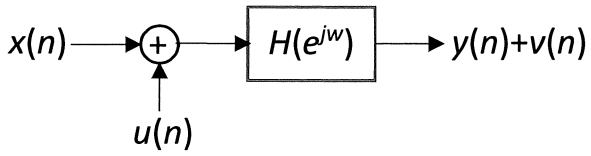

Figure 1

(i) If $u(n)$ has a mean (d.c.) value of $\eta_u = 0.01$, find η_v, the mean value of $v(n)$.

(ii) If $u(n)$ has a variance of $\sigma_u^2 = 4$, find σ_v^2, the variance of $v(n)$.

(iii) If $u(n)$ is white, find $S_v(\omega)$, the power spectrum density of $v(n)$.

(9 Marks)

2. (a) A recursive filter $y(n) = x(n) - 0.9y(n-1)$ is implemented as shown in Figure 2, where the processing times of the adder and the multiplier are shown in brackets.

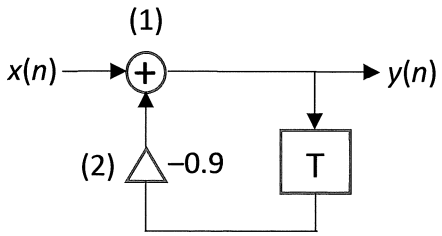

Figure 2

(i) What is the critical path of the above implementation?

(ii) In order to reduce the critical path, pipelining is used. The multiplier already has a latch. A latch is inserted at the adder as shown in Figure 3 on page 3, so that the feedback loop now has 2 latches. Express $y(n)$ using $y(n-2)$ instead of $y(n-1)$, and determine the multiplier value shown as '?' in Figure 3 on page 3.

(6 Marks)

Note: Question No. 2 continues on page 3

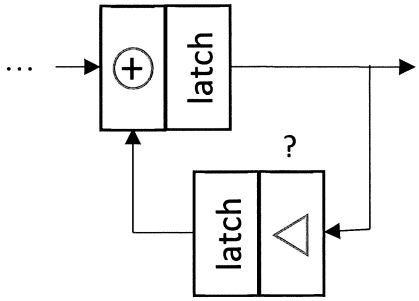

Figure 3

(b) (i) A ripple carry adder adds two 6-bit numbers. Draw a block diagram of this ripple carry adder using full adders.

(ii) Computation using a ripple carry adder takes a long time because of the carry propagation. If computation of each full adder requires 4 nano-seconds, explain how much computation time will be required by the 6-bit ripple carry adder in part (b)(i).

(iii) Explain how a carry select adder reduces the computation time in part (b)(ii). While reduced computation time is an advantage of carry select adder over ripple carry adder, does it have any disadvantage? Draw the block diagram of a 6-bit carry select adder by cascading 2 blocks of 3-bit adders.

(iv) Assume the computation time for each full adder is 4 nano-seconds. How much computation time is required for a 3-bit adder block used in your carry select adder of part (b)(iii)? Assume that each multiplexer introduces a computation delay of 2 nano-seconds. How much computation time is required by your carry select adder of part (b)(iii)?

(14 Marks)

3. (a) Pipelining and parallel processing are two popular techniques in VLSI. For each of the cases below, identify whether it is pipelining or parallel processing.

(i) The critical path is unchanged.

(ii) The critical path is reduced.

(iii) The hardware is replicated.

(iv) The latency is increased.

(4 Marks)

Note: Question No. 3 continues on page 4

(b) Describe the polyphase parallel FIR filter implementation for 2 polyphase components. The polyphase parallel FIR filter implementation increases the required number of multiply and add. What, then, is the advantage of the polyphase parallel FIR filter implementation?

(6 Marks)

(c) A bandlimited baseband signal is carrier modulated at frequency f_c. The bandwidth of the baseband signal is $\pm B/2$. Determine the sampled modulated signal spectrum if the sampling frequency is f_s. Hence, find the following:

(i) A suitable range of values for (f_s/B) in terms of R which would avoid aliasing, where R is given by $R = (2f_c + B)/2B$.

(ii) The lowest possible sampling frequency without spectral aliasing if $f_c = 16\ MHz$ and $B = 4\ MHz$.

(10 Marks)

4. (a) Obtain the input-output relationship for the discrete model of a 1st order $\Sigma - \Delta$ modulator shown in Figure 4. Extend the discrete model for a 2nd order $\Sigma - \Delta$ modulator and obtain its quantization noise power spectrum. Explain why the 2nd order modulator provides improved bit resolution in an Analog-to-Digital converter. The effect of over-sampling ratio (OSR) and the signal to quantization noise ratio (SQNR) should be noted in your answer.

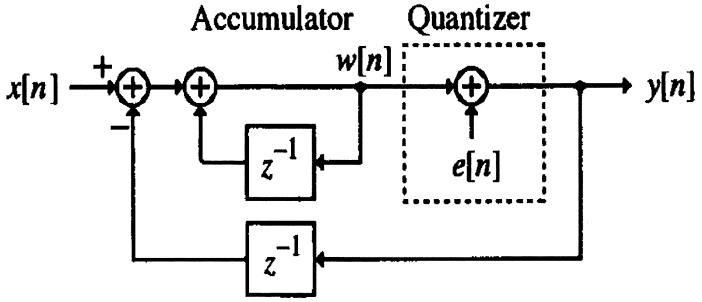

Figure 4

(7 Marks)

(b) A generic data computation unit of a Digital Signal Processor (DSP) is shown in Figure 5 on page 5. Explain why finite impulse response (FIR) filters can be efficiently implemented using this architecture.

Note: Question No. 4 continues on page 5

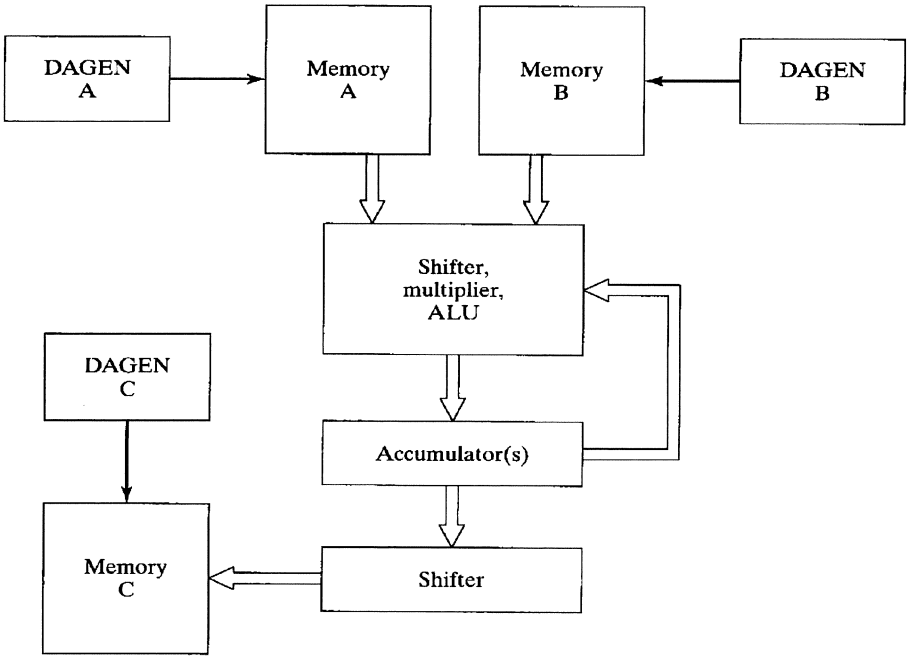

Figure 5

(6 Marks)

(c) An L-length finite impulse response (FIR) filter is implemented in block processing mode on a 120 MHz DSP. The sampling frequency is 1 MHz and the DSP requires $38 + N(L + 4)$ clock cycles to run the FIR filter routine, where N is the block size used in the processing. The real-time processing overheads require 20% of the sampling time. What would be the largest FIR filter length if the block size is 64 samples?

(7 Marks)

5. (a) Using a timing diagram, explain what happens during the following interrupt related operations of a Digital Signal Processor (DSP) operating in a real-time environment.

(i) Interrupt response
(ii) Interrupt service routine
(iii) Interrupt recovery
(iv) Task scheduling

(6 Marks)

(b) A finite impulse response (FIR) filter is implemented on a C54x DSP to process data using an input-output port. Explain the operation of the FIR filter program fragment shown in the following.

```
        STM     #coeff, AR1
        RPT     #15
        MVPD    #filco, *AR1+

        STM     #coeff, AR3
        STM     #dd, AR2
        STM     #yy, AR4

        STM     #16, BK
        STM     #1, AR0

loop:   RPTZ    A, #14
        MAC     *AR3+0%, *AR2+0%, A
        MAC     *AR3+0%, *AR2, A
        STH     A, *AR4+
        PORTR   adcport, *AR2
        B       loop
```

(8 Marks)

(c) Using the following instructions appropriately, modify the above program to perform block processing with a block size of 200.

```
STM     #num, BRC
RPTB    b_loop-1
MAR     *+ARn(#num)
```

(6 Marks)

END OF PAPER

EE6402 REAL-TIME DSP DESIGN & APPLICATIONS

Please read the following instructions carefully:

1. **Please do not turn over the question paper until you are told to do so. Disciplinary action may be taken against you if you do so.**

2. You are not allowed to leave the examination hall unless accompanied by an invigilator. You may raise your hand if you need to communicate with the invigilator.

3. Please write your Matriculation Number on the front of the answer book.

4. Please indicate clearly in the answer book (at the appropriate place) if you are continuing the answer to a question elsewhere in the book.