NANYANG TECHNOLOGICAL UNIVERSITY

SEMESTER 1 EXAMINATION 2015-2016

EE6402 – REAL-TIME DSP DESIGN AND APPLICATIONS

November/December 2015 Time Allowed: 3 hours

INSTRUCTIONS

1. This paper contains 5 questions and comprises 5 pages.
2. Answer **all** 5 questions.
3. All questions carry equal marks.
4. This is a closed-book examination.

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1. (a) A 3-tap transversal FIR filter has 8-bit positive coefficients given by $h(0) = 00010100$, $h(1) = 00001010$, $h(2) = 00100001$. The input signal $x(n)$ is also positive. Distributed arithmetic technique is used to perform the convolution.

(i) How many words of storage location are needed to store the table containing linear combinations of the coefficients?

(3 Marks)

(ii) Determine the value of the data stored in the table containing linear combinations of the coefficients.

(7 Marks)

(b) Let the N-bit numbers X and Y be given, respectively, by

$$X = x_1 2^{-1} + \ldots + x_{N-1} 2^{-N+1} + x_N 2^{-N}$$

and

$$Y = y_1 2^{-1} + \ldots + y_{N-1} 2^{-N+1} + y_N 2^{-N}$$

Note: Question No. 1 continues on page 2

where x_i and y_i are binary and have equal probabilities of being either 1 or 0. Figure 1 shows the process of multiplying X and Y producing P given by

$$P = r_1 2^{-1} + \ldots + r_{2N-1} 2^{-2N+1} + r_{2N} 2^{-2N}$$

where r_i for $N \geq i > 0$, is an integer given by

$$r_{N+i} = x_i y_N + x_{i+1} y_{N-1} + \ldots + x_{N-1} y_{i+1} + x_N y_i \quad .$$

Determine the expected value and variance of r_{N+i} for $N \geq i > 0$.

(10 Marks)

				x_1	x_2	x_3	⋯	x_N
			×	y_1	y_2	y_3	⋯	y_N
0	0	⋯	0	$x_1 y_N$	$x_2 y_N$	$x_3 y_N$	⋯	$x_N y_N$
0	0	⋯	$x_1 y_{N-1}$	$x_2 y_{N-1}$	$x_3 y_{N-1}$	$x_4 y_{N-1}$	⋯	0
0	0	⋯	$x_2 y_{N-2}$	$x_3 y_{N-2}$	$x_4 y_{N-2}$	$x_5 y_{N-2}$	⋯	0
⋯	⋯	⋯	⋯	⋯	⋯	⋯	⋯	⋯
0	0	⋯	$x_{N-4} y_4$	$x_{N-3} y_4$	$x_{N-2} y_4$	$x_{N-1} y_4$	⋯	0
0	0	⋯	$x_{N-3} y_3$	$x_{N-2} y_3$	$x_{N-1} y_3$	$x_N y_3$	⋯	0
0	0	⋯	$x_{N-2} y_2$	$x_{N-1} y_2$	$x_N y_2$	0	⋯	0
0	$x_1 y_1$	⋯	$x_{N-1} y_1$	$x_N y_1$	0	0	⋯	0
p_1	p_2	⋯	p_N	p_{N+1}	p_{N+2}	p_{N+3}	⋯	p_{2N}
		Column no.	N	$N+1$	$N+2$	$N+3$	⋯	$2N$
		Quantization Step size	Q	$2^{-1}Q$	$2^{-2}Q$	$2^{-3}Q$	⋯	$2^{-N}Q$

Figure 1

2. Let $H(z)$ denotes the z-transform transfer function of a linear phase FIR filter with length N and n^{th} impulse response $h(n)$, $0 \leq n \leq N-1$. Assume that N is even. In a given hardware implementation, the value of $h(n)$ is rounded to $[h(n)]$, $0 \leq n \leq N-1$, with quantization step size Q. The coefficient quantization error $e(n)$ is given by

$$e(n) = [h(n)] - h(n) \quad .$$

After rounding the coefficient values, its transfer function becomes $[H(z)]$. Let the frequency response deviation as a result of coefficient rounding be $E(e^{j\omega})$ given by

$$E(e^{j\omega}) = [H(e^{j\omega})] - H(e^{j\omega})$$

where $H(e^{j\omega})$ and $[H(e^{j\omega})]$ are the frequency responses of the filter before and after coefficient rounding, respectively.

Note: Question No. 2 continues on page 3

(a) Show that $E(e^{j\omega})$ can be expressed in the form

$$E(e^{j\omega}) = e^{-jP\omega} R(\omega)$$

where P is a real constant and $R(\omega)$ is a real trigonometric function.

Determine P and $R(\omega)$ in terms of $e(n)$.

(6 Marks)

(b) Determine an absolute bound for $|E(e^{j\omega})|$.

(4 Marks)

(c) Derive an expression for the expected value of $|E(e^{j\omega})|^2$.

(10 Marks)

3. (a) The recursive filter of Figure 2 is implemented using decimal arithmetic. The product after multiplication is rounded to the nearest integer. Explore its limit cycle oscillations. Explain how you can remove limit cycle oscillations.

(10 Marks)

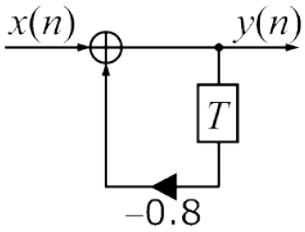

Figure 2

(b) The received bandpass signal of a communication system is given by $x(t) = A(t)Cos(2\pi f_0 t + \phi(t))$, where f_0 is the carrier frequency. The baseband signal is bandlimited to $\pm B/2$.

(i) Draw a block diagram to describe signal demodulation using inphase/quadrature (I/Q) sampling. Using analysis, the answer needs to clearly indicate how the sampled baseband signal is obtained.

(ii) Show the resulting spectra if the received signal is directly sampled using following 2 sampling frequencies: $f_{s1} = (2f_0 - B)/m$, $f_{s2} = (2f_0 + B)/(m+1)$, where m is a positive integer. Hence describe the procedure for obtaining the minimum bandpass sampling frequency without aliasing.

(10 Marks)

4. (a) (i) The analog voltage at the output of an *n*-bit Digital-to-Analog converter (DAC) is given by

$$V_o(a_{-1}2^{-1} + a_{-2}2^{-2} + \ .....+ \ a_{-n}2^{-n})$$

with a_{-n} denoting the n^{th} DAC bit value. What are the voltages corresponding to the maximum level, minimum level and the least-significant bit of the DAC?

(ii) Explain the difficulty in implementing the above DAC using analog components and show how a ($\Sigma - \Delta$) modulator architecture can be used to avoid these difficulties.

(6 Marks)

(b) Explain how a processor provides interrupt service through a vectored interrupt scheme as shown in Figure 3.

(7 Marks)

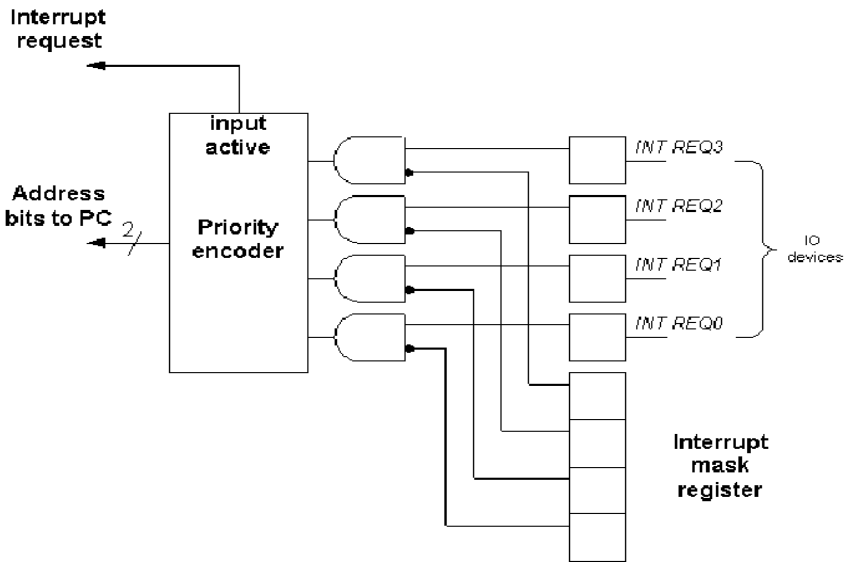

Figure 3

Note: Question No. 4 continues on page 5

(c) An *N*-length discrete Fourier transform (DFT) of a sequence $x(n)$ is given by

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-j2\pi kn/N} \qquad \text{for} \quad (k \leq 0 \leq N-1)\ .$$

Show that the above can be expressed as 2 (*N/2*)-length DFTs. Hence describe how the following codes would be useful in implementing a DFT in a digital signal processor.

```
STM   #aaddr, AR3          ;
STM   #baddr, AR2          ;
STM   #32, AR0             ;
RPT   #63                  ;
MVDD  *AR3+0B, *AR2+       ;
```

(7 Marks)

5. (a) Draw a diagram and explain why block processing using 'double buffering' is advantageous in real-time implementations.

(6 Marks)

(b) A 100-MIPS digital signal processor (DSP) implements an *L*-length finite impulse response (FIR) filter in block processing mode. The DSP requires $5 + B \times (L + 5)$ clocks to run the FIR filter where *B* is the block length. If the filter length is 64 and the block size is 256, determine the maximum possible sampling frequency for real-time implementation. Neglect the processing overheads.

(6 Marks)

(c) Explain how the C54x DSP architecture can be used to efficiently implement a symmetric FIR filter. Hence explain the following program fragment which uses the FIRS instruction to implement a symmetric even length FIR filter.

```
ADD     *AR3+, *AR2-, A
RPTZ    B,  #(L/2-1)
FIRS    *AR3+, *AR2-, #coeff
```

(8 Marks)

END OF PAPER