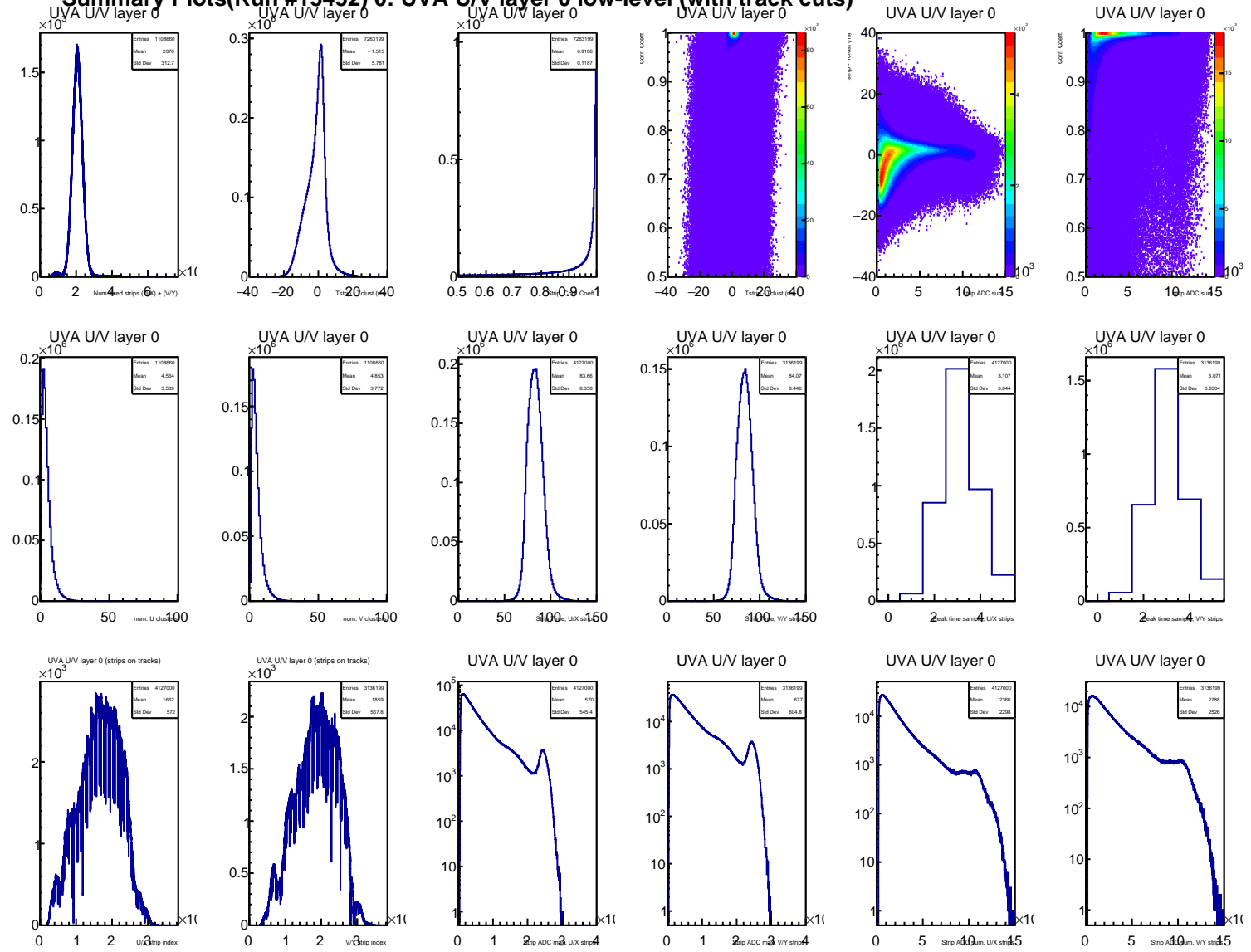
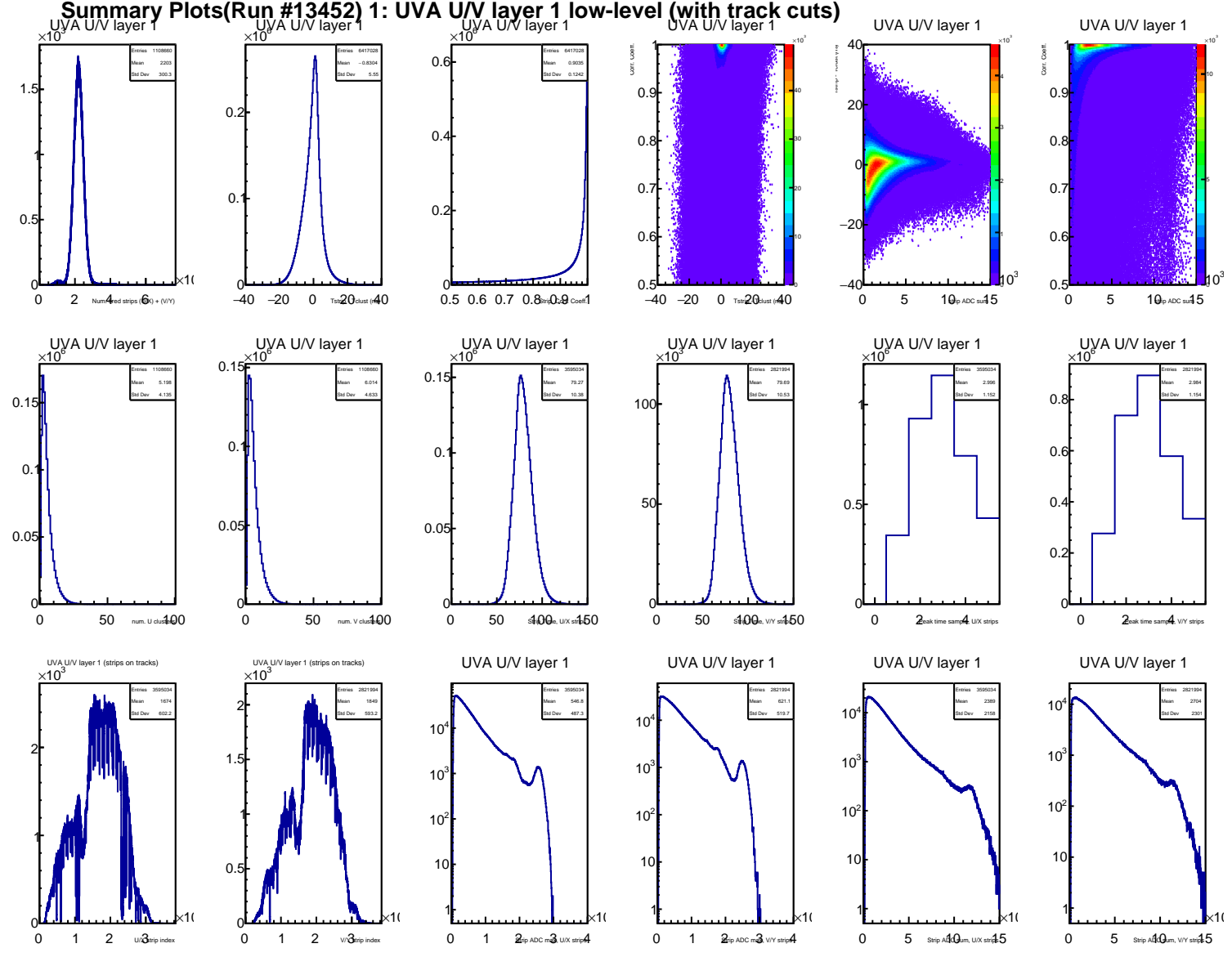


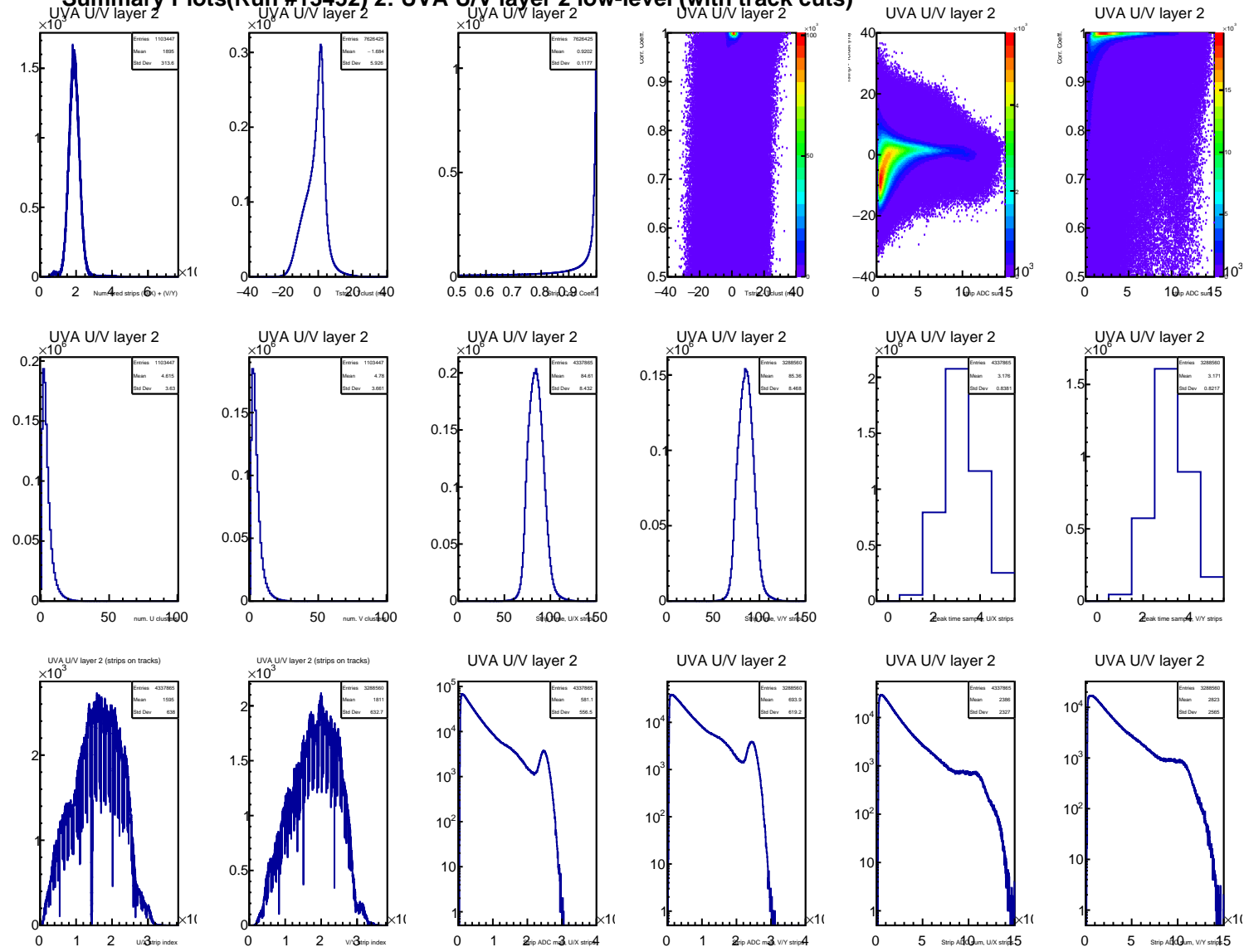
Summary Plots(Run #13452) 0: UVA U/V layer 0 low-level (with track cuts)



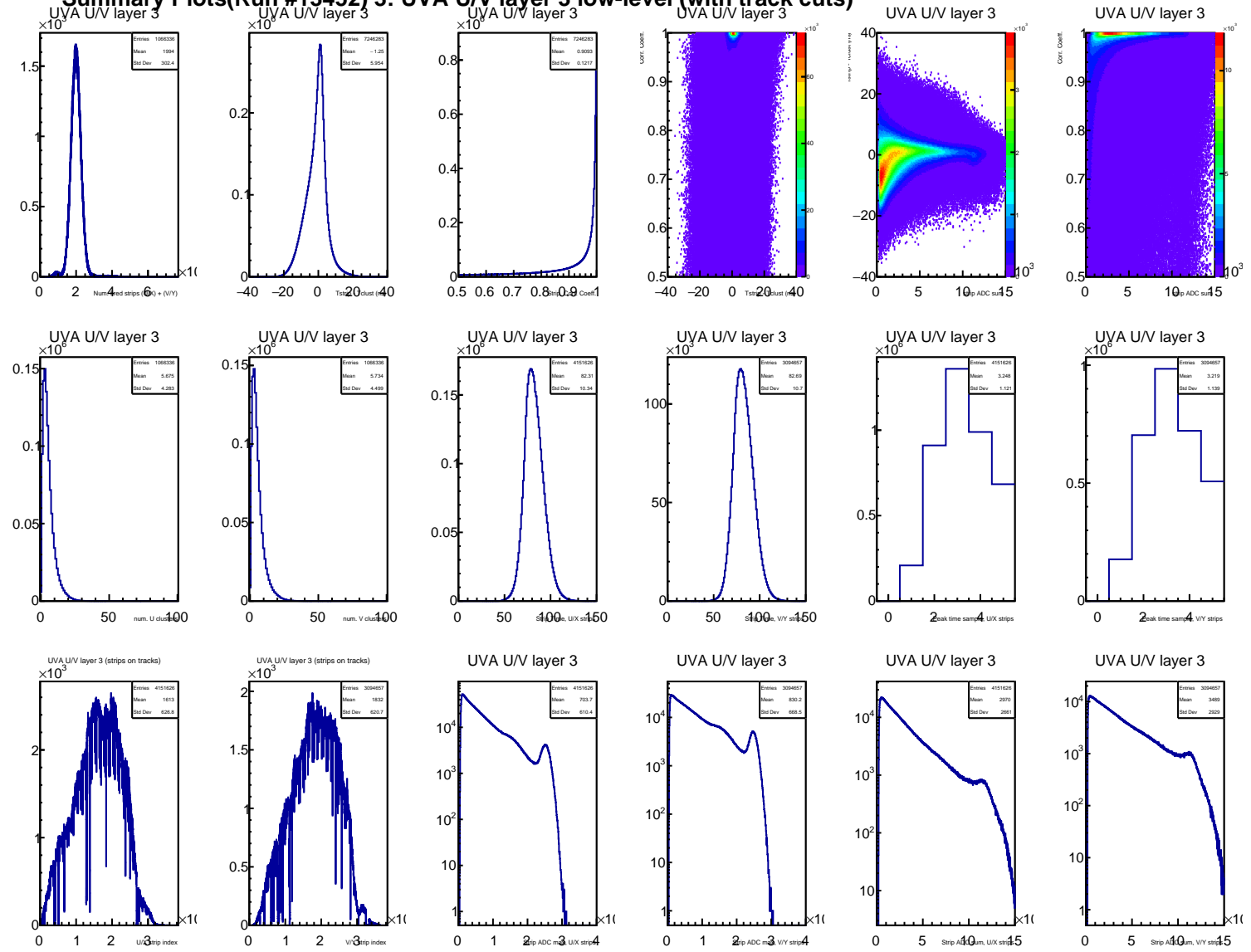
Summary Plots(Run #13452) 1: UVA U/V layer 1 low-level (with track cuts)



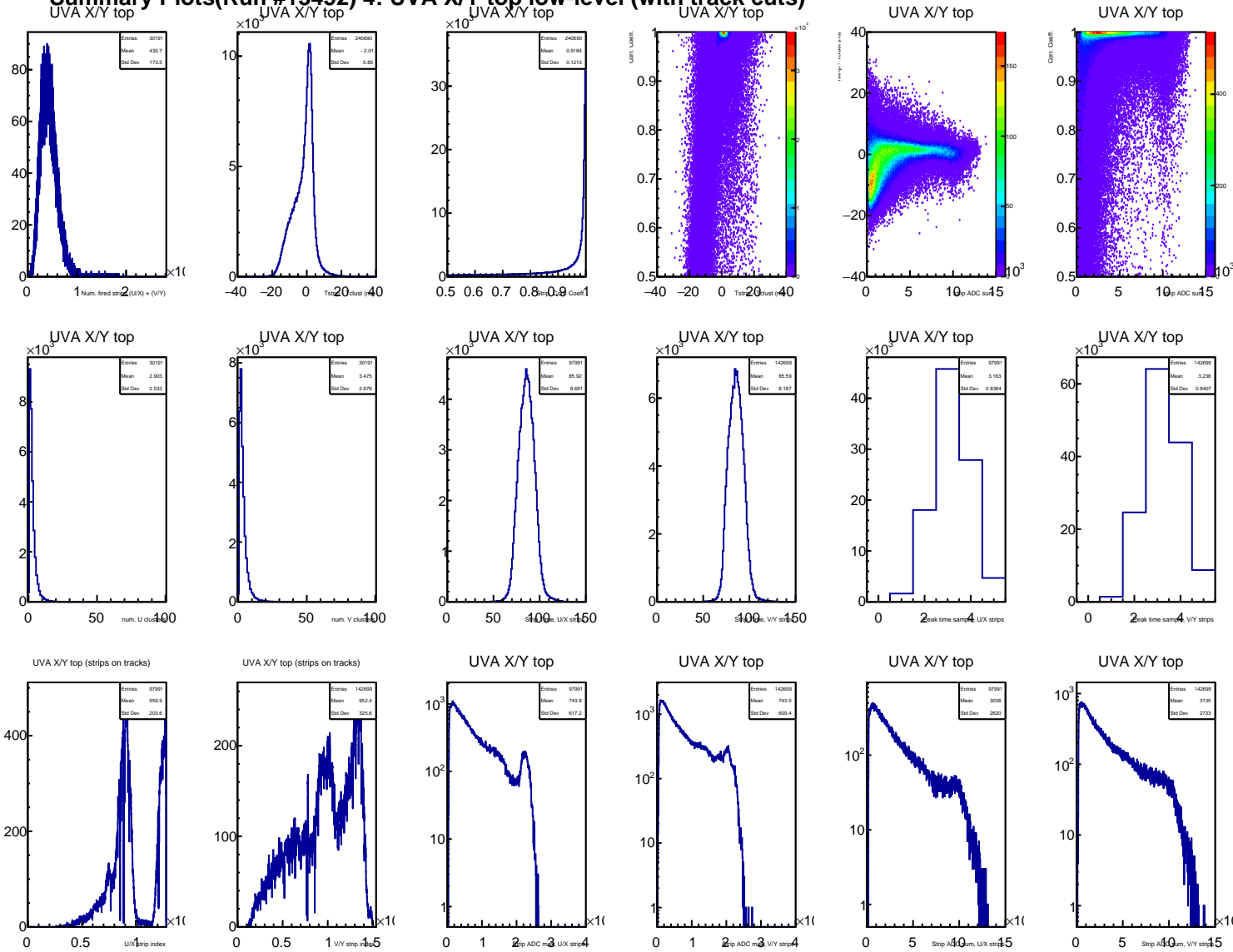
Summary Plots(Run #13452) 2: UVA U/V layer 2 low-level (with track cuts)



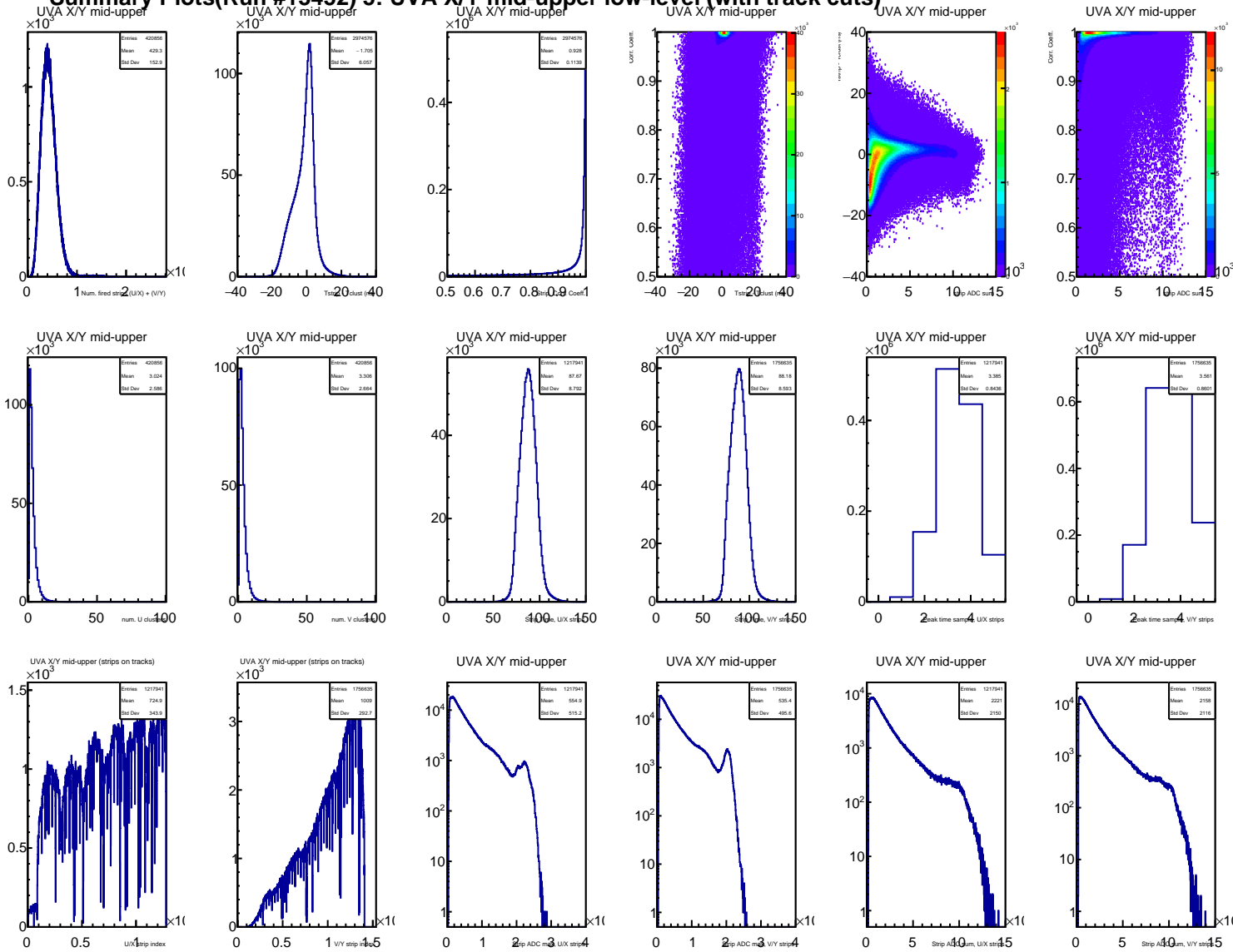
Summary Plots(Run #13452) 3: UVA U/V layer 3 low-level (with track cuts)



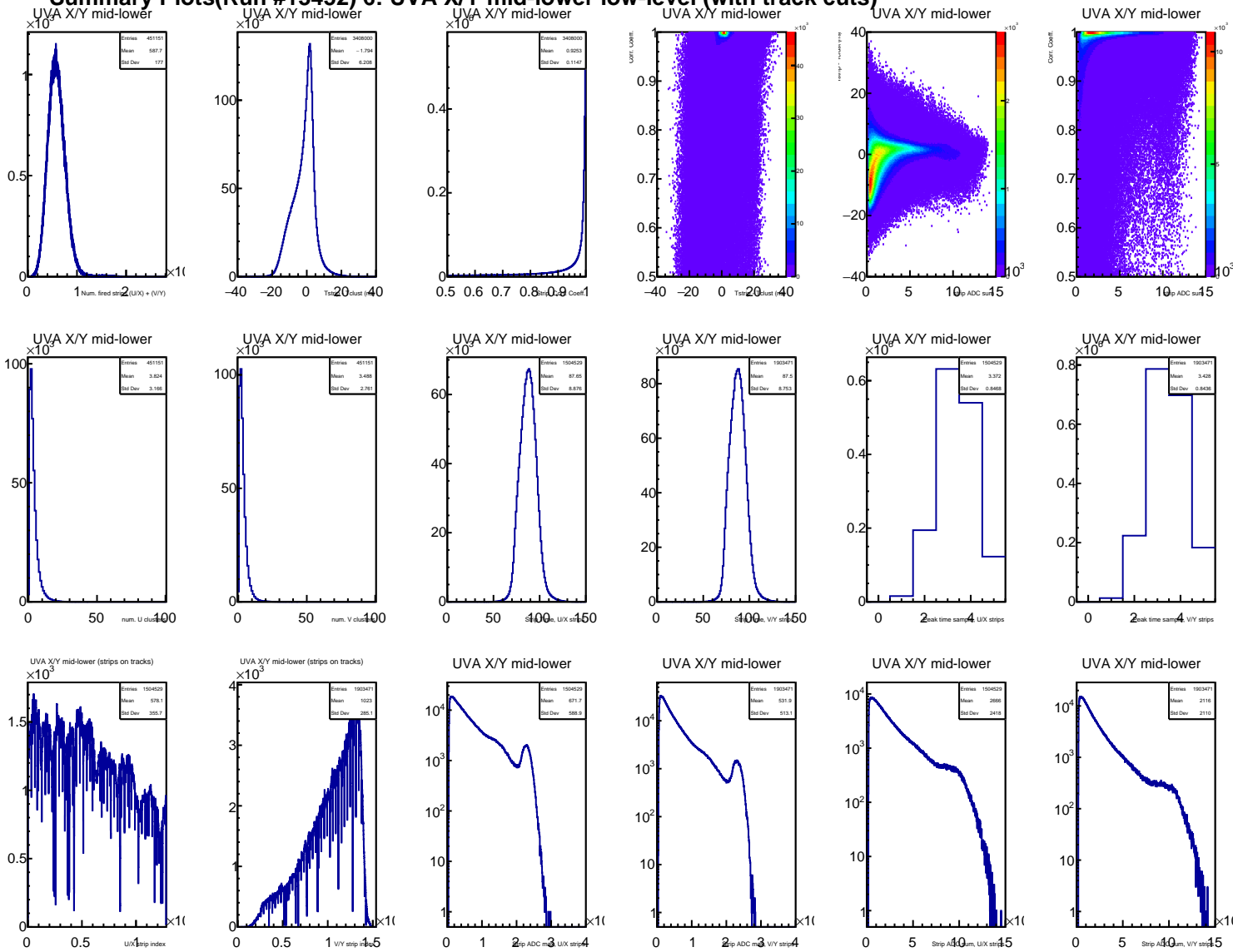
Summary Plots(Run #13452) 4: UVA X/Y top low-level (with track cuts)



Summary Plots(Run #13452) 5: UVA X/Y mid-upper (with track cuts)

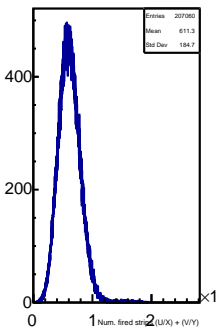


Summary Plots(Run #13452) 6: UVA X/Y mid-low-level (with track cuts)

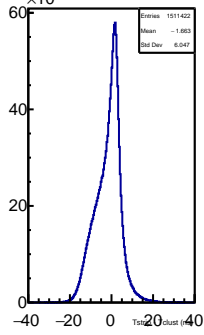


Summary Plots (Run #13452) 7: UVA X/Y bottom low-level (with track cuts)

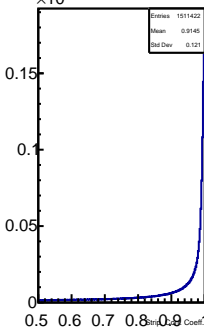
UVA X/Y bottom



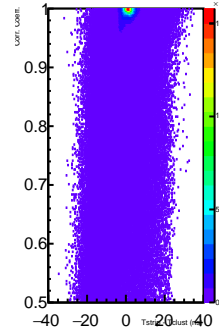
UVA X/Y bottom



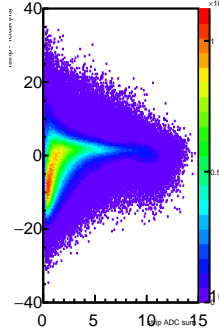
UVA X/Y bottom



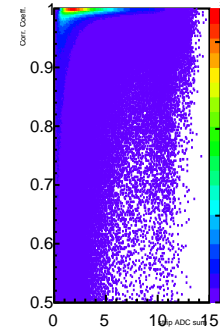
UVA X/Y bottom



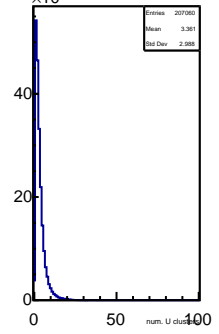
UVA X/Y bottom



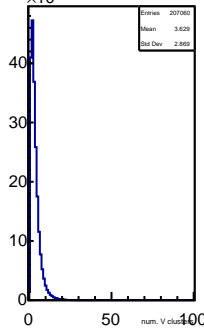
UVA X/Y bottom



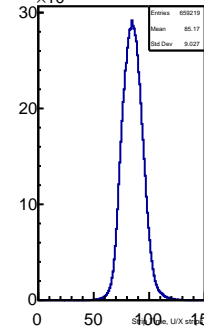
UVA X/Y bottom



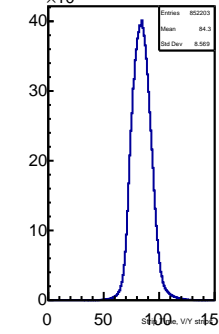
UVA X/Y bottom



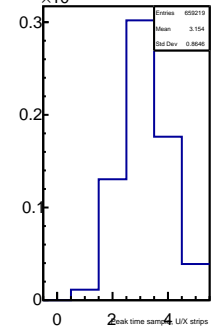
UVA X/Y bottom



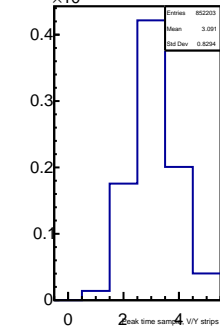
UVA X/Y bottom



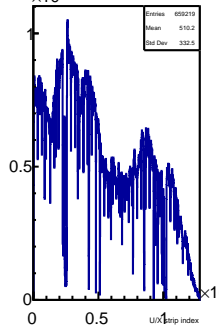
UVA X/Y bottom



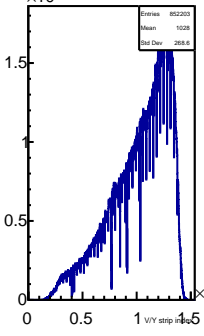
UVA X/Y bottom



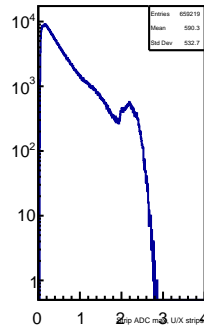
UVA X/Y bottom (strips on tracks)



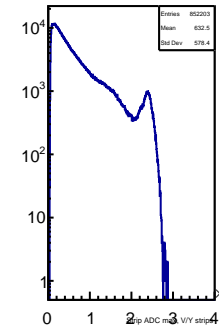
UVA X/Y bottom (strips on tracks)



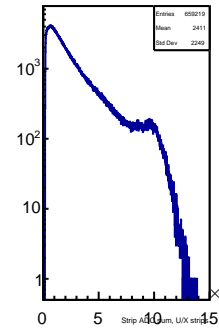
UVA X/Y bottom



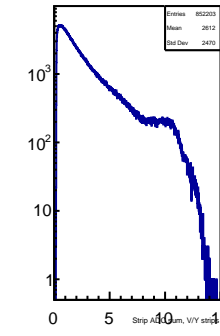
UVA X/Y bottom



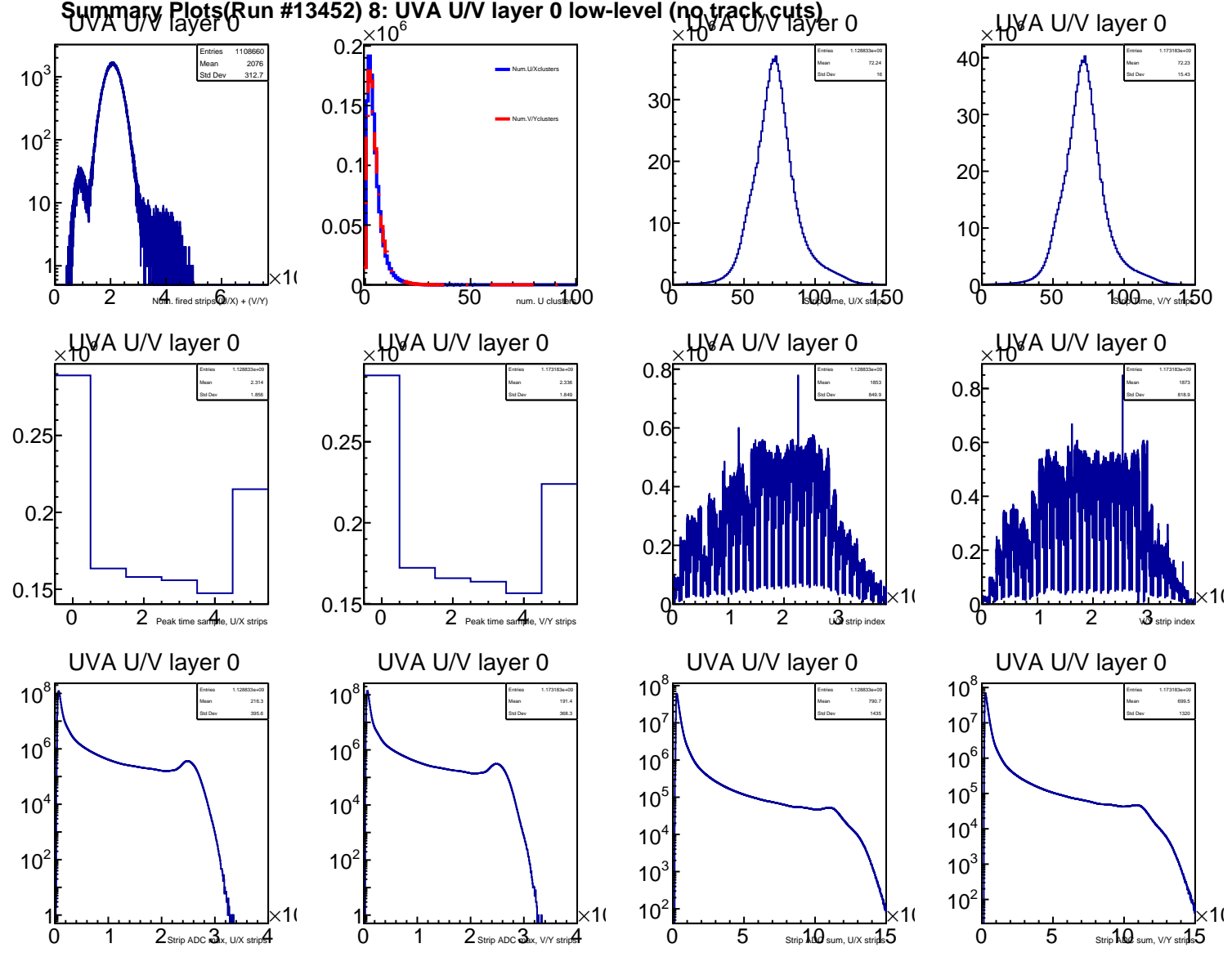
UVA X/Y bottom



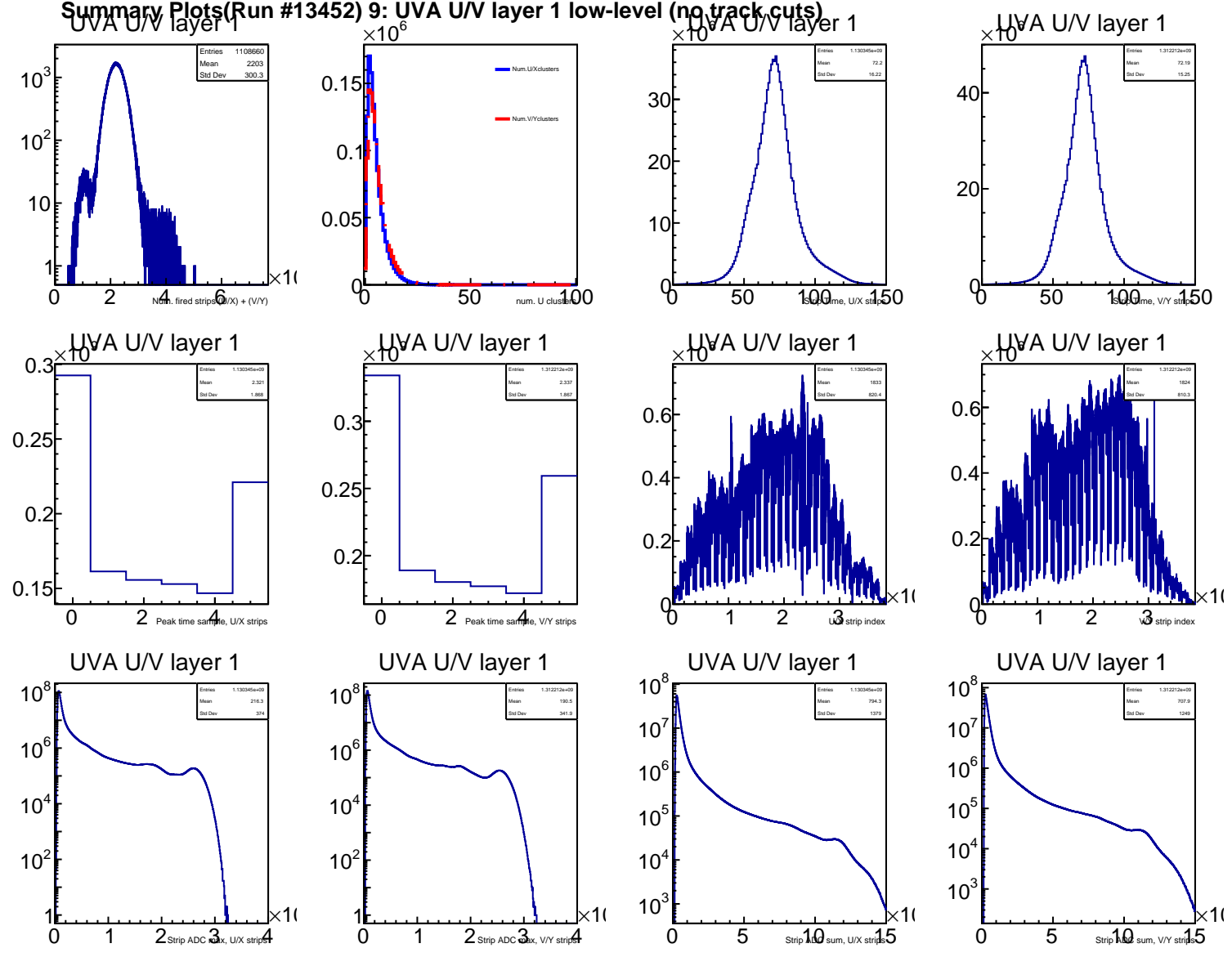
UVA X/Y bottom



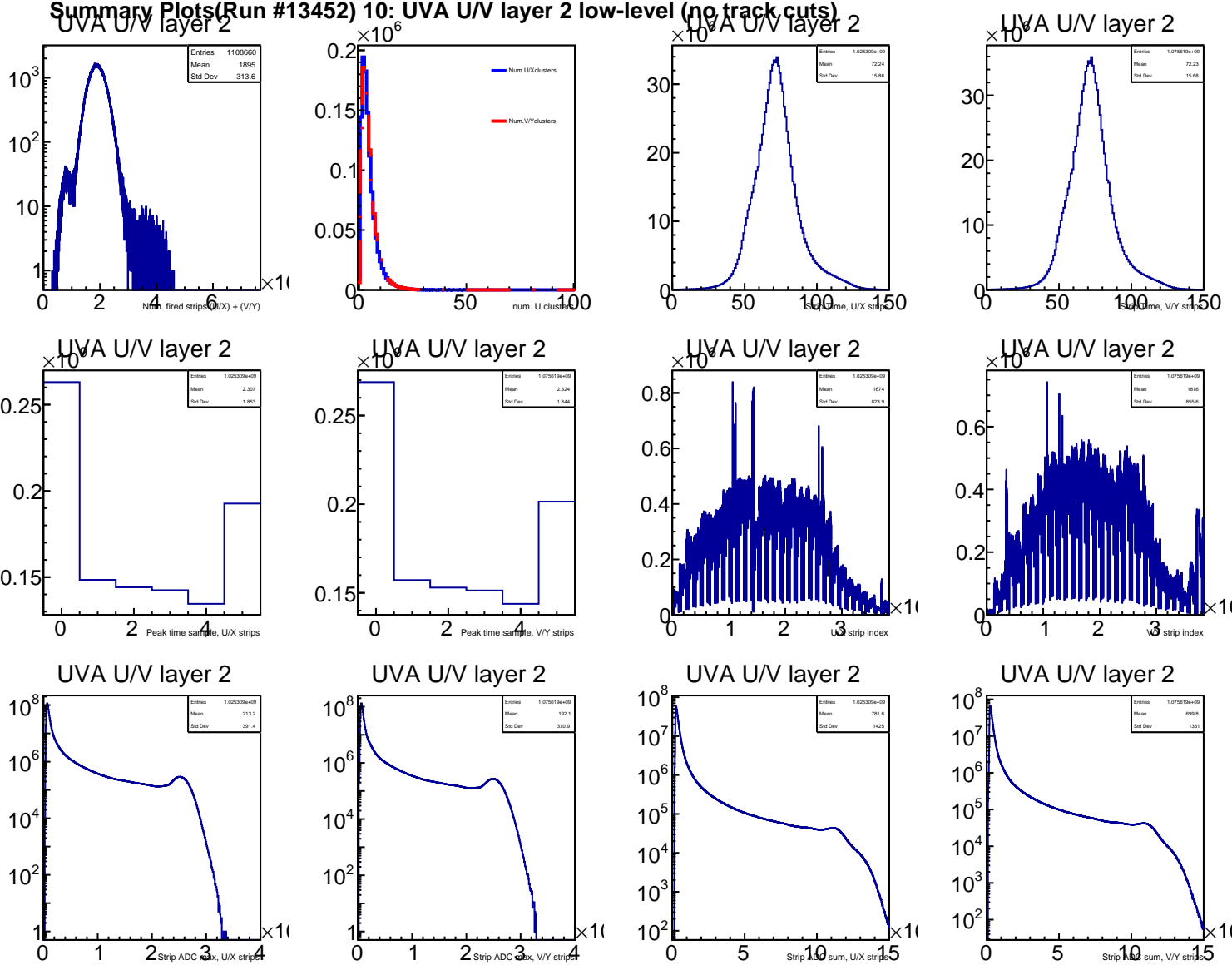
Summary Plots (Run #13452) 8: UVA U/V layer 0 low-level (no track cuts)



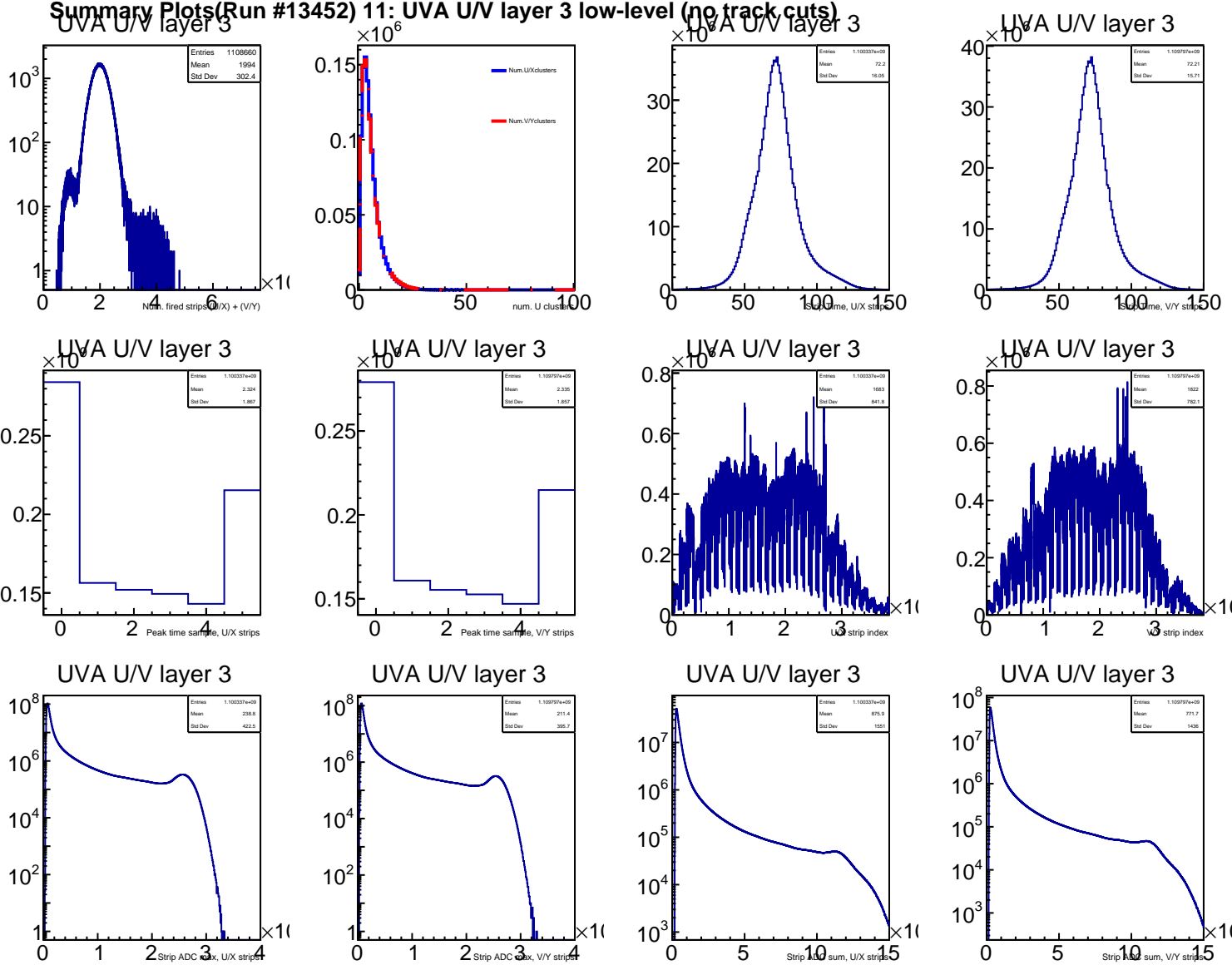
Summary Plots (Run #13452) 9: UVA U/V layer 1 low-level (no track cuts)



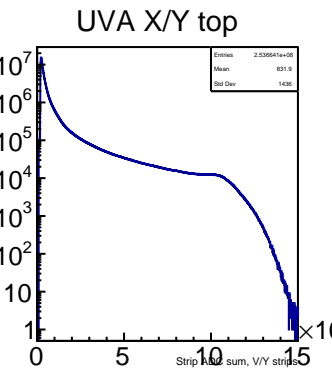
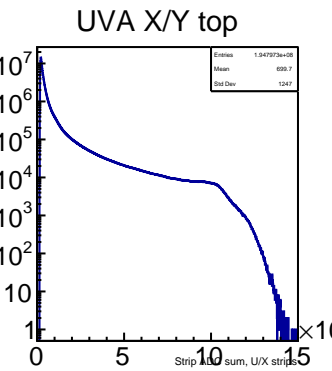
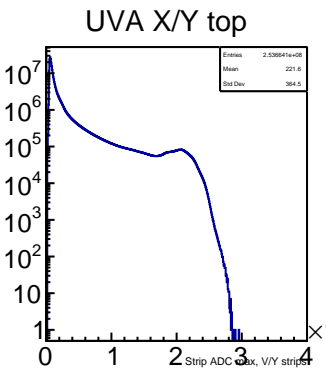
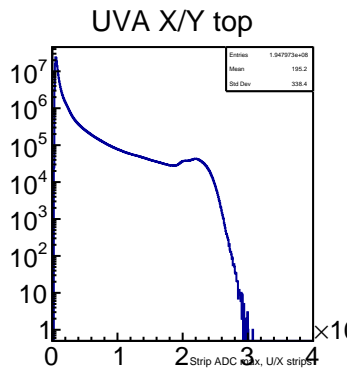
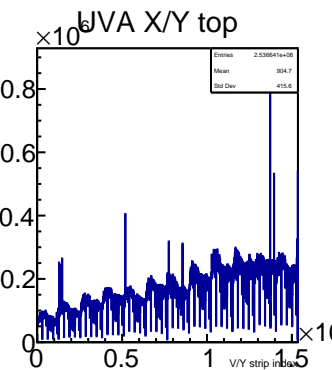
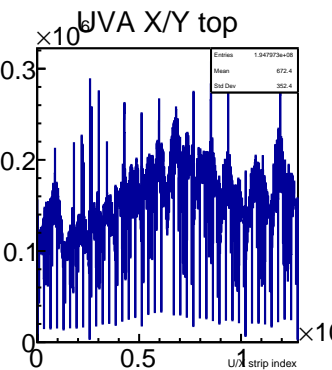
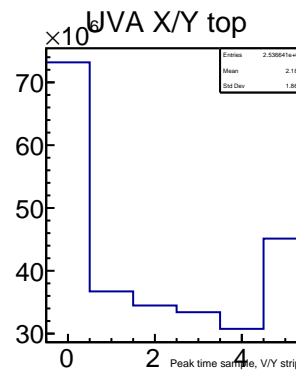
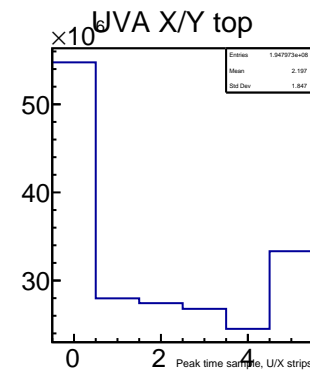
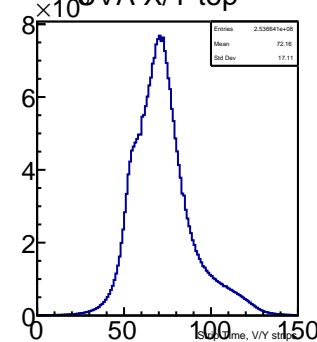
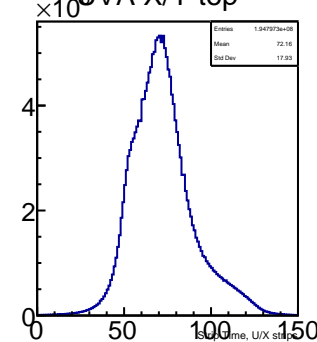
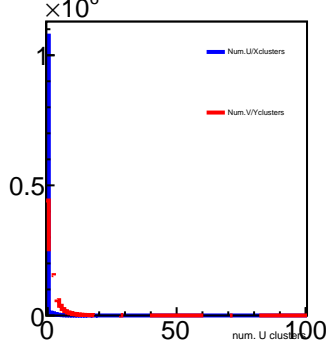
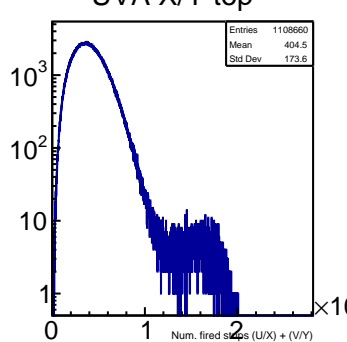
Summary Plots (Run #13452) 10: UVA U/V layer 2 low-level (no track cuts)



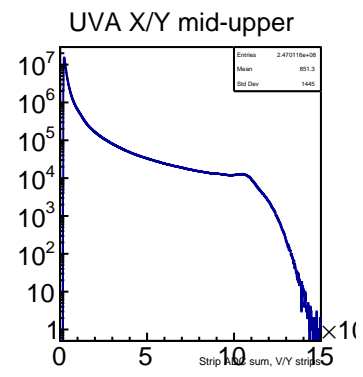
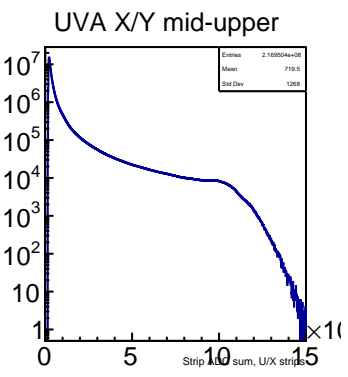
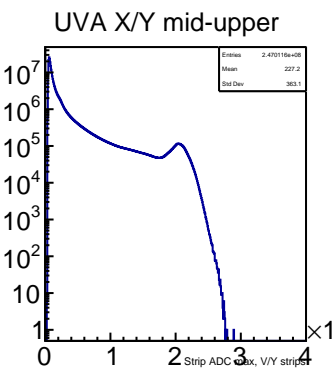
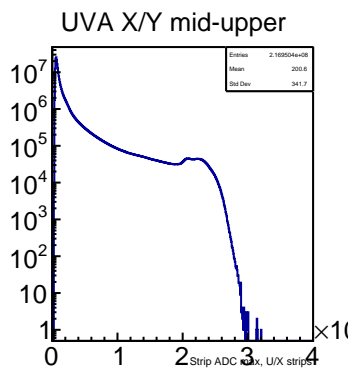
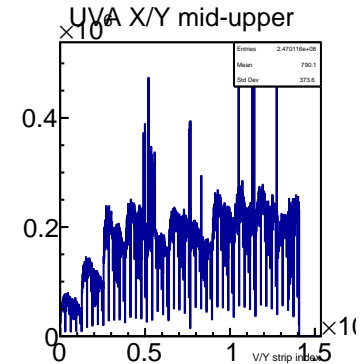
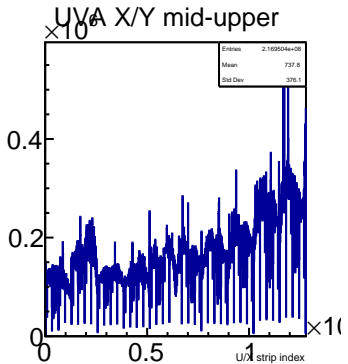
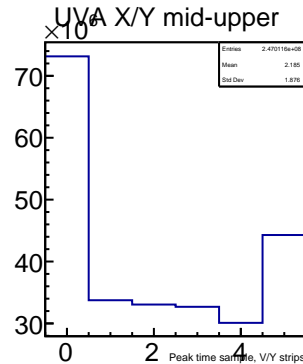
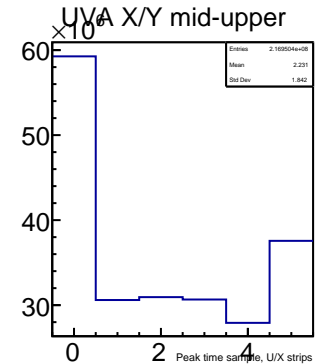
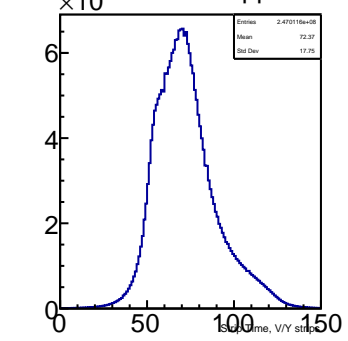
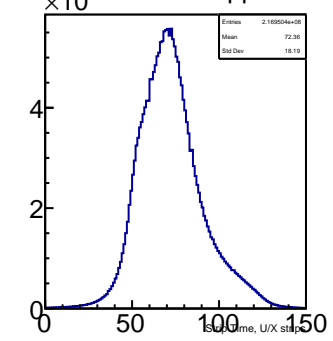
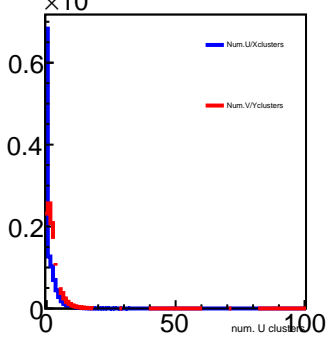
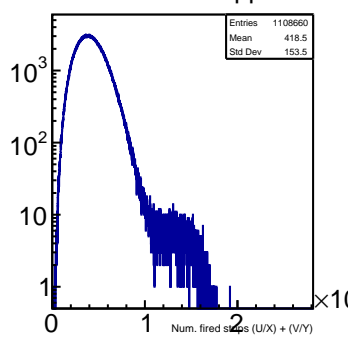
Summary Plots (Run #13452) 11: UVA U/V layer 3 low-level (no track cuts)



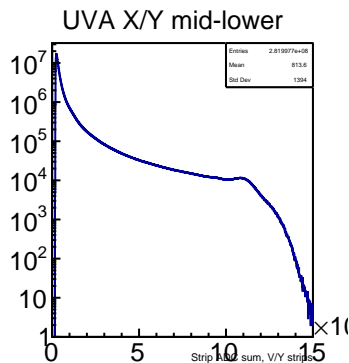
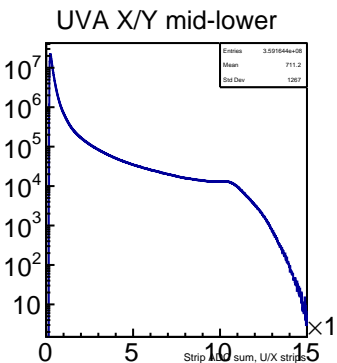
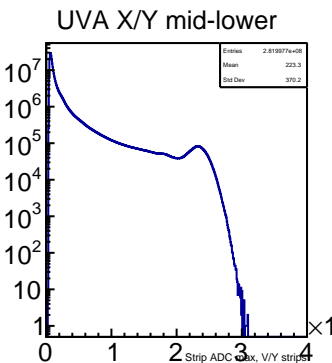
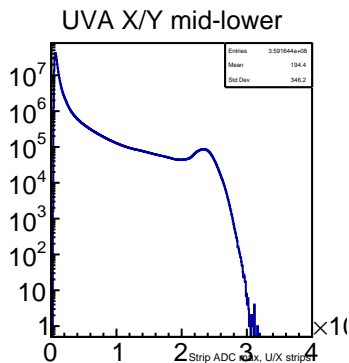
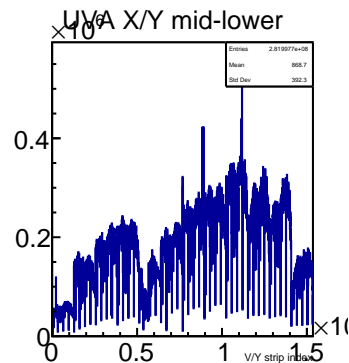
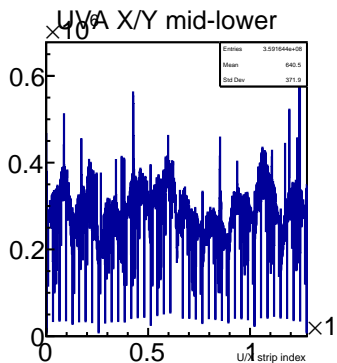
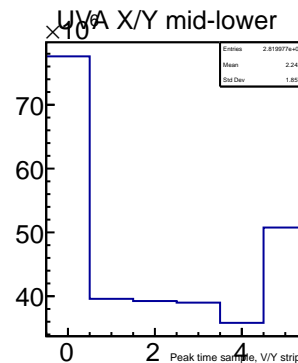
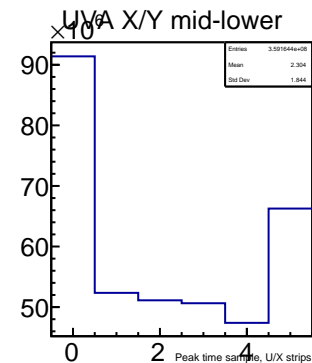
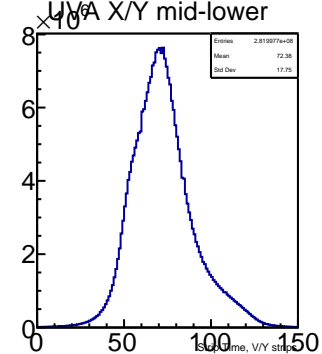
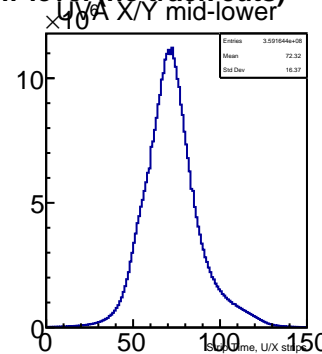
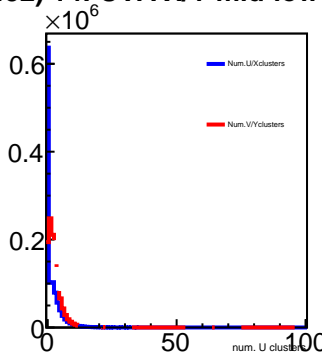
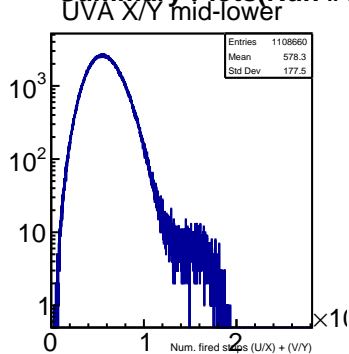
Summary Plots(Run #13452) 12: UVA X/Y top low-level (no track cuts)



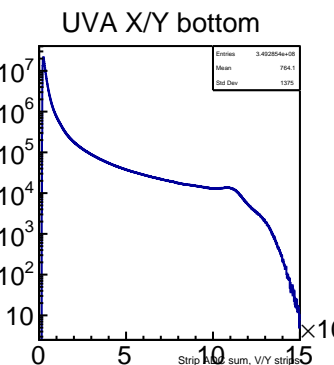
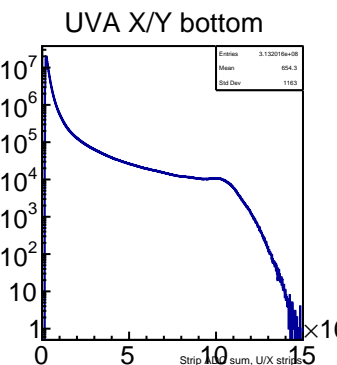
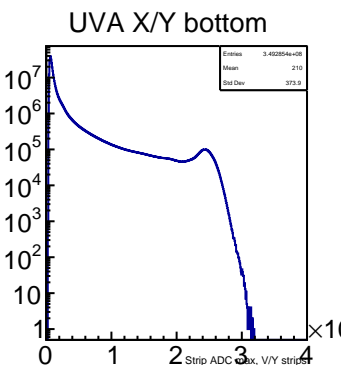
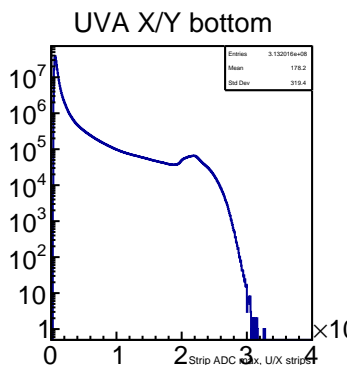
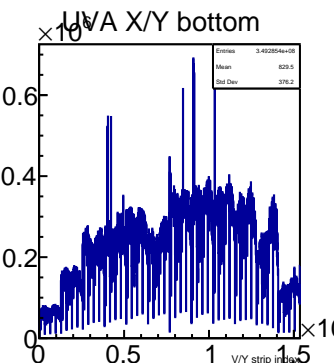
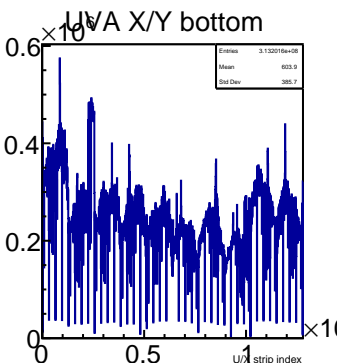
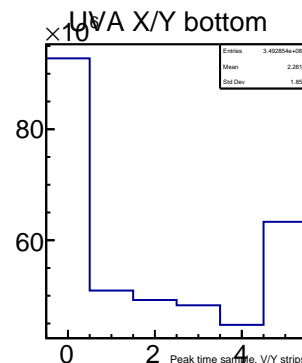
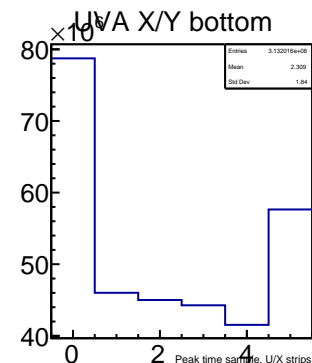
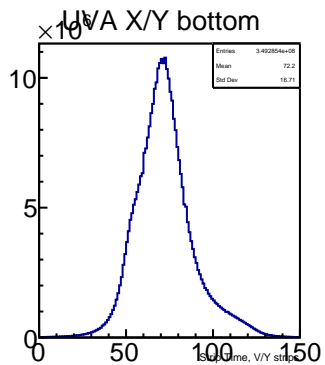
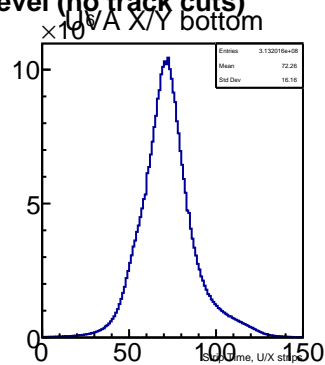
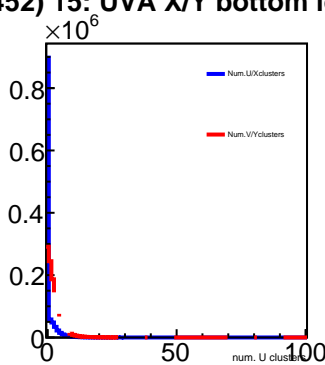
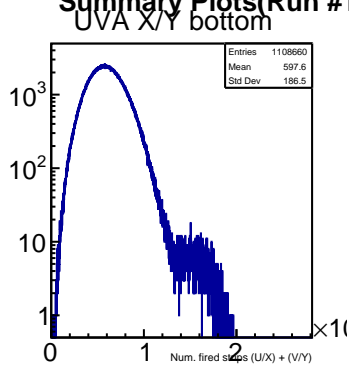
Summary Plots(Run #13452) 13: UVA X/Y mid-upper low-level (no track cuts)



Summary Plots(Run #13452) 14: UVA X/Y mid-low-level (no track cuts)

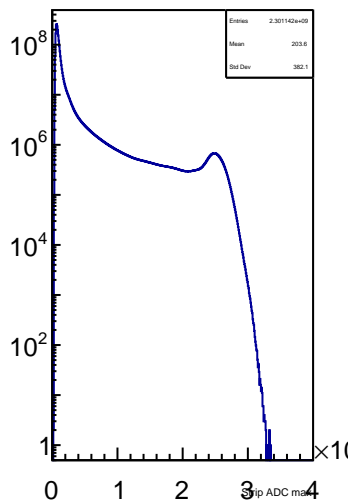


Summary Plots (Run #13452) 15: UVA X/Y bottom low-level (no track cuts)

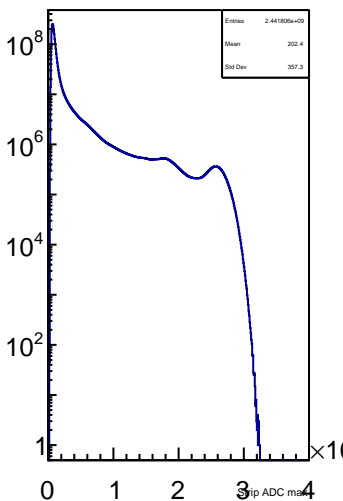


Summary Plots(Run #13452) 16: All modules strip ADC max

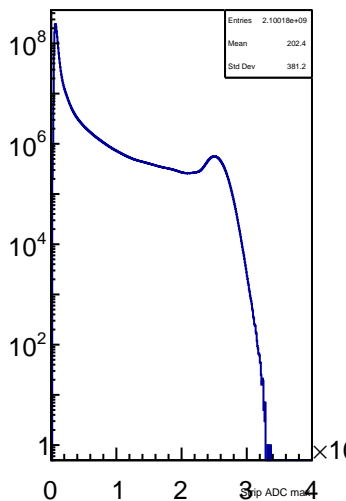
UVA U/V layer 0



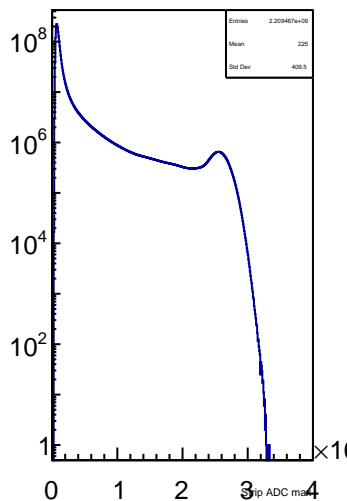
UVA U/V layer 1



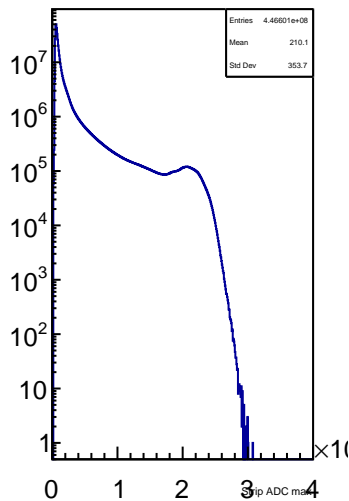
UVA U/V layer 2



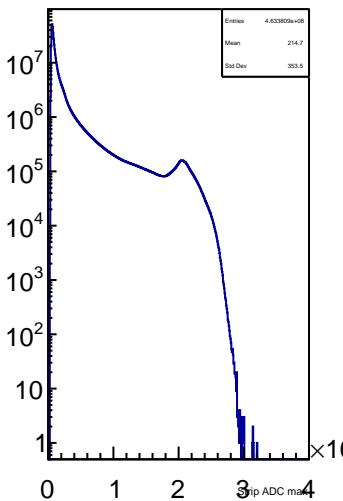
UVA U/V layer 3



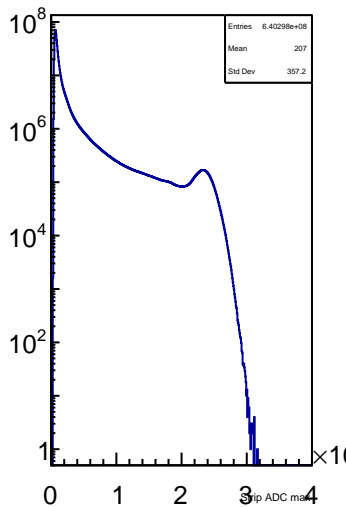
UVA X/Y top



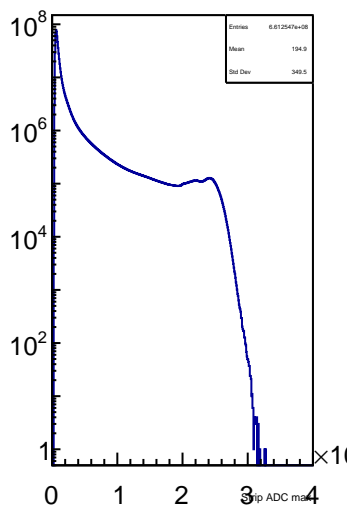
UVA X/Y mid-upper



UVA X/Y mid-lower

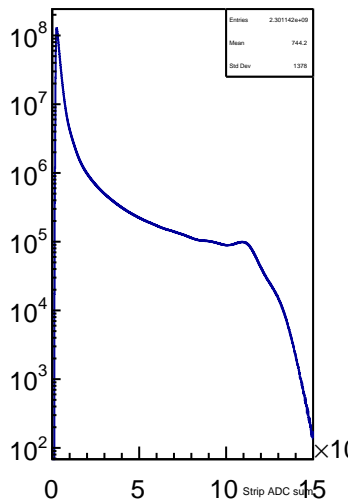


UVA X/Y bottom

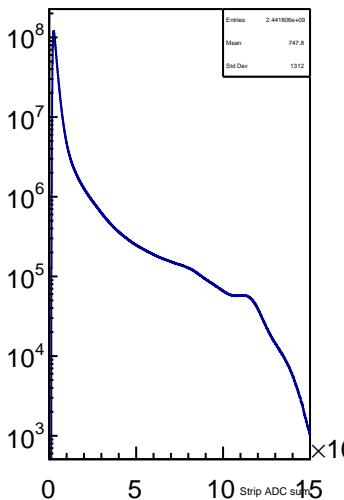


Summary Plots(Run #13452) 17: All modules strip ADC sum

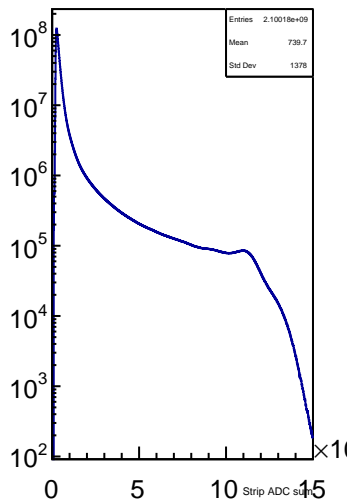
UVA U/V layer 0



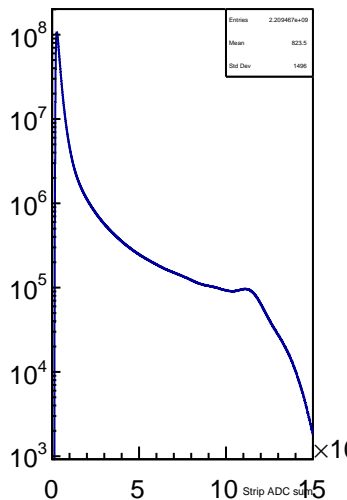
UVA U/V layer 1



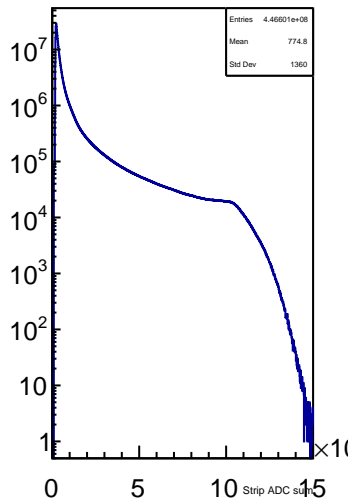
UVA U/V layer 2



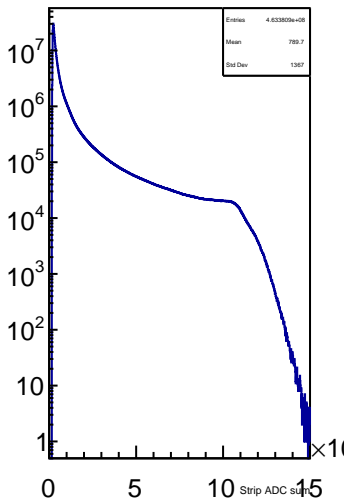
UVA U/V layer 3



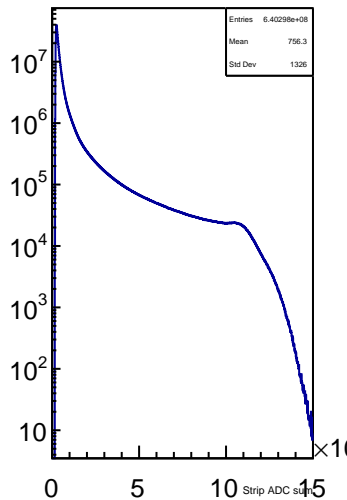
UVA X/Y top



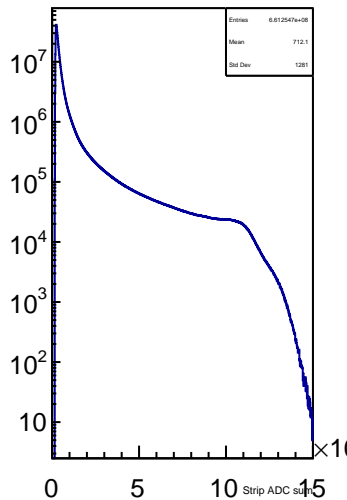
UVA X/Y mid-upper



UVA X/Y mid-lower

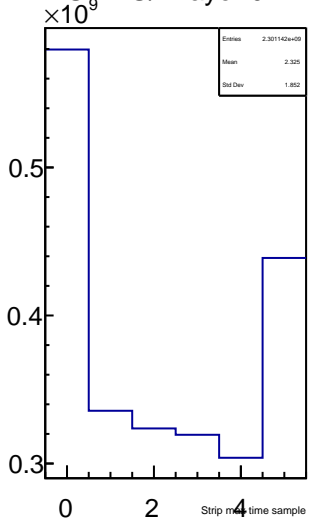


UVA X/Y bottom

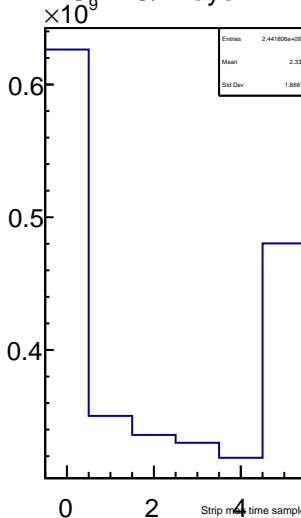


Summary Plots(Run #13452) 18: All modules max time sample

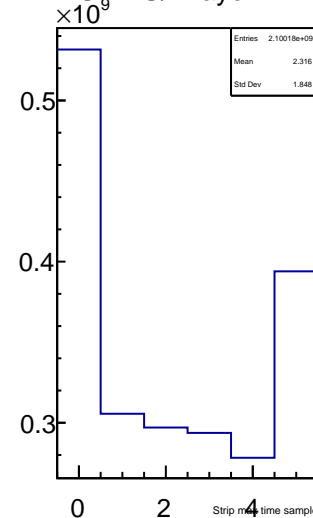
UYA U/V layer 0



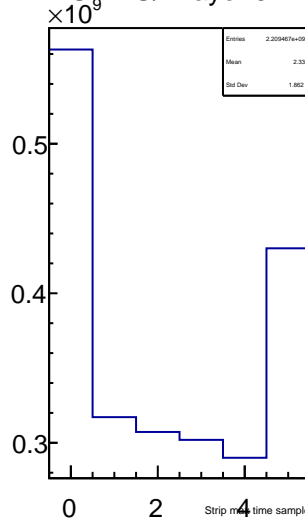
UYA U/V layer 1



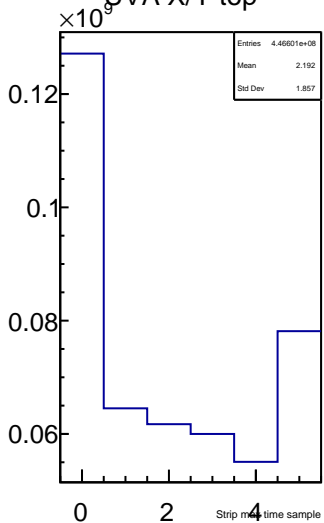
UYA U/V layer 2



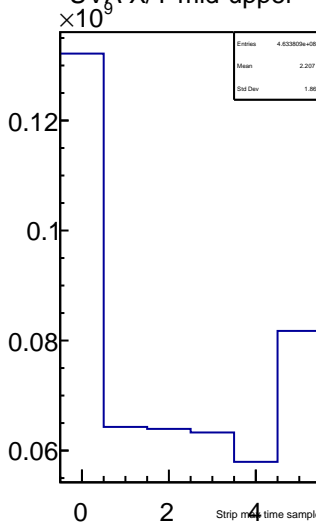
UYA U/V layer 3



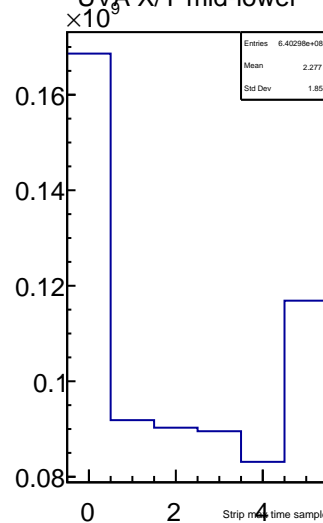
UYA X/Y top



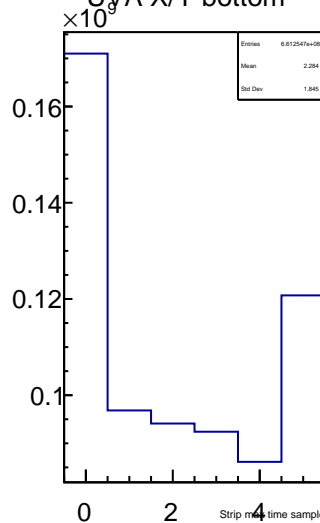
UYA X/Y mid-upper



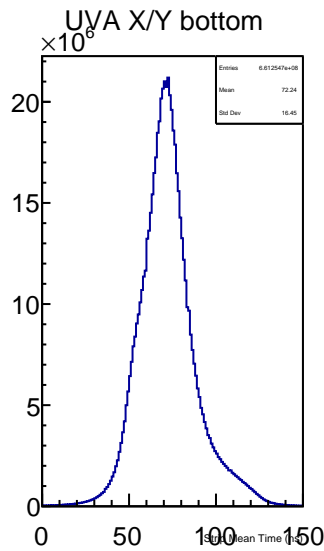
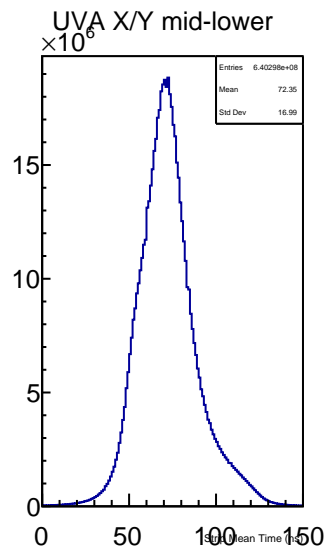
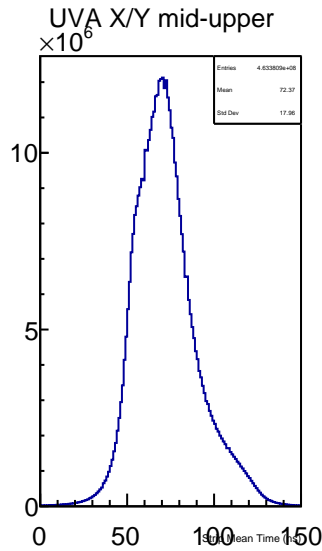
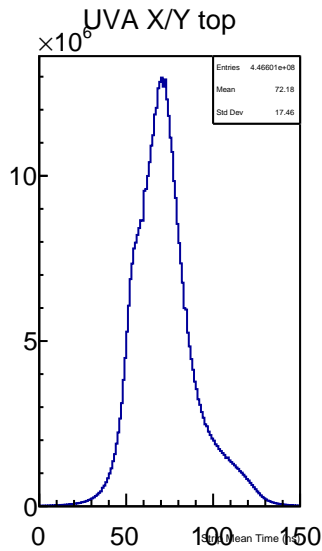
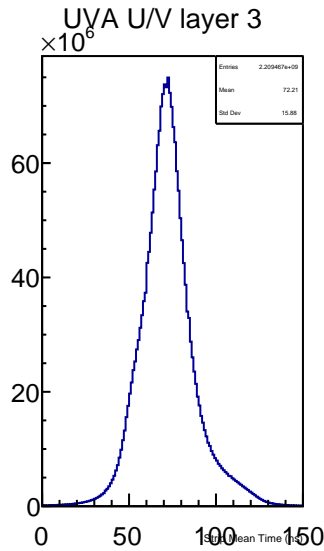
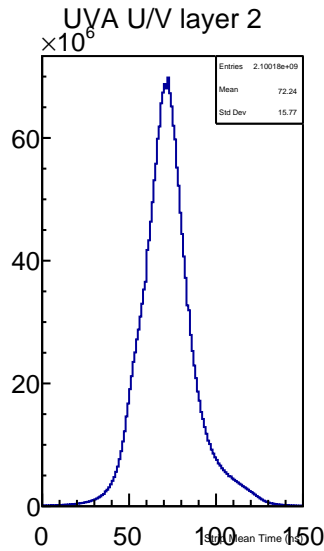
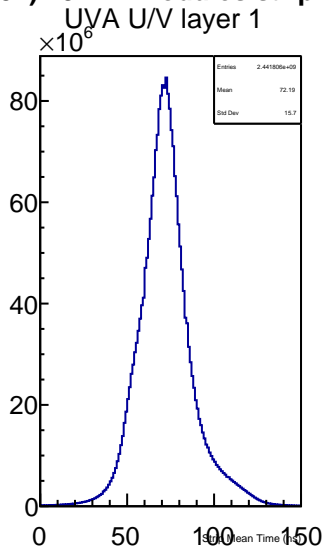
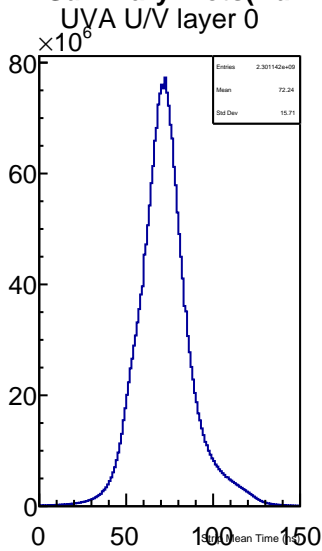
UYA X/Y mid-lower



UYA X/Y bottom

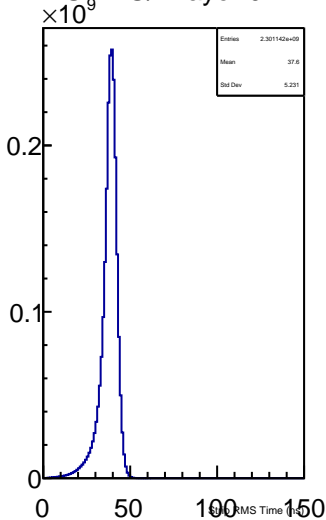


Summary Plots(Run #13452) 19: All modules strip time

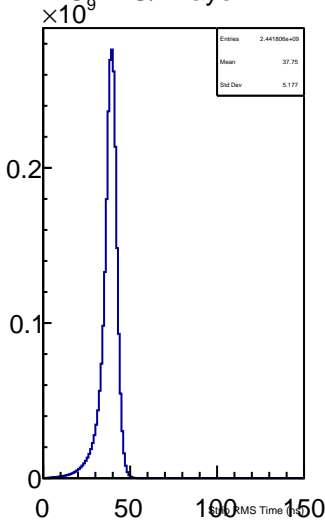


Summary Plots(Run #13452) 20: All modules strip rms time

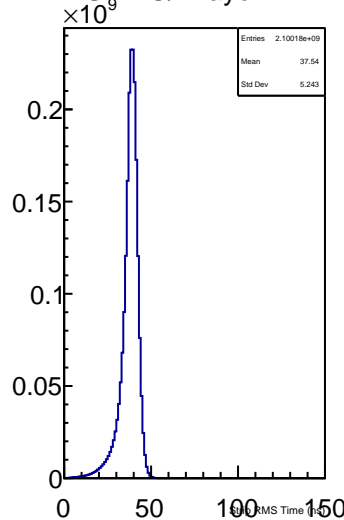
UYA U/V layer 0



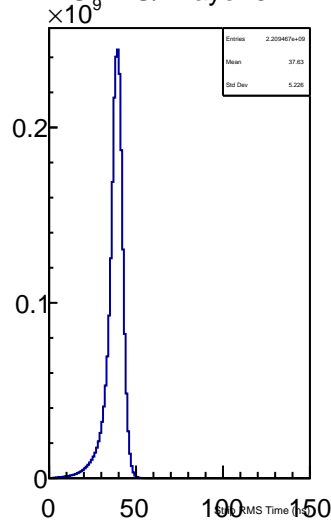
UYA U/V layer 1



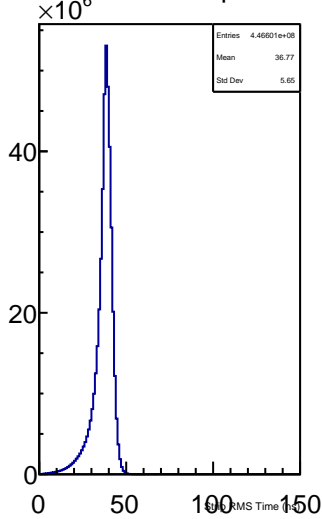
UYA U/V layer 2



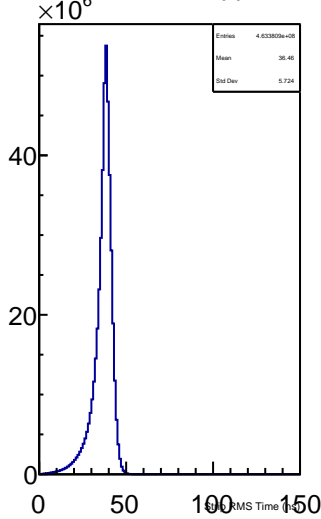
UYA U/V layer 3



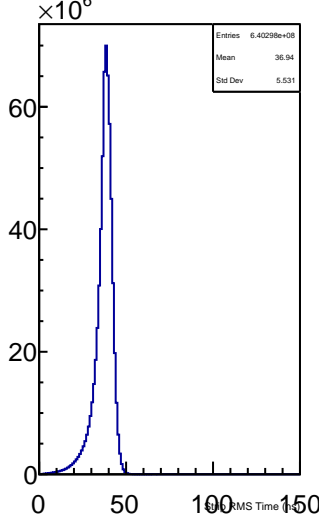
UYA X/Y top



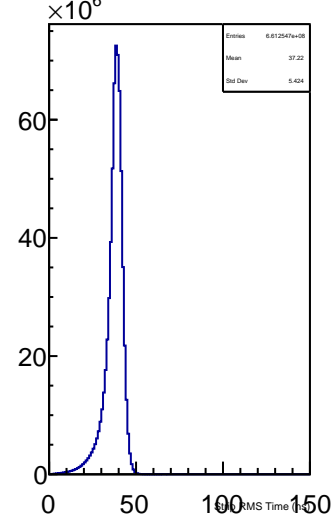
UYA X/Y mid-upper



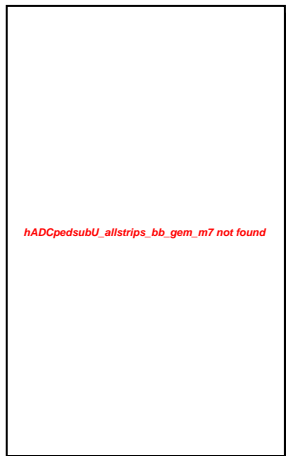
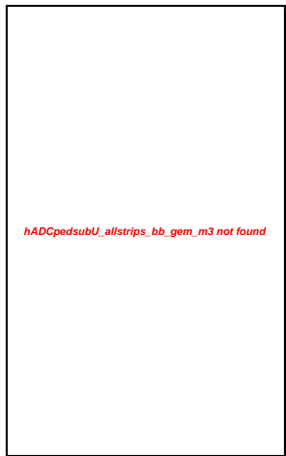
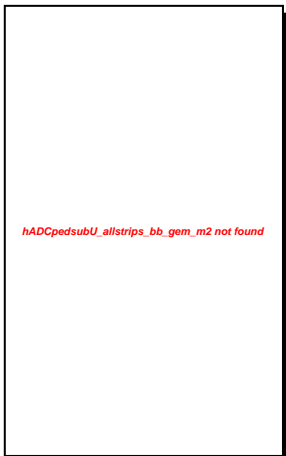
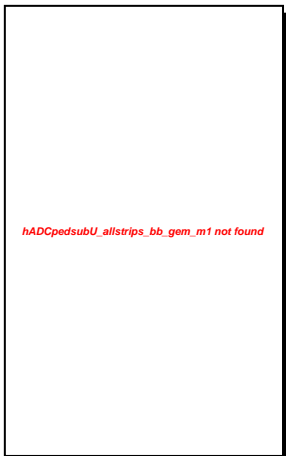
UYA X/Y mid-lower



UYA X/Y bottom



Summary Plots(Run #13452) 21: All modules U strip ADC no zero sup



Summary Plots(Run #13452) 22: All modules V strip ADC no zero sup

hADCpedsubV_allstrips_bb_gem_m0 not found

hADCpedsubV_allstrips_bb_gem_m1 not found

hADCpedsubV_allstrips_bb_gem_m2 not found

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