Scalable Quantum Layering in GoldCoreX: Towards Million-Qubit Hybrid Chips with Classical Interface Compatibility

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Abstract

GoldCoreX is a room-temperature quantum architecture based on gold atoms embedded in a diamond lattice. Building on validated single- and multi-qubit dynamics, this paper proposes a scale-up model enabling one million qubits per layer, stacked into ten-layer configurations. With +10 nm lateral separation and directional photonic control, the system remains decoherence-resistant while supporting hybrid classical-quantum logic. The form factor is engineered for compatibility with GPU sockets, PCIe, and standard system boards, enabling plug-in quantum acceleration.

1 Introduction

As quantum-classical hybrid systems move toward practical deployment, scalable quantum architectures must match the reliability and density of classical chips. Cryogenic approaches face size and integration limits. GoldCoreX offers a radically different pathway: high-density, room-temperature qubit arrays that fit within classical chip dimensions, yet provide trillions of entangling operations per second.

2 Qubit Density and Separation

Each gold atom qubit is embedded within a nanoscopic compression well in diamond, spaced $> 10\,\text{nm}$ from its neighbors.

2.1 Decoherence Considerations

This spacing mitigates:

- **Phonon coupling** between adjacent lattice points
- **Crosstalk** from entangling pulses or state collapse
- **Thermal diffusion** across layers

Simulations confirm fidelity $> 90\%$ per flip with detection loss and jitter.

3 Layered Stack Architecture

- **Each layer:** Up to 10^6 qubits
- **Vertical stack:** 10 layers (total 10^7 qubits per chip)
- **Interlayer shielding:** Carbon lattice + reflective isolation
- **Control:** Photon tunnel grid and THz pulse targeting

Layers are optically addressable and electrically isolated.

4 Elegant Gate Control

Unlike gate wire routing, GoldCoreX uses photon-based tunneling via:

- **Pressure-formed tunnels** in diamond crystal
- **Angle-resolved photonic targeting** of individual atoms
- **Optical diffraction elements** to control RX, CZ, and entanglement gates

This allows parallel, fast, and deterministic qubit operations with no physical switching noise.

5 Form Factor and Hybrid Compatibility

- Chip stack height: $\sim 3\,\text{mm}$
- Socket design: **GPU-sized BGA footprint**
- Power: Passive or low-watt THz pulse driver
- Host interface: PCIe or custom quantum-co-processor bus

The GoldCoreX chip is designed for drop-in retrofit onto existing motherboards, server racks, or embedded boards. No cryogenics or vacuum housing required.

6 Projected Capabilities

- 10^7 qubits $\rightarrow > 10^6$ entangled pairs simultaneously
- Up to 10^{13} gate ops/sec
- Compatible with QML, QFT, cryptographic primitives, and hybrid accelerators

7 Use Cases

1. AI model acceleration with entangled attention cores
2. Real-time simulation solvers (weather, particle physics)
3. Quantum cryptography for PCIe/NIC firmware
4. Quantum RAM extension for inference modules

8 Next Steps

- Fabrication of prototype slice with 10k qubits
- Layer bonding trials with interlayer THz alignment
- Integration with FPGA-based interface controller