1. Description

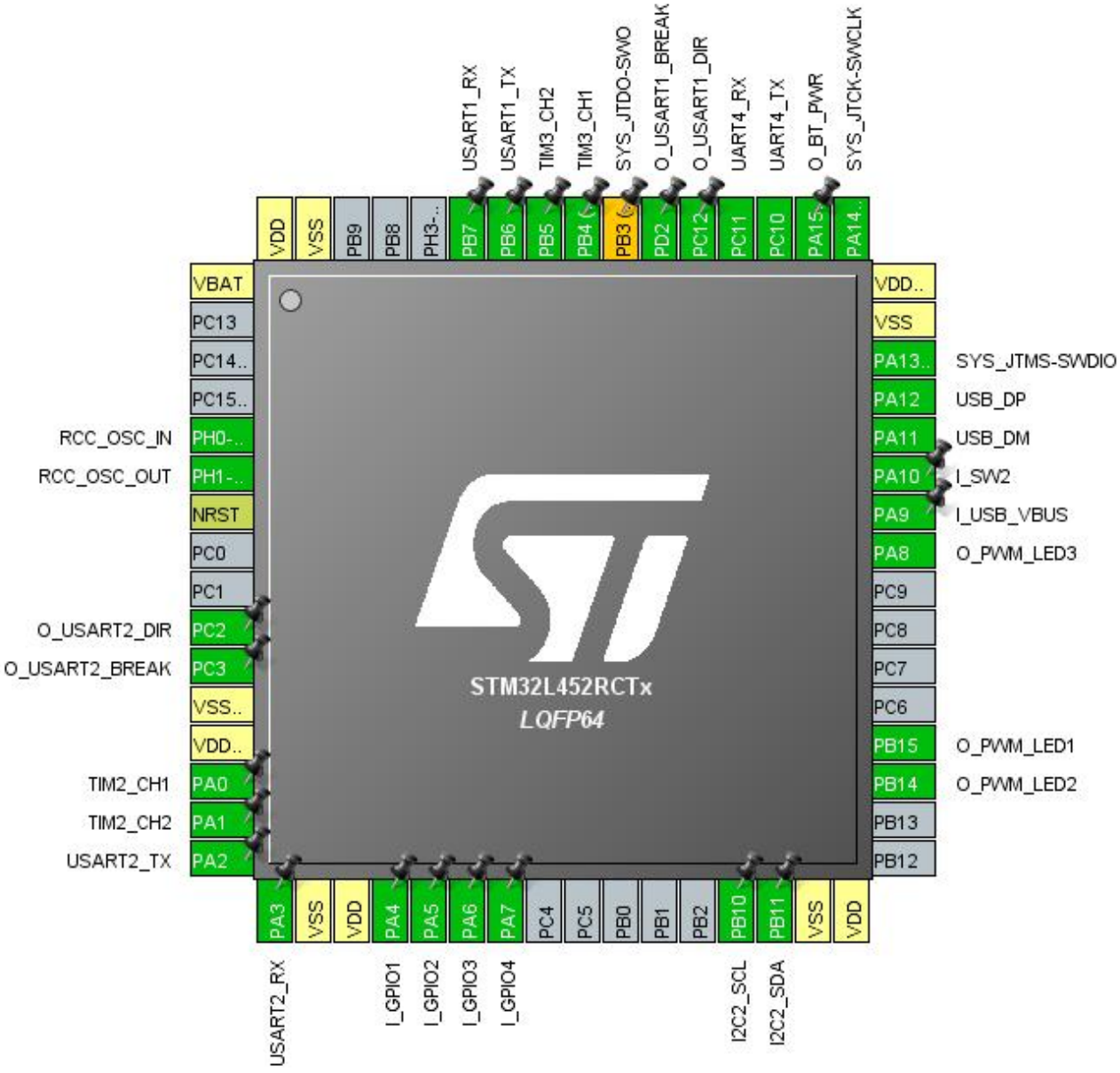
1.1. Project

Project Name	DMX_Merger
Board Name	custom
Generated with:	STM32CubeMX 5.0.1
Date	10/31/2019

1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x2
MCU name	STM32L452RCTx
MCU Package	LQFP64
MCU Pin number	64

2. Pinout Configuration



3. Pins Configuration

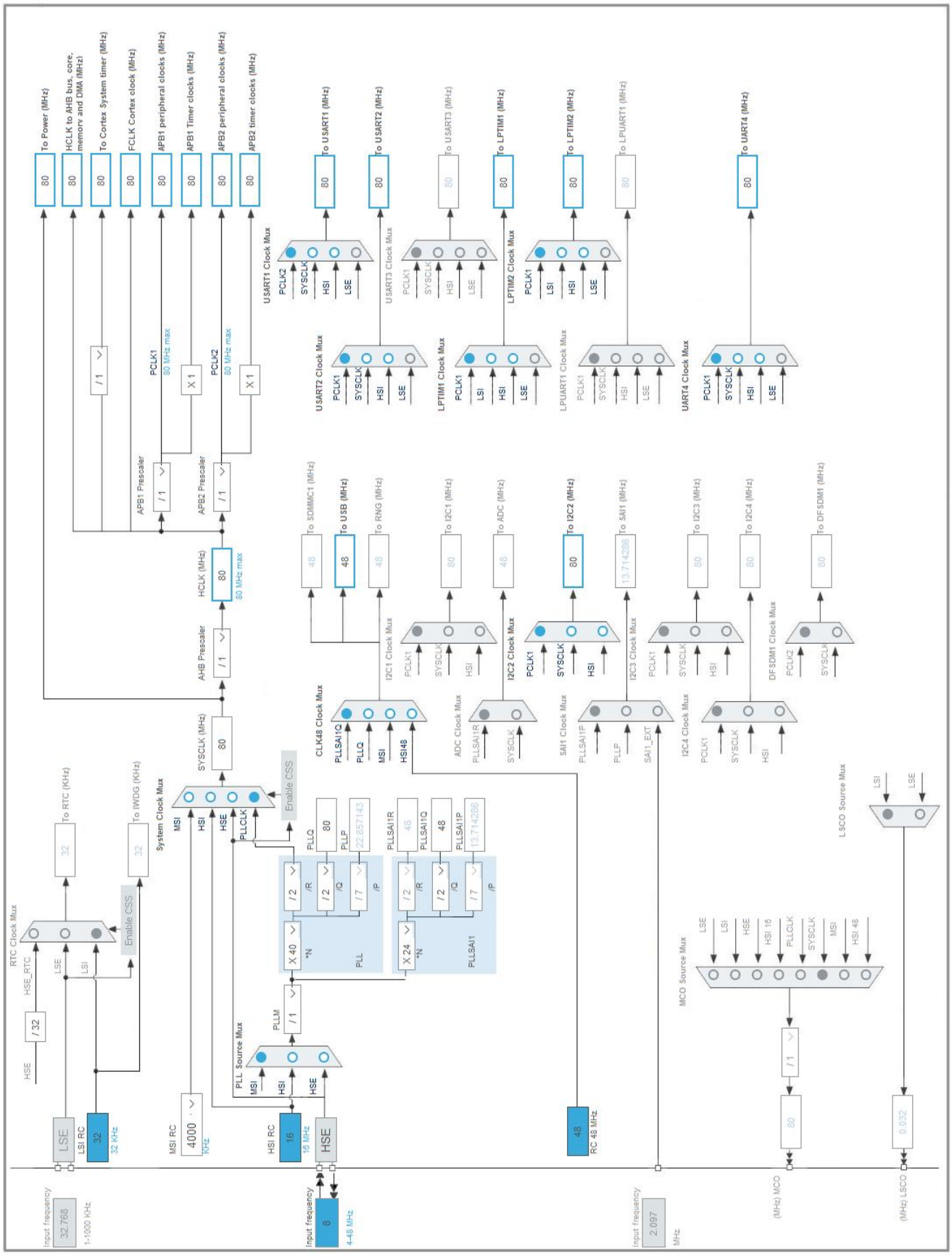
Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN (PH0)	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT (PH1)	I/O	RCC_OSC_OUT	
7	NRST	Reset		
10	PC2 *	I/O	GPIO_Output	O_USART2_DIR
11	PC3 *	I/O	GPIO_Output	O_USART2_BREAK
12	VSSA/VREF-	Power		
13	VDDA/VREF+	Power		
14	PA0	I/O	TIM2_CH1	
15	PA1	I/O	TIM2_CH2	
16	PA2	I/O	USART2_TX	
17	PA3	I/O	USART2_RX	
18	VSS	Power		
19	VDD	Power		
20	PA4 *	I/O	GPIO_Input	I_GPIO1
21	PA5 *	I/O	GPIO_Input	I_GPIO2
22	PA6 *	I/O	GPIO_Input	I_GPIO3
23	PA7 *	I/O	GPIO_Input	I_GPIO4
29	PB10	I/O	I2C2_SCL	
30	PB11	I/O	I2C2_SDA	
31	VSS	Power		
32	VDD	Power		
35	PB14	I/O	TIM15_CH1	O_PWM_LED2
36	PB15	I/O	TIM15_CH2	O_PWM_LED1
41	PA8	I/O	TIM1_CH1	O_PWM_LED3
42	PA9 *	I/O	GPIO_Input	I_USB_VBUS
43	PA10 *	I/O	GPIO_Input	I_SW2
44	PA11	I/O	USB_DM	
45	PA12	I/O	USB_DP	
46	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDDUSB	Power		
49	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	
50	PA15 (JTDI) *	I/O	GPIO_Output	O_BT_PWR
51	PC10	I/O	UART4_TX	
52	PC11	I/O	UART4_RX	

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
53	PC12 *	I/O	GPIO_Output	O_USART1_DIR
54	PD2 *	I/O	GPIO_Output	O_USART1_BREAK
55	PB3 (JTDO/TRACESWO) **	I/O	SYS_JTDO-SWO	
56	PB4 (NJTRST)	I/O	TIM3_CH1	
57	PB5	I/O	TIM3_CH2	
58	PB6	I/O	USART1_TX	
59	PB7	I/O	USART1_RX	
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	DMX_Merger
Project Folder	C:\Users\erics\Documents\embeddedAudioLab\Projects\PN0008_DMX_Merger\S
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_L4 V1.13.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x2
MCU	STM32L452RCTx
Datasheet	029968_Rev3

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. I2C2

I2C: I2C

7.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	Standard Mode
I2C Speed Frequency (KHz)	100
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	0x10909CEC

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.2. LPTIM1

Mode: Counts internal clock events

7.2.1. Parameter Settings:

Clock:

Clock Prescaler	Prescaler Div1

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

7.3. LPTIM2

Mode: Counts internal clock events

7.3.1. Parameter Settings:

Clock:

Clock Prescaler	Prescaler Div1

Preload:

Update Mode	Update Immediate

Trigger:

Trigger Source	Software Trigger

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Disabled
Data Cache	Enabled
Flash Latency(WS)	4 WS (5 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
MSI Auto Calibration	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM1

Channel1: PWM Generation CH1

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.7. TIM2

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.8. TIM3

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	**Falling Edge ***
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.9. TIM6

mode: Activated

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.10. TIM15

mode: Clock Source

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.11. TIM16

mode: Activated

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

7.12. UART4

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.13. USART1

Mode: Asynchronous

7.13.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.14. USART2

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.15. USB

mode: Device (FS)

7.15.1. Parameter Settings:

Basic Parameters:

Speed	Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Physical interface	Internal Phy
Sof Enable	Disabled

Power Parameters:

Low Power	Disabled
Link Power Management	Disabled
Battery Charging	Disabled

7.16. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.16.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SUPPORT_USER_STRING (Enable user string descriptor)	Disabled
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.16.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336

PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
SERIALNUMBER_STRING (Serial number)	00000000001A
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High** *	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High** *	
RCC	PH0-OSC_IN (PH0)	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13 (JTMS/SWDIO)	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14 (JTCK/SWCLK)	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PA8	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	O_PWM_LED3
TIM2	PA0	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PA1	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM3	PB4 (NJTRST)	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM15	PB14	TIM15_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	O_PWM_LED2
	PB15	TIM15_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	O_PWM_LED1
UART4	PC10	UART4_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC11	UART4_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USART1	PB6	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB7	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USB	PA11	USB_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
Single Mapped Signals	PB3 (JTDO/TRACESWO)	SYS_JTDO-SWO	n/a	n/a	n/a	
GPIO	PC2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	O_USART2_DIR
	PC3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	O_USART2_BREAK
	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	I_GPIO1
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	I_GPIO2
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	I_GPIO3
	PA7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	I_GPIO4
	PA9	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	I_USB_VBUS
	PA10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	I_SW2
	PA15 (JTDI)	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	O_BT_PWR
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	O_USART1_DIR
	PD2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	O_USART1_BREAK

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
TIM1 break interrupt and TIM15 global interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM3 global interrupt	true	0	0
USART1 global interrupt	true	0	0
USART2 global interrupt	true	0	0
TIM6 global interrupt, DAC channel1 underrun error interrupt	true	0	0
LPTIM1 global interrupt	true	0	0
LPTIM2 global interrupt	true	0	0
USB event interrupt through EXTI line 17	true	0	0
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 update interrupt and TIM16 global interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
I2C2 event interrupt	unused		
I2C2 error interrupt	unused		
UART4 global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report