Xinle (Eric) Song

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Education

University of California, Los Angeles — Los Angeles, CA
Bachelor of Science in Computer Engineering — *Sep. 2023 - June 2027*

- GPA: 3.862, Dean's Honors List
- Selected Coursework: Computer System Architecture, Digital Logic Design, Data Structures
- Received the John Richard Leffler Scholarship

Technical Skills

Languages: C/C++, Python, Verilog/SystemVerilog, JavaScript, HTML/CSS
Developer Tools: Vivado, Quartus, OpenMP, Fusion 360, CMake, GDB, Git, Bash
Technologies: Computer Architecture, FPGA, PCB Design, Embedded Systems, PID Control

Experience

UCLA ORCAS Lab — Jan. 2025 – Present
Undergraduate Research Assistant

- Researched the implementation of the **Vortex GPU** on lightweight FPGAs, simulated GPU Performance using a C++ GPU **simulator**.
- Co-designed the Vortex **driver library** to enable GPU acceleration in a **RISC-V** environment.
- Explored **resource management** and GPU instruction execution optimization strategies on **lightweight FPGAs** to enhance system performance.

UCLA Nanosystems CAD Lab — Oct. 2024 – Present
Undergraduate Research Assistant

- Integrated the **CATCH-model** with the **HISIM-Systolic Array Model**, produced a simulator specifically designed for **AI application-specific chiplets**.
- Simulated **size, power, and performance tradeoffs** in chiplet systems using the integrated models.
- Evaluated **yield tradeoffs** to optimize chiplet system designs for AI applications.

UCLA CHIPS Lab — Jan. 2024 – Oct. 2024
Undergraduate Research Assistant

- Adapted **software driver** for a **FlexTrate LED display** with a new driver chip and 11x11 dimensions.
- Developed a **pixel control algorithm** to display **"UCLA"** across 25 frames per letter.
- Created an **automated testing script** that reduced testing time by **70%**, streamlining pixel-by-pixel activation.

Projects

Pipelined RISC-V CPU Simulator | *C++11, Processor Design, GNU Make, Git* — Jan. 2025 – Present

- Developed a **5-stage** pipelined **RISC-V** CPU simulator implementing the RV32-I base ISA using C++11.
- Completed **decode, execute, and pipeline** timing logic, passing all functional and timing tests.
- Validated functionality with **GNU Make** and a Linux-based development environment (Ubuntu 18.04).
- Delivered a fully functional simulation with **accurate timing**, meeting all grading criteria.

Digital Audio Visualizer | *System Verilog, RTL Design, FPGA Programming, Git* — Sep. 2024 – Present

- Learning **RTL design** and **digital logic** to develop a project that displays audio frequency levels on a VGA display using **FFT (Fast Fourier Transform)**.
- Gaining hands-on experience with **sequential and combinational logic**, and industry tools like **Quartus**.

Brewin Interpreter | *Python, Abstract Syntax Tree (AST), Static Typing, Git* — Oct. 2024 – Dec. 2024

- Developed an interpreter for **Brewin**, supporting **static typing**, **user-defined structs**, and **coercion**.
- Implemented features such as **nested structs**, **default return values**, parameter passing by **value or object reference**, and exception handling.
- Implemented **static scoping**, **function calls**, using deque and dictionary, optimized variable search speed by 30%
- Verified functionality through **unit testing**, succeeded in **100%** of the test cases.