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# AVR1514: XMEGA-A1 Xplained Training - Direct Memory Access Controller



## Prerequisites

- Required knowledge
  - AVR1512: XMEGA-A1 Xplained Training - XMEGA Basics
- Software prerequisites
  - Atmel® AVR Studio® 5
- Hardware prerequisites
  - XMEGA-A1 Xplained evaluation board
  - JTAGICE3 (or AVR ONE! or JTAGICE mkII)
- Estimated completion time:
  - 2 hours

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## 8-bit Atmel Microcontrollers

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## Application Note

## 1 Introduction

This application note covers the basic features of the Atmel® AVR® XMEGA® Direct Memory Access Controller (DMAC). The goal for this training is to get started with simple memory transfers almost without using CPU time, and reading / writing to peripherals with hardly any CPU intervention.

There are four DMA channels that have individual source, destination, triggers, and block sizes. The DMA Controller can move data from one memory area to another, between memories and peripherals and between peripherals.

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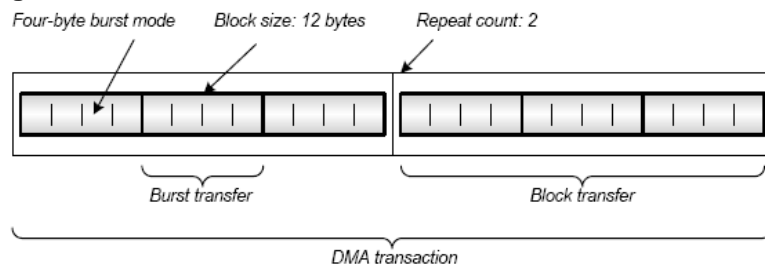
## 2 Setting up the DMA Controller

The Atmel® AVR® XMEGA® Direct Memory Access Controller (DMAC) is a highly flexible four-channel DMA Controller capable of transferring data between memories and peripherals with minimal CPU intervention. While the CPU spends time in low-power sleep modes or performs other tasks, the XMEGA DMAC offloads the CPU by taking care of mere data copying from one area to another. The following sub-chapters are meant to complement the understanding when doing the tasks in this training.

### 2.1 DMA Transaction

A complete DMA read and write operation between memories and/or peripherals is called a DMA transaction. A transaction is done in data blocks and the size of the transaction (number of bytes to transfer) is selectable from software and controlled by the block size and repeat counter settings. Each block transfer is divided into smaller bursts, see Figure 2-1.

**Figure 2-1. DMA Transaction**



When a DMA channel requests a data transfer, the bus arbiter will wait until the AVR core is not using the data bus and permit the DMA Controller to transfer data. Transfers are done in bursts of 1, 2, 4 or 8 bytes. Addressing can be static, incremental or decremental. Automatic reload of source and/or destination address can be done after each burst transfer, block transfer, when transfer is complete, or disabled. DMA transfers can be triggered by application software, peripherals and events.


The size of the block transfer is set by the Block Transfer Count Register, and can be anything from 1 byte to 64 Kbytes. A repeat counter can be enabled to set a number of repeated block transfers before a transaction is complete. The repeat is from 1 to 255 and unlimited repeat count can be achieved by setting the repeat count to zero.

A bus arbiter controls when the DMA controller and the AVR core can use the bus. The core always has priority, so as long as the core request access to the bus, any pending burst transfer must wait. The core requests bus access when it executes an instruction that write or read data to SRAM, IO memory, EEPROM and the External Bus Interface.

### 2.2 Addressing

If the source or destination is SRAM, the user will most likely want to increment or decrement the address pointer. Therefore, it is possible to set the DMAC source / destination in incremental or decremental mode.

*The DMAC will increment the address pointer automatically in incremental mode*



SRAM Address	Value
0x2066	34
0x2067	76
0x2068	13
0x2069	113

In incremental mode, the DMAC will start at the source address. After the first byte has been sent, the next byte will be read from the previous address plus one.

In decremental mode, it is opposite, where the DMAC will start at a given source address and proceed with the previous addresses.

The original source and destination addresses are stored by the DMA controller, so that the source and destination addresses can be individually configured to be reloaded at the following points:

- End of each burst transfer
- End of each block transfer
- End of transaction
- Never reload

When using the DMAC with a peripheral, such as the SPI, the data register is fixed, and it is important that the addressing mode is static.

## 2.3 Transfer Triggers

The main purpose of the DMA triggers is to synchronize the peripherals with the transfer rate. For instance, when using the USART at 9600 baud, the DMA should not be triggered more often than the transfer complete flag is set.

DMA transfers can only be started when a DMA transfer request is detected. A transfer request can be triggered from software, from an external trigger source (peripheral) or from an event. There are dedicated source trigger selections for each DMA channel. The available trigger sources may vary from one device to another, depending on the modules or peripherals that exist in the device (see the XMEGA manual for different transfer triggers).

## 2.4 Interrupts

The DMA Controller can generate interrupts when an error is detected on a DMA channel or when a transaction is complete for a DMA channel. Each DMA channel has a separate interrupt vector, and there are different interrupt flags for error and transaction complete. The transaction complete flag is set at the end of each Block Transfer even if unlimited repeat is enabled.

## 3 Overview

*Here is a short overview of the tasks in this training:*

### Task 1: Memory Copy

This task shows how to copy blocks of memory from one location to another without CPU intervention. The task is divided in two parts.

1. The first part will show how to copy memory in SRAM with the DMAC
2. The second part will show how to set up an interrupt to indicate that the transfer is done

### Task 2: Interrupt mode

This task shows how to implement a simple recorder that records a ten second sequence of switch presses and plays them back on the LEDs. The recording and playback process is performed without CPU intervention.

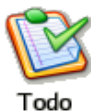
## 4 Task 1: Memory copy

DMA controllers are perfect for copying large chunks of memory from one location to another. This task will demonstrate the block memory copy routine from the driver file. It will also show how to set up the PMIC to get interrupt when the transfer is done.

*The goals for this task are that you know how to:*

- Use the driver code to set up the DMAC and start memory copy operations
- Set up the PMIC to trigger an interrupt when the transfer is done

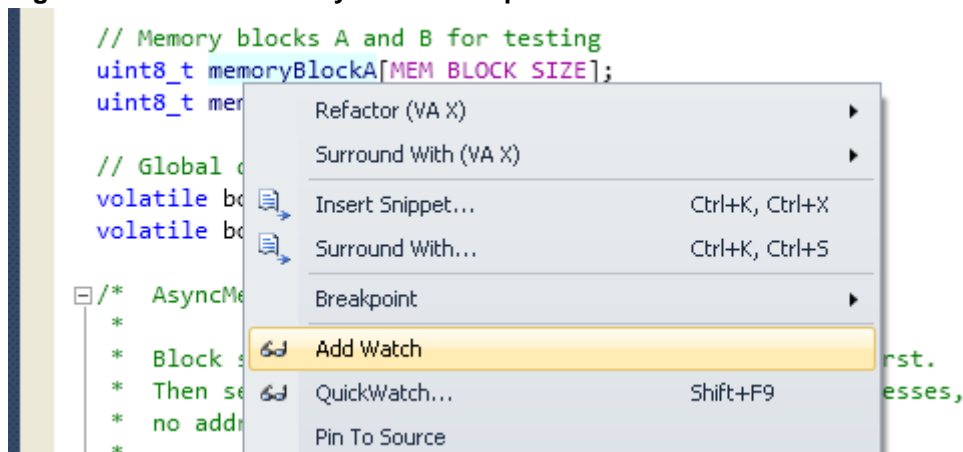
### 4.1 Memory Copy: Polling approach



TASK:

1. Locate the Atmel XMEGA-DMAC folder.
2. Open the `xmega_dmac.avrsln` solution file and set Task 1 active by selecting it as StartUp project.
3. Build the project (press F7) and start debugging (click on Play or press Alt+F5)
4. Locate the `memoryBlockA` and `memoryBlockB` definitions and add data watches for both of them ("Add watch..." in right-click menu), see Figure 4-1

Figure 4-1. Locate memory blocks at top of task1.c



5. In main(), right-click on the call to `MemCopy` and select "Run to Cursor" (or use Ctrl+F10) in the right-click menu, see Figure 4-2
6. Expand `memoryBlockA` and `memoryBlockB` in the watch window and look into their contents. Are they equal? See Figure 4-3

Figure 4-2. Run to cursor

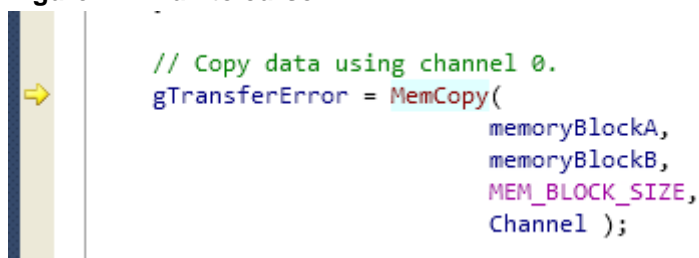


Figure 4-3. Compare memoryBlockA and memoryBlockB

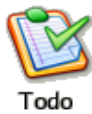
Watch 1		
Name	Value	Type
memoryBlockA	{uint8_t[100](data)@0x2066}	uint8_t[100](data)@0x2066
[0]	0	uint8_t(data)@0x2066
[1]	1	uint8_t(data)@0x2067
[2]	2	uint8_t(data)@0x2068
[3]	3	uint8_t(data)@0x2069
[4]	4	uint8_t(data)@0x206a
[5]	5	uint8_t(data)@0x206b
[6]	6	uint8_t(data)@0x206c
[7]	7	uint8_t(data)@0x206d
[8]	8	uint8_t(data)@0x206e

7. Step Over (F10) the call to `MemCopy` and look onto the contents of `memoryBlockA` and `memoryBlockB` again. Are they equal now?
8. Reset execution (Shift-F5) and run to `MemCopy` again. This time step into (press F11) to access the function. Further, step into `DMA_SetupBlock` to see how the

driver configures the DMAC for you. You may want to refer to the introduction chapter in order to answer these questions:

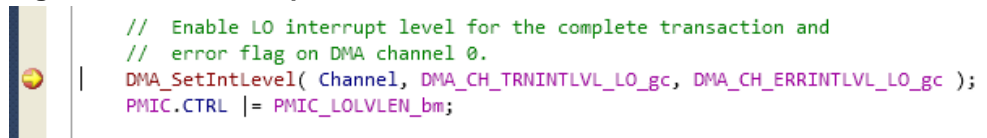
- a) Is the memory copy set up as static, incrementing or decrementing? Why is it set up this way?
- b) Could another DMA channel have been used?
- c) The software trigger source is used as default for this between memories transfer. Why do you think this is convenient when copying from SRAM to SRAM?
- d) What is the burst length? Why do you think it is configurable?

## 4.2 Memory Copy: Interrupt approach



1. Add a break-point to the start of test two, as shown in Figure 4-4. And press F5 to run

**Figure 4-4. Add break point here**



2. If the previous test went fine (no errors in the transfer), then we are ready for the next test. Single-step (press F10) some steps and notice that an interrupt is set up to trigger when the next DMA transaction has completed
3. Look at the function `AsyncMemCopy`. Notice that, in comparison with `MemCopy`, there is no call to `DMA_ReturnStatus_non_blocking`

The function `DMA_ReturnStatus_blocking` polls until the DMA transfer has finished. When using an interrupt instead to indicate that the transfer has finished, the CPU will be free to do other operations.

4. At the bottom of `task1.c`, add a break-point in the interrupt service routine `ISR(DMA_CH0_vect)`, as shown in Figure 4-5. Press F5 to run

Figure 4-5. Wait for interrupt

```

// DMA CH0 Interrupt service routine. Clear interrupt flags after check
ISR(DMA_CH0_vect)
{
    if (DMA.INTFLAGS & DMA_CH0TRNIF_bm)
    {
        DMA.INTFLAGS |= DMA_CH0TRNIF_bm;
        gTransferError = false;
    } else
    {
        DMA.INTFLAGS |= DMA_CH0ERRIF_bm;
        gTransferError = true;
    }
    gInterruptDone = true;
}

```

5. Run to completion (press F5) and break execution (Ctrl+F5) after a while. Verify that the transfer went well by comparing `memoryBlockA` and `memoryBlockB`

## 5 Task 2: Recorder

An application, for which the DMAC is really useful, is to copy data between memory and peripherals such as ADCs and DACs. This task shows how to implement a simple recorder that samples the switches for a period of time, stores it in a SRAM buffer, and then plays the data back on the LEDs over and over again. The exact same principle would be used if you should record sound with an ADC and play it back on a DAC.



The goal for this task is that you know how to:

- Configure the DMAC to copy data from peripheral to SRAM
- Configure the DMAC to copy data from SRAM to peripheral
- Use a timer tick as a trigger source for DMA data transfers

### TASK:



1. Locate the Atmel XMEGA-DMAC folder.
2. Open the `xmega_dmac.avrsln` solution file and set Task 2 active by selecting it as StartUp project.
3. Build the project (press F7), start debugging (click on Play), and run code (press F5) to use the recorder:
  - a) The LEDs flash once
  - b) Press any switch
  - c) The LEDs flashes again
  - d) You have approximately 10 seconds to hammer at the switches while the DMAC records the switch states
  - e) The LEDs flashes again
  - f) Press any switch
  - g) The LEDs flashes again



- h) The DMAC will play back the switch recording on the LEDs until a switch is pressed.<sup>1</sup>
  - i) The procedure starts over
4. Try changing the `SAMPLE_COUNT` definition or the sample rate. Recompile, run, and see what happens. See Figure 5-1

**Figure 5-1. Try changing `SAMPLE_COUNT`**

```
#define SAMPLE_COUNT 300 // How many switch state samples to store.  
uint8_t samples[SAMPLE_COUNT]; // Store switch state samples here.
```



5. Try to walk through the code and understand what happens. You may refer to the introduction chapter when answering these questions:
- a) In the `SetupReadChannel`, what is the source and what is the destination?
  - b) In the `SetupWriteChannel`, what is the source and what is the destination?
  - c) What would happen if you set the DMAC up with software trigger source, in this case?
  - d) For the Read-channel, why are the source address fixed and the destination address incremental?
  - e) Could the burst-length have been different, such as 4 or 8?

<sup>1</sup> Note that LED6 and LED7 are always lit when using the XMEGA-A1 Xplained. The reason for this is that the switches are distributed between PORTD and PORTR.



## 6 Summary

- Memory copy; DMAC from SRAM to SRAM
- Using interrupt source to indicate end of transfer
- Recording switch presses using DMAC. This application recorded the port pin input states and saved the information in SRAM. The information that was saved in SRAM was then set out to the LEDs. A timer overflow was used as a trigger source

## 7 Resources

- Atmel XMEGA Manual and Datasheets.
  - <http://www.atmel.com/xmega>
- Atmel AVR Studio 5
  - [http://www.atmel.com/microsite/avr\\_studio\\_5](http://www.atmel.com/microsite/avr_studio_5)
- Atmel IAR Embedded Workbench® compiler
  - <http://www.iar.com/>

## 8 Atmel Technical Support Center

Atmel has several support channels available:

- |               |   |                            |
|---------------|---|----------------------------|
| • Web portal: | <a href="http://support.atmel.no/">http://support.atmel.no/</a> | All Atmel microcontrollers |
| • Email:      | <a href="mailto:avr@atmel.com">avr@atmel.com</a>                | All AVR products           |
| • Email:      | <a href="mailto:avr32@atmel.com">avr32@atmel.com</a>            | All 32-bit AVR products    |

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**Atmel Corporation**  
2325 Orchard Parkway  
San Jose, CA 95131  
USA  
**Tel:** (+1)(408) 441-0311  
**Fax:** (+1)(408) 487-2600  
[www.atmel.com](http://www.atmel.com)

**Atmel Asia Limited**  
Unit 01-5 & 16, 19F  
BEA Tower, Millennium City 5  
418 Kwun Tong Road  
Kwun Tong, Kowloon  
HONG KONG  
**Tel:** (+852) 2245-6100  
**Fax:** (+852) 2722-1369

**Atmel Munich GmbH**  
Business Campus  
Parkring 4  
D-85748 Garching b. Munich  
GERMANY  
**Tel:** (+49) 89-31970-0  
**Fax:** (+49) 89-3194621

**Atmel Japan**  
9F, Tonetsu Shinkawa Bldg.  
1-24-8 Shinkawa  
Chou-ku, Tokyo 104-0033  
JAPAN  
**Tel:** (+81) 3523-3551  
**Fax:** (+81) 3523-7581

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