MICROPROCESSADORES E MICROCONTROLADORES

COMUNICAÇÃO

Diversos cenários:

COMUNICAÇÃO

Diversos cenários:

- Aparelhos ligados à internet

COMUNICAÇÃO

Diversos cenários:

- Aparelhos ligados à internet
- Envio de dados do MSP430 para um computador pessoal

COMUNICAÇÃO

Diversos cenários:

- Aparelhos ligados à internet
- Envio de dados do MSP430 para um computador pessoal
- Troca de dados entre dois MSP430

COMUNICAÇÃO

Diversos cenários:

- Aparelhos ligados à internet
- Envio de dados do MSP430 para um computador pessoal
- Troca de dados entre dois MSP430
- Troca de dados entre um MSP430 e um chip de memória externa

COMUNICAÇÃO

Diversos cenários:

- Aparelhos ligados à inte
- Envio de dados do MSP omputador pessoal
- Troca de dados entre d
- Troca de dados entre u m chip de memória externa

USB
Bluetooth
Wifi
Etc.

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

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O MSP430 consegue lidar diretamente com 4 tipos de comunicação serial:

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de comunicação serial:

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Software dedicado para realizar o protocolo desejado.

os seguem protocolos de comunicação.

es linguagens para o mesmo problema de dados (0s e 1s).

O MSP430 conseg lidar diretamente com 4 tipos de comunicação serial:

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de comunicação serial:

Protocolos realizados por hardware dedicado.

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de
rial:

Protocolos síncronos (o clock é enviado junto com os dados).

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de
rial:

O dispositivo que gera o clock é chamado de mestre.

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de
rial:

Os demais dispositivos são escravos.

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

Necessita de 3 fios (clock, transmissão e recepção): permite comunicação full duplex

egue lidar diretamente com 4 tipos de
rial:

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

Permite um quarto fio, para indicar o endereço do escravo (quando há mais de um deles)

segue lidar diretamente com 4 tipos de
rial:

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de
rial:

Possui dois fios (clock e dados): permite comunicação half-duplex

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

COMUNICAÇÃO

Todos estes exemplos seguem protocolos de comunicação.

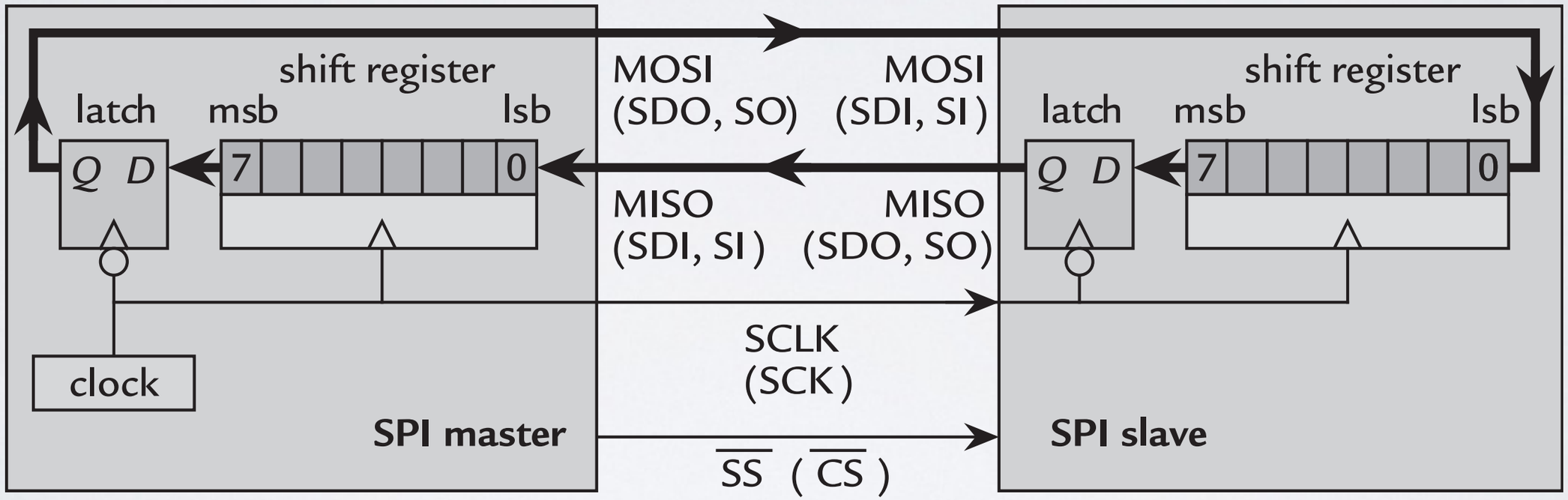
Algo como diferentes linguagens para o mesmo problema de
eber dados (0s e 1s).

segue lidar diretamente com 4 tipos de
rial:

- **Bit-banging**
- **SPI**
- **I2C**
- **Assíncrona**

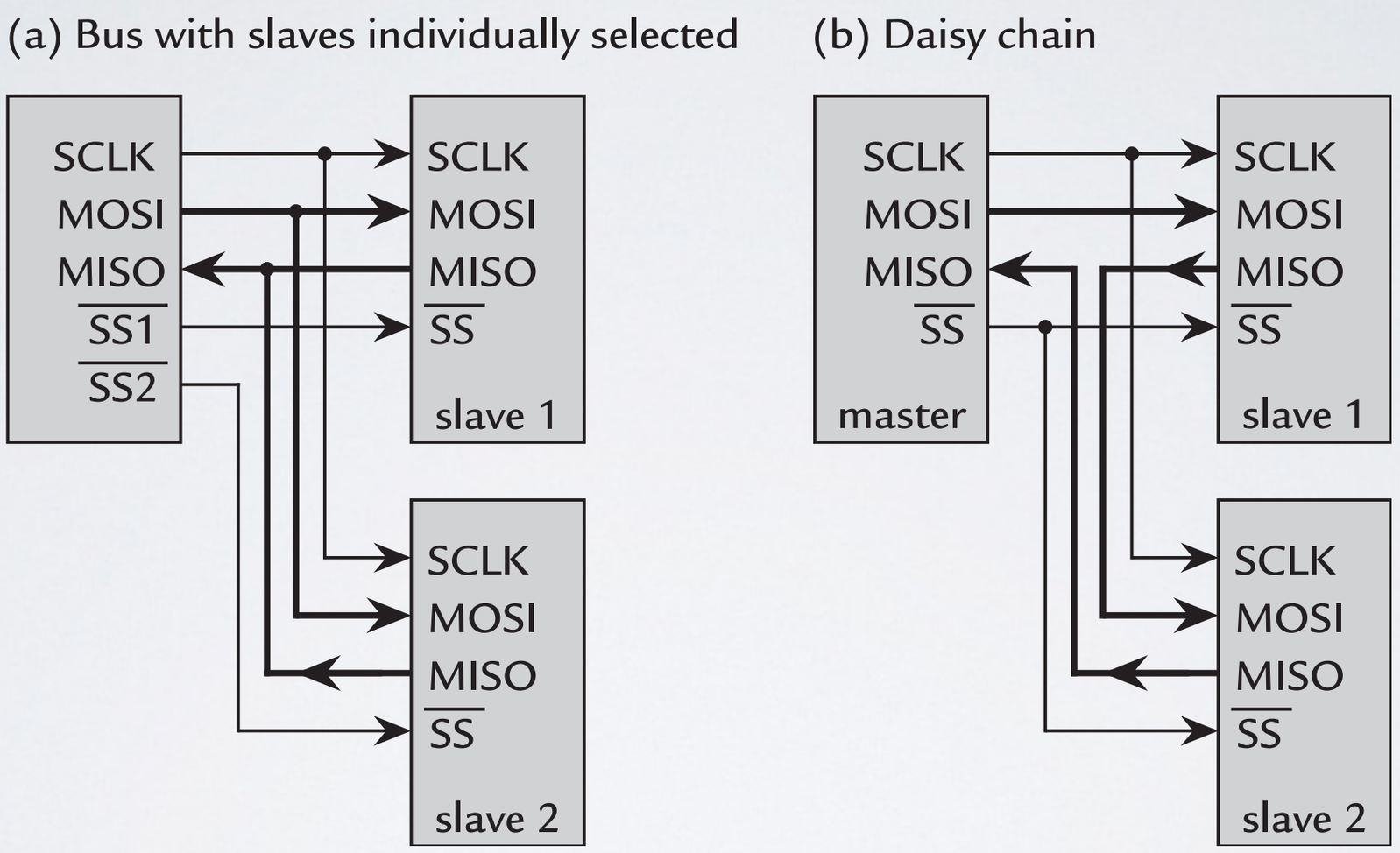
O fio de dados pode ser usado para indicar o endereço do escravo (quando há mais de um deles)

COMUNICAÇÃO



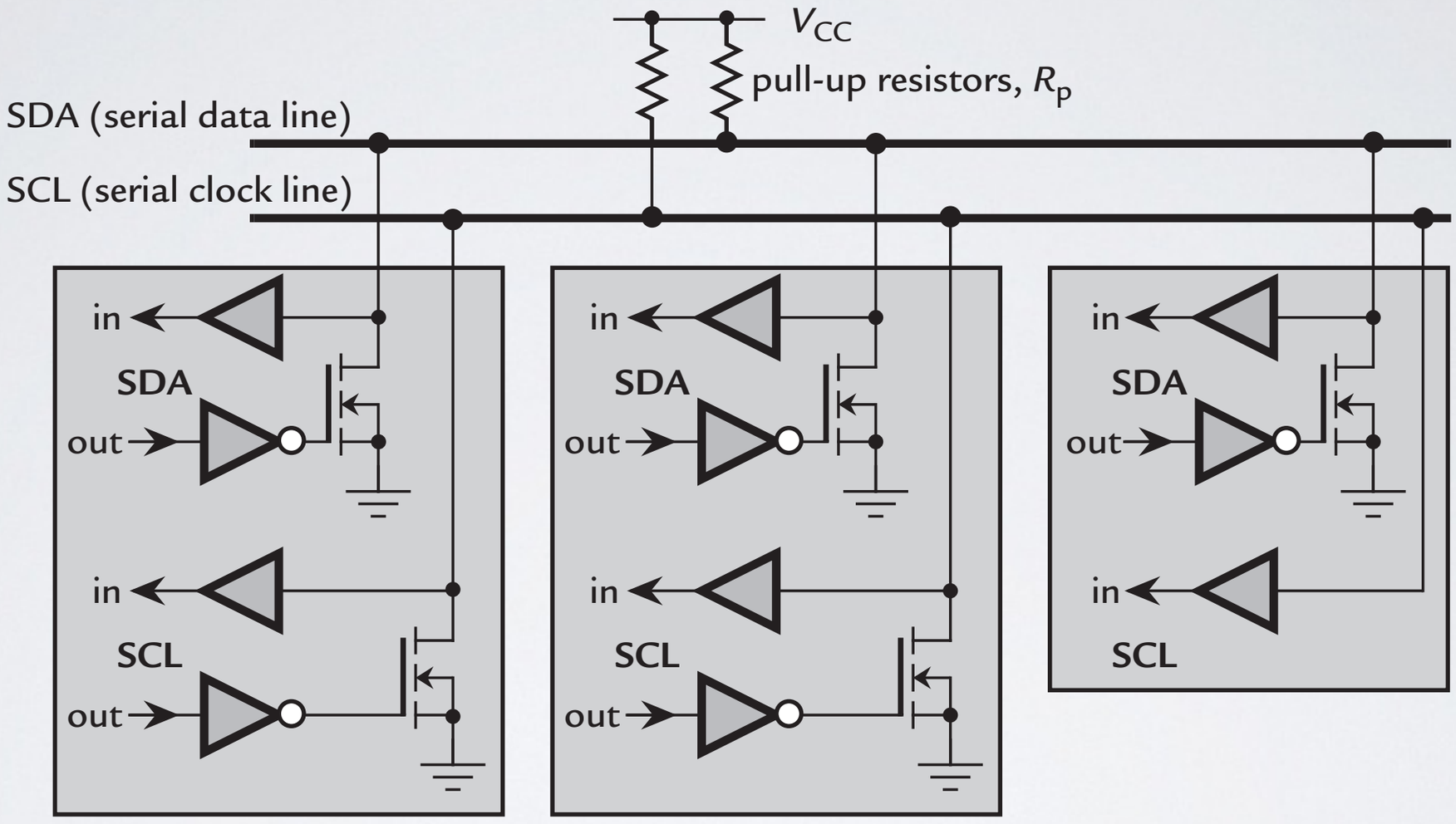
Comunicação SPI

COMUNICAÇÃO



Comunicação SPI com mais de um escravo

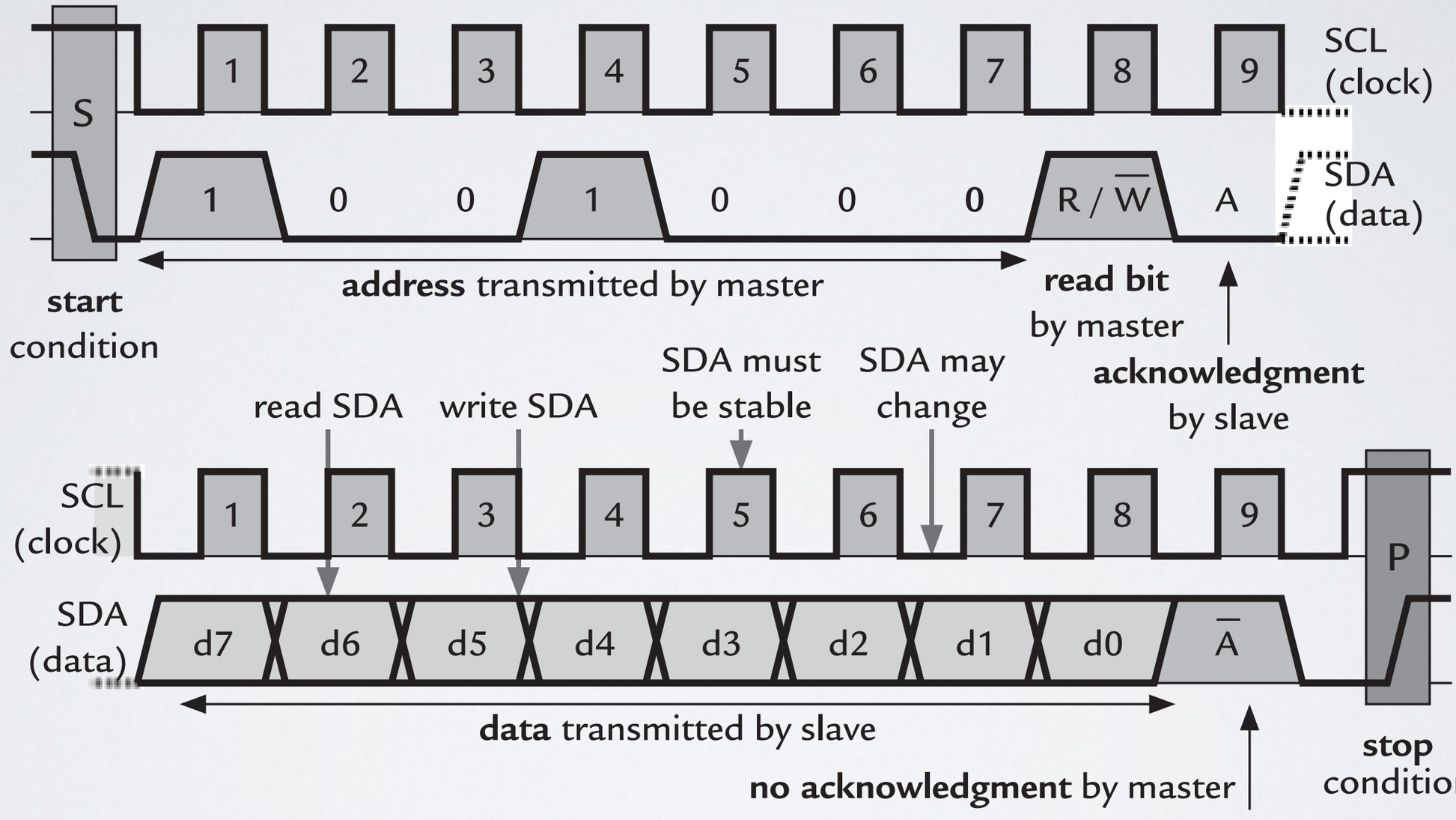
COMUNICAÇÃO



(a) master (b) slave (c) simpler slave

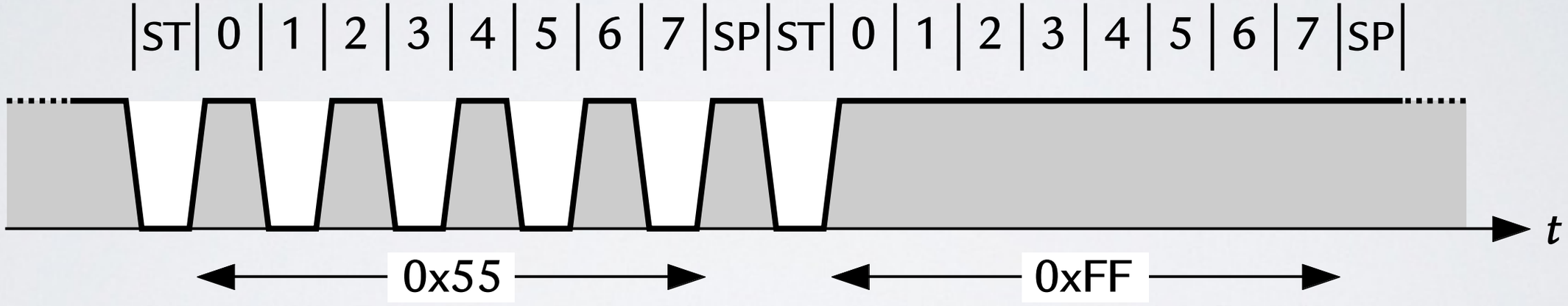
Comunicação I2C

COMUNICAÇÃO



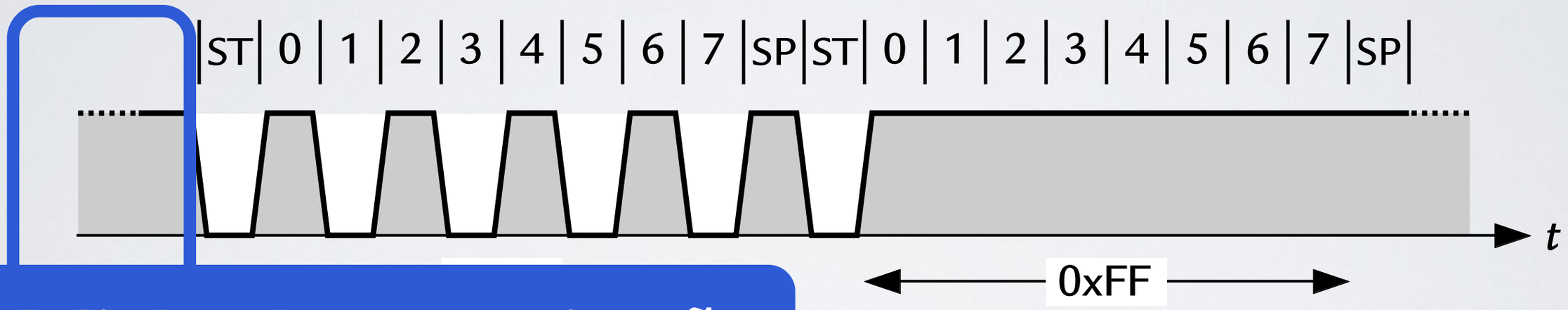
Protocolo I2C

COMUNICAÇÃO



Comunicação assíncrona

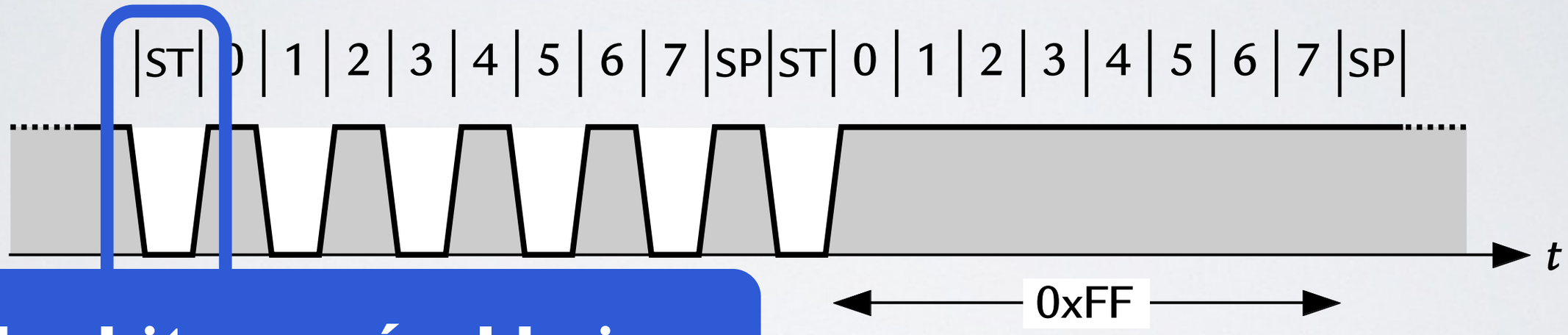
COMUNICAÇÃO



A linha de comunicação fica em nível alto enquanto não houver dados para transmitir

Comunicação assíncrona

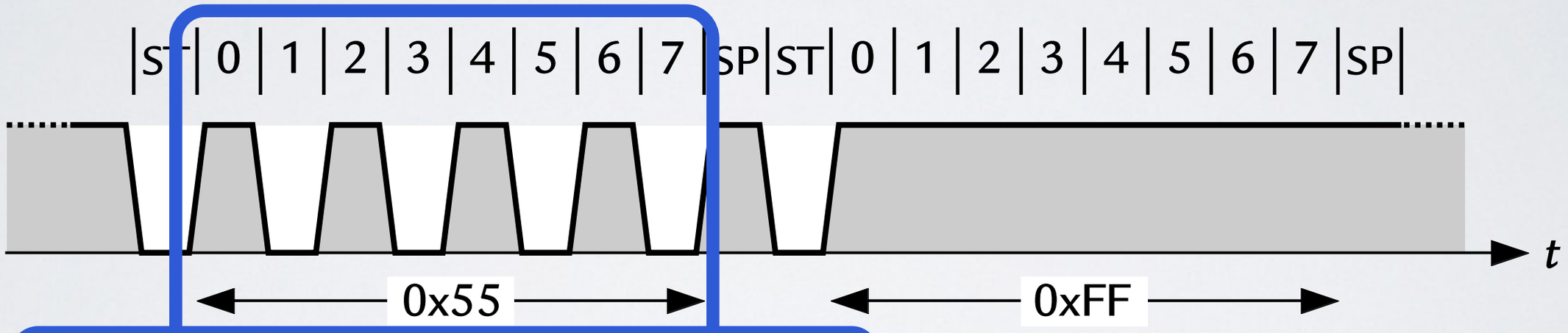
COMUNICAÇÃO



Um bit em nível baixo indica o começo da transmissão (START bit)

Comunicação assíncrona

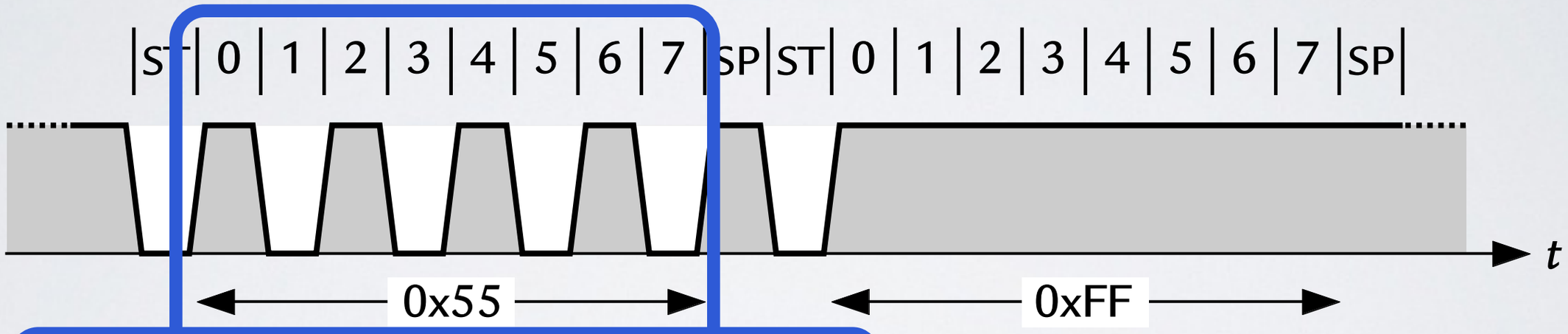
COMUNICAÇÃO



O byte de informação é enviado serialmente (neste caso, 0x55)

Comunicação assíncrona

COMUNICAÇÃO



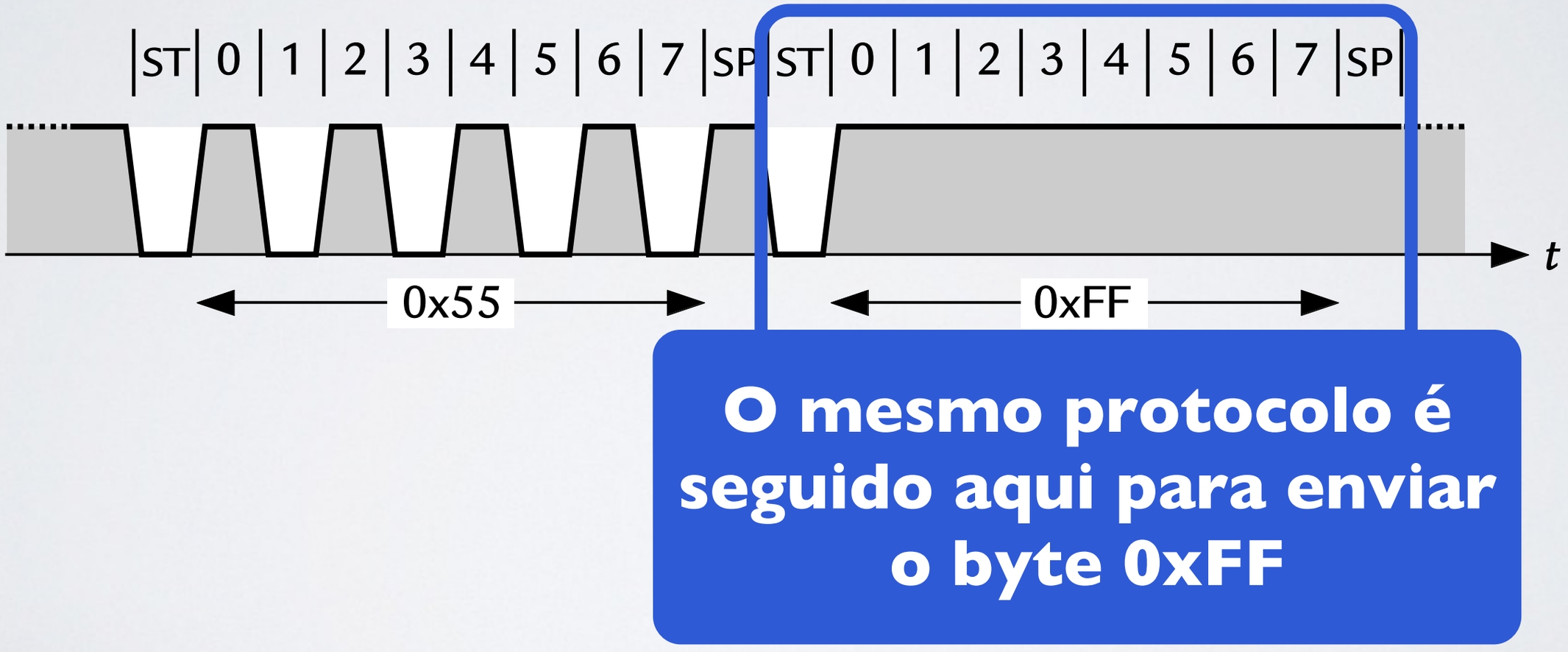
A ordem dos bits enviados deve ser determinada previamente (LSB ou MSB)

assíncrona

COMUNICAÇÃO

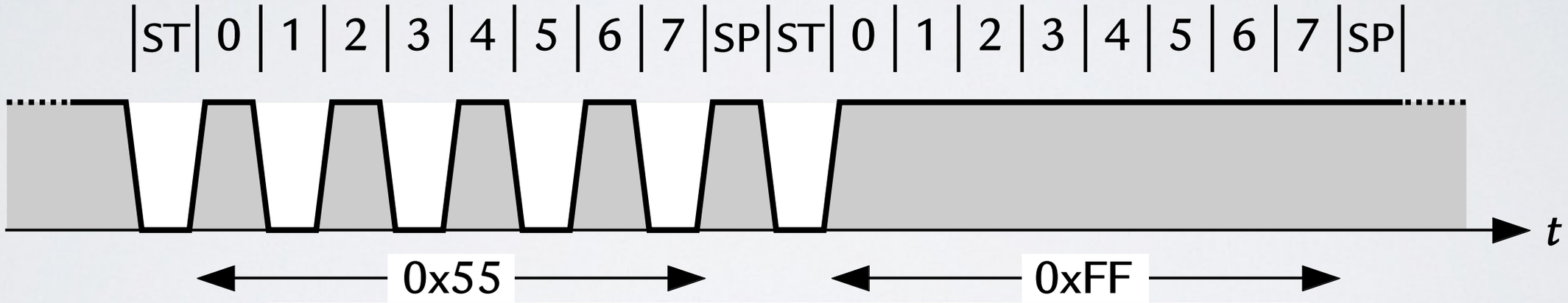
Comunicação assíncrona

COMUNICAÇÃO



Comunicação assíncrona

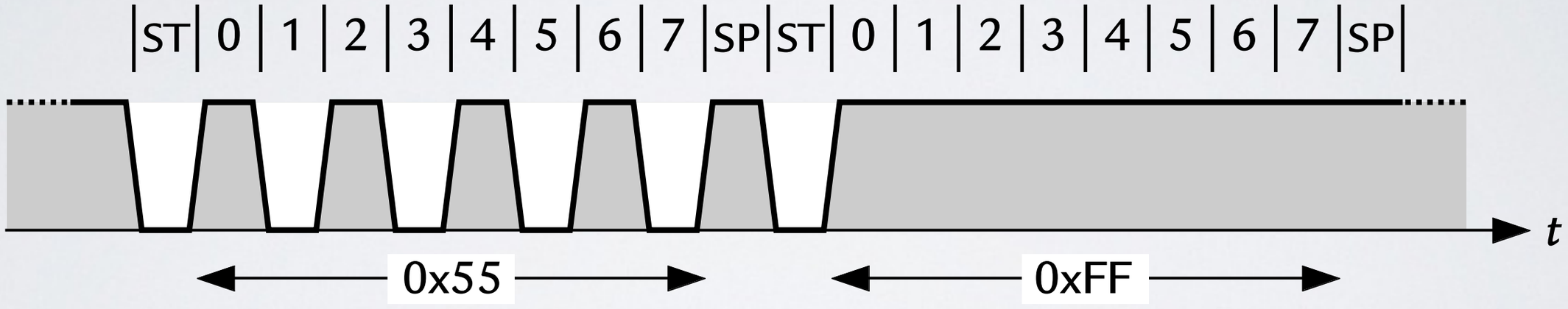
COMUNICAÇÃO



Não há sinal de clock. A temporização dos bits deve ser previamente conhecida pelo transmissor e pelo receptor

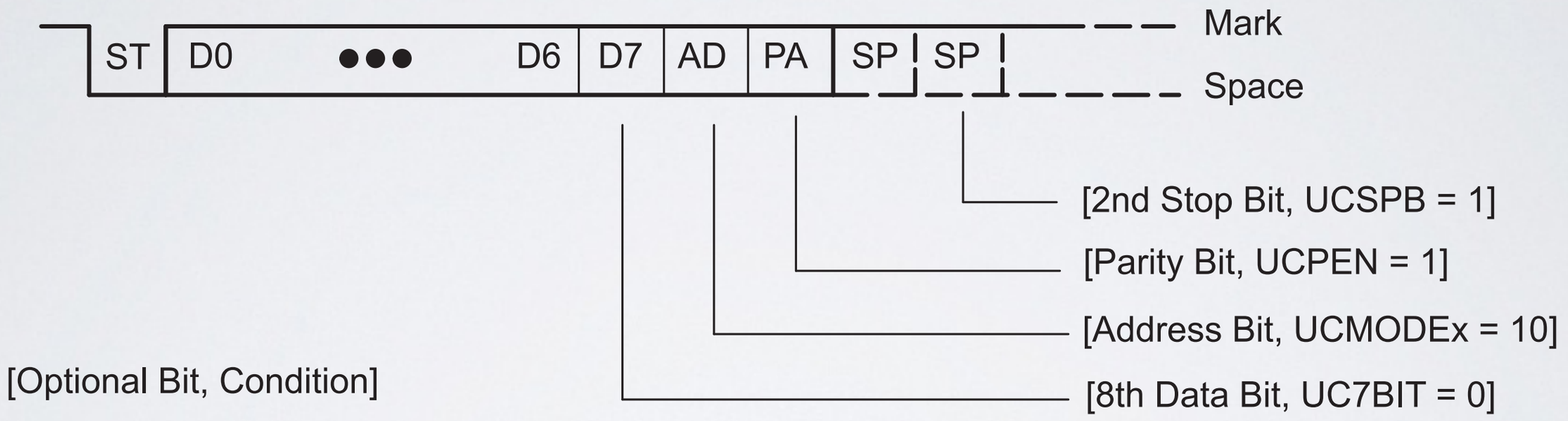
Comunicação assíncrona

COMUNICAÇÃO



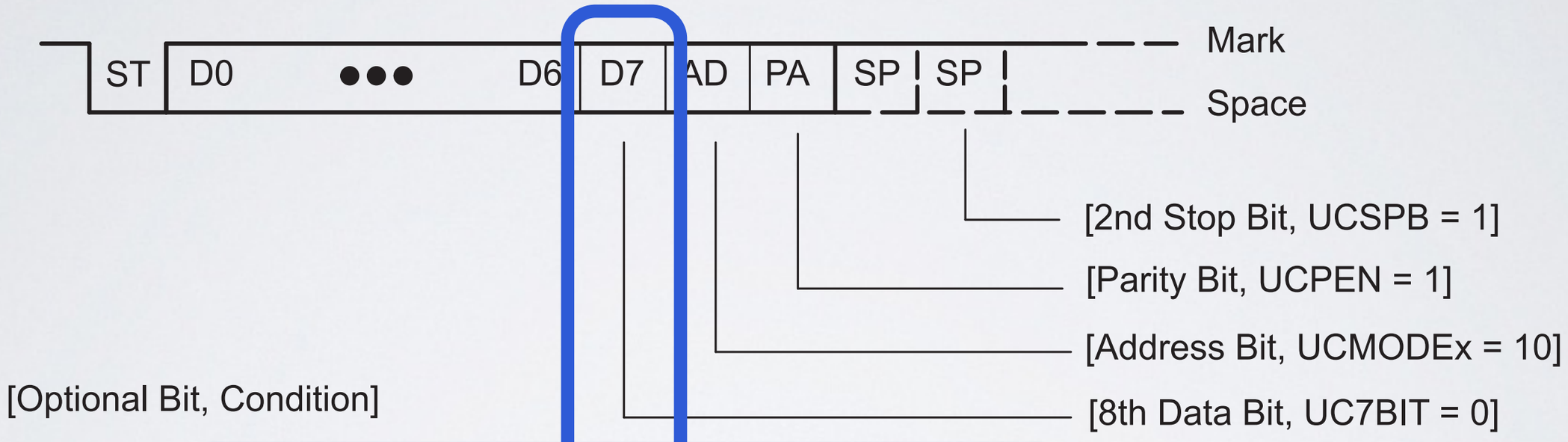
A taxa de transmissão é chamada de baud rate. Ela é diferente da taxa de dados, já que o protocolo prevê bits extra, como o START e o STOP.

COMUNICAÇÃO



Opções para comunicação assíncrona no MSP430

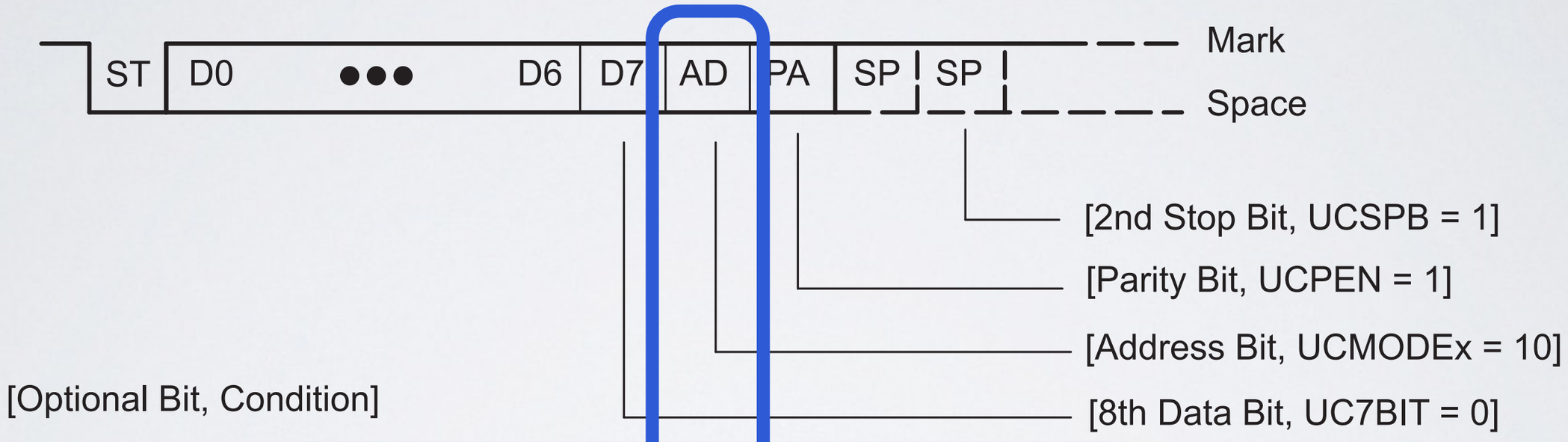
COMUNICAÇÃO



Pode-se enviar 7 ou 8 bits de informação (caracteres ASCII, por exemplo, têm somente 7 bits)

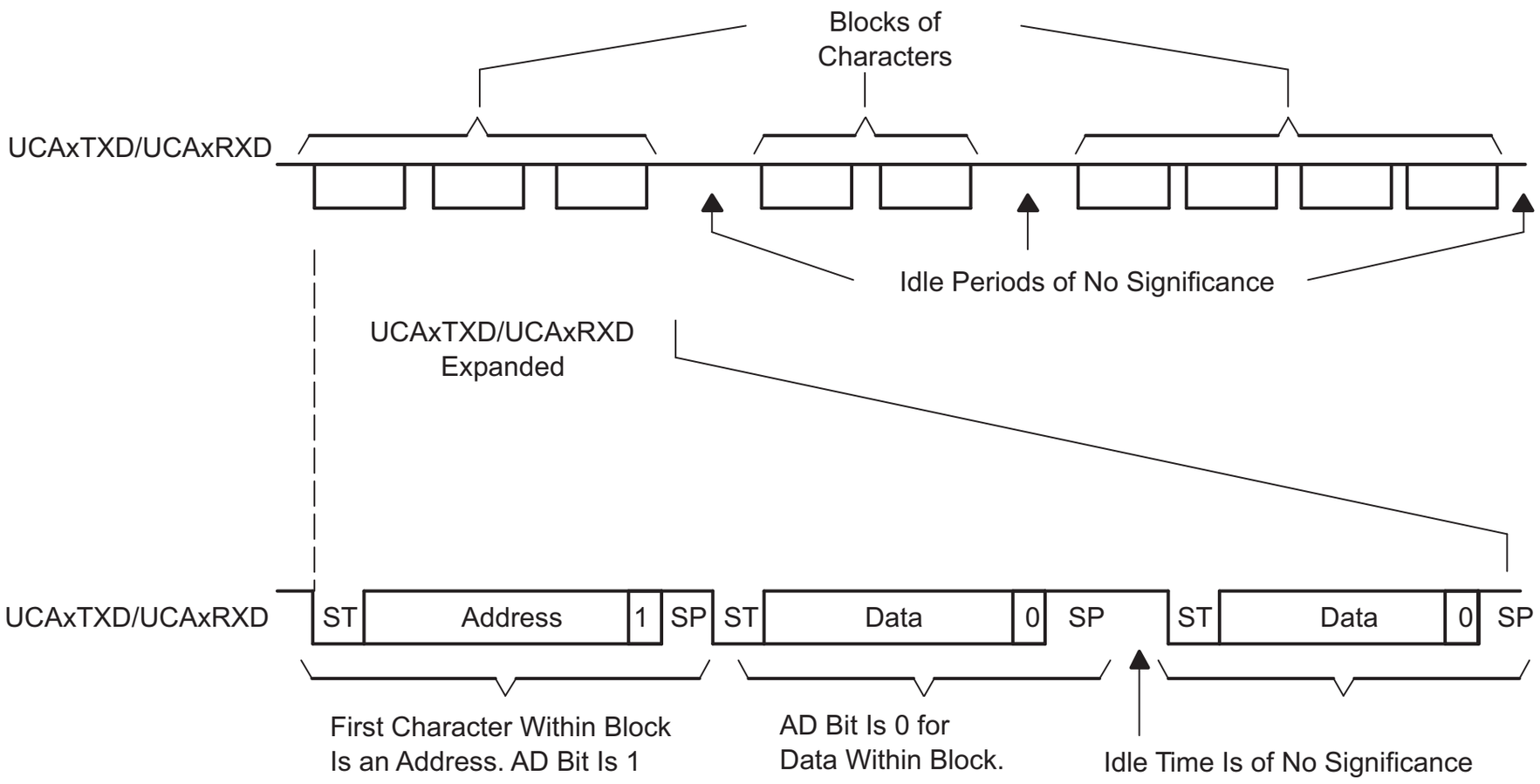
Op ona no MSP430

COMUNICAÇÃO



Pode-se acrescentar o envio de endereço, no caso de múltiplos transmissores e receptores

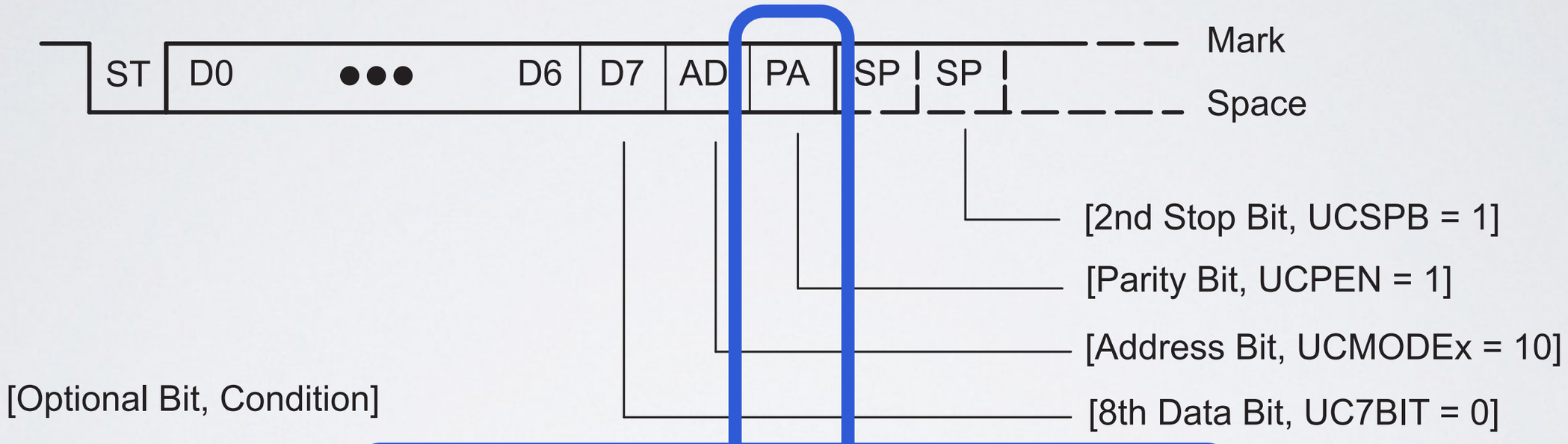
Opçõ a no MSP430



Pode-se acrescentar o envio de endereço, no caso de múltiplos transmissores e receptores

Opçõ a no MSP430

COMUNICAÇÃO



Pode-se enviar um bit de paridade, para o receptor conferir se houve erro na transmissão

Opções [illegible] MSP430

COMUNICAÇÃO

Pode-se enviar um segundo bit de STOP, para sistemas mais lentos não perderem o sincronismo

Opções para c 430

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

- 0 Parity disabled.
- 1 Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.

UCPAR Bit 6 Parity select. UCPAR is not used when parity is disabled.

- 0 Odd parity
- 1 Even parity

UCMSB Bit 5 MSB first select. Controls the direction of the receive and transmit shift register.

- 0 LSB first
- 1 MSB first

UC7BIT Bit 4 Character length. Selects 7-bit or 8-bit character length.

- 0 8-bit data
- 1 7-bit data

UCSPB Bit 3 Stop bit select. Number of stop bits.

- 0 One stop bit
- 1 Two stop bits

UCMODEx Bits 2-1 USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0.

- 00 UART mode
- 01 Idle-line multiprocessor mode
- 10 Address-bit multiprocessor mode
- 11 UART mode with automatic baud rate detection

UCSYNC Bit 0 Synchronous mode enable

- 0 Asynchronous mode
- 1 Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

Paridade

7	6	5	2	1	0
UCPEN	UCPAR	UCM	UCMODEx		UCSYNC
rw-0	rw-0	rw-	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

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- 01 Idle-line multiprocessor mode
- 10 Address-bit multiprocessor mode
- 11 UART mode with automatic baud rate detection

UCSYNC Bit 0 Synchronous mode enable

- 0 Asynchronous mode
- 1 Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Paridade par ou ímpar

UCPEN	Bit 7	Parity enable
	0	Parit
	1	Parit D) and expected (UCAxRXD). In address-bit multi in the parity calculation
UCPAR	Bit 6	Parity select. UCPAR is not used when parity is disabled.
	0	Odd parity
	1	Even parity
UCMSB	Bit 5	MSB first select. Controls the direction of the receive and transmit shift register.
	0	LSB first
	1	MSB first
UC7BIT	Bit 4	Character length. Selects 7-bit or 8-bit character length.
	0	8-bit data
	1	7-bit data
UCSPB	Bit 3	Stop bit select. Number of stop bits.
	0	One stop bit
	1	Two stop bits
UCMODEx	Bits 2-1	USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0.
	00	UART mode
	01	Idle-line multiprocessor mode
	10	Address-bit multiprocessor mode
	11	UART mode with automatic baud rate detection
UCSYNC	Bit 0	Synchronous mode enable
	0	Asynchronous mode
	1	Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

0 Parity disabled.

UCAxRXD). In address-bit
lation.

UCPAR Bit 6

Ordem de envio:
LSB->MSB ou vice-versa

UCMSB Bit 5 MSB first select. Controls the direction of the receive and transmit shift register.

0 LSB first

1 MSB first

UC7BIT Bit 4 Character length. Selects 7-bit or 8-bit character length.

0 8-bit data

1 7-bit data

UCSPB Bit 3 Stop bit select. Number of stop bits.

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1 Two stop bits

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10 Address-bit multiprocessor mode

11 UART mode with automatic baud rate detection

UCSYNC Bit 0 Synchronous mode enable

0 Asynchronous mode

1 Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

0 Parity disabled.

1 Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.

UCPAR Bit 6 Parity select. UCPAR is not used when parity is disabled.

UCMSB Bit 5 ster.

Tamanho dos dados:
7 ou 8 bits

UC7BIT Bit 4 Character length. Selects 7-bit or 8-bit character length.

0 8-bit data

1 7-bit data

UCSPB Bit 3 Stop bit select. Number of stop bits.

0 One stop bit

1 Two stop bits

UCMODEx Bits 2-1 USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0.

00 UART mode

01 Idle-line multiprocessor mode

10 Address-bit multiprocessor mode

11 UART mode with automatic baud rate detection

UCSYNC Bit 0 Synchronous mode enable

0 Asynchronous mode

1 Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

0 Parity disabled.

1 Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.

UCPAR Bit 6 Parity select. UCPAR is not used when parity is disabled.

0 Odd parity

1 Even parity

UCMSB Bit 5 MSB first select. Controls the direction of the receive and transmit shift register.

UC7BIT Bit 4

Bits de STOP: 1 ou 2

UCSPB Bit 3 Stop bit select. Number of stop bits.

0 One stop bit

1 Two stop bits

UCMODEx Bits 2-1 USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0.

00 UART mode

01 Idle-line multiprocessor mode

10 Address-bit multiprocessor mode

11 UART mode with automatic baud rate detection

UCSYNC Bit 0 Synchronous mode enable

0 Asynchronous mode

1 Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

- 0 Parity disabled.
- 1 Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.

UCPAR Bit 6 Parity select. UCPAR is not used when parity is disabled.

- 0 Odd parity

UCMSB

UC7BIT

UCSPB

Modos de operação assíncrona:
0 - modo comum
1 e 2 - modo com múltiplos escravos
3 - modo de detecção automática de baud rate

UCMODEx Bits 2-1 USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0.

- 00 UART mode
- 01 Idle-line multiprocessor mode
- 10 Address-bit multiprocessor mode
- 11 UART mode with automatic baud rate detection

UCSYNC Bit 0 Synchronous mode enable

- 0 Asynchronous mode
- 1 Synchronous mode

15.4.1 UCAxCTL0, USCI_Ax Control Register 0

7	6	5	4	3	2	1	0
UCPEN	**UCPAR**	**UCMSB**	**UC7BIT**	**UCSPB**	**UCMODEx**		**UCSYNC**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

UCPEN Bit 7 Parity enable

0 Parity disabled.

1 Parity enabled. Parity bit is generated (UCAxTXD) and expected (UCAxRXD). In address-bit multiprocessor mode, the address bit is included in the parity calculation.

UCPAR Bit 6 Parity select. UCPAR is not used when parity is disabled.

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UC7BIT Bit 4 Character length. Selects 7-bit or 8-bit character length.

0 8-bit data

1 7-bit data

UCSPB Bit 3 Stop bit select. Number of stop bits.

0 One stop bit

1 Two stop bits

UCMODEx Bits 2-1 USCI mode. The UCMODEx bits select the asynchronous mode when UCSYNC = 0.

0

0

1

UCSYNC Bit 0 Synchronous mode enable

0 Asynchronous mode

1 Synchronous mode

Habilitar modo assíncrono

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		**UCRXEIE**	**UCBRKIE**	**UCDORM**	**UCTXADDR**	**UCTXBRK**	**UCSWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

- 00 UCLK
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

UCRXEIE Bit 5 Receive erroneous-character interrupt-enable

- 0 Erroneous characters rejected and UCAxRXIFG is not set
- 1 Erroneous characters received will set UCAxRXIFG

UCBRKIE Bit 4 Receive break character interrupt-enable

- 0 Received break characters do not set UCAxRXIFG.
- 1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.

- 0 Not dormant. All received characters will set UCAxRXIFG.
- 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.

- 0 Next frame transmitted is data
- 1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.

- 0 Next frame transmitted is not a break
- 1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable

- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

- 00 UCLK
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

UCRXEIE Bit 5

UCBRKIE Bit 4

Fonte do sinal de clock para o modo assíncrono

- 1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.

- 0 Not dormant. All received characters will set UCAxRXIFG.
- 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.

- 0 Next frame transmitted is data
- 1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.

- 0 Next frame transmitted is not a break
- 1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable

- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx						UCTXBRK	UCSWRST
rw-0	rw-0					rw-0	rw-1

Habilitar tratamento de erros de recepção de dados (via paridade)

UCSSELx	Bits 7-6	
UCRXEIE	Bit 5	Receive erroneous-character interrupt-enable 0 Erroneous characters rejected and UCAxRXIFG is not set 1 Erroneous characters received will set UCAxRXIFG
UCBRKIE	Bit 4	Receive break character interrupt enable 0 Received break characters do not set UCAxRXIFG. 1 Received break characters set UCAxRXIFG.
UCDORM	Bit 3	Dormant. Puts USCI into sleep mode. 0 Not dormant. All received characters will set UCAxRXIFG. 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.
UCTXADDR	Bit 2	Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode. 0 Next frame transmitted is data 1 Next frame transmitted is an address
UCTXBRK	Bit 1	Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer. 0 Next frame transmitted is not a break 1 Next frame transmitted is a break or a break/synch
UCSWRST	Bit 0	Software reset enable 0 Disabled. USCI reset released for operation. 1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

Habilitar quebra de envio de dados (via recepção de pacote todo nulo, exceto pelo START bit)

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

UCRXEIE E

UCBRKIE Bit 4 Receive break character interrupt-enable
- 0 Received break characters do not set UCAxRXIFG.
- 1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.
- 0 Not dormant. All received characters will set UCAxRXIFG.
- 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.
- 0 Next frame transmitted is data
- 1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.
- 0 Next frame transmitted is not a break
- 1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable
- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		**UCRXEIE**	**UCBRKIE**	**UCDORM**	**UCTXADDR**	**UCTXBRK**	**UCSWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

00 UCLK

01 ACLK

10 SMCLK

UCRXEIE E

UCBRKIE E

Habilitar hibernação em caso de endereço errado

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.

0 Not dormant. All received characters will set UCAxRXIFG.

1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.

0 Next frame transmitted is data

1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.

0 Next frame transmitted is not a break

1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable

0 Disabled. USCI reset released for operation.

1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		**UCRXEIE**	**UCBRKIE**	**UCDORM**	**UCTXADDR**	**UCTXBRK**	**UCSWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

- 00 UCLK
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

UCRXEIE Bit 5 Receive erroneous-character interrupt-enable

- 0 Erroneous characters rejected and UCAxRXIFG is not set
- 1 Erroneous characters received will set UCAxRXIFG

UCBRKIE Bit 4 Receive break character interrupt-enable

- 0 Received break characters do not set UCAxRXIFG.
- 1 Received break characters set UCAxRXIFG.

UCDORM B

Transmitir dados ou endereço

will set
ation of a break

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.

- 0 Next frame transmitted is data
- 1 Next frame transmitted is an address

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.

- 0 Next frame transmitted is not a break
- 1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable

- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		**UCRXEIE**	**UCBRKIE**	**UCDORM**	**UCTXADDR**	**UCTXBRK**	**UCSWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

- 00 UCLK
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

UCRXEIE Bit 5 Receive erroneous-character interrupt-enable

- 0 Erroneous characters rejected and UCAxRXIFG is not set
- 1 Erroneous characters received will set UCAxRXIFG

UCBRKIE Bit 4 Receive break character interrupt-enable

- 0 Received break characters do not set UCAxRXIFG.
- 1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.

- 0 Not dormant. All received characters will set UCAxRXIFG.
- 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set

ation of a break

UCTXADDR E he selected

Transmitir caractere de quebra de envio de dados

UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automatic baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.

- 0 Next frame transmitted is not a break
- 1 Next frame transmitted is a break or a break/synch

UCSWRST Bit 0 Software reset enable

- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.2 UCAxCTL1, USCI_Ax Control Register 1

7	6	5	4	3	2	1	0
UCSSELx		**UCRXEIE**	**UCBRKIE**	**UCDORM**	**UCTXADDR**	**UCTXBRK**	**UCSWRST**
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1

UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock.

- 00 UCLK
- 01 ACLK
- 10 SMCLK
- 11 SMCLK

UCRXEIE Bit 5 Receive erroneous-character interrupt-enable

- 0 Erroneous characters rejected and UCAxRXIFG is not set
- 1 Erroneous characters received will set UCAxRXIFG

UCBRKIE Bit 4 Receive break character interrupt-enable

- 0 Received break characters do not set UCAxRXIFG.
- 1 Received break characters set UCAxRXIFG.

UCDORM Bit 3 Dormant. Puts USCI into sleep mode.

- 0 Not dormant. All received characters will set UCAxRXIFG.
- 1 Dormant. Only characters that are preceded by an idle-line or with address bit set will set UCAxRXIFG. In UART mode with automatic baud rate detection only the combination of a break and synch field will set UCAxRXIFG.

UCTXADDR Bit 2 Transmit address. Next frame to be transmitted will be marked as address depending on the selected multiprocessor mode.

- 0 Next frame transmitted is data

UCTXBRK B… …e with automatic …k/synch fields.

Resetar todo o sistema de comunicação via software

UCSWRST Bit 0 Software reset enable

- 0 Disabled. USCI reset released for operation.
- 1 Enabled. USCI logic held in reset state.

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register

7	6	5	4	3	2	1	0
UCRXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCRXBUFx Bits 7-0 The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCAxRXBUF resets the receive-error bits, the UCADDR or UCIDLE bit, and UCAxRXIFG. In 7-bit data mode, UCAxRXBUF is LSB justified and the MSB is always reset.

15.4.8 UCAxTXBUF, USCI_Ax Transmit Buffer Register

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCTXBUFx Bits 7-0 The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

Buffer de recepção de dados assíncronos

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register

7	6	5	4	3	2	1	0
UCRXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCRXBUFx	Bits 7-0	The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCAxRXBUF resets the receive-error bits, the UCADDR or UCIDLE bit, and UCAxRXIFG. In 7-bit data mode, UCAxRXBUF is LSB justified and the MSB is always reset.

15.4.8 UCAxTXBUF, USCI_Ax Transmit Buffer Register

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCTXBUFx	Bits 7-0	The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register

7	6	5	4	3	2	1	0
UCRXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCRXBUFx Bi… …the receive shift …t, and UCAxRXIFG.

Buffer de transmissão de dados assíncronos

15.4.8 UCAxTXBUF, USCI_Ax Transmit Buffer Register

7	6	5	4	3	2	1	0
UCTXBUFx							
rw	rw	rw	rw	rw	rw	rw	rw

UCTXBUFx Bits 7-0 The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

Table 15-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum TX Error [%]		Maximum RX Error [%]	
32,768	1200	27	2	0	-2.8	1.4	-5.9	2.0
32,768	2400	13	6	0	-4.8	6.0	-9.7	8.3
32,768	4800	6	7	0	-12.1	5.7	-13.4	19.0
32,768	9600	3	3	0	-21.1	15.2	-44.3	21.3
1,048,576	9600	109	2	0	-0.2	0.7	-1.0	0.8
1,048,576	19200	54	5	0	-1.1	1.0	-1.5	2.5
1,048,576	38400	27	2	0	-2.8	1.4	-5.9	2.0
1,048,576	56000	18	6	0	-3.9	1.1	-4.6	5.7
1,048,576	115200	9	1	0	-1.1	10.7	-11.5	11.3
1,048,576	128000	8	1	0	-8.9	7.5	-13.8	14.8
1,048,576	256000	4	1	0	-2.3	25.4	-13.4	38.8
1,000,000	9600	104	1	0	-0.5	0.6	-0.9	1.2
1,000,000	19200	52	0	0	-1.8	0	-2.6	0.9
1,000,000	38400	26	0	0	-1.8	0	-3.6	1.8
1,000,000	56000	17	7	0	-4.8	0.8	-8.0	3.2
1,000,000	115200	8	6	0	-7.8	6.4	-9.7	16.1
1,000,000	128000	7	7	0	-10.4	6.4	-18.0	11.6
1,000,000	256000	3	7	0	-29.6	0	-43.6	5.2
4,000,000	9600	416	6	0	-0.2	0.2	-0.2	0.4
4,000,000	19200	208	3	0	-0.2	0.5	-0.3	0.8
4,000,000	38400	104	1	0	-0.5	0.6	-0.9	1.2
4,000,000	56000	71	4	0	-0.6	1.0	-1.7	1.3
4,000,000	115200	34	6	0	-2.1	0.6	-2.5	3.1
4,000,000	128000	31	2	0	-0.8	1.6	-3.6	2.0
4,000,000	256000	15	5	0	-4.0	3.2	-8.4	5.2
8,000,000	9600	833	2	0	-0.1	0	-0.2	0.1
8,000,000	19200	416	6	0	-0.2	0.2	-0.2	0.4
8,000,000	38400	208	3	0	-0.2	0.5	-0.3	0.8
8,000,000	56000	142	7	0	-0.6	0.1	-0.7	0.8
8,000,000	115200	69	4	0	-0.6	0.8	-1.8	1.1
8,000,000	128000	62	4	0	-0.8	0	-1.2	1.2
8,000,000	256000	31	2	0	-0.8	1.6	-3.6	2.0
12,000,000	9600	1250	0	0	0	0	-0.05	0.05
12,000,000	19200	625	0	0	0	0	-0.2	0
12,000,000	38400	312	4	0	-0.2	0	-0.2	0.2
12,000,000	56000	214	2	0	-0.3	0.2	-0.4	0.5

Table 15-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum TX Error [%]		Maximum RX Error [%]	
32,768	1200	27	2	0	-2.8	1.4	-5.9	2.0
32,768	2400	13	6	0	-4.8	6.0	-9.7	8.3
32,768	4800	6	7	0	-12.1	5.7	-13.4	19.0
32,768	9600	3	3	0	-21.1	15.2	-44.3	21.3
1,048,576	9600	109	2	0	-0.2	0.7	-1.0	0.8
1,048,576	19200	54	5	0	-1.1	1.0	-1.5	2.5
1,048,576	38400	27	2	0	-2.8	1.4	-5.9	2.0
1,048,576	56000	18	6	0	-3.9	1.1	-4.6	5.7
1,048,576	115200	9	1	0	-1.1	10.7	-11.5	11.3
1,048,576	128000	8	1	0	-8.9	7.5	-13.8	14.8
1,048,576	256000	4	1	0	-2.3	25.4	-13.4	38.8
1,000,000	9600	104	1	0	-0.5	0.6	-0.9	1.2
1,000,000	19200	52	0	0	-1.8	0	-2.6	0.9
1,000,000	38400	26	0	0	-1.8	0	-3.6	1.8
1,000,000	56000	17	7	0	-4.8	0.8	-8.0	3.2
1,000,000	115200	8	6	0	-7.8	6.4	-9.7	16.1
1,000,000	128000	7	7	0	-10.4	6.4	-18.0	11.6
1,000,000	256000	3	7	0	-29.6	0	-43.6	5.2
4,000,000	9600	416	6	0	-0.2	0.2	-0.2	0.4
4,000,000	19200	208	3	0	-0.2	0.5	-0.3	0.8
4,000,000	38400	104	1	0	-0.5	0.6	-0.9	1.2
4,000,000	56000	71	4	0	-0.6	1.0	-1.7	1.3
4,000,000	115200	34	6	0	-2.1	0.6	-2.5	3.1
4,000,000	128000	31	2	0	-0.8	1.6	-3.6	2.0
4,000,000	256000	15	5	0	-4.0	3.2	-8.4	5.2
8,000,000	9600	833	2	0	-0.1	0	-0.2	0.1
8,000,000	19200	416	6	0	-0.2	0.2	-0.2	0.4
8,000,000	38400	208	3	0	-0.2	0.5	-0.3	0.8
8,000,000	56000	142	7	0	-0.6	0.1	-0.7	0.8
8,000,000	115200	69	4	0	-0.6	0.8	-1.8	1.1

Definição das baud rates mais comuns

Table 15-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0 (continued)

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum TX Error [%]		Maximum RX Error [%]	
12,000,000	115200	104	1	0	-0.5	0.6	-0.9	1.2
12,000,000	128000	93	6	0	-0.8	0	-1.5	0.4
12,000,000	256000	46	7	0	-1.9	0	-2.0	2.0
16,000,000	9600	1666	6	0	-0.05	0.05	-0.05	0.1
16,000,000	19200	833	2	0	-0.1	0.05	-0.2	0.1
16,000,000	38400	416	6	0	-0.2	0.2	-0.2	0.4
16,000,000	56000	285	6	0	-0.3	0.1	-0.5	0.2
16,000,000	115200	138	7	0	-0.7	0	-0.8	0.6
16,000,000	128000	125	0	0	0	0	-0.8	0
16,000,000	256000	62	4	0	-0.8	0	-1.2	1.2

Definição das baud rates mais comuns (continuação)

Table 15-5. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 1

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum TX Error [%]		Maximum RX Error [%]	
1,048,576	9600	6	0	13	-2.3	0	-2.2	0.8
1,048,576	19200	3	1	6	-4.6	3.2	-5.0	4.7
1,000,000	9600	6	0	8	-1.8	0	-2.2	0.4
1,000,000	19200	3	0	4	-1.8	0	-2.6	0.9
1,000,000	57600	1	7	0	-34.4	0	-33.4	0
4,000,000	9600	26	0	1	0	0.9	0	1.1
4,000,000	19200	13	0	0	-1.8	0	-1.9	0.2
4,000,000	38400	6	0	8	-1.8	0	-2.2	0.4
4,000,000	57600	4	5	3	-3.5	3.2	-1.8	6.4
4,000,000	115200	2	3	2	-2.1	4.8	-2.5	7.3
4,000,000	230400	1	7	0	-34.4	0	-33.4	0
8,000,000	9600	52	0	1	-0.4	0	-0.4	0.1
8,000,000	19200	26	0	1	0	0.9	0	1.1
8,000,000	38400	13	0	0	-1.8	0	-1.9	0.2
8,000,000	57600	8	0	11	0	0.88	0	1.6
8,000,000	115200	4	5	3	-3.5	3.2	-1.8	6.4
8,000,000	230400	2	3	2	-2.1	4.8	-2.5	7.3
8,000,000	460800	1	7	0	-34.4	0	-33.4	0
12,000,000	9600	78	0	2	0	0	-0.05	0.05
12,000,000	19200	39	0	1	0	0	0	0.2
12,000,000	38400	19	0	8	-1.8	0	-1.8	0.1
12,000,000	57600	13	0	0	-1.8	0	-1.9	0.2
12,000,000	115200	6	0	8	-1.8	0	-2.2	0.4
12,000,000	230400	3	0	4	-1.8	0	-2.6	0.9
16,000,000	9600	104	0	3	0	0.2	0	0.3
16,000,000	19200	52	0	1	-0.4	0	-0.4	0.1
16,000,000	38400	26	0	1	0	0.9	0	1.1
16,000,000	57600	17	0	6	0	0.9	-0.1	1.0
16,000,000	115200	8	0	11	0	0.9	0	1.6
16,000,000	230400	4	5	3	-3.5	3.2	-1.8	6.4
16,000,000	460800	2	3	2	-2.1	4.8	-2.5	7.3

Definição das baud rates mais comuns (continuação)