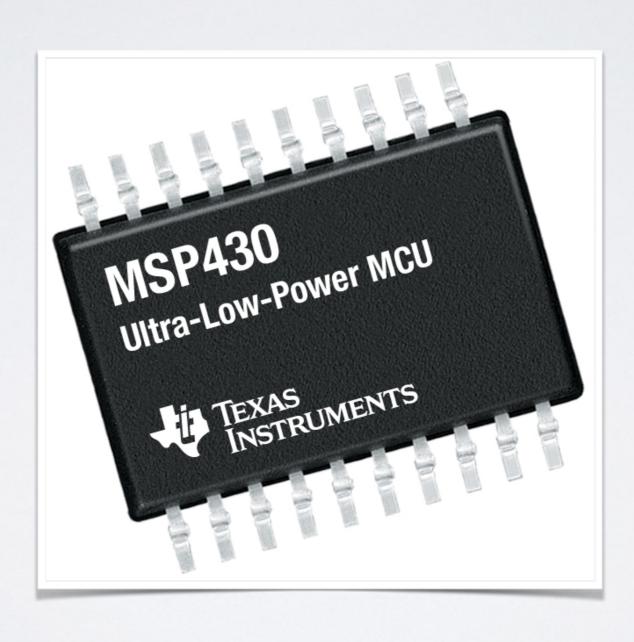
MICROPROCESSADORES E MICROCONTROLADORES



Diversos cenários:

Aparelhos ligados à internet

- Aparelhos ligados à internet
- Envio de dados do MSP430 para um computador pessoal

- Aparelhos ligados à internet
- Envio de dados do MSP430 para um computador pessoal
- Troca de dados entre dois MSP430

- Aparelhos ligados à internet
- Envio de dados do MSP430 para um computador pessoal
- Troca de dados entre dois MSP430
- Troca de dados entre um MSP430 e um chip de memória externa

Diversos cenários:

Aparelhos ligados à inte

Envio de dados do MSF

• Troca de dados entre d

 Troca de dados entre u externa USB Bluetooth Wifi Etc.

omputador pessoal

m chip de memória

Todos estes exemplos seguem protocolos de comunicação.

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

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Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de comunicação serial:

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de comunicação serial:

- Bit-banging
- SPI
- 12C
- Assíncrona

Software dedicado para realizar o protocolo desejado.

O MSP430 conseg comunicação serial:

os seguem protocolos de comunicação.

es linguagens para o mesmo problema de dados (0s e 1s).

lidar diretamente com 4 tipos de

- Bit-banging
- SPI
- 12C
- Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de comunicação serial:

Protocolos realizados por hardware dedicado.

• Bit-banging • SPI • I2C • Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de

Protocolos síncronos (o clock é enviado junto com os dados).

Rit-hanging

Bit-banging

• SPI

rial:

12C

Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de

O dispositivo que gera o clock é chamado de mestre.

- Bit-banging
- SPI

rial:

- 12C
- Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de

rial:

Os demais dispositivos são escravos.

- Bit-banging
- SPI
- 12C
- Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

Necessita de 3 fios (clock, transmissão e recepção): permite comunicação full duplex

egue lidar diretamente com 4 tipos de rial:

- Bit-banging
- SPI
- 12C
- Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

Permite um
quarto fio,
para indicar o
endereço do
escravo
(quando há
mais de um
deles)

quarto fio, regue lidar diretamente com 4 tipos de ara indicar o rial:

- Bit-banging
- SPI
- 12C
- Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

Algo como diferentes linguagens para o mesmo problema de transmitir e receber dados (0s e 1s).

O MSP430 consegue lidar diretamente com 4 tipos de

Possui dois fios (clock e dados): permite comunicação

half-duplex

- rial:
- Bit-banging
- SPI
- 12C
- Assíncrona

Todos estes exemplos seguem protocolos de comunicação.

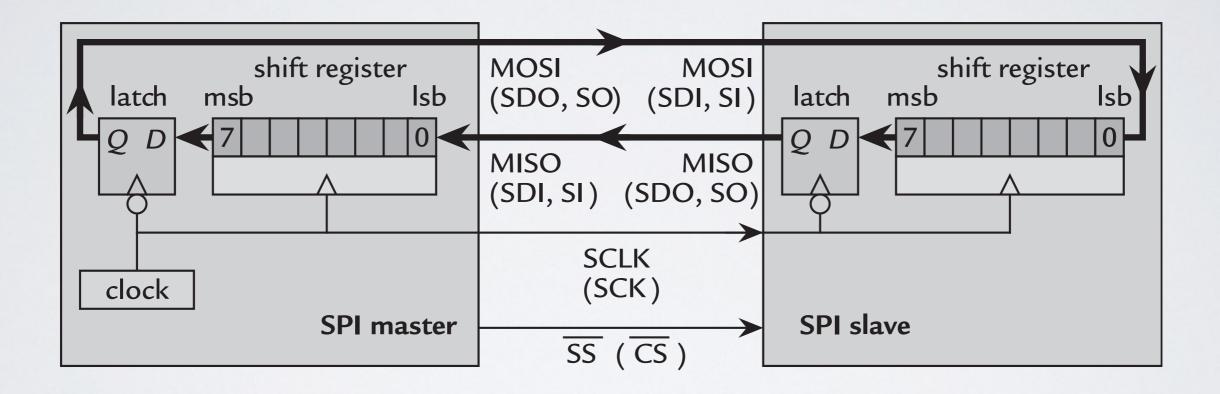
Algo como diferentes linguagens para o mesmo problema de

O fio de dados ber dados (0s e 1s).

pode ser usado para indicar o endereço do

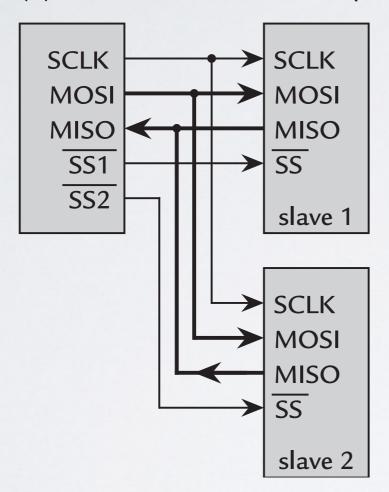
endereço do escravo (quando há mais de um deles) segue lidar diretamente com 4 tipos de rial:

- Bit-banging
- SPI
- 12C
- Assíncrona

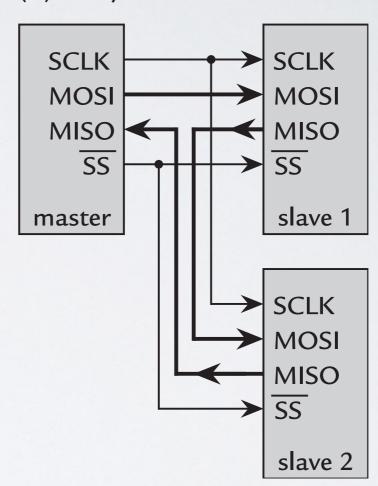


Comunicação SPI

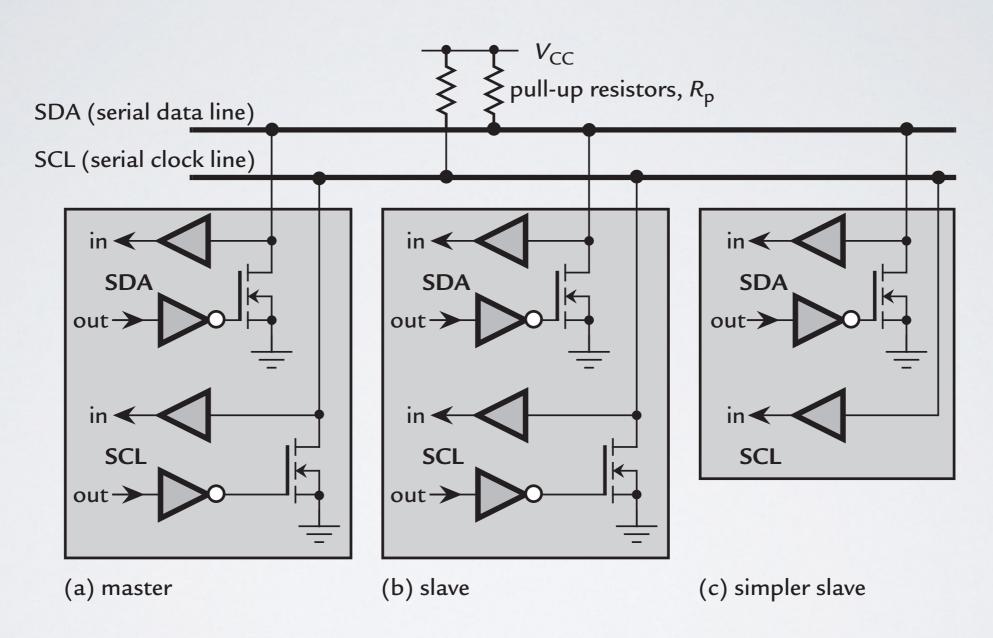
(a) Bus with slaves individually selected



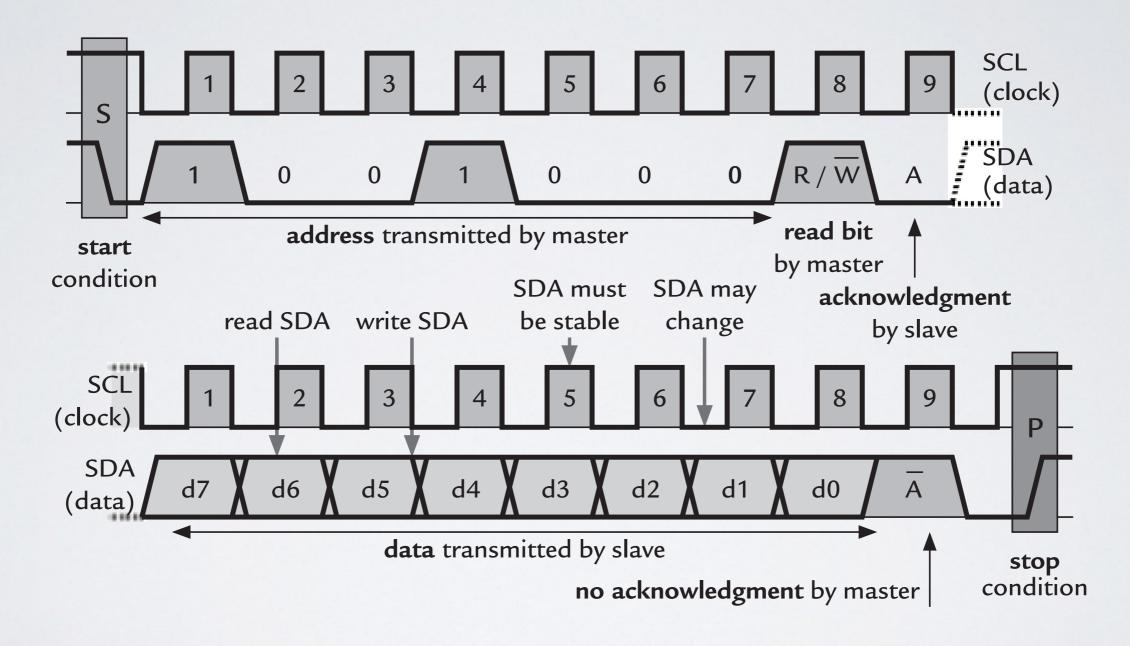
(b) Daisy chain



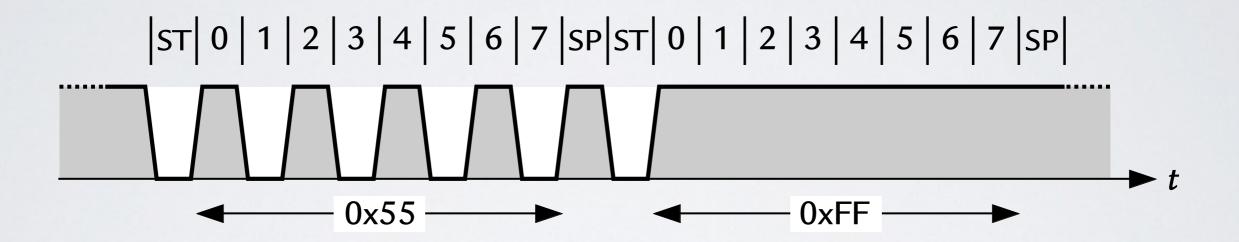
Comunicação SPI com mais de um escravo

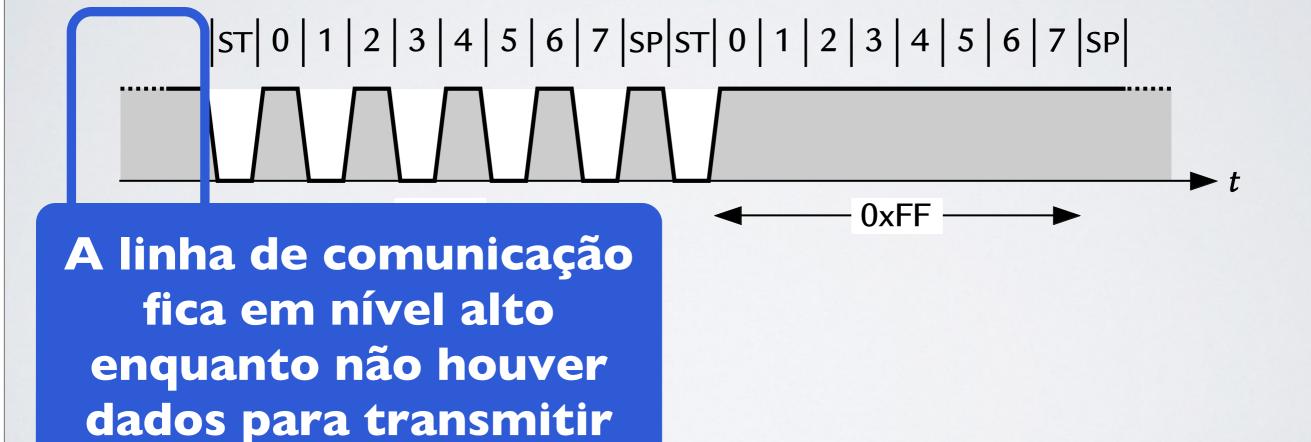


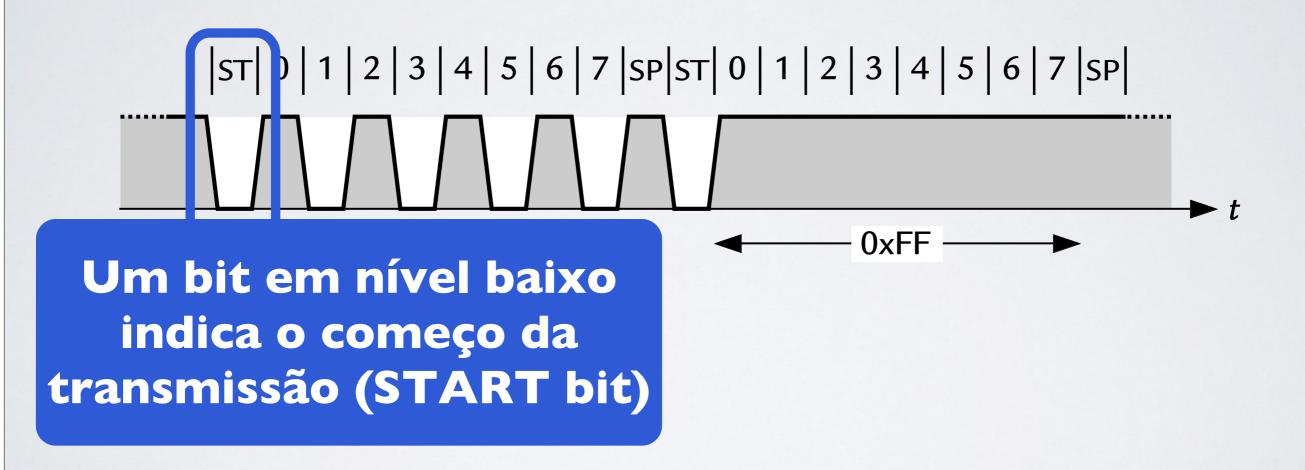
Comunicação I2C

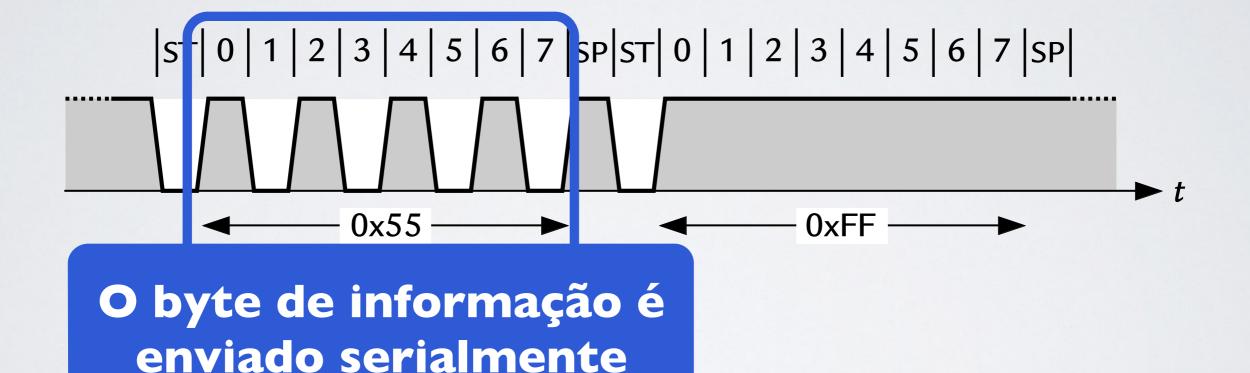


Protocolo I2C



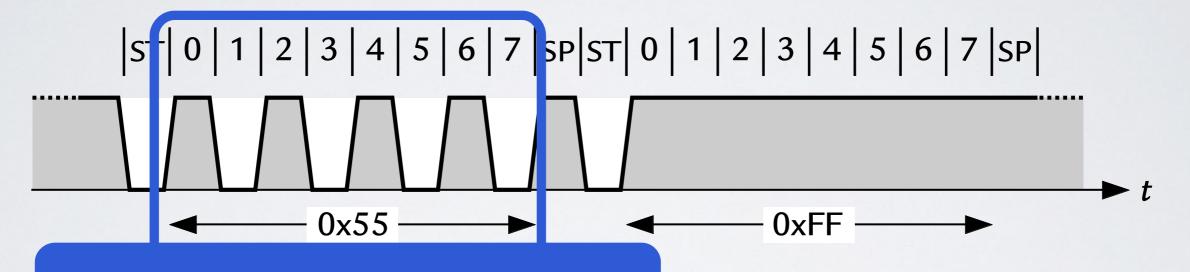






Comunicação assíncrona

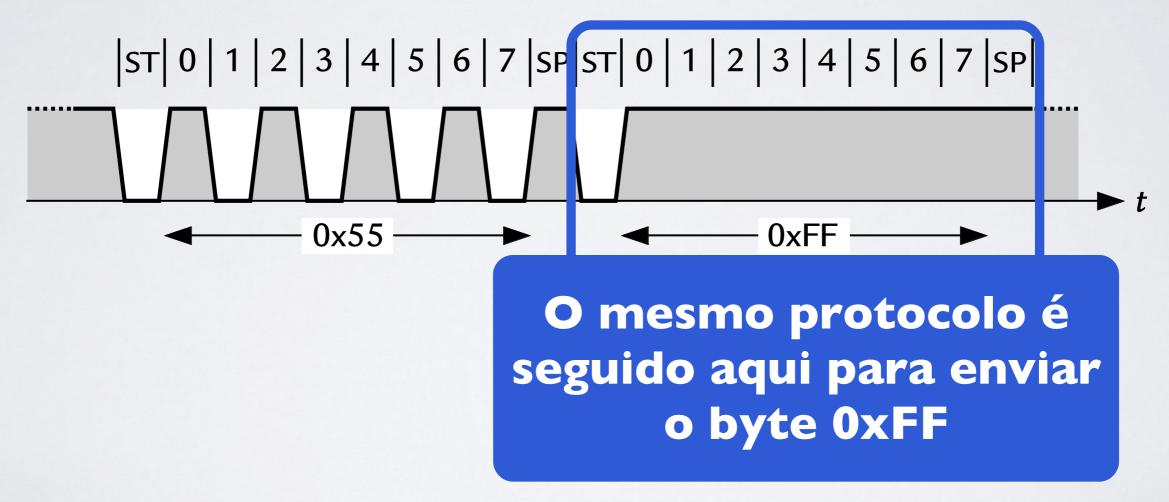
(neste caso, 0x55)

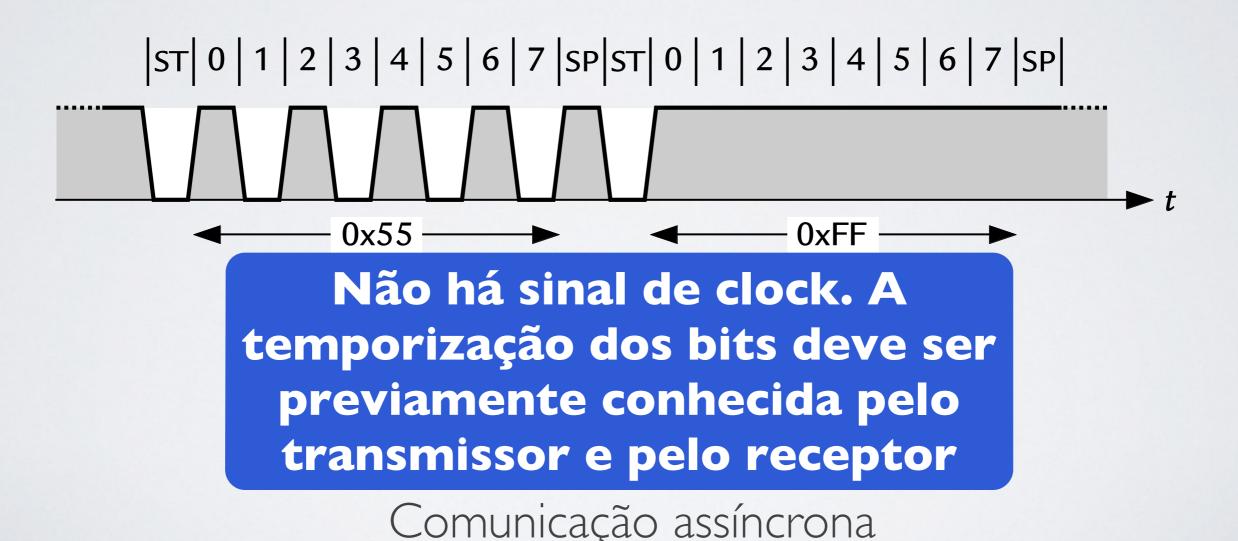


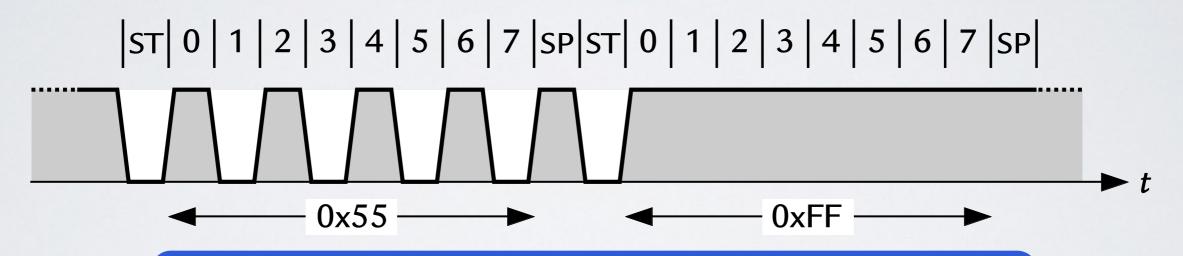
A ordem dos bits enviados deve ser determinada previamente (LSB ou MSB)

assíncrona

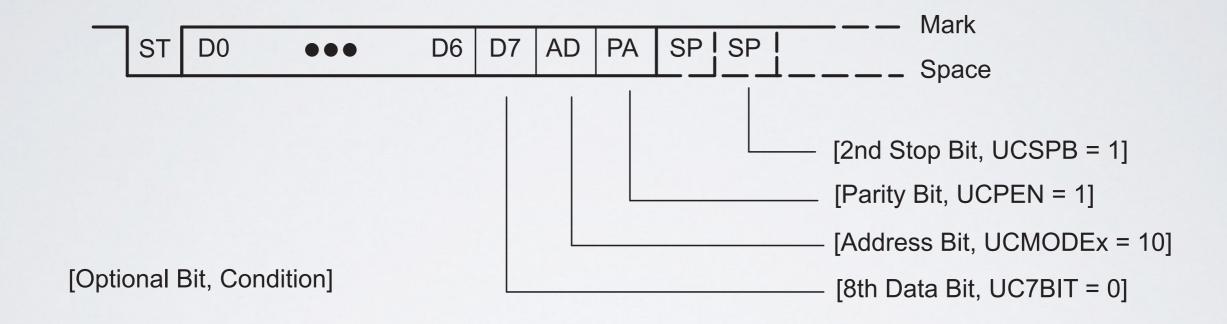




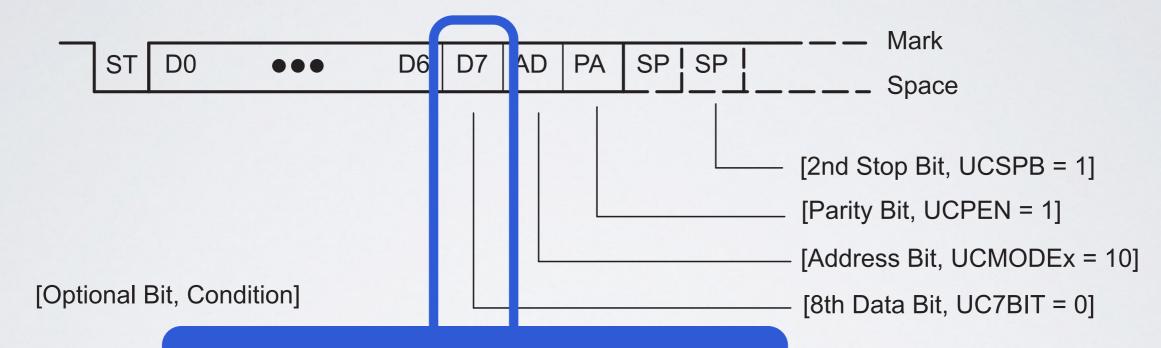




A taxa de transmissão é chamada de baud rate. Ela é diferente da taxa de dados, já que o protocolo prevê bits extra, como o START e o STOP.

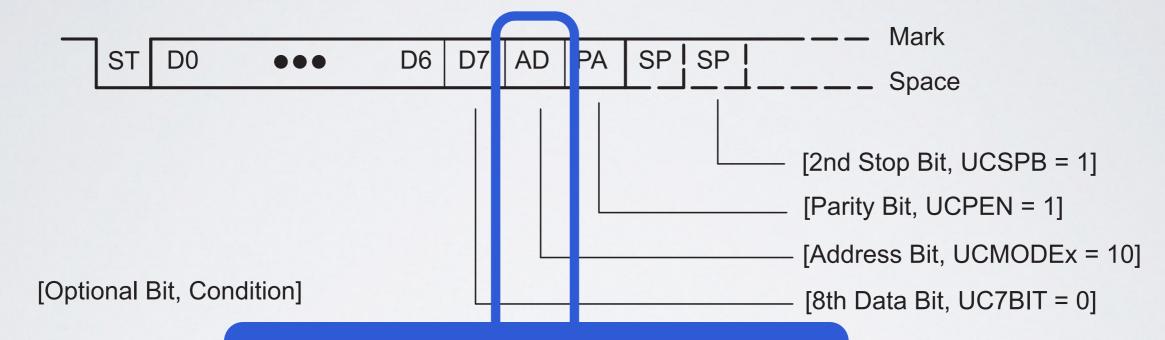


Opções para comunicação assíncrona no MSP430



Pode-se enviar 7 ou 8 bits de informação (caracteres ASCII, por exemplo, têm somente 7 bits)

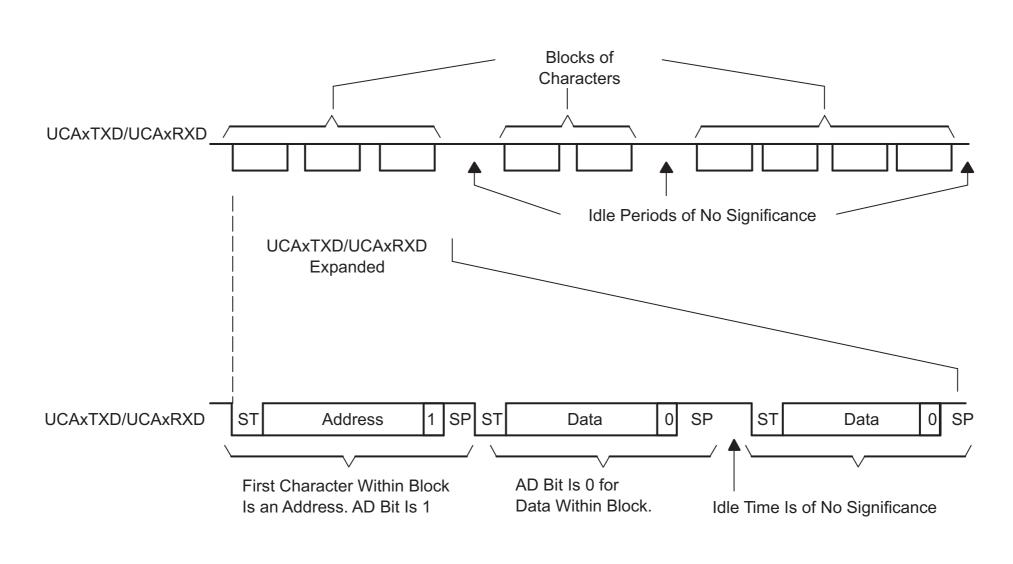
ona no MSP430



Pode-se acrescentar o envio de endereço, no caso de múltiplos transmissores e receptores

a no MSP430

Opçõ

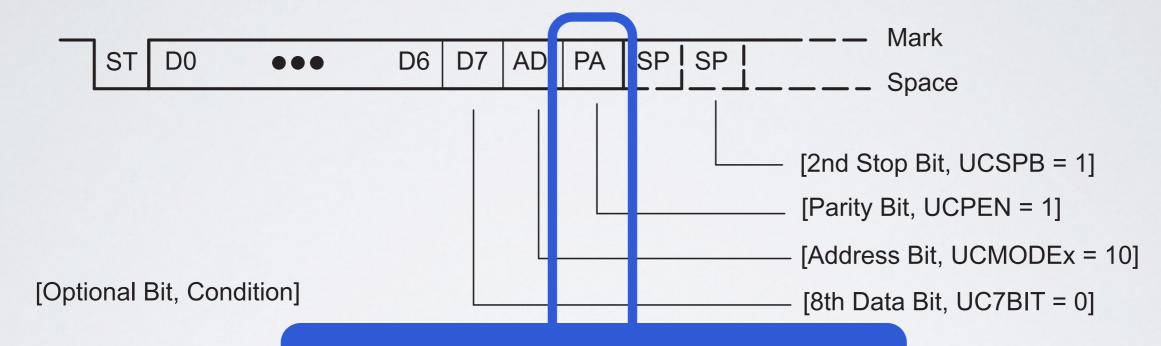


Pode-se acrescentar o envio de endereço, no caso de múltiplos transmissores e receptores

Opçõ

a no MSP430

COMUNICAÇÃO

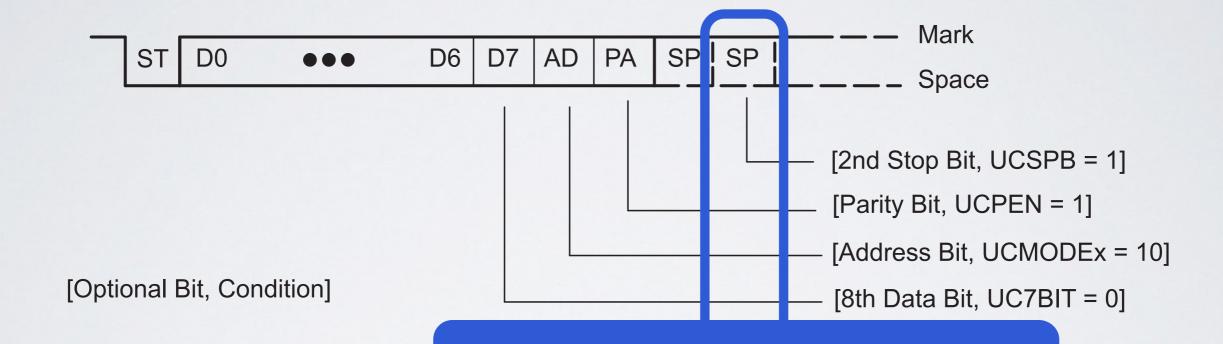


Pode-se enviar um bit de paridade, para o receptor conferir se houve erro na transmissão

Opções

MSP430

COMUNICAÇÃO



Pode-se enviar um segundo bit de STOP, para sistemas mais lentos não perderem o sincronismo

Opções para c

430

7	6		5	4	3	2	1	0
UCPEN	UCPA	R	UCMSB	UC7BIT	UCSPB	UCMO	DEx	UCSYNC
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parity	/ enable					
		0	Parity disable	ed.				
		1	_			D) and expected (d in the parity calcu		dress-bit
UCPAR	Bit 6	Parity	select. UCPAR	is not used wher	n parity is disabled	d.		
		0	Odd parity					
		1	Even parity					
UCMSB	Bit 5	MSB	first select. Con	trols the direction	of the receive and	d transmit shift reg	ster.	
		0	LSB first					
		1	MSB first					
UC7BIT	Bit 4	Chara	acter length. Sel	ects 7-bit or 8-bit	character length.			
		0	8-bit data					
		1	7-bit data					
UCSPB	Bit 3	Stop	bit select. Numb	per of stop bits.				
		0	One stop bit					
		1	Two stop bits	S				
UCMODEx	Bits 2-1	USCI	mode. The UC	MODEx bits selec	t the asynchronou	us mode when UCS	SYNC = 0.	
		00	UART mode					
		01	Idle-line mult	tiprocessor mode				
		10	Address-bit r	multiprocessor mo	ode			
		11	UART mode	with automatic ba	aud rate detection			
UCSYNC	Bit 0	Syncl	hronous mode e	enable				
		0	Asynchronou	ıs mode				
		1	Synchronous	s mode				

7	6	5	Paridade	2	1	0
UCPEN	UCPAR	UCM	rariuaue	UCN	MODEx	UCSYNC
rw-0	rw-0	rw-		rw-0	rw-∩	rw-0
UCPEN	Bit 7	Parity enable				
		0 Parity	disabled.			
		_	enabled. Parity bit is generated (UCAxTXI processor mode, the address bit is included	•	·	ddress-bit
UCPAR	שוו ס	Panty select.	JOPAK IS not used when parity is disabled.			
		0 Odd	parity			
		1 Even	parity			
UCMSB	Bit 5	MSB first sele	ct. Controls the direction of the receive and	transmit shift re	gister.	
		0 LSB	irst			
		1 MSB	first			
UC7BIT	Bit 4	Character len	gth. Selects 7-bit or 8-bit character length.			
		0 8-bit	data			
		1 7-bit	data			
UCSPB	Bit 3	Stop bit selec	. Number of stop bits.			
		0 One	stop bit			
		1 Two	stop bits			
UCMODEx	Bits 2-1	USCI mode. 7	he UCMODEx bits select the asynchronous	s mode when U	CSYNC = 0.	
		00 UAR	mode			
		01 Idle-li	ne multiprocessor mode			
		10 Addre	ess-bit multiprocessor mode			
		11 UAR	mode with automatic baud rate detection			
UCSYNC	Bit 0	Synchronous	mode enable			
		0 Asyn	chronous mode			
		1 Sync	nronous mode			

7	6		5	4	3	2	1	0
UCPEN	UCPAR		UCMSB	UC7BIT	UCSPB	UCMO	DDEx	UCSYNC
rw-0	rw-0		rw-0	~~· ^	···· ^	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parity	enable	aridad	e par			
		0	Parit		tara da la companya			
		1	Parit	ou ím	par) and expected (ddress-bit
UCPAR	Bit 6	Parity	select. UCPAF	R is not used wher	n parity is disable	'		
		0	Odd parity					
		1	Even parity					
UCMSB	Bit 5	MSB t	rirst select. Con	trois the direction	of the receive ar	nd transmit shift reg	ister.	
		0	LSB first					
		1	MSB first					
UC7BIT	Bit 4	Chara	cter length. Se	lects 7-bit or 8-bit	character length.			
		0	8-bit data					
		1	7-bit data					
UCSPB	Bit 3	Stop b	oit select. Numb	per of stop bits.				
		0	One stop bit					
		1	Two stop bit	S				
UCMODEx	Bits 2-1	USCI	mode. The UC	MODEx bits selec	t the asynchrono	ous mode when UC	SYNC = 0.	
		00	UART mode					
		01	Idle-line mul	tiprocessor mode				
		10	Address-bit	multiprocessor mo	ode			
		11	UART mode	with automatic ba	aud rate detection	1		
UCSYNC	Bit 0	Synch	ronous mode e	enable				
		0	Asynchronou	us mode				
		1	Synchronous	s mode				

7	6		5	4	3	2	1	0
UCPEN	UCPA	R	UCMSB	UC7BIT	UCSPB	UCM	ODEx	UCSYNC
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parity	y enable					
		0	Parity disable	ed.				
UCPAR	Bit 6	L			envio: vice-v		JCAxRXD). In a lation.	ddress-bit
UCMSB	Bit 5	MSB	first select. Con	trols the direction	of the receive and	transmit shift req	gister.	
		0	LSB first					
		1	MSB first					
UC/BII	BIT 4	Unara	acter lengtn. Se	ects /-bit or 8-bit	cnaracter lengtn.			
		0	8-bit data					
		1	7-bit data					
UCSPB	Bit 3	Stop	bit select. Numb	per of stop bits.				
		0	One stop bit					
		1	Two stop bits	S				
UCMODEx	Bits 2-1	USCI	I mode. The UC	MODEx bits selec	t the asynchronous	mode when UC	SYNC = 0.	
		00	UART mode					
		01	Idle-line mult	tiprocessor mode				
		10	Address-bit i	multiprocessor mo	ode			
		11	UART mode	with automatic ba	aud rate detection			
UCSYNC	Bit 0	Sync	hronous mode e	enable				
		0	Asynchronou	us mode				
		1	Synchronous	s mode				

7	6		5	4	3	2	1	0
UCPEN	UCPAI	R	UCMSB	UC7BIT	UCSPB	UCMO	DDEx	UCSYNC
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parity	v enable					
		0	Parity disabl	ed.				
		1	•			D) and expected (•	ddress-bit
UCPAR	Bit 6	Parity	select. UCPAF	R is not used when	n parity is disabled	l.		
UCMSB	Bit 5			anho d 7 ou 8	os dado bits	os:	ster.	
UC7BIT	Bit 4	Chara	acter length. Se	lects 7-bit or 8-bit	character length.			
		0	8-bit data					
		1	7-bit data					
UCSPB	धार उ	Stop	DIT SEIECT. INUME	per of stop bits.				
		0	One stop bit					
		1	Two stop bits	S				
UCMODEx	Bits 2-1	USCI	mode. The UC	MODEx bits selec	t the asynchronou	is mode when UC	SYNC = 0.	
		00	UART mode					
		01	Idle-line mul	tiprocessor mode				
		10	Address-bit i	multiprocessor mo	ode			
		11	UART mode	with automatic ba	aud rate detection			
UCSYNC	Bit 0	Syncl	nronous mode e	enable				
		0	Asynchronou	us mode				
		1	Synchronous	s mode				

7	6		5	4	3	2	1	0
UCPEN	UCPA	R	UCMSB	UC7BIT	UCSPB	UCMO	DDEx	UCSYNC
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parit	y enable					
		0	Parity disable	led.				
		1	_	-	nerated (UCAxTXI ress bit is included	•		ddress-bit
UCPAR	Bit 6	Parit	y select. UCPAF	R is not used wher	n parity is disabled			
		0	Odd parity					
		1	Even parity					
UCMSB	Bit 5	MSB	first select. Cor	ntrols the direction	of the receive and	transmit shift reg	ister.	
UC7BIT	Bit 4			its de S I ou				
UCSPB	Bit 3		bit select. Numl					
		0	One stop bit					
		1	Two stop bit					
UCIVIODEX	BIIS 2-1				t the asynchronou	s mode when UC	SYNC = 0.	
		00 01	UART mode					
		10		tiprocessor mode multiprocessor mo	nde			
		11			aud rate detection			
UCSYNC	Bit 0		chronous mode		add rate detection			
OCOTINO	Dit 0	0	Asynchrono					
		1	Synchronou					
			Cyriomoniou	o modo				

7	6	5	4	3	2		0
UCPEN	UCPAR	UCMSB	UC7BIT	UCSPB	UCM	ODEx	UCSYNC
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parity enable					
		0 Parity disab	led.				
				enerated (UCAxTXI ress bit is included			ddress-bit
UCPAR	Bit 6	Parity select. UCPAI	R is not used whe	n parity is disabled.			
		0 Odd parity					
			The second second	ação as		lai	
UC7BIT UCSPB	Ιe		- mode o com e detec	o comu múltipl	m os esc	ravos	
	Ιe	USCI mode. The UC 00 UART mode 01 Idle-line mu 10 Address-bit	- mode o com e detect bauce MODEx bits select tiprocessor mode multiprocessor mode	comu múltipl cção aut l rate et the asynchronous	m os esc tomáti	ravos ca de	
JCSPB JCMODEx	l e 3 -	USCI mode. The UC 00 UART mode 01 Idle-line mu 10 Address-bit	- mode o com e detect bauc MODEx bits select liprocessor mode multiprocessor me e with automatic b	comumúltiple cao auto la rate et the asynchronous	m os esc tomáti	ravos ca de	
JCSPB	I e 3 - Bits 2-1	USCI mode. The UCOO UART mode of Idle-line muse of UART mode of UART m	- mode o com e detect bauc MODEx bits select liprocessor mode multiprocessor mode with automatic be enable	comumúltiple cao auto la rate et the asynchronous	m os esc tomáti	ravos ca de	

7	6		5	4	3	2	1	0
UCPEN	UCPAI	R	UCMSB	UC7BIT	UCSPB	UCMO	DDEx	UCSYNC
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
UCPEN	Bit 7	Parity	y enable					
		0	Parity disabl	ed.				
		1	_	-	nerated (UCAxTX) ress bit is included	•		ldress-bit
UCPAR	Bit 6	Parity	y select. UCPAF	R is not used wher	n parity is disabled			
		0	Odd parity					
		1	Even parity					
UCMSB	Bit 5	MSB	first select. Con	trols the direction	of the receive and	d transmit shift reg	ister.	
		0	LSB first					
		1	MSB first					
UC7BIT	Bit 4	Char	acter length. Se	lects 7-bit or 8-bit	character length.			
		0	8-bit data					
		1	7-bit data					
UCSPB	Bit 3	Stop	bit select. Numb	per of stop bits.				
		0	One stop bit					
		1	Two stop bits	S				
UCMODEx	Bits 2-1	USC	I mode. The UC	MODEx bits selec	t the asynchronou	s mode when UC	SYNC = 0.	
		0						
		0	Habilit	tar mo	do assí	ncrono		
UCSYNC	Bit 0	Svnc	hronous mode e	enable				
		0						
		1	Synchronous					
UCMODEx		0 1 USC 0 0 1	one stop bit Two stop bit I mode. The UC Chronous mode e Asynchronous	s MODEx bits selection ar mode enable us mode				

7	6		5	4	3	2	1	0
UCS	SSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
UCSSELx	Bits 7-6	USCI	clock source se	elect. These bits s	elect the BRCLK	source clock.		
		00	UCLK					
		01	ACLK					
		10	SMCLK					
		11	SMCLK					
UCRXEIE	Bit 5	Rece	ive erroneous-cl	naracter interrupt-	enable			
		0	Erroneous ch	naracters rejected	and UCAxRXIFG	is not set		
		1	Erroneous ch	naracters received	d will set UCAxRX	(IFG		
UCBRKIE	Bit 4	Rece	ive break charad	cter interrupt-enab	ole			
		0	Received bre	eak characters do	not set UCAxRX	IFG.		
		1	Received bre	eak characters set	t UCAxRXIFG.			
UCDORM	Bit 3	Dorm	ant. Puts USCI	into sleep mode.				
		0	Not dormant	. All received char	racters will set UC	AxRXIFG.		
		1	UCAxRXIFG		with automatic ba	an idle-line or with ud rate detection o		
UCTXADDR	Bit 2		smit address. Ne processor mode		nsmitted will be n	narked as address	depending on the	selected
		0	Next frame to	ransmitted is data				
		1	Next frame to	ransmitted is an a	ddress			
UCTXBRK	Bit 1	baud	rate detection 0		en into UCAxTXE	the transmit buffer SUF to generate the		
		0	Next frame to	ransmitted is not a	a break			
		1	Next frame to	ransmitted is a bre	eak or a break/sy	nch		
UCSWRST	Bit 0	Softw	are reset enable	Э				
		0	Disabled. US	CI reset released	I for operation.			
		1	Enabled. US	CI logic held in re	set state.			

7	6		5	4	3	2	1	0
UC	SSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
TT (;;;; Q		777. 0	7734 Q	· · · · · ·	7777 🔾	Q	
UCSSELx	Bits 7-6	USC	l clock source se	elect These bits s	select the BRCLK	source clock		
OGGGEEX	Bito 7 0	00	UCLK	71000 Bito C	oloot the Brider	Course clock.		
		01	ACLK					
		10	SMCLK					
		11	SMCLK					
UCRXEIE	Bit 5	11	SWOLK					
OCHALIL	Dit 3		4	•				
			onte a	io sina	i de cic	ock par	a	
HCBBKIE	Di+ 4							
UCBRKIE	Bit 4		o n	nodo a	ssíncro	ono		
HODODM	D:1 0			tak characters se	t OUAXNAII G.			
UCDORM	Bit 3			into sleep mode.				
		0			racters will set UC			
		1			•	an idle-line or with ud rate detection o		
				eld will set UCAxF		du fale delection o	Thy the combinati	on or a break
UCTXADDR	Bit 2	Trans				narked as address	depending on the	e selected
			processor mode				3 - 1	
		0	Next frame to	ransmitted is data	a			
		1	Next frame to	ransmitted is an a	address			
UCTXBRK	Bit 1	Trans	smit break. Trans	smits a break with	n the next write to	the transmit buffer	r. In UART mode	with automatic
						BUF to generate the	e required break/s	synch fields.
				e written into the				
		0		ransmitted is not				
		1			eak or a break/sy	nch		
UCSWRST	Bit 0	Softw	vare reset enable	9				
		0	Disabled. US	SCI reset released	d for operation.			
		1	Enabled. US	CI logic held in re	eset state.			

7	6		1	0
UCS	SSELx		UCTXBRK	UCSWRST
rw-0	rw-0	Habilitar tratamento de	rw-0	rw-1
UCSSELx	Bits 7-6	erros de recepção de dados		
		(via paridade)		
UCRXEIE	Bit 5	Receive erroneous-character interrupt-enable		
		0 Erroneous characters rejected and UCAxRXIFG is not set		
		1 Erroneous characters received will set UCAxRXIFG		
USDRIKIE	Dit 1	Trocorre break character interrupt chable		
		0 Received break characters do not set UCAxRXIFG.		
		 Received break characters set UCAxRXIFG. 		
UCDORM	Bit 3	Dormant. Puts USCI into sleep mode.		
		0 Not dormant. All received characters will set UCAxRXIFG.		
		Dormant. Only characters that are preceded by an idle-line or with a UCAxRXIFG. In UART mode with automatic baud rate detection on and synch field will set UCAxRXIFG.		
UCTXADDR	Bit 2	Transmit address. Next frame to be transmitted will be marked as address of multiprocessor mode.	lepending on the	e selected
		Next frame transmitted is data		
		1 Next frame transmitted is an address		
UCTXBRK	Bit 1	Transmit break. Transmits a break with the next write to the transmit buffer. baud rate detection 055h must be written into UCAxTXBUF to generate the Otherwise 0h must be written into the transmit buffer.		
		Next frame transmitted is not a break		
		1 Next frame transmitted is a break or a break/synch		
UCSWRST	Bit 0	Software reset enable		
		O Disabled. USCI reset released for operation.		
		1 Enabled. USCI logic held in reset state.		

7	6		5	4	3	2	1	0
UCS	SSELx	U	ICRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
UCSSELx	Bito 7.6	LISCI do	ok source oc	last Those bits s	alast the PDCLK	source clock		
						io de d todo r		
UCRXEIE	E		excet	o pelo	STAR	T bit)		
UCBRKIE	Bit 4	Receive		ter interrupt-enab	ole	iii G		
					not set UCAxRXI	FG.		
		1	Received bre	ak characters set	t UCAxRXIFG.			
UCDORINI	סוו ט	וווווווטם	. Puis USUI	nto sieep mode.				
		0	Not dormant.	All received char	acters will set UC	AxRXIFG.		
			UCAxRXIFG		with automatic bar	an idle-line or with ud rate detection o		
UCTXADDR	Bit 2		address. Ne cessor mode.		nsmitted will be n	narked as address	depending on the	e selected
		0	Next frame tr	ansmitted is data				
		1	Next frame tr	ansmitted is an a	ddress			
UCTXBRK	Bit 1	baud rate	e detection 0		en into UCAxTXB	the transmit buffer UF to generate the		
		0	Next frame tr	ansmitted is not a	a break			
		1	Next frame tr	ansmitted is a bre	eak or a break/syr	nch		
UCSWRST	Bit 0	Software	reset enable					
		0	Disabled. US	CI reset released	for operation.			
		1	Enabled. US	CI logic held in re	set state.			

7	6	5	4	3	2	1	0
UCS	SSELx	UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
UCSSELx	Bits 7-6 U	I ACLK	elect. These bits s	elect the BRCLK	source clock.		
UCRXEIE	Ha	bilitar				de	
UCBRKIE	E	ei	ndereç	o erra	do		
UCDORM	Bit 3 D	ormant. Puts USCI	into sleep mode.				
	0	Not dormant	. All received char	racters will set UC	CAxRXIFG.		
	1	UCAxRXIFG		with automatic ba	an idle-line or with ud rate detection o		
UCTXADDR		ransmit address. No ultiprocessor mode		insmitted will be n	narked as address	depending on the	e selected
	0	Next frame t	ransmitted is data				
	1	Next frame t	ransmitted is an a	ıddress			
UCTXBRK	b	ransmit break. Tran aud rate detection (therwise 0h must b	055h must be writt	en into UCAxTXE			
	0	Next frame t	ransmitted is not a	a break			
	1	Next frame t	ransmitted is a bro	eak or a break/sy	nch		
UCSWRST	Bit 0 S	oftware reset enabl	е				
	0	Disabled. US	SCI reset released	for operation.			
	1	Enabled. US	CI logic held in re	eset state.			

7	6		5	4	3	2	1	0
UCS	SSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
UCSSELx	Bits 7-6	USCI	clock source se	elect. These bits s	elect the BRCLK	source clock.		
		00	UCLK					
		01	ACLK					
		10	SMCLK					
		11	SMCLK					
UCRXEIE	Bit 5	Recei	ve erroneous-cl	naracter interrupt-	enable			
		0	Erroneous cl	naracters rejected	and UCAxRXIFG	is not set		
		1	Erroneous cl	naracters received	will set UCAxRX	IFG		
UCBRKIE	Bit 4	Recei	ve break charad	cter interrupt-enab	ole			
		0	Received bre	eak characters do	not set UCAxRX	FG.		
		1	Received bre	eak characters set	t UCAxRXIFG.			
		Tra	ansmi	tir dad	os ou (endere		vill set on of a break
UCTXADDR	Bit 2		mit address. Ne processor mode		nsmitted will be n	narked as address	depending on the	e selected
		0	Next frame t	ransmitted is data				
		1	Next frame t	ransmitted is an a	ddress			
UCTXBRK	Bit 1	baud	rate detection 0		en into UCAxTXB	the transmit buffer UF to generate the		
		0	Next frame t	ransmitted is not a	a break			
		1	Next frame t	ransmitted is a bre	eak or a break/syı	nch		
UCSWRST	Bit 0	Softw	are reset enable	Э				
		0	Disabled. US	SCI reset released	for operation.			
		1	Enabled. US	CI logic held in re	set state.			

UCSSELX UCRXEIE UCBRKIE UCDORM UCTXADDR UCTXBRK UCSWR rw-0 rw-0 rw-0 rw-0 rw-0 rw-0 rw-0 rw-0 rw-1 UCSSELX Bits 7-6 USCI clock source select. These bits select the BRCLK source clock. 00 UCLK 01 ACLK 10 SMCLK 11 SMCLK UCRXEIE Bit 5 Receive erroneous-character interrupt-enable 0 Erroneous characters rejected and UCAxRXIFG is not set
UCSSELx Bits 7-6 USCI clock source select. These bits select the BRCLK source clock. 00 UCLK 01 ACLK 10 SMCLK 11 SMCLK Bit 5 Receive erroneous-character interrupt-enable
00 UCLK 01 ACLK 10 SMCLK 11 SMCLK UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
01 ACLK 10 SMCLK 11 SMCLK UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
10 SMCLK 11 SMCLK UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
11 SMCLK UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
UCRXEIE Bit 5 Receive erroneous-character interrupt-enable
U ETIOTEOUS CHAIACIEIS TETECIEU AND UCAXIDATEU IS HULSEL
1 Erroneous characters received will set UCAxRXIFG
UCBRKIE Bit 4 Receive break character interrupt-enable
0 Received break characters do not set UCAxRXIFG.
Received break characters do not set OOAXIIXII G. Received break characters set UCAxRXIFG.
UCDORM Bit 3 Dormant. Puts USCI into sleep mode.
0 Not dormant. All received characters will set UCAxRXIFG.
Dormant. Only characters that are preceded by an idle-line or with address bit set will set
ation of a brea
Transmitir caractere de ho solosted
The Selected
quebra de envio de dados
UCTXBRK Bit 1 Transmit break. Transmits a break with the next write to the transmit buffer. In UART mode with automa baud rate detection 055h must be written into UCAxTXBUF to generate the required break/synch fields. Otherwise 0h must be written into the transmit buffer.
Next frame transmitted is not a break
Next frame transmitted is a break or a break/synch
UCSWRST Bit 0 Software reset enable
0 Disabled. USCI reset released for operation.
1 Enabled. USCI logic held in reset state.

7	6		5	4	3	2	1	0
UC	SSELx		UCRXEIE	UCBRKIE	UCDORM	UCTXADDR	UCTXBRK	UCSWRST
rw-0	rw-0		rw-0	rw-0	rw-0	rw-0	rw-0	rw-1
UCSSELx	Bits 7-6	USC	I clock source se	elect. These bits s	elect the BRCLK	source clock.		
		00	UCLK					
		01	ACLK					
		10	SMCLK					
		11	SMCLK					
UCRXEIE	Bit 5	Rece	eive erroneous-c	haracter interrupt-	enable			
		0	Erroneous cl	naracters rejected	and UCAxRXIFG	is not set		
		1	Erroneous cl	naracters received	d will set UCAxRX	(IFG		
UCBRKIE	Bit 4	Rece	eive break chara	cter interrupt-enal	ole			
		0	Received bre	eak characters do	not set UCAxRXI	IFG.		
		1	Received bre	eak characters se	t UCAxRXIFG.			
UCDORM	Bit 3	Dorm	nant. Puts USCI	into sleep mode.				
		0	Not dormant	. All received cha	racters will set UC	AxRXIFG.		
		1	UCAxRXIFG	_	with automatic bar	an idle-line or with ud rate detection o		
UCTXADDR	Bit 2		smit address. Ne processor mode		unsmitted will be m	narked as address	depending on the	e selected
		0	Next frame t	ransmitted is data				
			_					
UCTXBRK	E		Reseta	ır todo	o siste	ema de	e	with automatic
						ftware	(/8	synch fields.
			comul	ncaçao 	via SU	rtware		
UCSWRST	Bit 0	Softw	vare reset enable	9	,			
		0	Disabled. US	SCI reset released	for operation.			

Enabled. USCI logic held in reset state.

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register

7	6	5	4	3	2	1	0
			UCR	(BUFx			
rw	rw	rw	rw	rw	rw	rw	rw
UCRXBUFx	Bits 7-0	The receive-data buffer register. Reading UCA In 7-bit data mode, UCA	XRXBUF resets	the receive-error b	oits, the UCADDR	or UCIDLE bit, a	

15.4.8 UCAxTXBUF, USCI_Ax Transmit Buffer Register

7	6	5	4	3	2	1	0
			UCTX	(BUFx			
rw	rw	rw	rw	rw	rw	rw	rw
UCTXBUFx	Bits 7-0	The transmit data but register and transmitt UCAxTXBUF is not u	ed on UCAxTXD.	Writing to the trai	•		

Buffer de recepção de dados assíncronos

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register

7	6	5	4	3	2	1	0			
UCRXBUFx										
rw	rw	rw	rw	rw	rw	rw	rw			

UCRXBUFX Bits /-0

The receive-data buffer is user accessible and contains the last received character from the receive shift register. Reading UCAxRXBUF resets the receive-error bits, the UCADDR or UCIDLE bit, and UCAxRXIFG. In 7-bit data mode, UCAxRXBUF is LSB justified and the MSB is always reset.

15.4.8 UCAxTXBUF, USCI_Ax Transmit Buffer Register

7	6	5	4	3	2	1	0
			UCTX	BUFx			
rw	rw	rw	rw	rw	rw	rw	rw

UCTXBUFx

Bits 7-0

The transmit data buffer is user accessible and holds the data waiting to be moved into the transmit shift register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

15.4.7 UCAxRXBUF, USCI_Ax Receive Buffer Register



register and transmitted on UCAxTXD. Writing to the transmit data buffer clears UCAxTXIFG. The MSB of UCAxTXBUF is not used for 7-bit data and is reset.

Table 15-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

BRCLK Frequency [Hz]	Frequency Baud Rate		UCBRSx	UCBRFx	Maximum 1	ΓX Error [%]	Maximum F	RX Error [%]
32,768	1200	27	2	0	-2.8	1.4	-5.9	2.0
32,768	2400	13	6	0	-4.8	6.0	-9.7	8.3
32,768	4800	6	7	0	-12.1	5.7	-13.4	19.0
32,768	9600	3	3	0	-21.1	15.2	-44.3	21.3
1,048,576	9600	109	2	0	-0.2	0.7	-1.0	0.8
1,048,576	19200	54	5	0	-1.1	1.0	-1.5	2.5
1,048,576	38400	27	2	0	-2.8	1.4	-5.9	2.0
1,048,576	56000	18	6	0	-3.9	1.1	-4.6	5.7
1,048,576	115200	9	1	0	-1.1	10.7	-11.5	11.3
1,048,576	128000	8	1	0	-8.9	7.5	-13.8	14.8
1,048,576	256000	4	1	0	-2.3	25.4	-13.4	38.8
1,000,000	9600	104	1	0	-0.5	0.6	-0.9	1.2
1,000,000	19200	52	0	0	-1.8	0	-2.6	0.9
1,000,000	38400	26	0	0	-1.8	0	-3.6	1.8
1,000,000	56000	17	7	0	-4.8	0.8	-8.0	3.2
1,000,000	115200	8	6	0	-7.8	6.4	-9.7	16.1
1,000,000	128000	7	7	0	-10.4	6.4	-18.0	11.6
1,000,000	256000	3	7	0	-29.6	0	-43.6	5.2
4,000,000	9600	416	6	0	-0.2	0.2	-0.2	0.4
4,000,000	19200	208	3	0	-0.2	0.5	-0.3	0.8
4,000,000	38400	104	1	0	-0.5	0.6	-0.9	1.2
4,000,000	56000	71	4	0	-0.6	1.0	-1.7	1.3
4,000,000	115200	34	6	0	-2.1	0.6	-2.5	3.1
4,000,000	128000	31	2	0	-0.8	1.6	-3.6	2.0
4,000,000	256000	15	5	0	-4.0	3.2	-8.4	5.2
8,000,000	9600	833	2	0	-0.1	0	-0.2	0.1
8,000,000	19200	416	6	0	-0.2	0.2	-0.2	0.4
8,000,000	38400	208	3	0	-0.2	0.5	-0.3	0.8
8,000,000	56000	142	7	0	-0.6	0.1	-0.7	0.8
8,000,000	115200	69	4	0	-0.6	0.8	-1.8	1.1
8,000,000	128000	62	4	0	-0.8	0	-1.2	1.2
8,000,000	256000	31	2	0	-0.8	1.6	-3.6	2.0
12,000,000	9600	1250	0	0	0	0	-0.05	0.05
12,000,000	19200	625	0	0	0	0	-0.2	0
12,000,000	38400	312	4	0	-0.2	0	-0.2	0.2
12,000,000	56000	214	2	0	-0.3	0.2	-0.4	0.5

Table 15-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum TX Error [%]		Maximum F	XX Error [%]
32,768	1200	27	2	0	-2.8	1.4	-5.9	2.0
32,768	2400	13	6	0	-4.8	6.0	-9.7	8.3
32,768	4800	6	7	0	-12.1	5.7	-13.4	19.0
32,768	9600	3	3	0	-21.1	15.2	-44.3	21.3
1,048,576	9600	109	2	0	-0.2	0.7	-1.0	0.8
1,048,576	19200	54	5	0	-1.1	1.0	-1.5	2.5
1,048,576	38400	27	2	0	-2.8	1.4	-5.9	2.0
1,048,576	56000	18	6	0	-3.9	1.1	-4.6	5.7
1,048,576	115200	9	1	0	-1.1	10.7	-11.5	11.3
1,048,576	128000	8	1	0	-8.9	7.5	-13.8	14.8
1,048,576	256000	4	1	0	-2.3	25.4	-13.4	38.8
1,000,000	9600	104	1	0	-0.5	0.6	-0.9	1.2
1,000,000	19200	52	0	0	-1.8	0	-2.6	0.9
1,000,000	38400	26	0	0	-1.8	0	-3.6	1.8
1,000,000	56000	17	7	0	-4.8	0.8	-8.0	3.2
1,000,000	115200	8	6	0	-7.8	6.4	-9.7	16.1
1,000,000	128000	7	7	0	-10.4	6.4	-18.0	11.6
1,000,000	256000	3	7	0	-29.6	0	-43.6	5.2
4,000,000	9600	416	6	0	-0.2	0.2	-0.2	0.4
4,000,000	19200	208	3	0	-0.2	0.5	-0.3	0.8
4,000,000	38400	104	1	0	-0.5	0.6	-0.9	1.2
4,000,000	56000	71	4	0	-0.6	1.0	-1.7	1.3
4,000,000	115200	34	6	0	-2.1	0.6	-2.5	3.1
4,000,000	128000	31	2	0	-0.8	1.6	-3.6	2.0
4,000,000	256000	15	5	0	-4.0	3.2	-8.4	5.2
8,000,000	9600	833	2	0	-0.1	0	-0.2	0.1
8,000,000	19200	416	6	0	-0.2	0.2	-0.2	0.4
8,000,000	38400	208	3	0	-0.2	0.5	-0.3	0.8
8,000,000	56000	142	7	0	-0.6	0.1	-0.7	0.8
8,000,000	115200	69	4	0	-0.6	0.8	-1.8	1.1

Definição das baud rates mais comuns

Table 15-4. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 0 (continued)

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum 1	TX Error [%]	Maximum F	XX Error [%]
12,000,000	115200	104	1	0	-0.5	0.6	-0.9	1.2
12,000,000	128000	93	6	0	-0.8	0	-1.5	0.4
12,000,000	256000	46	7	0	-1.9	0	-2.0	2.0
16,000,000	9600	1666	6	0	-0.05	0.05	-0.05	0.1
16,000,000	19200	833	2	0	-0.1	0.05	-0.2	0.1
16,000,000	38400	416	6	0	-0.2	0.2	-0.2	0.4
16,000,000	56000	285	6	0	-0.3	0.1	-0.5	0.2
16,000,000	115200	138	7	0	-0.7	0	-0.8	0.6
16,000,000	128000	125	0	0	0	0	-0.8	0
16,000,000	256000	62	4	0	-0.8	0	-1.2	1.2

Definição das baud rates mais comuns (continuação)

Table 15-5. Commonly Used Baud Rates, Settings, and Errors, UCOS16 = 1

BRCLK Frequency [Hz]	Baud Rate [Baud]	UCBRx	UCBRSx	UCBRFx	Maximum 1	X Error [%]	Maximum F	RX Error [%]
1,048,576	9600	6	0	13	-2.3	0	-2.2	0.8
1,048,576	19200	3	1	6	-4.6	3.2	-5.0	4.7
1,000,000	9600	6	0	8	-1.8	0	-2.2	0.4
1,000,000	19200	3	0	4	-1.8	0	-2.6	0.9
1,000,000	57600	1	7	0	-34.4	0	-33.4	0
4,000,000	9600	26	0	1	0	0.9	0	1.1
4,000,000	19200	13	0	0	-1.8	0	-1.9	0.2
4,000,000	38400	6	0	8	-1.8	0	-2.2	0.4
4,000,000	57600	4	5	3	-3.5	3.2	-1.8	6.4
4,000,000	115200	2	3	2	-2.1	4.8	-2.5	7.3
4,000,000	230400	1	7	0	-34.4	0	-33.4	0
8,000,000	9600	52	0	1	-0.4	0	-0.4	0.1
8,000,000	19200	26	0	1	0	0.9	0	1.1
8,000,000	38400	13	0	0	-1.8	0	-1.9	0.2
8,000,000	57600	8	0	11	0	0.88	0	1.6
8,000,000	115200	4	5	3	-3.5	3.2	-1.8	6.4
8,000,000	230400	2	3	2	-2.1	4.8	-2.5	7.3
8,000,000	460800	1	7	0	-34.4	0	-33.4	0
12,000,000	9600	78	0	2	0	0	-0.05	0.05
12,000,000	19200	39	0	1	0	0	0	0.2
12,000,000	38400	19	0	8	-1.8	0	-1.8	0.1
12,000,000	57600	13	0	0	-1.8	0	-1.9	0.2
12,000,000	115200	6	0	8	-1.8	0	-2.2	0.4
12,000,000	230400	3	0	4	-1.8	0	-2.6	0.9
16,000,000	9600	104	0	3	0	0.2	0	0.3
16,000,000	19200	52	0	1	-0.4	0	-0.4	0.1
16,000,000	38400	26	0	1	0	0.9	0	1.1
16,000,000	57600	17	0	6	0	0.9	-0.1	1.0
16,000,000	115200	8	0	11	0	0.9	0	1.6
16,000,000	230400	4	5	3	-3.5	3.2	-1.8	6.4
16,000,000	460800	2	3	2	-2.1	4.8	-2.5	7.3

Definição das baud rates mais comuns (continuação)