

Universidad de Costa Rica

Facultad de Ingeniería

Escuela de Ingeniería Eléctrica

IE-0624: Laboratorio de Microcontroladores

II ciclo 2024

Proyecto Final

Display de disponibilidad integrado a calendario

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27 de noviembre de 2024

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1. Resumen

Este proyecto tiene como objetivo desarrollar un prototipo con capacidad de mostrar en tiempo real la disponibilidad de un usuario, buscando disminuir interrupciones en entornos laborales y educativos. Se usa un NodeMCU ESP8266 para la conexión WiFi y un display ST7735 TFT para visualizar la información, integrando con la API de Google Calendar para obtener y agregar eventos. En la interfaz gráfica del display se muestran los detalles de las reuniones: el nombre, la fecha y la descripción. Los usuarios pueden navegar entre eventos o crear nuevos mediante botones físicos. El sistema está diseñado para operar de manera segura y eficiente, aprovechando la infraestructura de AWS para escalar y brindar protección de datos con protocolos HTTPS. Este prototipo busca optimizar la gestión del tiempo y fomentar un entorno más organizado y productivo; además de poner en práctica los conocimientos adquiridos en el curso.

Repositorio de GitHub <https://github.com/ErickMaRi/Laboratorios-Grupales-IE0624>

2. Objetivos

2.1. Objetivo General

Desarrollar un prototipo funcional que permita visualizar en tiempo real la disponibilidad de un usuario, utilizando un NodeMCU ESP8266 y un ST7735 TFT Display.

2.2. Objetivos específicos

- Establecer la conexión del NodeMCU ESP8266 a una red WiFi para la transmisión de datos.
- Integrar el sistema con una API de correo electrónico para obtener información sobre reuniones y eventos del calendario del usuario.
- Visualizar la información obtenida de la API en el ST7735 TFT Display de manera clara y comprensible.

3. Alcances

- Se busca desarrollar un dispositivo que permita a los usuarios visualizar la disponibilidad de una oficina o persona en tiempo real mediante una integración con Google Calendar.
- Se debe implementar conectividad a WiFi usando el NodeMCU ESP8266 para transmitir datos del calendario a través de internet.
- Es necesario integrar el sistema con la pantalla ST7735 TFT para poder mostrar la información de reuniones y/o eventos.
- Diseñar un sistema IoT seguro que utilice protocolos HTTPS para garantizar la privacidad y seguridad de los datos transmitidos.
- Proporcionar una interfaz física con botones que permita a los usuarios navegar entre eventos y crear reuniones nuevas directamente desde el dispositivo.

- Utilizar servicios en la nube como AWS para escalar el sistema y garantizar su disponibilidad en distintos entornos.
- Fomentar la optimización del tiempo y la productividad en entornos laborales y académicos al reducir interrupciones innecesarias.

4. Justificación

Actualmente, para los entornos laborales y académicos, son aspectos clave gestionar de manera eficiente el tiempo y mantener comunicación constante para maximizar la productividad. Sin embargo, resulta muy sencillo generar interrupciones innecesarias que pueden impactar de manera negativa la concentración y funcionalidad de los trabajadores. Este problema es particularmente notorio en lugares como oficinas de profesores, oficinas en casa y salas de reuniones, en los que la disponibilidad de las personas no es evidente para quienes necesitan contactarlas.

Desarrollar un prototipo que permita ver en tiempo real la disponibilidad de una persona o sala permite minimizar estas interrupciones. Utilizando un NodeMCU ESP8266, un ST7735 TFT Display y la integración con una API de correo electrónico, el sistema podrá mostrar la información actualizada sobre reuniones y eventos del calendario del usuario. Facilitando la comunicación efectiva y permitiendo a las personas tomar decisiones informadas antes de interrumpir al usuario.

Este proyecto busca no solo mejorar la organización personal, sino también ayudar a crear un entorno de trabajo más ordenado, eficiente y respetuoso con los tiempos de todo el personal.

5. Nota teórica

5.1. NodeMCU(ESP8266)

El ESP8266 es un módulo muy utilizado en aplicaciones de IoT ya que permite integrar conectividad WiFi en diseños compactos de bajo costo. EL NodeMCU ESP8266 tiene un microcontrolador Tensilica L106 de 32 bits y bajo consumo. Frecuencia de reloj de hasta 160 MHz, RAM de 36 kB y soporte para memoria Flash externa de hasta 16 MB. Permite utilizar múltiples interfaces como UART, SPI, I2C y PWM. Adicionalmente, es capaz de operar en modo estación y punto de acceso. Consumo muy bajo en modo de suspensión y potencia de transmisión de +20 dBm. [2] ESP8266 es muy utilizado para aplicaciones como automatización del hogar, sensores conectados y dispositivos portátiles.

5.1.1. Diagrama de pines

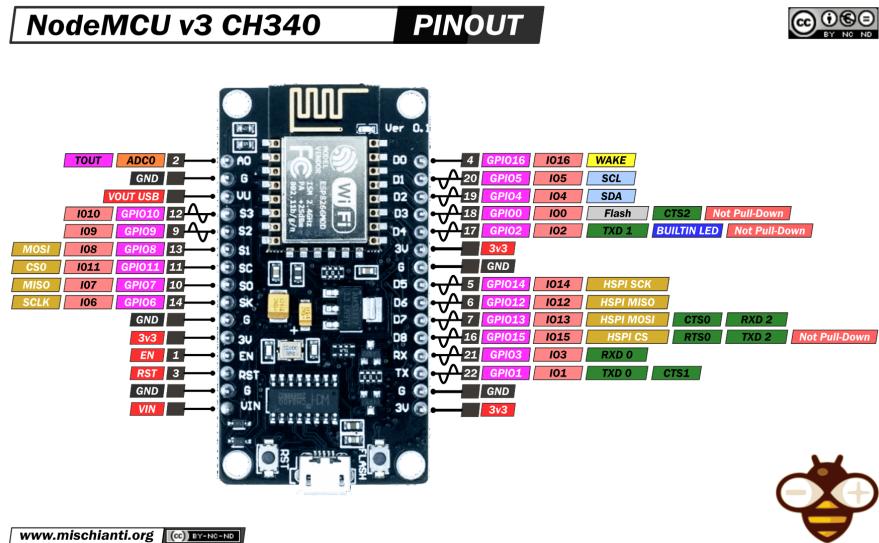


Figura 1: Diagrama de pines de NodeMCU ESP8266 [1]

5.1.2. Diagrama de bloques

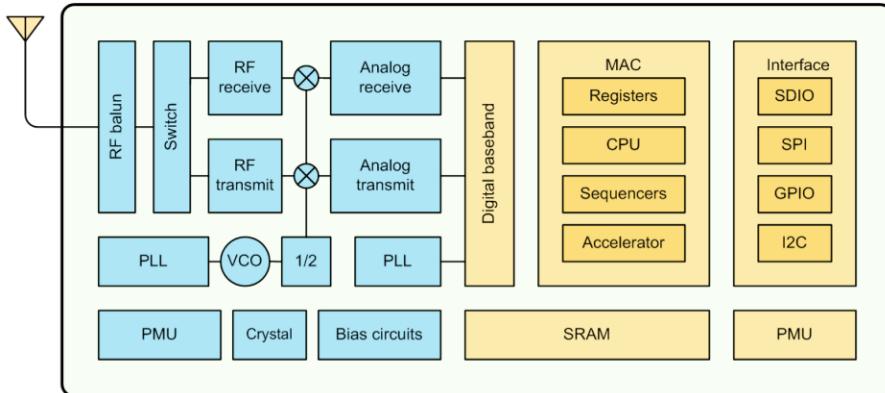


Figura 2: Diagrama de bloques de NodeMCU ESP8266 [2]

5.1.3. Registros, periféricos y módulos

Debido a que la placa se programa de manera similar a Arduino no es necesario detallar los registros. En lo referente a periféricos se tiene:

- **GPIO:** 17 pines con funciones adicionales como PWM, SPI y I2C.
- **ADC:** Resolución de 10 bits, útil mide señales analógicas entre 0 y 1V.
- **UART:** Dos interfaces UART.
- **SPI y I2C:** Comunicación con sensores y otros dispositivos.
- **PWM:** Cuatro salidas disponibles.
- **RTC:** Funciona en modos de bajo consumo.

5.2. ST7735 TFT Display

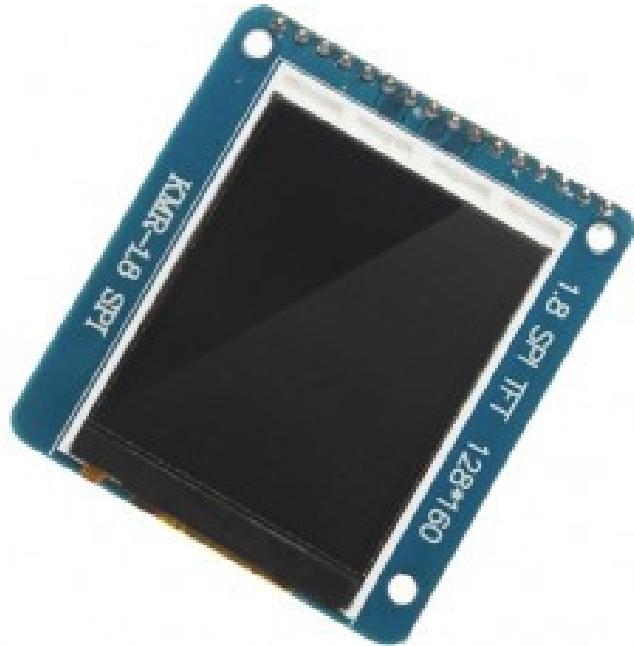


Figura 3: Figura tomada de *CrCibernetica*, proveedor del cual uno de nosotros compró el módulo.

Podemos ver en la figura 3 la pantalla ST7735, un módulo barato y fácil de usar, que tiene aplicaciones en una amplia gama de proyectos que requieran un display de bajo framerate con una profundidad de color moderna (18 bits). Esta pantalla dispone de un controlador que nos permite realizar comandos simples, para dibujar líneas y barrer los pixeles. Aunque el módulo opera normalmente a cinco voltios, generalmente dispone de un jumper que permite cortocircuitar el regulador de tensión de forma que el sistema opere a 3.3 voltios. [3]

5.2.1. Diagrama de pines

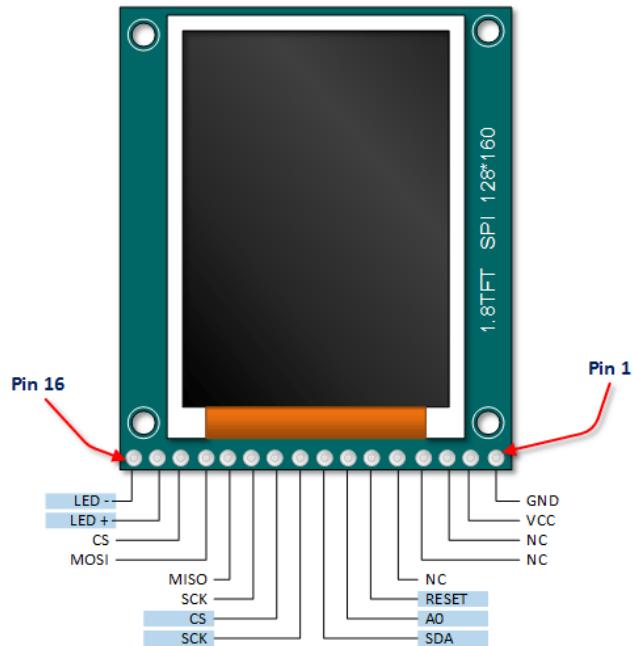


Figura 4: Pinout de la pantalla tomado de *las notas técnicas de Nan Qin*

Aunque el orden de los pines puede cambiar respecto a los que vemos en la figura 4, además de los nombres que tiene el PCB escrito, se usaron los pines desde *MISO* hasta *RESET*, además de los pines que sirven para alimentar la retroiluminación de la pantalla, el riel *VCC* y *GND*.

5.2.2. Topología

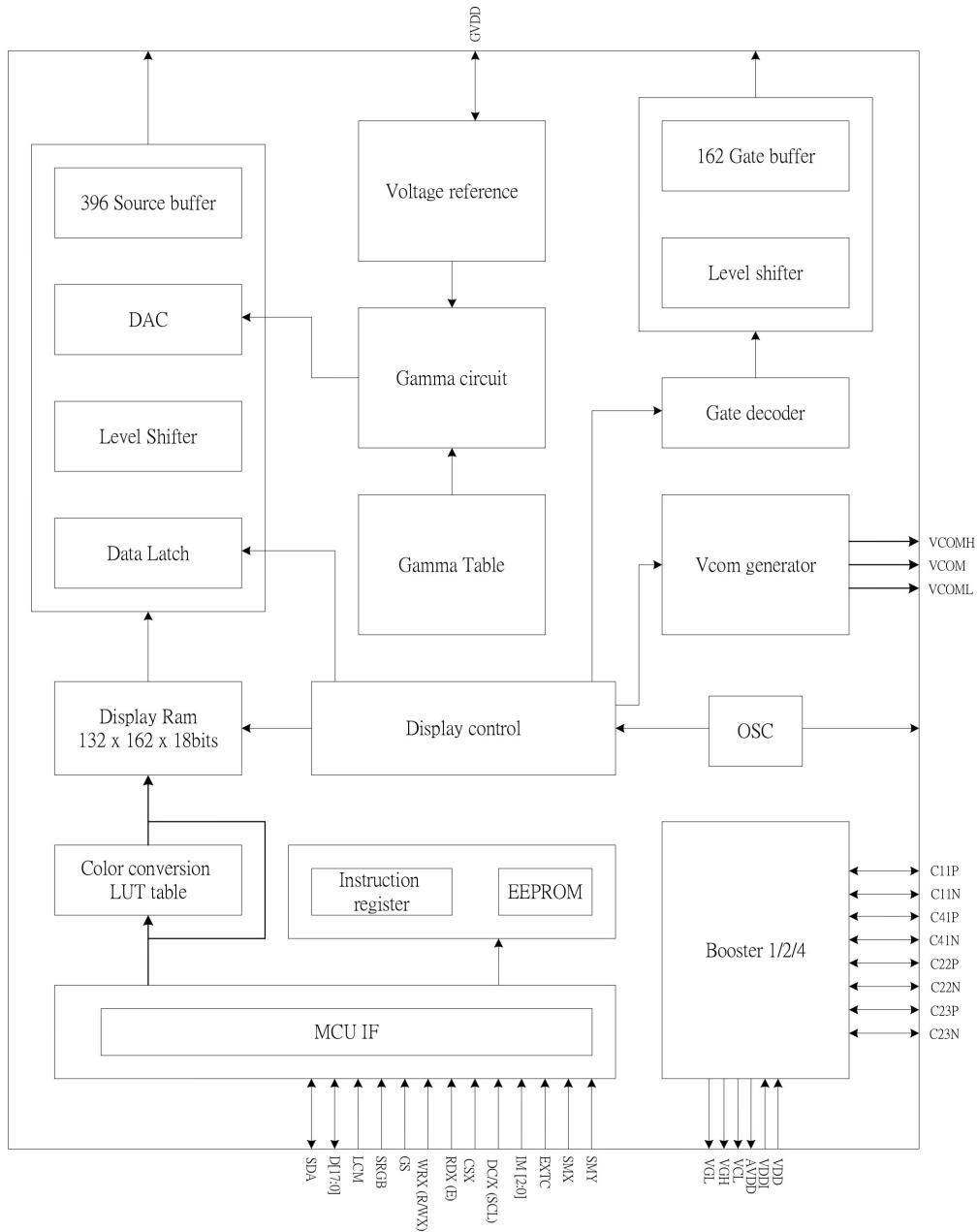


Figura 5: Diagrama de bloques del módulo visto desde los pines, tomado de la hoja de datos [3]

El diagrama de la figura 5 muestra la arquitectura que gestiona la visualización en la pantalla, incluye un buffer para los datos de entrada, un DAC para producir el rango de colores y una memoria (RAM) de 132x162 píxeles a 18 bits. Los 18 bits que representan la profundidad de color se procesan mediante un lookup table y un circuito de gamma para poder ajustar el brillo y contraste. El controlador se comunica con el microcontrolador a través de la interfaz SPI.

5.2.3. Registros, periféricos y módulos

El controlador de la pantalla ST7735 maneja una gama de registros y módulos que le permiten producir una imagen y comunicar datos. En esta línea el principal módulo es el de SPI

(Serial Peripheral Interface) el cual media la transmisión de los datos entre el microcontrolador y la pantalla. La pantalla es compatible con los modos SPI estándar (modo 0 y modo 3), lo que lo hace bastante versátil para diversos sistemas.

5.3. Conceptos importantes para el diseño del proyecto

5.4. IOT

El internet de las cosas, la interconexión de los dispositivos a través del internet, permitiéndoles recoger, procesar e intercambiar datos de autónomamente, habilitando industrias como la manufactura, la agricultura y la salud, al promover la toma de decisiones basada en datos [4].

5.5. Google Cloud

Google Cloud es una plataforma de servicios en la nube que ofrece herramientas y servicios para el procesamiento de datos, almacenamiento y despliegue de aplicaciones. Su infraestructura, que incluye productos como Google Kubernetes Engine y BigQuery, es altamente escalable y permite a las empresas crear aplicaciones de alta disponibilidad y bajo costo [5].

5.6. HTTPS

HyperText Transfer Protocol Secure, la versión segura del protocolo HTTP, cifra los datos (SSL/TLS) para asegurarse que las comunicaciones no sean interceptadas ni manipuladas [6].

5.7. AWS

Utilizada en una amplia cantidad de soluciones dentro y fuera del dominio del IoT, es una plataforma de servicios en la nube que proporciona soluciones de almacenamiento, análisis de datos, procesamiento, etc [7].

5.8. FastAPI

Framework web para la creación de APIs ligeras en Python. De fácil uso y una excelente opción para desarrollar pequeños servicios web, como los que encontraríamos en aplicaciones del IoT [8].

5.9. Librerías importantes

5.9.1. Código .ino

Para implementar la comunicación con el calendario y la pantalla se utilizaron varias librerías que habilitaron el desarrollo en el NodeMCU:

- **ESP8266WiFi.h**: Permite el uso del ESP8266 para comunicación vía WiFi. En el código permite la conexión a internet mediante la declaración de la contraseña y el nombre de la red (**password** y **ssid**).
- **ESP8266HTTPClient.h**: Permite realizar solicitudes HTTP a servidores web. En el código la usamos para enviar un GET al endpoint (Amazon API Gateway) afín de recuperar y agregar eventos.

- `WiFiClientSecureBearSSL.h`: Esta librería es parte del soporte para conexiones HTTPS. En el código, la usamos para realizar solicitudes a los endpoints seguros.
- `Adafruit_GFX.h` y `Adafruit_ST7735.h`: Las responsables de manejar la pantalla. `Adafruit_GFX` permite dibujar texto y figuras, mientras que `Adafruit_ST7735` sirve para simplificar la comunicación con el controlador del ST7735 que usamos.
- `SPI.h`: Necesaria para comunicarse por SPI con los periféricos, para ser específico, nuestra pantalla.
- `NTPClient.h` y `WiFiUdp.h`: Necesarias para sincronizar el tiempo del NodeMCU usando el protocolo NTP (Network Time Protocol). `NTPClient` gestiona la conexión a un servidor NTP mientras `WiFiUdp` se encarga de la transmisión de datos a través de UDP, por el cual nos comunicamos con el servidor del tiempo, como por ejemplo `pool.ntp.org`.

6. Desarrollo

6.1. Acceso al API

Para interactuar con Google Calendar, se usa la API oficial y un sistema de autenticación basado en OAuth2. Las credenciales del usuario son almacenadas en un archivo JSON (`token.json`) y se verificadas antes de cada solicitud. Si las credenciales han expirado, se intentan refrescar automáticamente.

Se trabajaron 2 funcionalidades:

- Recuperar reuniones programadas durante las próximas 24 horas.
- Crear eventos nuevos especificando detalles necesarios.

Este enfoque asegura un acceso eficiente y seguro a los datos del calendario. A modo de ejemplo el código utilizado para obtener los datos del calendario se incluye a continuación.

```
def obtener_eventos_y_enviar():
    creds = get_credentials() # Obtener credenciales válidas
    if not creds:
        return None

    try:
        service = build("calendar", "v3", credentials=creds)
        ahora = datetime.datetime.now(datetime.timezone.utc).isoformat()
        tiempo_final = (datetime.datetime.now(datetime.timezone.utc) +
                        datetime.timedelta(days=1)).isoformat()

        # Recuperar eventos para las próximas 24 horas
        events_result = service.events().list(
            calendarId="primary",
            timeMin=ahora,
            timeMax=tiempo_final,
            singleEvents=True,
            orderBy="startTime"
        ).execute()
```

```

eventos = events_result.get("items", [])
if not eventos:
    return None

except HttpError as error:
    print(f"Error al acceder al calendario: {error}")
    return None

```

6.2. AWS/HTTPS

La aplicación se despliega en AWS Lambda utilizando Mangum para adaptar FastAPI. Con esto se aprovecha la escalabilidad y alta disponibilidad de AWS. El tráfico se protege con HTTPS mediante SSL proporcionado por AWS Certificate Manager, logrando seguridad de las comunicaciones.

Los endpoints definidos, como la creación y consulta de eventos, están accesibles públicamente a través de API Gateway, lo que permite un funcionamiento confiable y seguro. Integración de FastAPI con AWS Lambda utilizando Mangum:

```

from mangum import Mangum

app = FastAPI()

# Definir endpoints aquí...

# Adaptar la aplicación para AWS Lambda
handler = Mangum(app)

```

6.3. Display

Para mostrar los datos empleamos una interfaz gráfica donde se muestran los detalles de los eventos, como el nombre, la fecha, la hora y una descripción que se desplaza píxel por píxel, con una velocidad que es un parámetro ajustable. Al iniciar el sistema, se producen en la pantalla mensajes sin estilizar que comunican el proceso por el cual el sistema se conecta a la red, sincroniza el reloj y obtiene los datos del calendario.

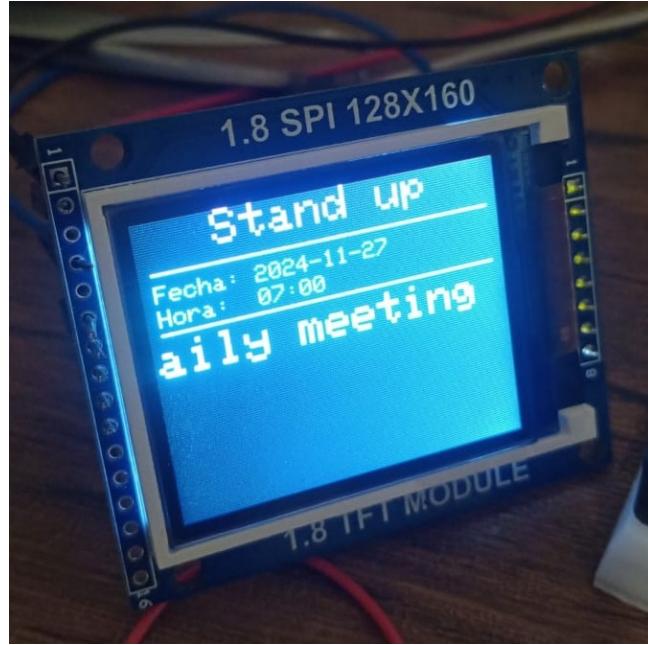


Figura 6: Observe desde arriba hacia abajo: nombre, fecha, hora y descripción deslizante "Daily meeting".

Para un evento dado, se presentan los datos de tamaño fijo y pequeños (nombre, fecha, hora) en la parte superior de la pantalla, mientras que la descripción se muestra en una sección inferior desplazando el texto a la izquierda (como podemos ver en la figura 6), afán de mostrar descripciones más grandes que las que puede contener la pantalla en un solo instante. El desplazamiento se implementó usando un índice que cambia respecto la velocidad del texto. Se actualiza la pantalla cada vez que el usuario navega entre los eventos.

6.4. Botones

La interfaz que recibe las entradas del usuario corresponde a dos botones: uno para navegar hacia el evento anterior (`BUTTON_PREV_PIN`) y otro para avanzar al siguiente evento (`BUTTON_NEXT_PIN`). Además de permitir el desplazamiento en el calendario, ambos botones permiten dos acciones más, para hacer la implementación más práctica y simplificada:

- El botón "Previo", además de permitir ir hacia atrás en el calendario, si se mantiene presionado por más de 2 segundos envía un GET al endpoint, afín de poder asegurarse de que encuentra el evento actual, a sabiendas de la hora sincronizada con el servidor NTP, refresca la pantalla y muestra los datos del evento actual.
- El botón "Siguiente" permite avanzar al siguiente evento en el calendario, pero si se presiona por más de 2 segundos, solicita la creación de un nuevo evento si no hay colisiones.

6.5. Crear reunión nueva

A solicitud del profesor, se agregó la opción de crear reuniones desde la aplicación. Esta funcionalidad fue implementada utilizando FastAPI para manejar tanto la interfaz de usuario como la comunicación con la API de Google Calendar. El formulario para la creación de reuniones se encuentra alojado en un endpoint accesible desde AWS, proporcionando una solución robusta y escalable.

6.5.1. Detalles del funcionamiento

- Formulario para la creación de reuniones: Se definió un formulario que se puede acceder desde el endpoint `GET /new_meeting`. En el que se muestra una interfaz diseñada con HTML y CSS, donde el usuario puede ingresar detalles de la reunión, como fecha, hora, ubicación, asistentes y descripción. Se puede encontrar en `new_meeting_form.html`.
- Endpoint para crear la reunión: El endpoint `POST /create_meeting` recibe los datos enviados desde el formulario y los procesa para crear un evento en Google Calendar. Se puede resumir en:
 - Agregar la información de zona horaria.
 - Convertir los asistentes ingresados en una lista de diccionarios para respetar el formato de Google Calendar.
 - Autenticarse con la API de Google Calendar usando credenciales válidas.
 - Crear el evento y manejar posibles errores.
- Integración con Google Calendar: La API de Google Calendar se usa para gestionar la creación de eventos. En caso de éxito, se muestra una página de confirmación con el ID del evento. Si ocurre un error (por ejemplo, fallos de autenticación o problemas de red), se notifica al usuario mediante una página de error personalizada.
- Interfaz de usuario: https://bq19t3sb3d.execute-api.us-east-2.amazonaws.com/Prod/new_meeting

Nueva reunión

Fecha y hora de inicio:

Fecha y hora de finalización:

Resumen:

Descripción:

Location:

Asistentes (correos separados por comas):

Create Meeting

Figura 7: Interfaz gráfica para crear reuniones

7. Resultados

A pesar de las dificultades asociadas a prototipar sin una carcasa con periféricos sensibles a los errores, logramos producir un sistema que sin tener que sostener todos los datos del calendario en el borde, se sirve de una ventana y una conexión a internet para recibir y publicar información de forma agradable a la vista.

La demostración de las funcionalidades del sistema (desde acceder al internet, coordinar el reloj, comunicarse con la API, presentar los eventos, avanzar, retroceder, ir al evento actual y publicar un evento) se tiene documentada en el siguiente **video de YouTube**

8. Conclusiones y recomendaciones

Es riesgoso implementar un sistema compuesto de subsistemas poco robustamente conectados, como teníamos con un Arduino que requería comunicarse a través de un módulo, por estas razones era mejor optar por subsistemas que integran nativamente los componentes que sepamos por experiencia o conocimiento técnico que son vulnerables a arribar muertos o morir en el desarrollo.

Los sistemas diseñados para brindar soluciones con IoT aligeran la carga puesta sobre los dispositivos en el borde, levantando los requerimientos en memoria para poder sostener un contenido en apariencia arbitrariamente grande.

No siempre el precio es un indicador directo de la calidad de un producto o de su rendimiento en una implementación dada, pues el proyecto emplea ahora un controlador que cuesta menos que el Arduino propuesto originalmente y que soluciona el nexo entre el controlador y la conexión Wi-Fi. La poca disponibilidad de dispositivos como el controlador por el cual se optó hubiese encarecido el proyecto gravemente, al tener que elegir equipo sobredimensionado que vendría de la mano con el rediseño del alcance del proyecto o un desperdicio de las capacidades del mismo.

Para desarrollar un sistema habilitado por el internet de las cosas, es necesario realizar la verificación de las funcionalidades del sistemas para distintas tasas de transmisión de datos, afín de evaluar la eficacia del código y su robustez.

Para aplicaciones escaladas de este proyecto se recomienda el uso de pantallas basadas en la tecnología ePaper, los cuales normalmente encontramos en los lectores electrónicos de libros, por su menor consumo energético y porque la aplicación no requiere la reproducción de animaciones, es posible desarrollar una aplicación que desplace el texto por grupos de palabras con baja frecuencia de forma automática o con el uso de más botones. Una pantalla de la misma resolución por Crystalfontz [9] reporta una corriente al actualizar la pantalla de 10mA (I_{UPDATE}) de la mano no consumir energía para mantener la imagen (para alargar la vida útil de la pantalla es necesario refrescar la imagen cada cierto tiempo, por lo que el consumo no es exactamente cero), estas especificaciones se acoplan mejor con las necesidades de nuestro letrero inteligente que una pantalla LCD típica.

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9. Anexos

9.1. Hoja de datos de NodeMCU(ESP8266)



ESP8266EX Datasheet

Version 4.3

Espressif Systems IOT Team

<http://bbs.espressif.com/>

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1. General Overview

1.1. Introduction

Espressif Systems' Smart Connectivity Platform (ESCP) is a set of high performance, high integration wireless SOCs, designed for space and power constrained mobile platform designers. It provides unsurpassed ability to embed WiFi capabilities within other systems, or to function as a standalone application, with the lowest cost, and minimal space requirement.

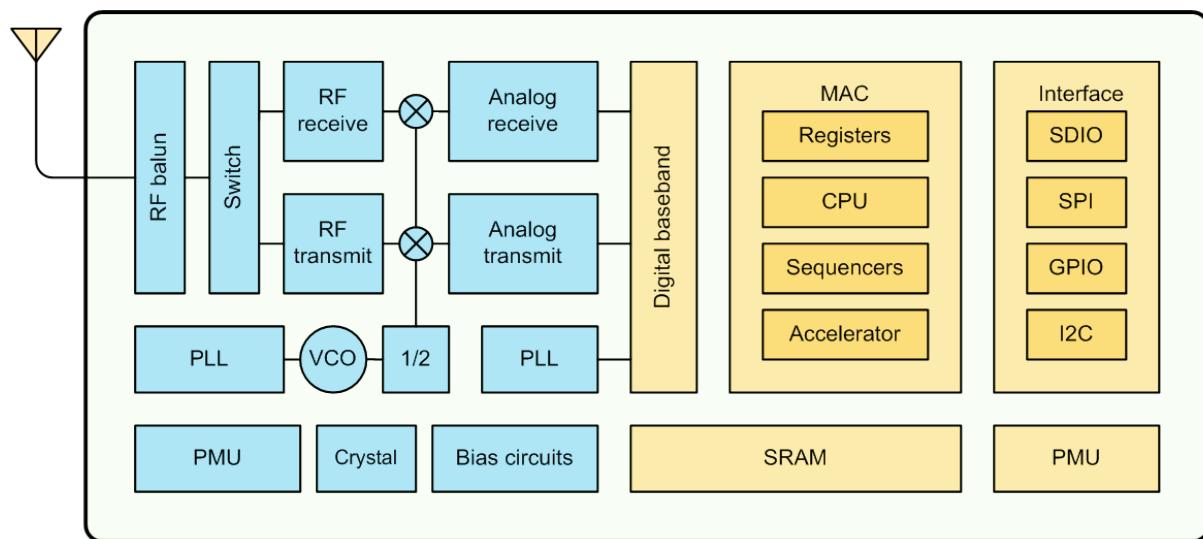


Figure 1 ESP8266EX Block Diagram

ESP8266EX offers a complete and self-contained WiFi networking solution; it can be used to host the application or to offload WiFi networking functions from another application processor.

When ESP8266EX hosts the application, it boots up directly from an external flash. It has integrated cache to improve the performance of the system in such applications.

Alternately, serving as a WiFi adapter, wireless internet access can be added to any micro controller-based design with simple connectivity (SPI/SDIO or I2C/UART interface).

ESP8266EX is among the most integrated WiFi chip in the industry; it integrates the antenna switches, RF balun, power amplifier, low noise receive amplifier, filters, power management modules, it requires minimal external circuitry, and the entire solution, including front-end module, is designed to occupy minimal PCB area.

ESP8266EX also integrates an enhanced version of Tensilica's L106 Diamond series 32-bit processor, with on-chip SRAM, besides the WiFi functionalities. ESP8266EX is often integrated with external sensors and other application specific devices through its GPIOs; sample codes for such applications are provided in the software development kit (SDK).



Espressif Systems' Smart Connectivity Platform (ESCP) demonstrates sophisticated system-level features include fast sleep/wake context switching for energy-efficient VoIP, adaptive radio biasing for low-power operation, advance signal processing, and spur cancellation and radio co-existence features for common cellular, Bluetooth, DDR, LVDS, LCD interference mitigation.

1.2. Features

- 802.11 b/g/n
- Integrated low power 32-bit MCU
- Integrated 10-bit ADC
- Integrated TCP/IP protocol stack
- Integrated TR switch, balun, LNA, power amplifier and matching network
- Integrated PLL, regulators, and power management units
- Supports antenna diversity
- WiFi 2.4 GHz, support WPA/WPA2
- Support STA/AP/STA+AP operation modes
- Support Smart Link Function for both Android and iOS devices
- SDIO 2.0, (H) SPI, UART, I2C, I2S, IR Remote Control, PWM, GPIO
- STBC, 1x1 MIMO, 2x1 MIMO
- A-MPDU & A-MSDU aggregation & 0.4s guard interval
- Deep sleep power <10uA, Power down leakage current < 5uA
- Wake up and transmit packets in < 2ms
- Standby power consumption of < 1.0mW (DTIM3)
- +20 dBm output power in 802.11b mode
- Operating temperature range -40C ~ 125C
- FCC, CE, TELEC, WiFi Alliance, and SRRC certified

1.3. Parameters

Table 1 Parameters



Categories	Items	Values
WiFi Parameters	Certificates	FCC/CE/TELEC/SRRC
	WiFi Protocols	802.11 b/g/n
	Frequency Range	2.4G-2.5G (2400M-2483.5M)
	Tx Power	802.11 b: +20 dBm
		802.11 g: +17 dBm
		802.11 n: +14 dBm
	Rx Sensitivity	802.11 b: -91 dbm (11 Mbps)
		802.11 g: -75 dbm (54 Mbps)
		802.11 n: -72 dbm (MCS7)
	Types of Antenna	PCB Trace, External, IPEX Connector, Ceramic Chip
Hardware Parameters	Peripheral Bus	UART/SDIO/SPI/I2C/I2S/IR Remote Control
		GPIO/PWM
	Operating Voltage	3.0~3.6V
	Operating Current	Average value: 80mA
	Operating Temperature Range	-40°~125°
	Ambient Temperature Range	Normal temperature
	Package Size	5x5mm
	External Interface	N/A
Software Parameters	WiFi mode	station/softAP/SoftAP+station
	Security	WPA/WPA2
	Encryption	WEP/TKIP/AES
	Firmware Upgrade	UART Download / OTA (via network)
	Ssoftware Development	Supports Cloud Server Development / SDK for custom firmware development
	Network Protocols	IPv4, TCP/UDP/HTTP/FTP



User Configuration	AT Instruction Set, Cloud Server, Android/ iOS App
--------------------	---

1.4. Ultra Low Power Technology

ESP8266EX has been designed for mobile, wearable electronics and Internet of Things applications with the aim of achieving the lowest power consumption with a combination of several proprietary techniques. The power saving architecture operates mainly in 3 modes: active mode, sleep mode and deep sleep mode.

By using advance power management techniques and logic to power-down functions not required and to control switching between sleep and active modes, ESP8266EX consumes about than 60uA in deep sleep mode (with RTC clock still running) and less than 1.0mA (DTIM=3) or less than 0.5mA (DTIM=10) to stay connected to the access point.

When in sleep mode, only the calibrated real-time clock and watchdog remains active. The real-time clock can be programmed to wake up the ESP8266EX at any required interval.

The ESP8266EX can be programmed to wake up when a specified condition is detected. This minimal wake-up time feature of the ESP8266EX can be utilized by mobile device SOCs, allowing them to remain in the low-power standby mode until WiFi is needed.

In order to satisfy the power demand of mobile and wearable electronics, ESP8266EX can be programmed to reduce the output power of the PA to fit various application profiles, by trading off range for power consumption.

1.5. Major Applications

Major fields of ESP8266EX applications to Internet-of-Things include:

- Home Appliances
- Home Automation
- Smart Plug and lights
- Mesh Network
- Industrial Wireless Control
- Baby Monitors
- IP Cameras
- Sensor Networks
- Wearable Electronics



- WiFi Location-aware Devices
- Security ID Tags
- WiFi Position System Beacons



2. Hardware Overview

2.1. Pin Definitions

The pin assignments for 32-pin QFN package is illustrated in Fig.2.

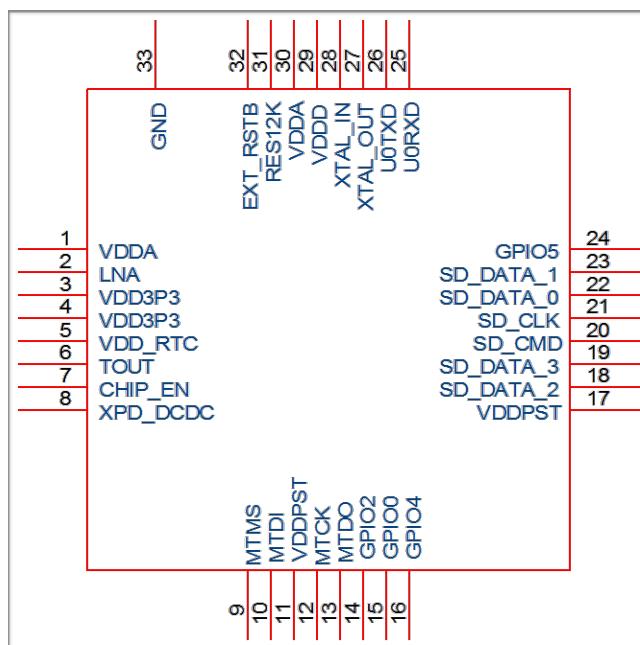


Figure 2 Pin Assignments

Table 2 below presents an overview on the general pin attributes and the functions of each pin.

Table 2 Pin Definitions

Pin	Name	Type	Function
1	VDDA	P	Analog Power 3.0 ~3.6V
2	LNA	I/O	RF Antenna Interface. Chip Output Impedance=50Ω No matching required but we recommend that the n-type matching network is retained.
3	VDD3P3	P	Amplifier Power 3.0~3.6V
4	VDD3P3	P	Amplifier Power 3.0~3.6V
5	VDD_RTC	P	NC (1.1V)



6	TOUT	I	ADC Pin (note: an internal pin of the chip) can be used to check the power voltage of VDD3P3 (Pin 3 and Pin4) or the input voltage of TOUT (Pin 6). These two functions cannot be used simultaneously.
7	CHIP_EN	I	Chip Enable. High: On, chip works properly; Low: Off, small current
8	XPD_DCDC	I/O	Deep-Sleep Wakeup; GPIO16
9	MTMS	I/O	GPIO14; HSPI_CLK
10	MTDI	I/O	GPIO12; HSPI_MISO
11	VDDPST	P	Digital/IO Power Supply (1.8V~3.3V)
12	MTCK	I/O	GPIO13; HSPI_MOSI; UART0_CTS
13	MTDO	I/O	GPIO15; HSPI_CS; UART0_RTS
14	GPIO2	I/O	UART Tx during flash programming; GPIO2
15	GPIO0	I/O	GPIO0; SPI_CS2
16	GPIO4	I/O	GPIO4
17	VDDPST	P	Digital/IO Power Supply (1.8V~3.3V)
18	SDIO_DATA_2	I/O	Connect to SD_D2 (Series R: 200Ω); SPIHD; HSPIHD; GPIO9
19	SDIO_DATA_3	I/O	Connect to SD_D3 (Series R: 200Ω); SPIWP; HSPIWP; GPIO10
20	SDIO_CMD	I/O	Connect to SD_CMD (Series R: 200Ω); SPI_CS0; GPIO11
21	SDIO_CLK	I/O	Connect to SD_CLK (Series R: 200Ω); SPI_CLK; GPIO6
22	SDIO_DATA_0	I/O	Connect to SD_D0 (Series R: 200Ω); SPI_MSIO; GPIO7
23	SDIO_DATA_1	I/O	Connect to SD_D1 (Series R: 200Ω); SPI_MOSI; GPIO8
24	GPIO5	I/O	GPIO5
25	U0RXD	I/O	UART Rx during flash programming; GPIO3
26	U0TXD	I/O	UART Tx during flash progamming; GPIO1; SPI_CS1
27	XTAL_OUT	I/O	Connect to crystal oscillator output, can be used to provide BT clock input
28	XTAL_IN	I/O	Connect to crystal oscillator input
29	VDDD	P	Analog Power 3.0V~3.6V
30	VDDA	P	Analog Power 3.0V~3.6V
31	RES12K	I	Serial connection with a 12 kΩ resistor and connect to the ground
32	EXT_RSTB	I	External reset signal (Low voltage level: Active)



Note: GPIO2, GPIO0, MTDO can be configurable as 3-bit SDIO mode.

2.2. Electrical Characteristics

Table 3 ESP8266EX Electrical Characteristics

Parameters		Conditions	Min	Typical	Max	Unit
Storage Temperature Range			-40	Normal	125	°C
Maximum Soldering Temperature		IPC/JEDEC J-STD-020			260	°C
Working Voltage Value			3.0	3.3	3.6	V
I/O	V_{IL}/V_{IH}		-0.3/0.75 V_{IO}		0.25 $V_{IO}/3.6$	V
	V_{OL}/V_{OH}		N/0.8 V_{IO}		0.1 V_{IO}/N	
	I_{MAX}				12	mA
Electrostatic Discharge (HBM)		TAMB=25°C			2	kV
Electrostatic Discharge (CDM)		TAMB=25°C			0.5	kV

2.3. Power Consumption

The following current consumption is based on 3.3V supply, and 25°C ambient, using internal regulators. Measurements are done at antenna port without SAW filter. All the transmitter's measurements are based on 90% duty cycle, continuous transmit mode.

Table 4 Description on Power Consumption

Parameters	Min	Typical	Max	Unit
Tx802.11b, CCK 11Mbps, P OUT=+17dBm		170		mA
Tx 802.11g, OFDM 54Mbps, P OUT =+15dBm		140		mA
Tx 802.11n, MCS7, P OUT =+13dBm		120		mA
Rx 802.11b, 1024 bytes packet length , -80dBm		50		mA
Rx 802.11g, 1024 bytes packet length, -70dBm		56		mA
Rx 802.11n, 1024 bytes packet length, -65dBm		56		mA
Modem-Sleep①		15		mA
Light-Sleep②		0.9		mA
Deep-Sleep③		10		uA
Power Off		0.5		uA



①: Modem-Sleep requires the CPU to be working, as in PWM or I2S applications. According to 802.11 standards (like U-APSD), it saves power to shut down the WiFi Modem circuit while maintaining a WiFi connection with no data transmission. E.g. in DTIM3, to maintain a sleep 300ms-wake 3ms cycle to receive AP's Beacon packages, the current is about 15mA

②: During Light-Sleep, the CPU may be suspended in applications like WiFi switch. Without data transmission, the WiFi Modem circuit can be turned off and CPU suspended to save power according to the 802.11 standard (U-APSD). E.g. in DTIM3, to maintain a sleep 300ms-wake 3ms cycle to receive AP's Beacon packages, the current is about 0.9mA.

③: Deep-Sleep does not require WiFi connection to be maintained. For application with long time lags between data transmission, e.g. a temperature sensor that checks the temperature every 100s, sleep 300s and waking up to connect to the AP (taking about 0.3~1s), the overall average current is less than 1mA.

2.4. Receiver Sensitivity

The following are measured under room temperature conditions with 3.3V and 1.1V power supplies.

Table 5 Receiver Sensitivity

Parameters	Min	Typical	Max	Unit
Input frequency	2412		2484	MHz
Input impedance		50		Ω
Input reflection			-10	dB
Output power of PA for 72.2Mbps	15.5	16.5	17.5	dBm
Output power of PA for 11b mode	19.5	20.5	21.5	dBm
Sensitivity				
DSSS, 1Mbps		-98		dBm
CCK, 11Mbps		-91		dBm
6Mbps (1/2 BPSK)		-93		dBm
54Mbps (3/4 64-QAM)		-75		dBm
HT20, MCS7 (65Mbps, 72.2Mbps)		-72		dBm
Adjacent Channel Rejection				
OFDM, 6Mbps		37		dB
OFDM, 54Mbps		21		dB
HT20, MCS0		37		dB
HT20, MCS7		20		dB



2.5. MCU

ESP8266EX is embedded with Tensilica L106 32-bit micro controller (MCU), which features extra low power consumption and 16-bit RSIC. The CPU clock speed is 80MHz. It can also reach a maximum value of 160MHz. Real Time Operation System (RTOS) is enabled. Currently, only 20% of MIPS has been occupied by the WiFi stack, the rest can all be used for user application programming and development. The following interfaces can be used to connect to the MCU embedded in ESP8266EX:

- Programmable RAM/ROM interfaces (iBus), which can be connected with memory controller, and can also be used to visit external flash;
- Data RAM interface (dBus), which can be connected with memory controller;
- AHB interface, can be used to visit the register.

2.6. Memory Organization

2.6.1. Internal SRAM and ROM

ESP8266EX WiFi SoC is embedded with memory controller, including SRAM and ROM. MCU can visit the memory units through iBus, dBus, and AHB interfaces. All memory units can be visited upon request, while a memory arbiter will decide the running sequence according to the time when these requests are received by the processor.

According to our current version of SDK provided, SRAM space that is available to users is assigned as below:

- **RAM size < 36kB**, that is to say, when ESP8266EX is working under the station mode and is connected to the router, programmable space accessible to user in heap and data section is around 36kB.)
- There is no programmable ROM in the SoC, therefore, user program must be stored in an external SPI flash.

2.6.2. External SPI Flash

An external SPI flash is used together with ESP8266EX to store user programs. Theoretically speaking, up to 16 Mbyte memory capacity can be supported.

Suggested SPI Flash memory capacity:

- OTA is disabled: the minimum flash memory that can be supported is 512 kByte;
- OTA is enabled: the minimum flash memory that can be supported is 1 Mbyte.

Several SPI modes can be supported, including Standard SPI, Dual SPI, DIO SPI, QIO SPI, and Quad SPI.



Therefore, please choose the correct SPI mode when you are downloading into the flash, otherwise firmwares/programs that you downloaded may not work in the right way.

2.7. AHB and APB Blocks

The AHB blocks performs the function of an arbiter, controls the AHB interfaces from the MAC, SDIO (host) and CPU. Depending on the address, the AHB data requests can go into one of the two slaves: APB block, or flash controller (usually for standalone applications).

Data requests to the memory controller are usually high speed requests, and requests to the APB block are usually register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within ESP8266's main blocks. Depending on the address, the APB request can go to the radio, SI/SPI, SDIO (host), GPIO, UART, real-time clock (RTC), MAC or digital baseband.



3. Pins and Definitions

The chipset encapsulates variable analog and data transmission I/Os, descriptions and definitions of which are explained below in detail.

3.1. GPIO

3.1.1. General Purpose Input/Output Interface (GPIO)

There are up to 17 GPIO pins. They can be assigned to various functions by the firmware. Each GPIO can be configured with internal pull-up (except XPD_DCDC, which is configured with internal pull-down), input available for sampling by a software register, input triggering an edge or level CPU interrupt, input triggering a level wakeup interrupt, open-drain or push-pull output driver, or output source from a software register, or a sigma-delta PWM DAC.

These pins are multiplexed with other functions such as I2C, I2S, UART, PWM, IR Remote Control, etc. Data I/O soldering pad is bidirectional and tri-state that include data input and output controlling buffer. Besides, I/O can be set as a specific state and remains like this. For example, if you intend to lower the power consumption of the chip, all data input and output enable signals can be set as remaining low power state. You can transport some specific state into the I/O. When the I/O is not powered by external circuits, the I/O will remain to be the state that it was used the last time. Some positive feedback is generated by the state-remaining function of the pins, therefore, if the external driving power must be stronger than the positive feedback. Even so, the driving power that is needed is within 5uA.

Table 6 Pin Definitions of GPIOs

Variables	Symbol	Min	Max	Unit
Input Low Voltage	V_{IL}	-0.3	$0.25 \times V_{IO}$	V
Input High Voltage	V_{IH}	$0.75 \times V_{IO}$	3.3	V
Input Leakage Current	I_{IL}		50	nA
Output Low Voltage	V_{OL}		$0.1 \times V_{IO}$	V
Output High Voltage	V_{OH}	$0.8 \times V_{IO}$		V
Input Pin Resistance Value	C_{pad}		2	pF
VDDIO	V_{IO}	1.8	3.3	V
Maximum Driving Power	I_{MAX}		12	mA
Temerperature	T_{amb}	-40	125	°C

All digital IO pins are protected from over-voltage with a snap-back circuit connected between the pad and ground. The snap back voltage is typically about 6V, and the holding voltage is 5.8V. This



provides protection from over-voltages and ESD. The output devices are also protected from reversed voltages with diodes.

3.2. Secure Digital Input/Output Interface (SDIO)

One Slave SDIO has been defined by ESP8266EX, the definitions of which are described in Table 7 below. 4bit 25MHz SDIO v1.1 and 4bit 50MHz SDIO v2.0 are supported.

Table 7 Pin Definitions of SDIOs

Pin Name	Pin Num	IO	Function Name
SDIO_CLK	21	IO6	SDIO_CLK
SDIO_DATA0	22	IO7	SDIO_DATA0
SDIO_DATA1	23	IO8	SDIO_DATA1
SDIO_DATA_2	18	IO9	SDIO_DATA_2
SDIO_DATA_3	19	IO10	SDIO_DATA_3
SDIO_CMD	20	IO11	SDIO_CMD

3.3. Serial Peripheral Interface (SPI/HSPI)

Currently, one general Slave/Master SPI, one Slave SDID/SPI, and one general Slave/Master HSPI have been defined by ESP8266EX. Functions of all these pins can be implemented via hardware. The pin definitions are described below:

3.3.1. General SPI (Master/Slave)

Table 8 Pin Definitions of General SPIs

Pin Name	Pin Num	IO	Function Name
SDIO_CLK	21	IO6	SPICLK
SDIO_DATA0	22	IO7	SPIQ/MISO
SDIO_DATA1	23	IO8	SPID/MOSI
SDIO_DATA_2	18	IO9	SPIHD
SDIO_DATA_3	19	IO10	SPIWP
SDIO_CMD	20	IO11	SPICS0
U0TXD	26	IO1	SPICS1
GPIO0	15	IO0	SPICS2



3.3.2. SDIO / SPI (Slave)

Table 9 Pin Definitions of SDIO / SPI (Slave)

Pin Name	Pin Num	IO	Function Name
SDIO_CLK	21	IO6	SPI_SLAVE_CLK
SDIO_DATA0	22	IO7	SPI_SLAVE_MISO
SDIO_DATA1	23	IO8	SPI_SLAVE_INT
SDIO_DATA_2	18	IO9	NC
SDIO_DATA_3	19	IO10	SPI_SLAVE_CS
SDIO_CMD	20	IO11	SPI_SLAVE_MOSI

3.3.3. HSPI (Master/Slave)

Table 10 Pin Definitions of HSPI (Master/Slave)

Pin Name	Pin Num	IO	Function Name
MTMS	9	IO14	HSPICLK
MTDI	10	IO12	HSPIQ/MISO
MTCK	12	IO13	HSPID/MOSI
MTDO	13	IO15	HPSICS

Note:

- SPI mode can be implemented via software programming. The clock frequency can reach up to a maximum value of 80MHz.
- Function of Slave SDIO/SPI interface can be implemented via hardware, and linked list DMA (Direct Memory Access) is supported, software overheads are smaller. However, there is no linked list DMA on general SPI and HSPI, and the software overheads are larger, therefore, the data transmitting speed will be restrained by software processing speed.

3.4. Inter-integrated Circuit Interface (I2C)

One I2C, which is mainly used to connect with micro controller and other peripheral equipment such as sensors, is defined by ESP8266EX. The present pin definition of I2C is as defined below:



Table 11 Pin Definitions of I2C

Pin Name	Pin Num	IO	Function Name
MTMS	9	IO14	I2C_SCL
GPIO2	14	IO2	I2C_SDA

Both I2C-Master and I2C-Slave are supported. I2C interface functionality can be realized via software programming, the clock frequency can be up to around 100KHz at most. It should be noted that I2C clock frequency should be higher than the slowest clock frequency of the slave device.

3.5. I2S

Currently one I2S data input interface and one I2S data output interface are defined. I2S interface is mainly used in applications such as data collection, processing, and transmission of audio data, as well as the input and output of serial data. For example, LED lights (WS2812 series) are supported. The pin definition of I2S is as defined below:

Table 12 Pin Definitions of I2S

I2S Data Input:			
Pin Name	Pin Num	IO	Function Name
MTDI	10	IO12	I2SI_DATA
MTCK	12	IO13	I2SI_BCK
MTMS	9	IO14	I2SI_WS

I2S Data Output:			
Pin Name	Pin Num	IO	Function Name
MTDO	13	IO15	I2SO_BCK
U0RXD	25	IO3	I2SO_DATA
GPIO2	14	IO2	I2SO_WS

I2S functionality can be realized via software programming, the GPIOs that will be used are multiplexed, and linked list DMA is supported.

3.6. Universal Asynchronous Receiver Transmitter (UART)

Two UART interfaces, UART0 and UART1, have been defined by ESP8266EX, the definitions are as below:



Table 13 Pin Definitions of UART Interfaces

Pin Type	Pin Name	Pin Num	IO	Function Name
UART0	U0RXD	25	IO3	U0RXD
	U0TXD	26	IO1	U0TXD
	MTDO	13	IO15	U0RTS
	MTCK	12	IO13	U0CTS
UART1	GPIO2	14	IO2	U1TXD
	SD_D1	23	IO8	U1RXD

Data transfers to/from UART interfaces can be implemented via hardware. The data transmission speed via UART interfaces can reach 115200*40 (4.5Mbps).

UART0 can be for communication. It supports fluid control. Since UART1 features only data transmit signal (Tx), it is usually used for printing log.

Notes: By default, UART0 will output some printed information when the device is powered on and is booting up. The baud rate of the printed information is closely related to the frequency of the external crystal oscillator. If the frequency of the crystal oscillator is 40MHz, then the baud rate for printing is 115200; if the frequency of the crystal oscillator is 26MHz, then the baud rate for printing is 74880. If the printed information exerts any influence on the functionality of your device, you'd better block the printing during the power-on period by changing ([U0TXD](#), [U0RXD](#)) to ([MTDO](#), [MTCK](#)).

3.7. Pulse-Width Modulation (PWM)

Four PWM output interfaces have been defined by ESP8266EX. They can be extended by users themselves. The present pin definitions of the PWM interfaces are defined as below:

Table 14 Pin Definitions of PWM Interfaces

Pin Name	Pin Num	IO	Function Name
MTDI	10	IO12	PWM0
MTDO	13	IO15	PWM1
MTMS	9	IO14	PWM2
GPIO4	16	IO4	PWM3

The functionality of PWM interfaces can be implemented via software programming. For example, in the LED smart light demo, the function of PWM is realized by interruption of the timer, the minimum resolution can reach as much as 44 ns. PWM frequency range is adjustable from 1000 us to 10000 us,



i.e., between 100Hz and 1KHz. When the PWM frequency is at 1 KHz, the duty ratio will reach 1/22727, and over 14 bit resolution will be achieved at 1KHz refresh rate.

3.8. IR Remote Control

Currently, only one Infrared remote control interface is defined, the pin definition is as below:

Table 14 Pin Definition of IR Remote Control

Pin Name	Pin Num	IO	Function Name
MTMS	9	IO12	IR Tx
GPIO5	24	IO5	IR Rx

The functionality of Infrared remote control interface can be implemented via software programming. NEC coding, modulation, and demodulation are used by this interface. The frequency of modulated carrier signal is 38KHz, while the duty ratio of the square wave is 1/3. The length of data transmission, which is around 1m, is determined by two factors: one is the maximum value of rated current, the other is internal current-limiting resistance value in the infrared receiver. The larger the resistance value, the lower the current, so is the power, and vice versa. The transmission angle is between 15° and 30°, and is mainly determined by the radiation direction of the infrared receiver.

Notes: Among the eight interfaces mentioned above, most of them can be multiplexed. Pin definitions that can be defined is not limited to the eight ones herein mentioned, customers can self customise the functions of the pins according to their specific application scenarios. Functions of these pins can be implemented via software programming and hardware.

3.9. ADC (Analog-to-digital Converter)

ESP8266EX is embedded with a 10-bit precision SARADC. Currently, TOUT (Pin6) is defined as ADC interface, the definition of which is described below:

Pin Name	Pin Num	Function Name
TOUT	6	ADC Interface

Table 16 Pin Definition of ADC

The following two applications can be implemented using ADC (Pin6). However, these two applications cannot be implemented concurrently.

- Test the power supply voltage of VDD3P3 (Pin 3 and Pin 4).

The function used to test the power supply voltage on PA_VDD pin is: `uint16 system_get_vdd33(void)`

- Test the input voltage of TOUT (Pin 6):



The function used to test the input voltage of TOUT is: `uint16 system_adc_read(void)`

RF-init parameter in the following passage refers to `esp_init_data_default.bin`

Application One: Test the power supply voltage of VDD3P3 (Pin 3 and Pin 4).

Hardware Design: TOUT must be dangled.

RF-init Parameter: The 107th byte of `esp_init_data_default.bin` (0 - 127 byte), "vdd33_const", must set to be 0xFF, i.e., the value of "vdd33_const" is 255.

RF Calibration Process: Optimize the RF circuit conditions based on the testing results of VDD3P3 (Pin 3 and Pin 4).

User Programming: Use `system_get_vdd33` instead of `system_adc_read`.

Application Two: Test the input voltage of TOUT (Pin 6).

Hardware Design: The input voltage range is 0 to 1.0 V when TOUT is connected to external circuit.

RF-init Parameter: The value of the 107th byte of `esp_init_data_default.bin` (0 - 127 byte), "vdd33_const", must be set to be the real power supply voltage of Pin 3 and Pin 4.

The working power voltage range of ESP8266EX is between 1.8V and 3.6V, while the unit of "vdd33_const" is 0.1V, therefore, the effective value range of "vdd33_const" is 18 to 36.

RF Calibration Process: Optimize the RF circuit conditions based on the value of "vdd33_const". The permissible error is $\pm 0.2V$.

User Programming: Use `system_adc_read` instead of `system_get_vdd33`.

Note One:

In **RF_init** parameter `esp_init_data_default.bin` (0 - 127 byte), the 107th byte is defined as "vdd33_const". Definitions of "vdd33_const" is described below:

- (1) If `vdd33_const = 0xff`, the power voltage of Pin 3 and Pin 4 will be tested by the internal self-calibration process of ESP8266EX chipset itself. RF circuit conditions should be optimized according to the testing results.



- (2) If $18 \leq vdd33_const \leq 36$, ESP8266EX RF Calibration and optimization process is implemented via $(vdd33_const/10)$.
- (3) If $vdd33_const < 18$ or $36 < vdd33_const < 255$, ESP8266EX RF Calibration and optimization process is implemented via the default value 3.0V.

Note Two:

Function `system_get_vdd33` is used to test the power supply voltage of VDD3P3 (Pin 3 and Pin 4). Details on this function are described below:

- (1) Pin Tout must be dangled. The 107th byte of `esp_init_data_default.bin` (0 - 127 byte), "vdd33_const", must set to be 0xFF.
- (2) If the 107th byte of `esp_init_data_default.bin` (0 - 127 byte), "vdd33_const", is equal to `0xff`, the returned value of function `system_get_vdd33` will be an effective value, otherwise `0xffff` will be returned.
- (3) The unit of the returned value is: 1/1024 V.

Note Three:

Function `system_adc_read` is defined to test the input voltage of Pin TOUT (Pin 6). Details on this function are described below:

- (1) The value of the 107th byte of `esp_init_data_default.bin` (0 - 127 byte), "vdd33_const", must be set to be the real power supply voltage of Pin 3 and Pin 4.
- (2) If the 107th byte of `esp_init_data_default.bin` (0 - 127 byte), "vdd33_const", is NOT equal to `0xff`, the returned value of `system_adc_read` will be an effective value of the input voltage of Pin TOUT, otherwise `0xffff` will be returned.
- (3) The unit of the returned value is: 1/1024 V.

3.10. LED Light and Button

ESP8266EX features up to 17 GPIOs, all of which can be assigned to realise various functions of LED lights and buttons. Definitions of some GPIOs that are assigned with certain functions in our demo application design are shown below:

Table 17 Pin Definitions of LED and Button

Pin Name	Pin Num	IO	Function Name
MTCK	12	IO13	Button (Reset)
GPIO0	15	IO0	WiFi Light
MTDI	10	IO12	Link Light



Altogether three interfaces have been defined, one is for the button, and the other two is for LED light. Generally, **MTCK** is used to control the reset button, **GPIO0** is used as an signal to indicate the WiFi working state, **MTDI** is used as a signal light to indicate communication between the device and the server.

Note: Among the nine interfaces mentioned above, most of them can be multiplexed. Pin definitions that can be defined is not limited to the eight ones herein mentioned, customers can self customise the functions of the pins according to their specific application scenarios. Functions of these pins can be implemented via software programming and hardware.



4. Firmware & Software Development Kit

The application and firmware is executed in on-chip ROM and SRAM, which loads the instructions during wake-up, through the SDIO interface, from the external flash.

The firmware implements TCP/IP, the full 802.11 b/g/n/e/i WLAN MAC protocol and WiFi Direct specification. It supports not only basic service set (BSS) operations under the distributed control function (DCF) but also P2P group operation compliant with the latest WiFi P2P protocol. Low level protocol functions are handled automatically by ESP8266:

- RTS/CTS
- acknowledgement
- fragmentation and defragmentation
- aggregation
- frame encapsulation (802.11h/RFC 1042)
- automatic beacon monitoring / scanning, and
- P2P WiFi direct

Passive or active scanning, as well as P2P discovery procedure is performed autonomously once initiated by the appropriate command. Power management is handled with minimum host interaction to minimize active duty period.

4.1. Features

The SDK includes the following library functions:

- 802.11 b/g/n/d/e/i/k/r support;
- WiFi Direct (P2P) support;
- P2P Discovery, P2P Group Owner mode, P2P Power Management
- Infrastructure BSS Station mode / P2P mode / softAP mode support;
- Hardware accelerators for CCMP (CBC-MAC, counter mode), TKIP (MIC, RC4), WAPI (SMS4), WEP (RC4), CRC;
- WPA/WPA2 PSK, and WPS driver;
- Additional 802.11i security features such as pre-authentication, and TSN;
- Open Interface for various upper layer authentication schemes over EAP such as TLS, PEAP, LEAP, SIM, AKA, or customer specific;
- 802.11n support (2.4GHz);
- Supports MIMO 1×1 and 2×1, STBC, A-MPDU and A-MSDU aggregation and 0.4μs guard interval;



- WMM power save U-APSD;
- Multiple queue management to fully utilize traffic prioritization defined by 802.11e standard;
- UMA compliant and certified;
- 802.1h/RFC1042 frame encapsulation;
- Scattered DMA for optimal CPU off load on Zero Copy data transfer operations;
- Antenna diversity and selection (software managed hardware);
- Clock/power gating combined with 802.11-compliant power management dynamically adapted to current connection condition providing minimal power consumption;
- Adaptive rate fallback algorithm sets the optimum transmission rate and Tx power based on actual SNR and packet loss information;
- Automatic retransmission and response on MAC to avoid packet discarding on slow host environment;
- Seamless roaming support;
- Configurable packet traffic arbitration (PTA) with dedicated slave processor based design provides flexible and exact timing Bluetooth co-existence support for a wide range of Bluetooth Chip vendors;
- Dual and single antenna Bluetooth co-existence support with optional simultaneous receive (WiFi/Bluetooth) capability.

5. Power Management

The chip can be put into the following states:

- **OFF**: CHIP_PD pin is low. The RTC is disabled. All registers are cleared.
- **DEEP_SLEEP**: Only RTC is powered on - the rest of the chip is powered off. Recovery memory of RTC can keep basic WiFi connecting information.
- **SLEEP**: Only the RTC is operating. The crystal oscillator is disabled. Any wakeup events (MAC, host, RTC timer, external interrupts) will put the chip into the WAKEUP state.
- **WAKEUP**: In this state, the system goes from the sleep states to the PWR state. The crystal oscillator and PLLs are enabled.
- **ON**: the high speed clock is operational and sent to each block enabled by the clock control register. Lower level clock gating is implemented at the block level, including the CPU, which can be gated off using the WAITI instruction, while the system is on.

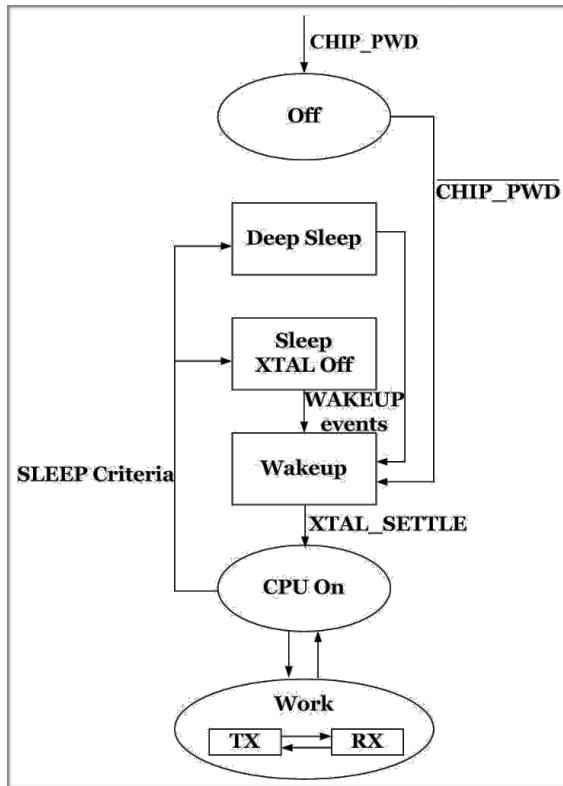


Figure 3 Illustration of Power Management

6. Clock Management

6.1. High Frequency Clock

The high frequency clock on ESP8266EX is used to drive both transmit and receive mixers. This clock is generated from the internal crystal oscillator and an external crystal. The crystal frequency can range from 26MHz to 52MHz.

While internal calibration of the crystal oscillator ensures that a wide range of crystals can be used, in general, the quality of the crystal is still a factor to consider, to have reasonable phase noise that is required for good performance. When the crystal selected is sub-optimal due to large frequency drifts or poor Q-factor, the maximum throughput and sensitivity of the WiFi system is degraded. Please refer to the application notes on how the frequency offset can be measured.



Table 18 High Frequency Clock

Parameter	Symbol	Min	Max	Unit
Frequency	FXO	26	52	MHz
Loading capacitance	CL		32	pF
Motional capacitance	CM	2	5	pF
Series resistance	RS	0	65	Ω
Frequency tolerance	Δ FXO	-15	15	ppm
Frequency vs temperature (-25°C ~ 75°C)	Δ FXO,Temp	-15	15	ppm

6.2. External Reference Requirements

For an externally generated clock, the frequency can range from 26MHz to 52MHz can be used. For good performance of the radio, the following characteristics are expected of the clock:

Table 19 External Clock Reference

Parameter	Symbol	Min	Max	Unit
Clock amplitude	VXO	0.2	1	Vpp
External clock accuracy	Δ FXO,EXT	-15	15	ppm
Phase noise @1kHz offset, 40MHz clock			-120	dBc/Hz
Phase noise @10kHz offset, 40MHz clock			-130	dBc/Hz
Phase noise @100kHz offset, 40MHz clock			-138	dBc/Hz

7. Radio

The ESP8266EX radio consists of the following main blocks:

- 2.4GHz receiver
- 2.4GHz transmitter
- High speed clock generators and crystal oscillator
- Real time clock
- Bias and regulators
- Power management



7.1. Channel Frequencies

The RF transceiver supports the following channels according to the IEEE802.11b/g/n standards.

Table 20 Frequency Channel

Channel No	Frequency (MHz)	Channel No	Frequency (MHz)
1	2412	8	2447
2	2417	9	2452
3	2422	10	2457
4	2427	11	2462
5	2432	12	2467
6	2437	13	2472
7	2442	14	2484

7.2. 2.4 GHz Receiver

The 2.4GHz receiver downconverts the RF signal to quadrature baseband signals and converts them to the digital domain with 2 high resolution high speed ADCs. To adapt to varying signal channel conditions, RF filters, automatic gain control (AGC), DC offset cancelation circuits and baseband filters are integrated within ESP8266EX.

7.3. 2.4 GHz Transmitter

The 2.4GHz transmitter up-converts the quadrature baseband signals to 2.4GHz, and drives the antenna with a high powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier, enabling a state of art performance of delivering +19.5dBm average power for 802.11b transmission and +16dBm for 802.11n transmission.

Additional calibrations are integrated to cancel any imperfections of the radio, such as:

- carrier leakage,
- I/Q phase matching, and
- baseband nonlinearities

This reduces the amount of time required and test equipment required for production testing.

7.4. Clock Generator

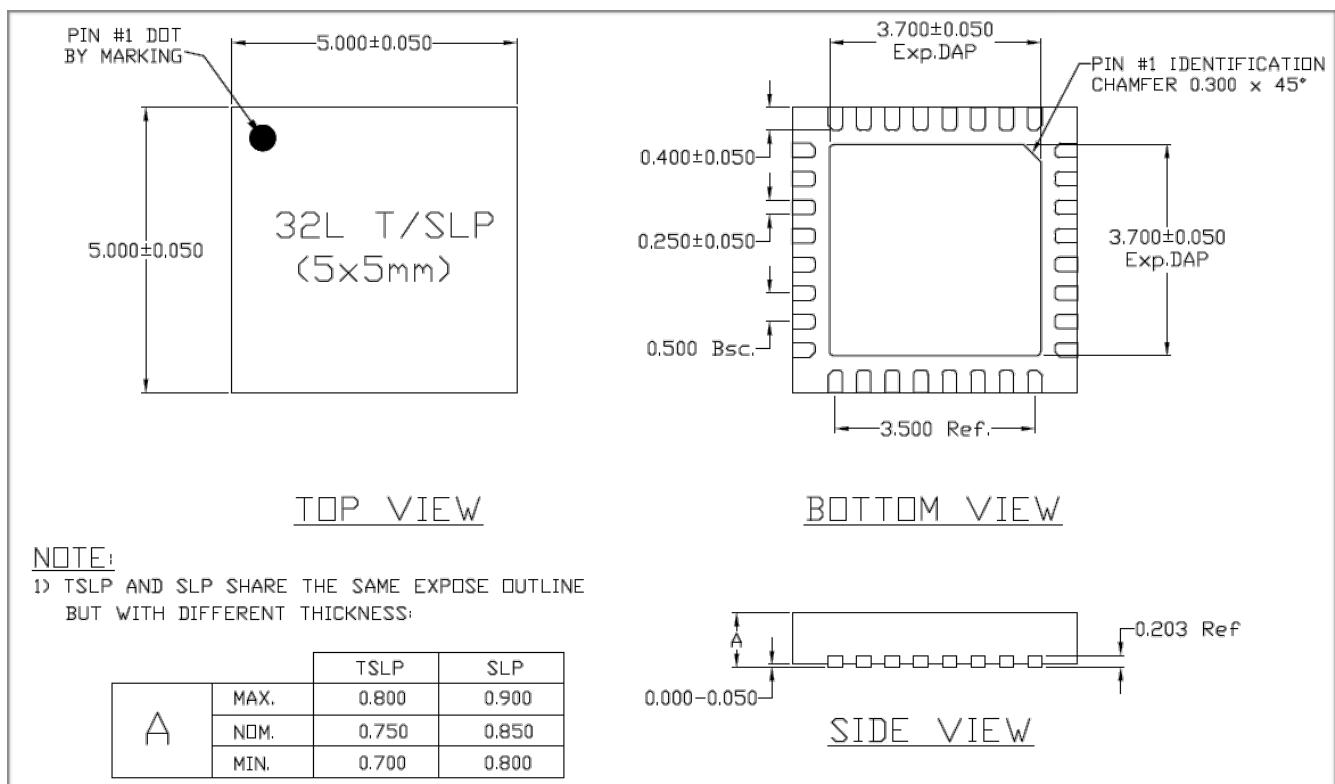
The clock generator generates quadrature 2.4 GHz clock signals for the receiver and transmitter. All components of the clock generator are integrated on-chip, including:



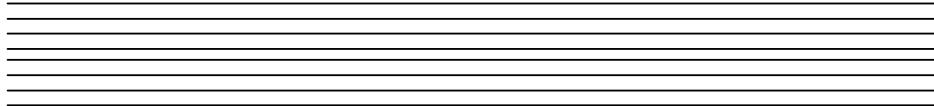
- inductor,
- varactor, and
- loop filter

The clock generator has built-in calibration and self test circuits. Quadrature clock phases and phase noise are optimized on-chip with patented calibration algorithms to ensure the best receiver and transmitter performance.

8. Appendix: QFN32 Package Size



9.2. Hoja de datos de ST7735 TFT Display



Sitronix

ST7735

262K Color Single-Chip TFT Controller/Driver

1 Introduction

The ST7735 is a single-chip controller/driver for 262K-color, graphic type TFT-LCD. It consists of 396 source line and 162 gate line driving circuits. This chip is capable of connecting directly to an external microprocessor, and accepts Serial Peripheral Interface (SPI), 8-bit/9-bit/16-bit/18-bit parallel interface. Display data can be stored in the on-chip display data RAM of 132 x 162 x 18 bits. It can perform display data RAM read/write operation with no external operation clock to minimize power consumption. In addition, because of the integrated power supply circuits necessary to drive liquid crystal, it is possible to make a display system with fewer components.

2 Features

Single chip TFT-LCD Controller/Driver with RAM

On-chip Display Data RAM (i.e. Frame Memory)

- 132 (H) x RGB x 162 (V) bits

LCD Driver Output Circuits:

- Source Outputs: 132 RGB channels

- Gate Outputs: 162 channels

- Common electrode output

Display Resolution

- 132 (RGB) x 162

- (GM[2:0]= "000", DDRAM: 132 x 18-bits x 162)

- 128 (RGB) x 160

- (GM[2:0]= "011", DDRAM: 128 x 18-bits x 160)

Display Colors (Color Mode)

- Full Color: 262K, RGB=(666) max., Idle Mode OFF

- Color Reduce: 8-color, RGB=(111), Idle Mode ON

Programmable Pixel Color Format (Color Depth) for Various Display Data input Format

- 12-bit/pixel: RGB=(444) using the 384k-bit frame memory and LUT

- 16-bit/pixel: RGB=(565) using the 384k-bit frame memory and LUT

- 18-bit/pixel: RGB=(666) using the 384k-bit frame memory and LUT

Various Interfaces

- Parallel 8080-series MCU Interface

- (8-bit, 9-bit, 16-bit & 18-bit)

- 3-line serial interface

- 4-line serial interface

Display Features

- Programmable partial display duty

- Line inversion, frame inversion

- Support both normal-black & normal-white LC

- Software programmable color depth mode

Built-in Circuits

- DC/DC converter

- Adjustable VCOM generation

- Non-volatile (NV) memory to store initial register setting

- Oscillator for display clock generation

- Factory default value (module ID, module version, etc) are stored in NV memory

- Timing controller

Built-in NV Memory for LCD Initial Register Setting

- 7-bits for ID2

- 8-bits for ID3

- 7-bits for VCOM adjustment

Wide Supply Voltage Range

- I/O Voltage (VDDI to DGND): 1.65V~VDD
(VDDI ≤ VDD)

- Analog Voltage (VDD to AGND): 2.6V~3.3V

On-Chip Power System

- Source Voltage (GVDD to AGND): 3.0V~5.0V

- VCOM HIGH level (VCOMH to AGND): 2.5V to 5.0V

- VCOM LOW level (VCOML to AGND): -2.4V to 0.0V

- Gate driver HIGH level (VGH to AGND):
+10.0V to +15V

- Gate driver LOW level (VGL to AGND):
-12.4V to -7.5V

Operating Temperature: -30°C to +85°C

ST7735

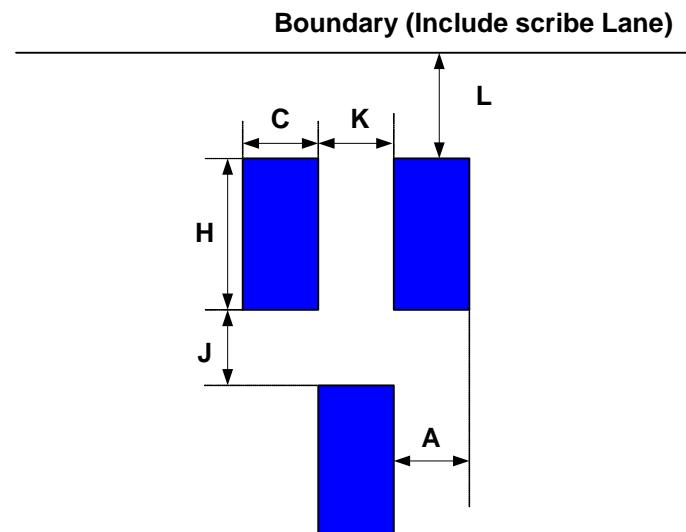
Parallel Interface: 8-bit/9-bit/16-bit/18-bit
Serial Interface: 3-line/4-line



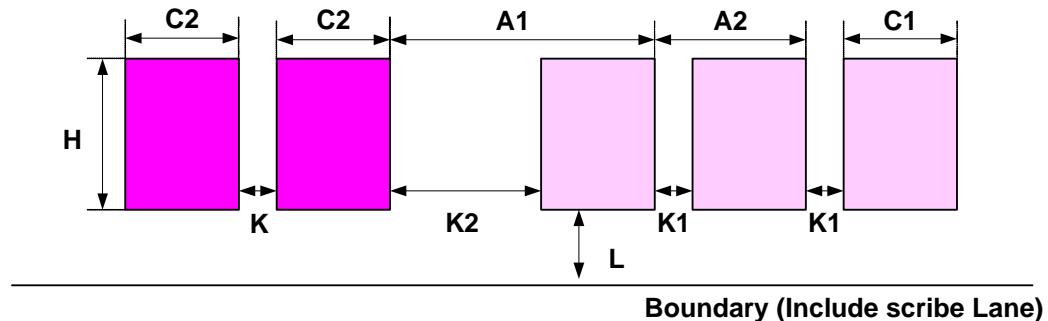
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3 Pad arrangement

3.1 Output Bump Dimension

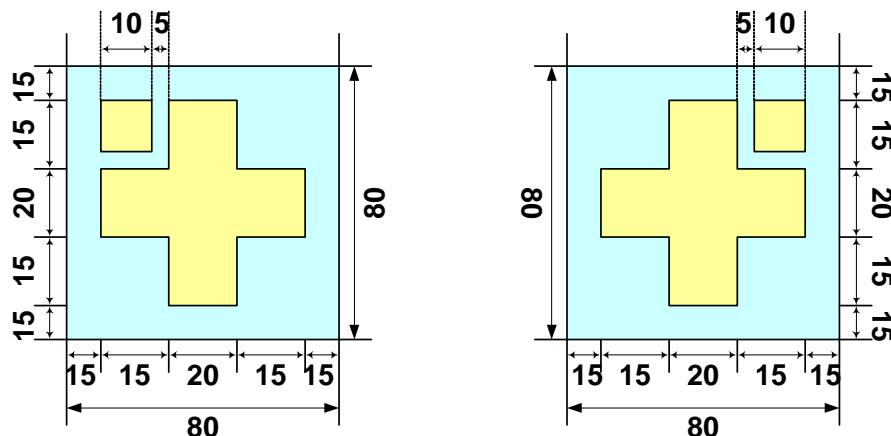


Item	Symbol	Size
Bump pitch	A	16 um
Bump width	C	16 um
Bump height	H	98 um
Bump gap1 (Vertical)	J	19 um
Bump gap2 (Horizontal)	K	16 um
Bump area	C x H	1568 um ²
Chip Boundary (include scribe Lane)	L	59 um

3.2 Input Bump Dimension

Item	Symbol	Size
Bump pitch 1	A_1	67 um
Bump pitch 2	A_2	50 um
Bump width 1	C_1	35 um
Bump width 2	C_2	40 um
Bump height	H	90 um
Bump gap	K	20 um
Bump gap1	K_1	15 um
Bump gap2	K_2	32 um
Bump area 1	$C_1 \times H$	3150 um ²
Bump area 2	$C_2 \times H$	3690 um ²
Chip Boundary(include scribe Lane)	L	59 um

3.3 Alignment Mark Dimension



3.4 Chip Information

Chip size (um x um): 9900 x 670

PAD coordinate: pad center

Coordinate origin: chip center

Chip thickness (um): 300 (TYP)

Bump height (um): 15 (TYP)

Bump hardness (HV): 75 (TYP)

4 Pad Center Coordinates

No.	PAD Name	X	Y
1	DUMMY	-4750	-231
2	VDDIO	-4700	-231
3	EXTC	-4650	-231
4	DGNDO	-4600	-231
5	IM0	-4550	-231
6	VDDIO	-4500	-231
7	IM1	-4450	-231
8	DGNDO	-4400	-231
9	DUMMY	-4350	-231
10	VDDIO	-4300	-231
11	TPI[1]	-4250	-231
12	DGNDO	-4200	-231
13	TPI[2]	-4150	-231
14	VDDIO	-4100	-231
15	SRGB	-4050	-231
16	DGNDO	-4000	-231
17	SMX	-3950	-231
18	VDDIO	-3900	-231
19	SMY	-3850	-231
20	DGNDO	-3800	-231
21	DUMMY	-3750	-231
22	VDDIO	-3700	-231
23	DUMMY	-3650	-231
24	DGNDO	-3600	-231
25	DUMMY	-3550	-231
26	VDDIO	-3500	-231
27	DUMMY	-3450	-231
28	DGNDO	-3400	-231
29	DUMMY	-3350	-231
30	VDDIO	-3300	-231
31	LCM	-3250	-231
32	DGNDO	-3200	-231
33	DUMMY	-3150	-231
34	VDDIO	-3100	-231
35	GM2	-3050	-231
36	DGNDO	-3000	-231
37	GM1	-2950	-231
38	VDDIO	-2900	-231
39	GM0	-2850	-231
40	DGNDO	-2800	-231
41	DUMMY	-2750	-231
42	GS	-2700	-231
43	SPI4W	-2650	-231
44	VDDIO	-2600	-231
45	TPO[8]	-2550	-231
46	TPO[7]	-2500	-231
47	TPO[6]	-2450	-231
48	TPO[5]	-2400	-231
49	TPO[4]	-2350	-231
50	OSC	-2300	-231

No.	PAD Name	X	Y
51	VDD	-2250	-231
52	VDD	-2200	-231
53	VDD	-2150	-231
54	VDD	-2100	-231
55	VDD	-2050	-231
56	VDD	-2000	-231
57	AGND	-1950	-231
58	AGND	-1900	-231
59	AGND	-1850	-231
60	AGND	-1800	-231
61	AGND	-1750	-231
62	AGND	-1700	-231
63	RDX	-1630	-231
64	D/CX	-1570	-231
65	TESEL	-1510	-231
66	DGNDO	-1450	-231
67	D17	-1390	-231
68	D16	-1330	-231
69	D15	-1270	-231
70	D14	-1210	-231
71	D13	-1150	-231
72	D12	-1090	-231
73	D11	-1030	-231
74	D10	-970	-231
75	D9	-910	-231
76	D8	-850	-231
77	D1	-790	-231
78	D3	-730	-231
79	D5	-670	-231
80	D7	-610	-231
81	TE	-550	-231
82	RESX	-490	-231
83	CSX	-430	-231
84	D6	-370	-231
85	D4	-310	-231
86	D2	-250	-231
87	IM2	-190	-231
88	D0	-130	-231
89	WRX	-70	-231
90	DUMMY	0	-231
91	DUMMY	50	-231
92	DUMMY	100	-231
93	DUMMY	150	-231
94	TPO[3]	200	-231
95	TPO[2]	250	-231
96	TPO[1]	300	-231
97	DGND	350	-231
98	DGND	400	-231
99	DGND	450	-231
100	DGND	500	-231

No.	PAD Name	X	Y
101	DGND	550	-231
102	DGND	600	-231
103	VDDI	650	-231
104	VDDI	700	-231
105	VDDI	750	-231
106	VDDI	800	-231
107	VDDI	850	-231
108	VDDI	900	-231
109	VCC	950	-231
110	VCC	1000	-231
111	VCCO	1050	-231
112	VCI1	1100	-231
113	VCI1	1150	-231
114	VCI1	1200	-231
115	VREF	1250	-231
116	VREF	1300	-231
117	VREF	1350	-231
118	DUMMY	1400	-231
119	DUMMY	1450	-231
120	AVDD	1500	-231
121	AVDD	1550	-231
122	AVDD	1600	-231
123	AVDDO	1650	-231
124	AVDDO	1700	-231
125	GVDD	1750	-231
126	GVDD	1800	-231
127	GVDD	1850	-231
128	DUMMY	1900	-231
129	DUMMY	1950	-231
130	C11P	2000	-231
131	C11P	2050	-231
132	C11P	2100	-231
133	C11P	2150	-231
134	C11N	2200	-231
135	C11N	2250	-231
136	C11N	2300	-231
137	C11N	2350	-231
138	C12P	2400	-231
139	C12P	2450	-231
140	C12P	2500	-231
141	C12P	2550	-231
142	C12N	2600	-231
143	C12N	2650	-231
144	C12N	2700	-231
145	C12N	2750	-231
146	AGND	2800	-231
147	AGND	2850	-231
148	AGND	2900	-231
149	VCL	2950	-231
150	VCL	3000	-231

No.	PAD Name	X	Y
151	VCL	3050	-231
152	C41P	3100	-231
153	C41P	3150	-231
154	C41P	3200	-231
155	C41N	3250	-231
156	C41N	3300	-231
157	C41N	3350	-231
158	C22P	3400	-231
159	C22P	3450	-231
160	C22P	3500	-231
161	C22N	3550	-231
162	C22N	3600	-231
163	C22N	3650	-231
164	C23P	3700	-231
165	C23P	3750	-231
166	C23P	3800	-231
167	C23N	3850	-231
168	C23N	3900	-231
169	C23N	3950	-231
170	VGL	4000	-231
171	VGL	4050	-231
172	VGL	4100	-231
173	VGH	4150	-231
174	VGH	4200	-231
175	VGHO	4250	-231
176	VCOMH	4300	-231
177	VCOMH	4350	-231
178	VCOMH	4400	-231
179	VCOML	4450	-231
180	VCOML	4500	-231
181	VCOML	4550	-231
182	VCOM	4600	-231
183	VCOM	4650	-231
184	VCOM	4700	-231
185	DUMMY	4750	-231
186	DUMMY	4772	110
187	DUMMY	4756	227
188	G162	4740	110
189	G160	4724	227
190	G158	4708	110
191	G156	4692	227
192	G154	4676	110
193	G152	4660	227
194	G150	4644	110
195	G148	4628	227
196	G146	4612	110
197	G144	4596	227
198	G142	4580	110
199	G140	4564	227
200	G138	4548	110

No.	PAD Name	X	Y
201	G136	4532	227
202	G134	4516	110
203	G132	4500	227
204	G130	4484	110
205	G128	4468	227
206	G126	4452	110
207	G124	4436	227
208	G122	4420	110
209	G120	4404	227
210	G118	4388	110
211	G116	4372	227
212	G114	4356	110
213	G112	4340	227
214	G110	4324	110
215	G108	4308	227
216	G106	4292	110
217	G104	4276	227
218	G102	4260	110
219	G100	4244	227
220	G98	4228	110
221	G96	4212	227
222	G94	4196	110
223	G92	4180	227
224	G90	4164	110
225	G88	4148	227
226	G86	4132	110
227	G84	4116	227
228	G82	4100	110
229	G80	4084	227
230	G78	4068	110
231	G76	4052	227
232	G74	4036	110
233	G72	4020	227
234	G70	4004	110
235	G68	3988	227
236	G66	3972	110
237	G64	3956	227
238	G62	3940	110
239	G60	3924	227
240	G58	3908	110
241	G56	3892	227
242	G54	3876	110
243	G52	3860	227
244	G50	3844	110
245	G48	3828	227
246	G46	3812	110
247	G44	3796	227
248	G42	3780	110
249	G40	3764	227
250	G38	3748	110

No.	PAD Name	X	Y
251	G36	3732	227
252	G34	3716	110
253	G32	3700	227
254	G30	3684	110
255	G28	3668	227
256	G26	3652	110
257	G24	3636	227
258	G22	3620	110
259	G20	3604	227
260	G18	3588	110
261	G16	3572	227
262	G14	3556	110
263	G12	3540	227
264	G10	3524	110
265	G8	3508	227
266	G6	3492	110
267	G4	3476	227
268	G2	3460	110
269	DUMMY	3444	227
270	DUMMY	3428	110
271	DUMMY	3412	227
272	DUMMY	3396	110
273	S396	3380	227
274	S395	3364	110
275	S394	3348	227
276	S393	3332	110
277	S392	3316	227
278	S391	3300	110
279	S390	3284	227
280	S389	3268	110
281	S388	3252	227
282	S387	3236	110
283	S386	3220	227
284	S385	3204	110
285	S384	3188	227
286	S383	3172	110
287	S382	3156	227
288	S381	3140	110
289	S380	3124	227
290	S379	3108	110
291	S378	3092	227
292	S377	3076	110
293	S376	3060	227
294	S375	3044	110
295	S374	3028	227
296	S373	3012	110
297	S372	2996	227
298	S371	2980	110
299	S370	2964	227
300	S369	2948	110

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No.	PAD Name	X	Y
301	S368	2932	227
302	S367	2916	110
303	S366	2900	227
304	S365	2884	110
305	S364	2868	227
306	S363	2852	110
307	S362	2836	227
308	S361	2820	110
309	S360	2804	227
310	S359	2788	110
311	S358	2772	227
312	S357	2756	110
313	S356	2740	227
314	S355	2724	110
315	S354	2708	227
316	S353	2692	110
317	S352	2676	227
318	S351	2660	110
319	S350	2644	227
320	S349	2628	110
321	S348	2612	227
322	S347	2596	110
323	S346	2580	227
324	S345	2564	110
325	S344	2548	227
326	S343	2532	110
327	S342	2516	227
328	S341	2500	110
329	S340	2484	227
330	S339	2468	110
331	S338	2452	227
332	S337	2436	110
333	S336	2420	227
334	S335	2404	110
335	S334	2388	227
336	S333	2372	110
337	S332	2356	227
338	S331	2340	110
339	S330	2324	227
340	S329	2308	110
341	S328	2292	227
342	S327	2276	110
343	S326	2260	227
344	S325	2244	110
345	S324	2228	227
346	S323	2212	110
347	S322	2196	227
348	S321	2180	110
349	S320	2164	227
350	S319	2148	110

No.	PAD Name	X	Y
351	S318	2132	227
352	S317	2116	110
353	S316	2100	227
354	S315	2084	110
355	S314	2068	227
356	S313	2052	110
357	S312	2036	227
358	S311	2020	110
359	S310	2004	227
360	S309	1988	110
361	S308	1972	227
362	S307	1956	110
363	S306	1940	227
364	S305	1924	110
365	S304	1908	227
366	S303	1892	110
367	S302	1876	227
368	S301	1860	110
369	S300	1844	227
370	S299	1828	110
371	S298	1812	227
372	S297	1796	110
373	S296	1780	227
374	S295	1764	110
375	S294	1748	227
376	S293	1732	110
377	S292	1716	227
378	S291	1700	110
379	S290	1684	227
380	S289	1668	110
381	S288	1652	227
382	S287	1636	110
383	S286	1620	227
384	S285	1604	110
385	S284	1588	227
386	S283	1572	110
387	S282	1556	227
388	S281	1540	110
389	S280	1524	227
390	S279	1508	110
391	S278	1492	227
392	S277	1476	110
393	S276	1460	227
394	S275	1444	110
395	S274	1428	227
396	S273	1412	110
397	S272	1396	227
398	S271	1380	110
399	S270	1364	227
400	S269	1348	110

No.	PAD Name	X	Y
401	S268	1332	227
402	S267	1316	110
403	S266	1300	227
404	S265	1284	110
405	S264	1268	227
406	S263	1252	110
407	S262	1236	227
408	S261	1220	110
409	S260	1204	227
410	S259	1188	110
411	S258	1172	227
412	S257	1156	110
413	S256	1140	227
414	S255	1124	110
415	S254	1108	227
416	S253	1092	110
417	S252	1076	227
418	S251	1060	110
419	S250	1044	227
420	S249	1028	110
421	S248	1012	227
422	S247	996	110
423	S246	980	227
424	S245	964	110
425	S244	948	227
426	S243	932	110
427	S242	916	227
428	S241	900	110
429	S240	884	227
430	S239	868	110
431	S238	852	227
432	S237	836	110
433	S236	820	227
434	S235	804	110
435	S234	788	227
436	S233	772	110
437	S232	756	227
438	S231	740	110
439	S230	724	227
440	S229	708	110
441	S228	692	227
442	S227	676	110
443	S226	660	227
444	S225	644	110
445	S224	628	227
446	S223	612	110
447	S222	596	227
448	S221	580	110
449	S220	564	227
450	S219	548	110

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No.	PAD Name	X	Y
451	S218	532	227
452	S217	516	110
453	S216	500	227
454	S215	484	110
455	S214	468	227
456	S213	452	110
457	S212	436	227
458	S211	420	110
459	S210	404	227
460	S209	388	110
461	S208	372	227
462	S207	356	110
463	S206	340	227
464	S205	324	110
465	S204	308	227
466	S203	292	110
467	S202	276	227
468	S201	260	110
469	S200	244	227
470	S199	228	110
471	DUMMY	212	227
472	DUMMY	196	110
473	DUMMY	-196	110
474	DUMMY	-212	227
475	S198	-228	110
476	S197	-244	227
477	S196	-260	110
478	S195	-276	227
479	S194	-292	110
480	S193	-308	227
481	S192	-324	110
482	S191	-340	227
483	S190	-356	110
484	S189	-372	227
485	S188	-388	110
486	S187	-404	227
487	S186	-420	110
488	S185	-436	227
489	S184	-452	110
490	S183	-468	227
491	S182	-484	110
492	S181	-500	227
493	S180	-516	110
494	S179	-532	227
495	S178	-548	110
496	S177	-564	227
497	S176	-580	110
498	S175	-596	227
499	S174	-612	110
500	S173	-628	227

No.	PAD Name	X	Y
501	S172	-644	110
502	S171	-660	227
503	S170	-676	110
504	S169	-692	227
505	S168	-708	110
506	S167	-724	227
507	S166	-740	110
508	S165	-756	227
509	S164	-772	110
510	S163	-788	227
511	S162	-804	110
512	S161	-820	227
513	S160	-836	110
514	S159	-852	227
515	S158	-868	110
516	S157	-884	227
517	S156	-900	110
518	S155	-916	227
519	S154	-932	110
520	S153	-948	227
521	S152	-964	110
522	S151	-980	227
523	S150	-996	110
524	S149	-1012	227
525	S148	-1028	110
526	S147	-1044	227
527	S146	-1060	110
528	S145	-1076	227
529	S144	-1092	110
530	S143	-1108	227
531	S142	-1124	110
532	S141	-1140	227
533	S140	-1156	110
534	S139	-1172	227
535	S138	-1188	110
536	S137	-1204	227
537	S136	-1220	110
538	S135	-1236	227
539	S134	-1252	110
540	S133	-1268	227
541	S132	-1284	110
542	S131	-1300	227
543	S130	-1316	110
544	S129	-1332	227
545	S128	-1348	110
546	S127	-1364	227
547	S126	-1380	110
548	S125	-1396	227
549	S124	-1412	110
550	S123	-1428	227

No.	PAD Name	X	Y
551	S122	-1444	110
552	S121	-1460	227
553	S120	-1476	110
554	S119	-1492	227
555	S118	-1508	110
556	S117	-1524	227
557	S116	-1540	110
558	S115	-1556	227
559	S114	-1572	110
560	S113	-1588	227
561	S112	-1604	110
562	S111	-1620	227
563	S110	-1636	110
564	S109	-1652	227
565	S108	-1668	110
566	S107	-1684	227
567	S106	-1700	110
568	S105	-1716	227
569	S104	-1732	110
570	S103	-1748	227
571	S102	-1764	110
572	S101	-1780	227
573	S100	-1796	110
574	S99	-1812	227
575	S98	-1828	110
576	S97	-1844	227
577	S96	-1860	110
578	S95	-1876	227
579	S94	-1892	110
580	S93	-1908	227
581	S92	-1924	110
582	S91	-1940	227
583	S90	-1956	110
584	S89	-1972	227
585	S88	-1988	110
586	S87	-2004	227
587	S86	-2020	110
588	S85	-2036	227
589	S84	-2052	110
590	S83	-2068	227
591	S82	-2084	110
592	S81	-2100	227
593	S80	-2116	110
594	S79	-2132	227
595	S78	-2148	110
596	S77	-2164	227
597	S76	-2180	110
598	S75	-2196	227
599	S74	-2212	110
600	S73	-2228	227

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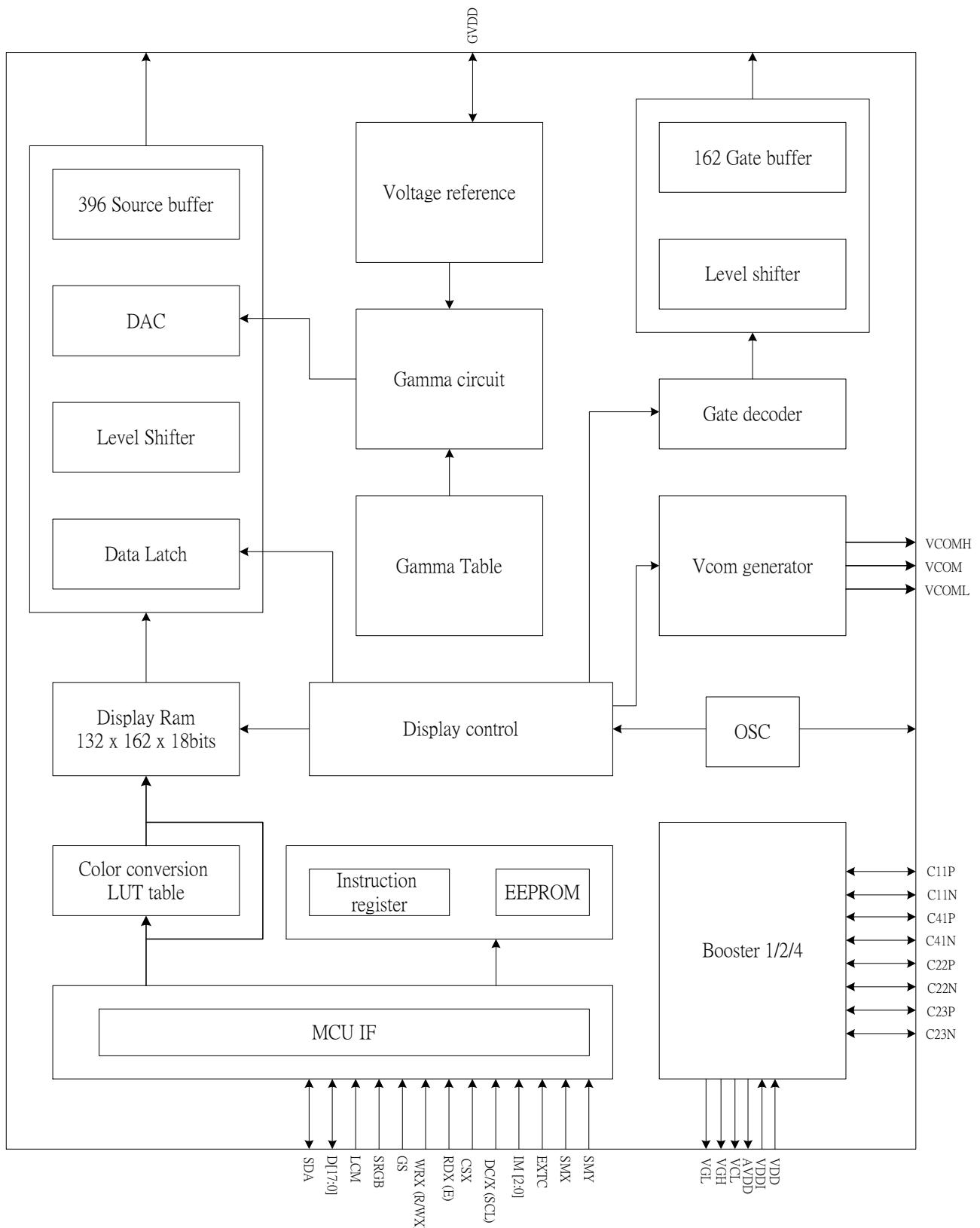
No.	PAD Name	X	Y
601	S72	-2244	110
602	S71	-2260	227
603	S70	-2276	110
604	S69	-2292	227
605	S68	-2308	110
606	S67	-2324	227
607	S66	-2340	110
608	S65	-2356	227
609	S64	-2372	110
610	S63	-2388	227
611	S62	-2404	110
612	S61	-2420	227
613	S60	-2436	110
614	S59	-2452	227
615	S58	-2468	110
616	S57	-2484	227
617	S56	-2500	110
618	S55	-2516	227
619	S54	-2532	110
620	S53	-2548	227
621	S52	-2564	110
622	S51	-2580	227
623	S50	-2596	110
624	S49	-2612	227
625	S48	-2628	110
626	S47	-2644	227
627	S46	-2660	110
628	S45	-2676	227
629	S44	-2692	110
630	S43	-2708	227
631	S42	-2724	110
632	S41	-2740	227
633	S40	-2756	110
634	S39	-2772	227
635	S38	-2788	110
636	S37	-2804	227
637	S36	-2820	110
638	S35	-2836	227
639	S34	-2852	110
640	S33	-2868	227
641	S32	-2884	110
642	S31	-2900	227
643	S30	-2916	110
644	S29	-2932	227
645	S28	-2948	110
646	S27	-2964	227
647	S26	-2980	110
648	S25	-2996	227
649	S24	-3012	110
650	S23	-3028	227

No.	PAD Name	X	Y
651	S22	-3044	110
652	S21	-3060	227
653	S20	-3076	110
654	S19	-3092	227
655	S18	-3108	110
656	S17	-3124	227
657	S16	-3140	110
658	S15	-3156	227
659	S14	-3172	110
660	S13	-3188	227
661	S12	-3204	110
662	S11	-3220	227
663	S10	-3236	110
664	S9	-3252	227
665	S8	-3268	110
666	S7	-3284	227
667	S6	-3300	110
668	S5	-3316	227
669	S4	-3332	110
670	S3	-3348	227
671	S2	-3364	110
672	S1	-3380	227
673	DUMMY	-3396	110
674	DUMMY	-3412	227
675	DUMMY	-3428	110
676	DUMMY	-3444	227
677	G1	-3460	110
678	G3	-3476	227
679	G5	-3492	110
680	G7	-3508	227
681	G9	-3524	110
682	G11	-3540	227
683	G13	-3556	110
684	G15	-3572	227
685	G17	-3588	110
686	G19	-3604	227
687	G21	-3620	110
688	G23	-3636	227
689	G25	-3652	110
690	G27	-3668	227
691	G29	-3684	110
692	G31	-3700	227
693	G33	-3716	110
694	G35	-3732	227
695	G37	-3748	110
696	G39	-3764	227
697	G41	-3780	110
698	G43	-3796	227
699	G45	-3812	110
700	G47	-3828	227

No.	PAD Name	X	Y
701	G49	-3844	110
702	G51	-3860	227
703	G53	-3876	110
704	G55	-3892	227
705	G57	-3908	110
706	G59	-3924	227
707	G61	-3940	110
708	G63	-3956	227
709	G65	-3972	110
710	G67	-3988	227
711	G69	-4004	110
712	G71	-4020	227
713	G73	-4036	110
714	G75	-4052	227
715	G77	-4068	110
716	G79	-4084	227
717	G81	-4100	110
718	G83	-4116	227
719	G85	-4132	110
720	G87	-4148	227
721	G89	-4164	110
722	G91	-4180	227
723	G93	-4196	110
724	G95	-4212	227
725	G97	-4228	110
726	G99	-4244	227
727	G101	-4260	110
728	G103	-4276	227
729	G105	-4292	110
730	G107	-4308	227
731	G109	-4324	110
732	G111	-4340	227
733	G113	-4356	110
734	G115	-4372	227
735	G117	-4388	110
736	G119	-4404	227
737	G121	-4420	110
738	G123	-4436	227
739	G125	-4452	110
740	G127	-4468	227
741	G129	-4484	110
742	G131	-4500	227
743	G133	-4516	110
744	G135	-4532	227
745	G137	-4548	110
746	G139	-4564	227
747	G141	-4580	110
748	G143	-4596	227
749	G145	-4612	110
750	G147	-4628	227

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5 Block diagram



6 Driver IC Pin Description

6.1 Power Supply Pin

Name	I/O	Description	Connect pin
VDD	I	Power supply for analog, digital system and booster circuit.	VDD
VDDI	I	Power supply for I/O system.	VDDI
AGND	I	System ground for analog system and booster circuit.	GND
DGND	I	System ground for I/O system and digital system.	GND

6.2 Interface logic pin

Name	I/O	Description	Connect pin															
IM2	I	MCU Parallel interface bus and Serial interface select IM2='1', Parallel interface IM2='0', Serial interface	DGND/VDDI															
IM1,IM0	I	- MCU parallel interface type selection -If not used, please fix this pin at VDDI or DGND level. <table border="1"><tr><th>IM1</th><th>IM0</th><th>Parallel interface</th></tr><tr><td>0</td><td>0</td><td>MCU 8-bit parallel</td></tr><tr><td>0</td><td>1</td><td>MCU 16-bit parallel</td></tr><tr><td>1</td><td>0</td><td>MCU 9-bit parallel</td></tr><tr><td>1</td><td>1</td><td>MCU 18-bit parallel</td></tr></table>	IM1	IM0	Parallel interface	0	0	MCU 8-bit parallel	0	1	MCU 16-bit parallel	1	0	MCU 9-bit parallel	1	1	MCU 18-bit parallel	DGND/VDDI
IM1	IM0	Parallel interface																
0	0	MCU 8-bit parallel																
0	1	MCU 16-bit parallel																
1	0	MCU 9-bit parallel																
1	1	MCU 18-bit parallel																
SPI4W	I	- SPI4W='0', 3-line SPI enable. - SPI4W='1', 4-line SPI enable. -If not used, please fix this pin at DGND level.	DGND/VDDI															
RESX	I	-This signal will reset the device and it must be applied to properly initialize the chip. -Signal is active low.	MCU															
CSX	I	-Chip selection pin -Low enable.	MCU															
D/CX (SCL)	I	-Display data/command selection pin in MCU interface. -D/CX='1': display data or parameter. -D/CX='0': command data. -In serial interface, this is used as SCL. -If not used, please fix this pin at VDDI or DGND level.	MCU															
RDX	I	-Read enable in 8080 MCU parallel interface. -If not used, please fix this pin at VDDI or DGND level.	MCU															
WRX (D/CX)	I	-Write enable in MCU parallel interface. -In 4-line SPI, this pin is used as D/CX (data/ command selection). -If not used, please fix this pin at VDDI or DGND level.	MCU															
D[17:0]	I/O	-D[17:0] are used as MCU parallel interface data bus.	MCU															

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		-D0 is the serial input/output signal in serial interface mode. -In serial interface, D[17:1] are not used and should be fixed at VDDI or DGND level.	
TE	O	-Tearing effect output pin to synchronizes MCU to frame rate, activated by S/W command. -If not used, please open this pin.	MCU
OSC	O	-Monitoring pin of internal oscillator clock and is turned ON/OFF by S/W command. -When this pin is inactive (function OFF), this pin is DGND level. -If not used, please open this pin.	-

Note1. When in parallel mode, no use data pin must be connected to "1" or "0".

Note2. When CSX="1", there is no influence to the parallel and serial interface.

6.3 Mode selection pin

Name	I/O	Description				Connect pin																		
EXTC	I	<p>-During normal operation, please open this pin</p> <table border="1"> <tr> <td>EXTC</td><td colspan="3">Enable/disable modification of extend command</td></tr> <tr> <td>0</td><td colspan="3">System function command list can be used.</td></tr> <tr> <td>1</td><td colspan="3">All command list can be used.</td></tr> </table>				EXTC	Enable/disable modification of extend command			0	System function command list can be used.			1	All command list can be used.			Open						
EXTC	Enable/disable modification of extend command																							
0	System function command list can be used.																							
1	All command list can be used.																							
GM2, GM1, GM0	I	<p>-Panel resolution selection pins.</p> <table border="1"> <tr> <td>G M 2</td><td>G M 1</td><td>G M 0</td><td colspan="3">Selection of panel resolution</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td colspan="3">132RGB x 162 (S1~S396 & G1~G162 output)</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td colspan="3" rowspan="2">128RGB x 160 (S7~S390 & G2~G161 output)</td></tr> </table>				G M 2	G M 1	G M 0	Selection of panel resolution			0	0	0	132RGB x 162 (S1~S396 & G1~G162 output)			0	1	1	128RGB x 160 (S7~S390 & G2~G161 output)			VDDI/DGND
G M 2	G M 1	G M 0	Selection of panel resolution																					
0	0	0	132RGB x 162 (S1~S396 & G1~G162 output)																					
0	1	1	128RGB x 160 (S7~S390 & G2~G161 output)																					
SRGB	I	<p>-RGB direction select H/W pin for color filter setting.</p> <table border="1"> <tr> <td>SRGB</td><td colspan="3">RGB arrangement</td></tr> <tr> <td>0</td><td colspan="3">S1, S2, S3 filter order = 'R', 'G', 'B'</td></tr> <tr> <td>1</td><td colspan="3">S1, S2, S3 filter order = 'B', 'G', 'R'</td></tr> </table>				SRGB	RGB arrangement			0	S1, S2, S3 filter order = ' R ', ' G ', ' B '			1	S1, S2, S3 filter order = ' B ', ' G ', ' R '			VDDI/DGND						
SRGB	RGB arrangement																							
0	S1, S2, S3 filter order = ' R ', ' G ', ' B '																							
1	S1, S2, S3 filter order = ' B ', ' G ', ' R '																							
SMX	I	<p>-Module source output direction H/W selection pin.</p> <table border="1"> <tr> <td>SMX</td><td colspan="3">Scanning direction of source output</td></tr> <tr> <td></td><td>GM= '000'</td><td>GM= '011'</td><td></td></tr> <tr> <td>0</td><td>S1 -> S396</td><td>S7 -> S390</td><td></td></tr> <tr> <td>1</td><td>S396 -> S1</td><td>S390 -> S7</td><td></td></tr> </table>				SMX	Scanning direction of source output				GM= '000'	GM= '011'		0	S1 -> S396	S7 -> S390		1	S396 -> S1	S390 -> S7		VDDI/DGND		
SMX	Scanning direction of source output																							
	GM= '000'	GM= '011'																						
0	S1 -> S396	S7 -> S390																						
1	S396 -> S1	S390 -> S7																						
SMY	I	<p>-Module Gate output direction H/W selection pin.</p> <table border="1"> <tr> <td>SMY</td><td colspan="3">Scanning direction of gate output</td></tr> <tr> <td></td><td>GM= '000'</td><td>GM= '011'</td><td></td></tr> <tr> <td>0</td><td>G1 -> G162</td><td>G2 -> G161</td><td></td></tr> <tr> <td>1</td><td>G162 -> G1</td><td>G161 -> G2</td><td></td></tr> </table>				SMY	Scanning direction of gate output				GM= '000'	GM= '011'		0	G1 -> G162	G2 -> G161		1	G162 -> G1	G161 -> G2		VDDI/DGND		
SMY	Scanning direction of gate output																							
	GM= '000'	GM= '011'																						
0	G1 -> G162	G2 -> G161																						
1	G162 -> G1	G161 -> G2																						
LCM	I	<p>-Liquid crystal (LC) type selection pins.</p> <table border="1"> <tr> <td>LCM</td><td colspan="3">Selection of LC type</td></tr> <tr> <td>0</td><td colspan="3">Normally white LC type</td></tr> <tr> <td>1</td><td colspan="3">Normally black LC type</td></tr> </table>				LCM	Selection of LC type			0	Normally white LC type			1	Normally black LC type			VDDI/DGND						
LCM	Selection of LC type																							
0	Normally white LC type																							
1	Normally black LC type																							
GS	I	<p>-Gamma curve selection pin.</p> <table border="1"> <tr> <td>GS</td><td colspan="3">Selection of gamma curve</td></tr> <tr> <td>0</td><td colspan="3">GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8</td></tr> <tr> <td>1</td><td colspan="3">GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0</td></tr> </table>				GS	Selection of gamma curve			0	GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8			1	GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0			VDDI/DGND						
GS	Selection of gamma curve																							
0	GC0=1.0, GC1=2.5, GC2=2.2, GC3=1.8																							
1	GC0=2.2, GC1=1.8, GC2=2.5, GC3=1.0																							

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TESEL	I	<p>Input pin to select horizontal line number in TE signal. This pin is only for GM[2:0]='000' mode TESEL='0' , TE output 162 lines TESEL='1' , TE output 160 lines</p>	VDDI/DGND
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6.4 Driver output pins

Name	I/O	Description	Connect pin
S1 to S396	O	- Source driver output pins.	-
G1 to G162	O	- Gate driver output pins.	-
VCI1	I/O	- Hi-Z	-
AVDD	I	- Power input pin for analog circuits. - In normal usage, connect it to AVDDO. - AVDD = 5.3V.	AVDDO
AVDDO	O	- Output of step-up circuit 1 - Connect a capacitor for stabilization.	Capacitor
VCL	O	- A power supply pin for generating VCOML. - Connect a capacitor for stabilization.	Capacitor
VGH	I	- Power input pin for gate driver circuit. - In normal usage, connect it to VGHO.	VGHO
VGHO	O	- Positive output pin of the step-up circuit 2. - Connect a capacitor for stabilization.	Capacitor
VGL	I	- Power input pin for gate driver circuit. - Negative output of the step-up circuit 2 is connected inside the driver. - Connect a capacitor for stabilization.	Capacitor
VREF	O	- A reference voltage for power system. - This test pin for Driver vendor test used.	-
GVDD	O	- A power output of grayscale voltage generator. - When internal GVDD generator is not used, connect an external power supply (AVDD-0.5V) to this pin.	-
VCOMH	O	- Positive voltage output of VCOM. - Connect a capacitor for stabilization.	Capacitor
VCOML	O	- Negative voltage output of VCOM. - Connect a capacitor for stabilization.	Capacitor
VCOM	O	- A power supply for the TFT-LCD common electrode.	Common electrode
C11P, C11N	O	- Capacitor connecting pins for step-up circuit 1 (for AVDDO)	Step-up Capacitor
C22P, C22N C23P, C23N C41P, C41N	O	- Capacitor connecting pins for step-up circuit 2 and 4 (for VGHO, VGL, VCL)	Step-up Capacitor

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VDDIO	O	-VDDI voltage output level for monitoring.	-
DGND	O	-DGND voltage output level for monitoring.	-
VCC	I	-Power input pin for internal digital reference voltage. -In normal usage, connect it to VCCO.	VCCO
VCCO	O	-Monitoring pin of internal digital reference voltage. -Connect a capacitor for stabilization.	Capacitor

6.5 Test pins

Name	I/O	Description	Connect pin
TPI[2] TPI[1]	I	-These test pins for Driver vendor test used. -Please connect these pins to DGND.	DGND
TPO[8] TPO[7] TPO[6] TPO[5] TPO[4] TPO[3] TPO[2] TPO[1]	O	-These test pins for Driver vendor test used. -Please open these pins.	Open
Dummy	-	-These pins are dummy (have no function inside). -Can allow signal traces pass through these pads on TFT glass. -Please open these pins.	Open

7 Driver electrical characteristics

7.1 Absolute operation range

Item	Symbol	Rating	Unit
Supply voltage	VDD	-0.3 ~ +4.6	V
Supply voltage (Logic)	VDDI	-0.3 ~ +4.6	V
Supply voltage (Digital)	VCC	-0.3 ~ +1.95	V
Driver supply voltage	VGH-VGL	-0.3 ~ +30.0	V
Logic input voltage range	VIN	0.3 ~ VDDI +0.3	V
Logic output voltage range	VO	0.3 ~ VDDI +0.3	V
Operating temperature range	TOPR	-30 ~ +85	°C
Storage temperature range	TSTG	-40 ~ +125	°C

Note: If one of the above items is exceeded its maximum limitation momentarily, the quality of the product may be degraded. Absolute maximum limitation, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the recommend range.

7.2 DC characteristic

Parameter	Symbol	Condition	Specification			Unit	Related Pins
			Min	Typ	Max		
Power & operation voltage							
System voltage	VDD	Operating voltage	2.6	2.75	3.3	V	
Interface operation voltage	VDDI	I/O supply voltage	1.65	1.9	3.3	V	
Gate driver high voltage	VGH		10		15	V	
Gate driver low voltage	VGL		-12.4		-7.5	V	
Gate driver supply voltage		VGH-VGL	17.5		27.5	V	
Input / Output							
Logic-high input voltage	VIH		0.7VDDI		VDDI	V	Note 1
Logic-low input voltage	VIL		VSS		0.3VDDI	V	Note 1
Logic-high output voltage	VOH	IOH = -1.0mA	0.8VDDI		VDDI	V	Note 1
Logic-low output voltage	VOL	IOL = +1.0mA	VSS		0.2VDDI	V	Note 1
Logic-high input current	IIH	VIN = VDDI			1	uA	Note 1

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Logic-low input current	IIL	VIN = VSS	-1			uA	Note 1
Input leakage current	IIL	IOH = -1.0mA	-0.1		+0.1	uA	Note 1
VCOM voltage							
VCOM high voltage	VCOMH	Ccom=12nF	2.5		5.0	V	
VCOM low voltage	VCOML	Ccom=12nF	-2.4		0.0	V	
VCOM amplitude	VCOMAC	VCOMH-VCOML	4.0		6.0	V	
Source driver							
Source output range	Vsout		0.1		AVDD-0.1	V	
Gamma reference voltage	GVDD		3.0		5.0	V	
Source output settling time	Tr	Below with 99% precision			20	us	Note 2
Output offset voltage	Voffset				35	mV	Note 3

Notes:

1. $VDDI=1.65 \text{ to } 3.3V$, $VDD=2.6 \text{ to } 3.3V$, $AGND=DGND=0V$, $TA= -30 \text{ to } 85^\circ C$
2. Source channel loading= $2K\Omega + 12pF/\text{channel}$, Gate channel loading= $5K\Omega + 40pF/\text{channel}$.
3. The Max. value is between measured point of source output and gamma setting value.

7.3 Power consumption

VDD=2.8V, VDDI=1.8V, Ta=25°C , Frame rate = 60Hz, the registers setting are IC default setting.

Operation mode	Inversion mode	Image	Current consumption			
			Typical		Maximum	
			IDDI (mA)	IDD (mA)	IDDI (mA)	IDD (mA)
Normal mode	One Line	Note 1	0.01	0.5	0.02	0.7
		Note 2	0.01	0.5	0.02	0.7
Partial + Idle mode (40 lines)	One Line	Note 1	0.01	0.3	0.02	0.5
		Note 2	0.01	0.3	0.02	0.5
Sleep-in mode	N/A	N/A	0.005	0.015	0.01	0.03

Notes:

1. All pixels black.
2. All pixels white.
3. The Current Consumption is DC characteristics of ST7735

8 Timing chart

8.1 Parallel interface characteristics: 18, 16, 9 or 8-bit bus (8080 series MCU interface)

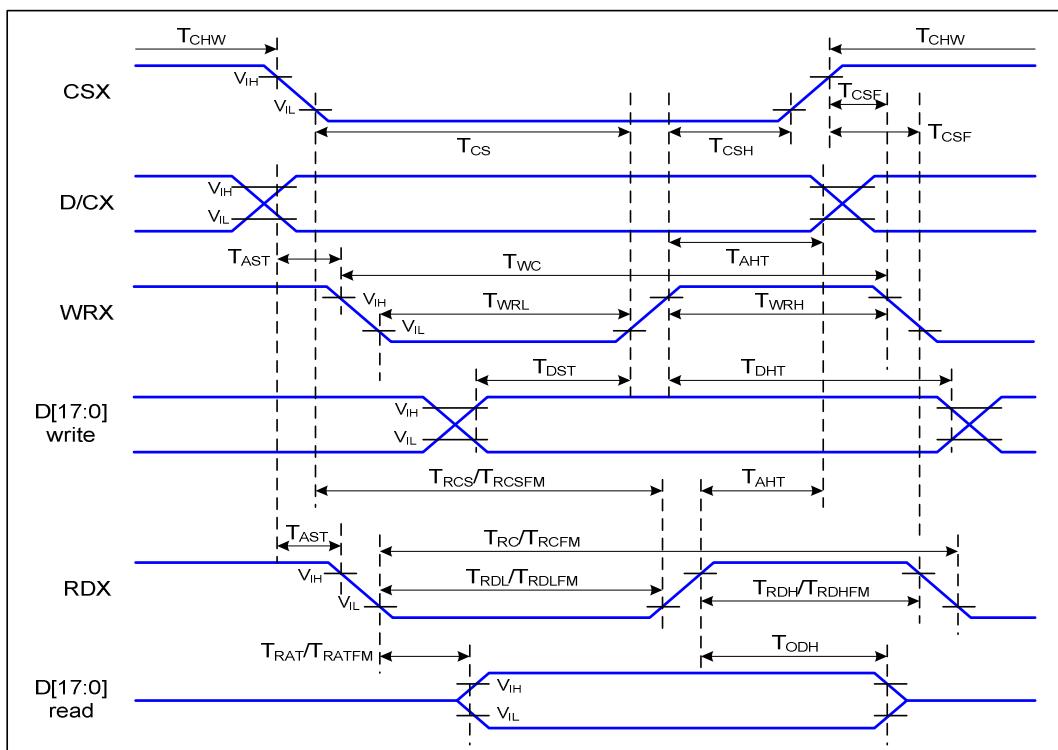


Fig. 8.1.1 Parallel interface timing characteristics (8080 series MCU interface)

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	TAST	Address setup time	10		ns	-
	TAHT	Address hold time (Write/Read)	10		ns	
CSX	TCHW	Chip select "H" pulse width	0		ns	-
	TCS	Chip select setup time (Write)	15		ns	
	TRCS	Chip select setup time (Read ID)	45		ns	
	TRCSFM	Chip select setup time (Read FM)	350		ns	
	TCSF	Chip select wait time (Write/Read)	10		ns	
	TCSH	Chip select hold time	10		ns	
WRX	TWC	Write cycle	100		ns	-
	TWRH	Control pulse "H" duration	30		ns	
	TWRL	Control pulse "L" duration	30		ns	
RDX (ID)	TRC	Read cycle (ID)	160		ns	When read ID data
	TRDH	Control pulse "H" duration (ID)	90		ns	
	TRDL	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	TRCFM	Read cycle (FM)	450		ns	When read from frame memory
	TRDHFM	Control pulse "H" duration (FM)	150		ns	
	TRDLFM	Control pulse "L" duration (FM)	150		ns	

D[17:0]	TDST	Data setup time	10		ns	For CL=30pF
	TDHT	Data hold time	10		ns	
	TRAT	Read access time (ID)		40	ns	
	TRATFM	Read access time (FM)		40	ns	
	TODH	Output disable time		80	ns	

Table 8.1.1 Parallel Interface Characteristics

Note: VDDI=1.65 to 3.3V, VDD=2.6 to 3.3V, AGND=DGND=0V, Ta=25 °C

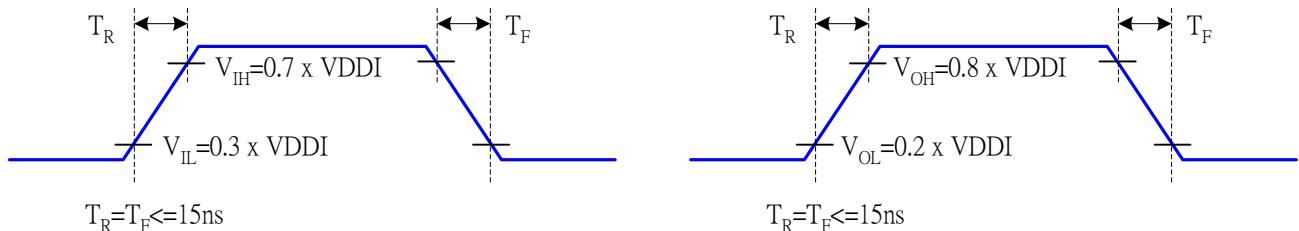


Fig. 8.1.2 Rising and falling timing for input and output signal

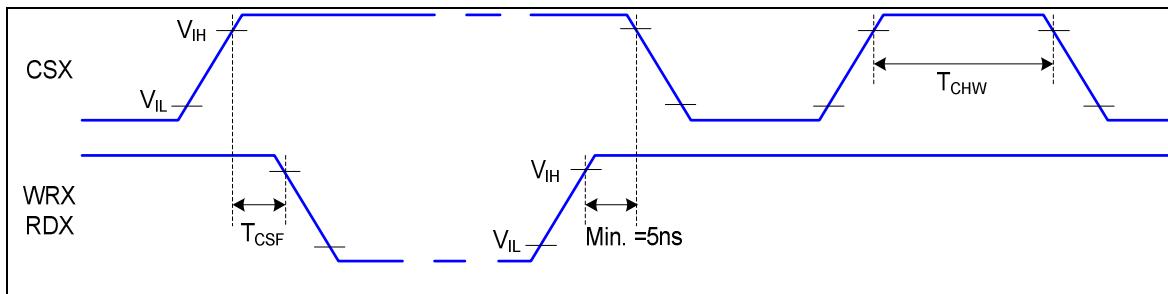


Fig. 8.1.3 Chip selection (CSX) timing

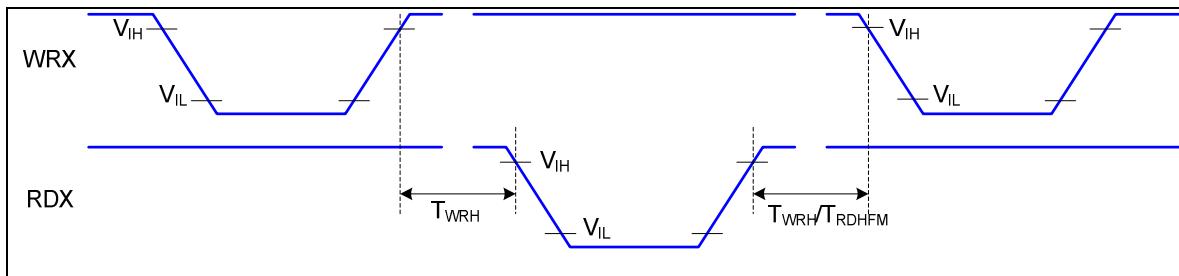


Fig. 8.1.4 Write-to-read and read-to-write timing

Note: The rising time and falling time (T_R , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

8.2 Serial interface characteristics (3-line serial)

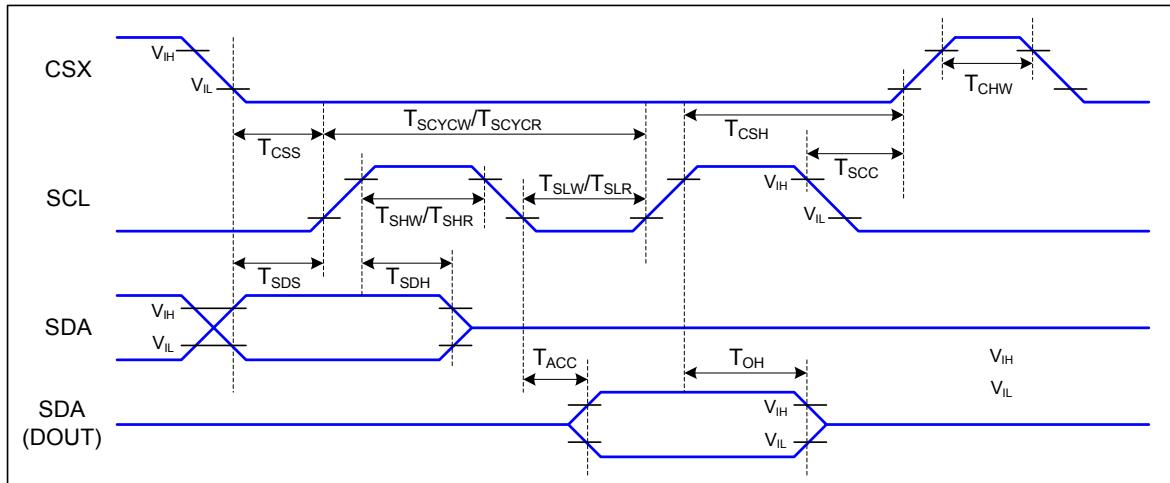


Fig. 8.2.1 3-line serial interface timing

Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	T _{CSS}	Chip select setup time (write)	15		ns	
	T _{CSH}	Chip select hold time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{SCC}	Chip select hold time (read)	65		ns	
	T _{CHW}	Chip select "H" pulse width	40		ns	
SCL	T _{SCYCW}	Serial clock cycle (Write)	66		ns	
	T _{SHW}	SCL "H" pulse width (Write)	30		ns	
	T _{SLW}	SCL "L" pulse width (Write)	30		ns	
	T _{SCYCR}	Serial clock cycle (Read)	150		ns	
	T _{SHR}	SCL "H" pulse width (Read)	60		ns	
	T _{SLR}	SCL "L" pulse width (Read)	60		ns	
SDA (DIN) (DOUT)	T _{SDS}	Data setup time	10		ns	For maximum CL=30pF For minimum CL=8pF
	T _{SDH}	Data hold time	10		ns	
	T _{AACC}	Access time	10	50	ns	
	T _{OH}	Output disable time		50	ns	

Table 8.2.1 3-line Serial Interface Characteristics

Note 1: $VDDI=1.65$ to $3.3V$, $VDD=2.6$ to $3.3V$, $AGND=DGND=0V$, $T_a=25^{\circ}C$

Note 2: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of $VDDI$ for Input signals.

8.3 Serial interface characteristics (4-line serial)

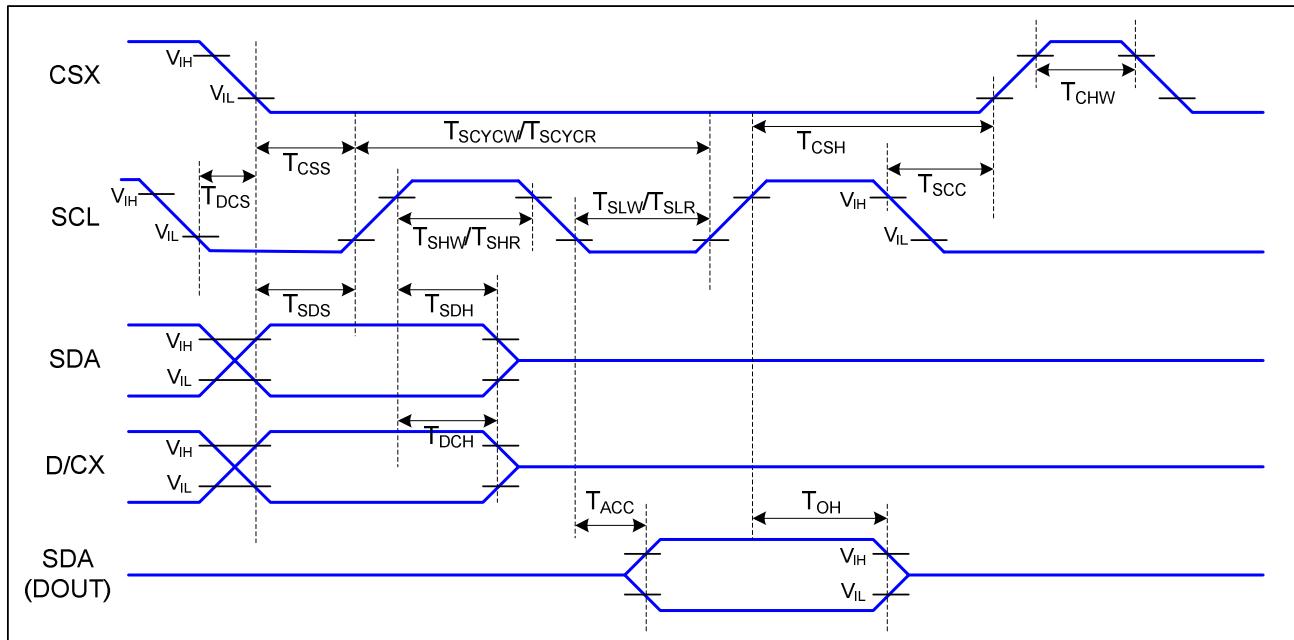


Fig. 8.3.1 4-line serial interface timing

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T _{CSS}	Chip select setup time (write)	15		ns	-write command & data ram
	T _{TCSH}	Chip select hold time (write)	15		ns	
	T _{CSS}	Chip select setup time (read)	60		ns	
	T _{TSCC}	Chip select hold time (read)	65		ns	
	T _{TCHW}	Chip select "H" pulse width	40		ns	
SCL	T _{TSCYCWR}	Serial clock cycle (Write)	66		ns	-write command & data ram
	T _{TSHW}	SCL "H" pulse width (Write)	30		ns	
	T _{TSLW}	SCL "L" pulse width (Write)	30		ns	
	T _{TSCYCR}	Serial clock cycle (Read)	150		ns	-read command & data ram
	T _{TSHR}	SCL "H" pulse width (Read)	60		ns	
	T _{TSRL}	SCL "L" pulse width (Read)	60		ns	
D/CX	T _{TDCH}	D/CX hold time	10		ns	For maximum CL=30pF
	T _{TDCH}	D/CX setup time	0		ns	
SDA (DIN) (DOUT)	T _{SDS}	Data setup time	10		ns	For minimum CL=8pF
	T _{SDH}	Data hold time	10		ns	
	T _{TACC}	Access time	10	50	ns	For maximum CL=30pF
	T _{TOH}	Output disable time		50	ns	

Table 8.3.1 4-line Serial Interface Characteristics

Note 1: V_{DDI}=1.65 to 3.3V, V_{DD}=2.6 to 3.3V, AGND=DGND=0V, Ta=25 °C

Note 2: The rising time and falling time (T_r , T_f) of input signal are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of V_{DDI} for Input signals.

9 Function description

9.1 Interface type selection

The selection of given interfaces are done by setting IM2, IM1, and IM0 pins as shown in following table.

IM2	IM1	IM0	Interface	Read back selection
0	-	-	3-line serial interface	Via the read instruction
1	0	0	8080 MCU 8-bit parallel	RDX strobe (8-bit read data and 8-bit read parameter)
1	0	1	8080 MCU 16-bit parallel	RDX strobe (16-bit read data and 8-bit read parameter)
1	1	0	8080 MCU 9-bit parallel	RDX strobe (9-bit read data and 8-bit read parameter)
1	1	1	8080 MCU 18-bit parallel	RDX strobe (18-bit read data and 8-bit read parameter)

Table 9.1.1 Selection of MCU interface

IM2	IM1	IM0	Interface	RDX	WRX	D/CX	Read back selection
0	-	-	3-line serial	Note1	Note1	SCL	D[17:1]: unused, D0: SDA
1	0	0	8080 8-bit parallel	RDX	WRX	D/CX	D[17:8]: unused, D7-D0: 8-bit data
1	0	1	8080 16-bit parallel	RDX	WRX	D/CX	D[17:16]: unused, D15-D0: 16-bit data
1	1	0	8080 9-bit parallel	RDX	WRX	D/CX	D[17:9]: unused, D8-D0: 9-bit data
1	1	1	8080 18-bit parallel	RDX	WRX	D/CX	D17-D0: 18-bit data

Table 9.1.2 Pin connection according to various MCU interface

Note1: Unused pins can be open, or connected to DGND or VDDI.

9.2 8080-series MCU parallel interface

The MCU can use one of following interfaces: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-line with 16-data parallel interface or 21-lines with 18-data parallel interface. The chip-select CSX (active low) enables/disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write enable, RDX is the parallel data read enable and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command. The interface functions of 8080-series parallel interface are given in following table.

IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Read back selection
1	0	0	8-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 8-bit display data or 8-bit parameter (D7 to D0)
				1	↑	1	Read 8-bit display data (D7 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)
1	0	1	16-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 16-bit display data or 8-bit parameter (D15 to D0)
				1	↑	1	Read 16-bit display data (D15 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)
1	1	0	9-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 9-bit display data or 8-bit parameter (D8 to D0)
				1	↑	1	Read 9-bit display data (D8 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)
1	1	1	18-bit parallel	0	1	↑	Write 8-bit command (D7 to D0)
				1	1	↑	Write 18-bit display data or 8-bit parameter (D17 to D0)
				1	↑	1	Read 18-bit display data (D17 to D0)
				1	↑	1	Read 8-bit parameter or status (D7 to D0)

Table 9.2.1 The function of 8080-series parallel interface

Note: applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

9.2.1 Write cycle sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low ($=0'$) and vice versa it is data ($=1'$).

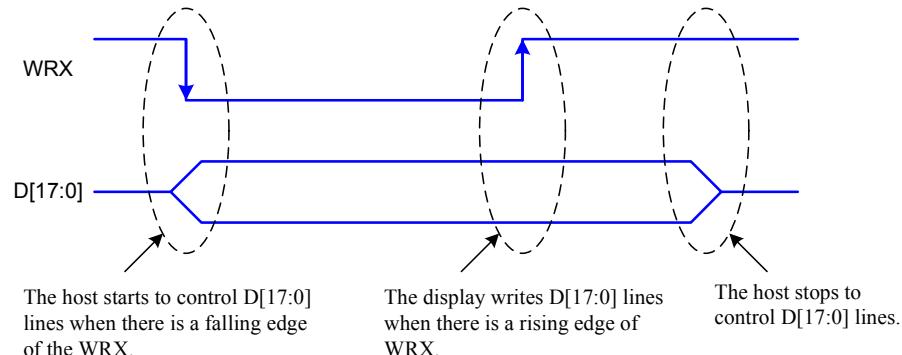


Fig. 9.2.1 8080-series WRX protocol

Note: WRX is an unsynchronized signal (It can be stopped).

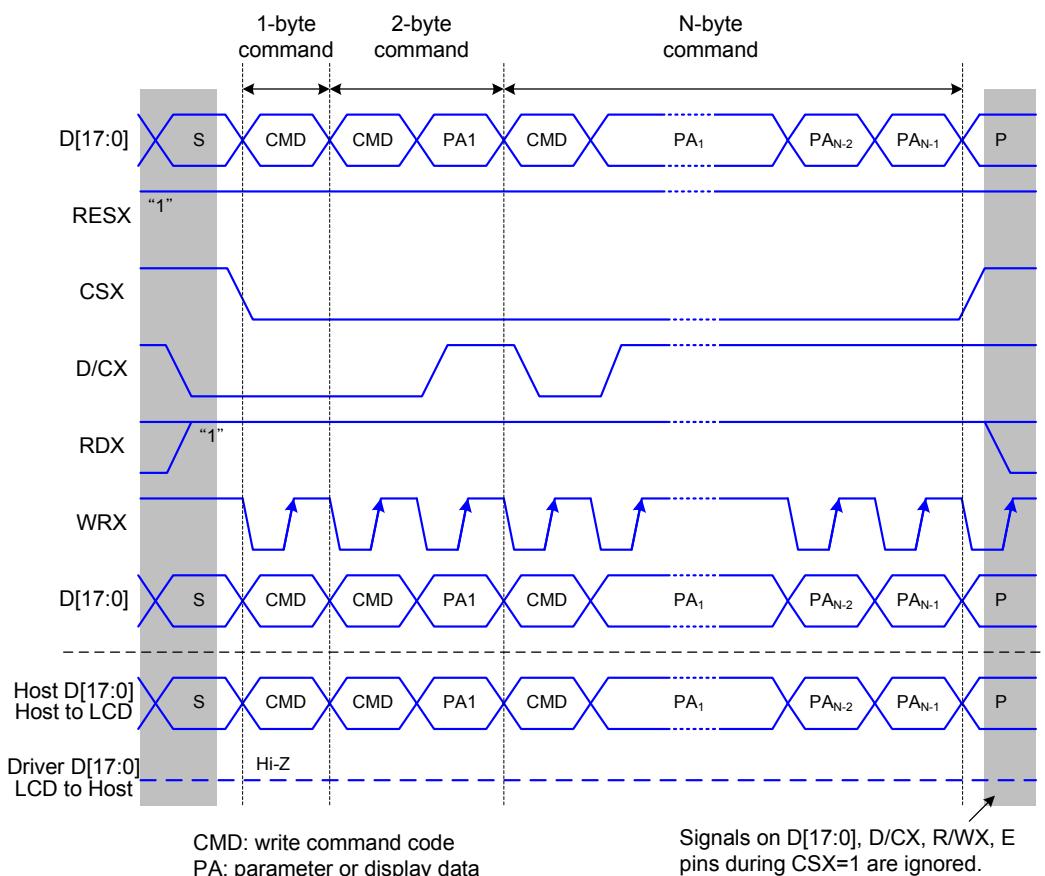


Fig. 9.2.2 8080-series parallel bus protocol, write to register or display RAM

9.2.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

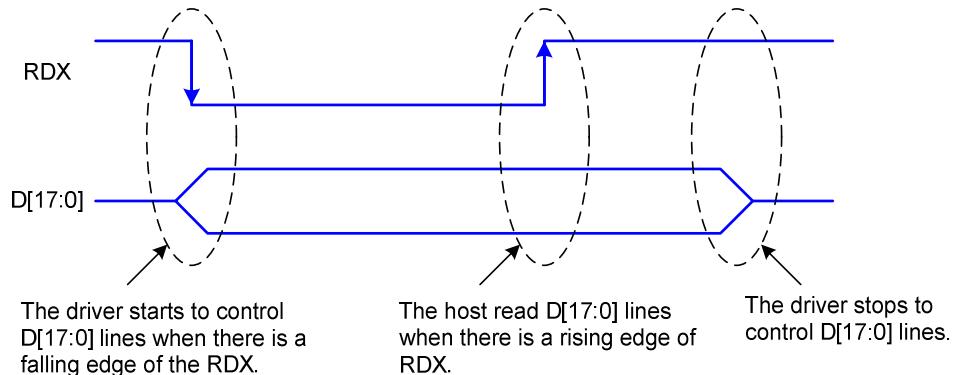


Fig. 9.2.3 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

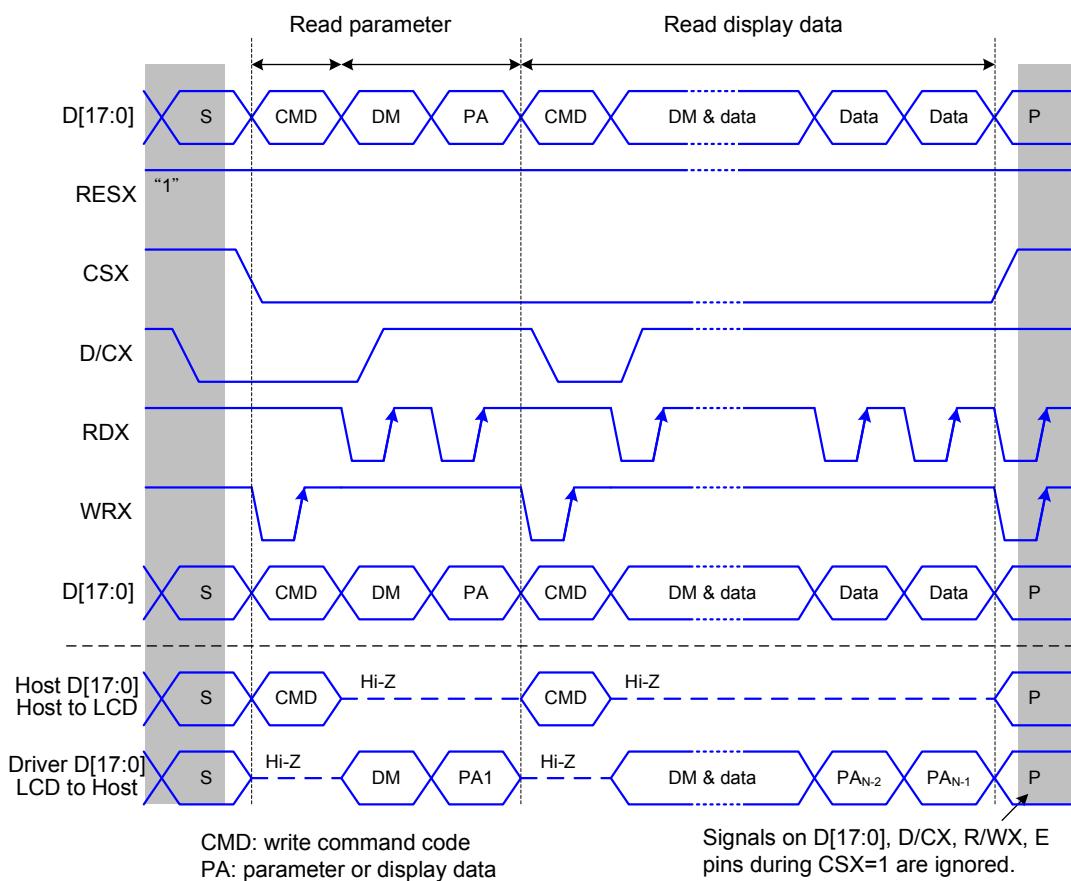


Fig. 9.2.4 8080-series parallel bus protocol, read data from register or display RAM

9.3 Serial interface

The selection of this interface is done by IM2. See the Table 9.3.1.

IM2	SPI4W	Interface	Read back selection
0	0	3-line serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)
0	1	4-line serial interface	Via the read instruction (8-bit, 24-bit and 32-bit read parameter)

Table 9.3.1 Selection of serial interface

The serial interface is either 3-line/9-bit or 4-line/8-bit bi-directional interface for communication between the micro controller and the LCD driver. The 3-line serial interface use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output), and the 4-line serial interface use: CSX (chip enable), D/CX (data/ command flag), SCL (serial clock) and SDA (serial data input/output). Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

9.3.1 Command Write Mode

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-line serial data packet contains a control bit D/CX and a transmission byte. In 4-line serial interface, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (memory write command), or command register as parameter.

Any instruction can be sent in any order to the driver. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

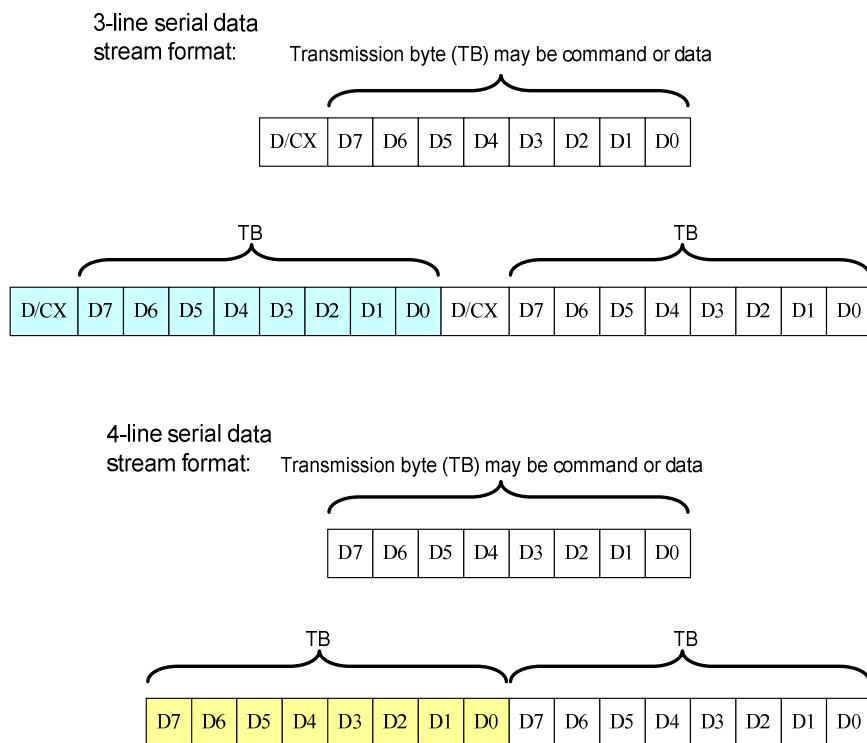


Fig. 9.3.1 Serial interface data stream format

When CSX is “high”, SCL clock is ignored. During the high period of CSX the serial interface is initialized. At the falling edge of CSX, SCL can be high or low (see Fig 9.3.2). SDA is sampled at the rising edge of SCL. D/CX indicates whether the byte is command (D/CX='0') or parameter/RAM data (D/CX='1'). D/CX is sampled when first rising edge of SCL (3-line serial interface) or 8th rising edge of SCL (4-line serial interface). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-line serial interface) or D7 (4-line serial interface) of the next byte at the next rising edge of SCL.

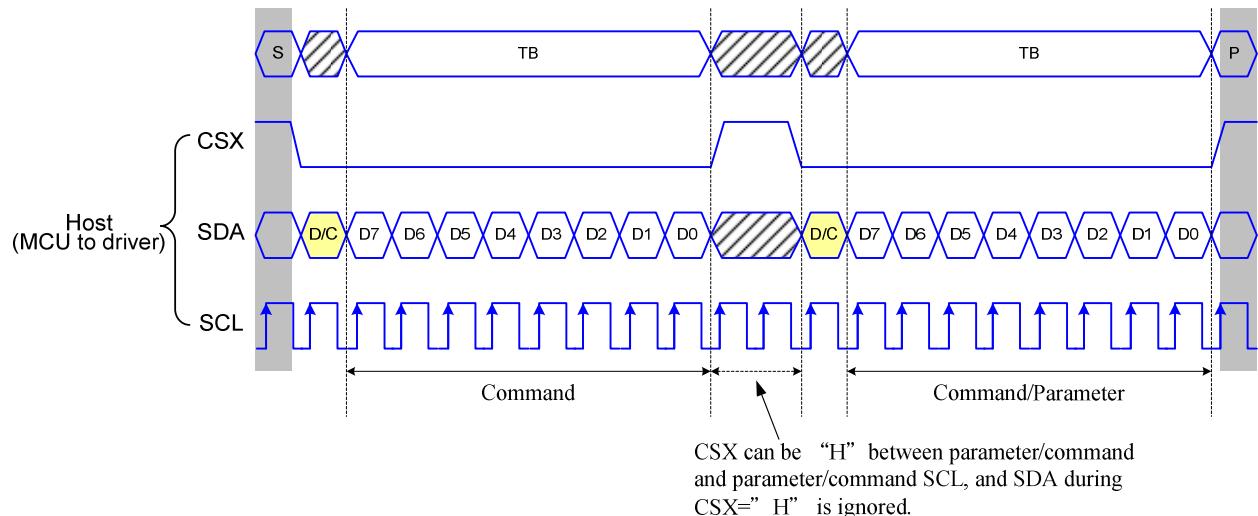


Fig. 9.3.2 3-line serial interface write protocol (write to register with control bit in transmission)

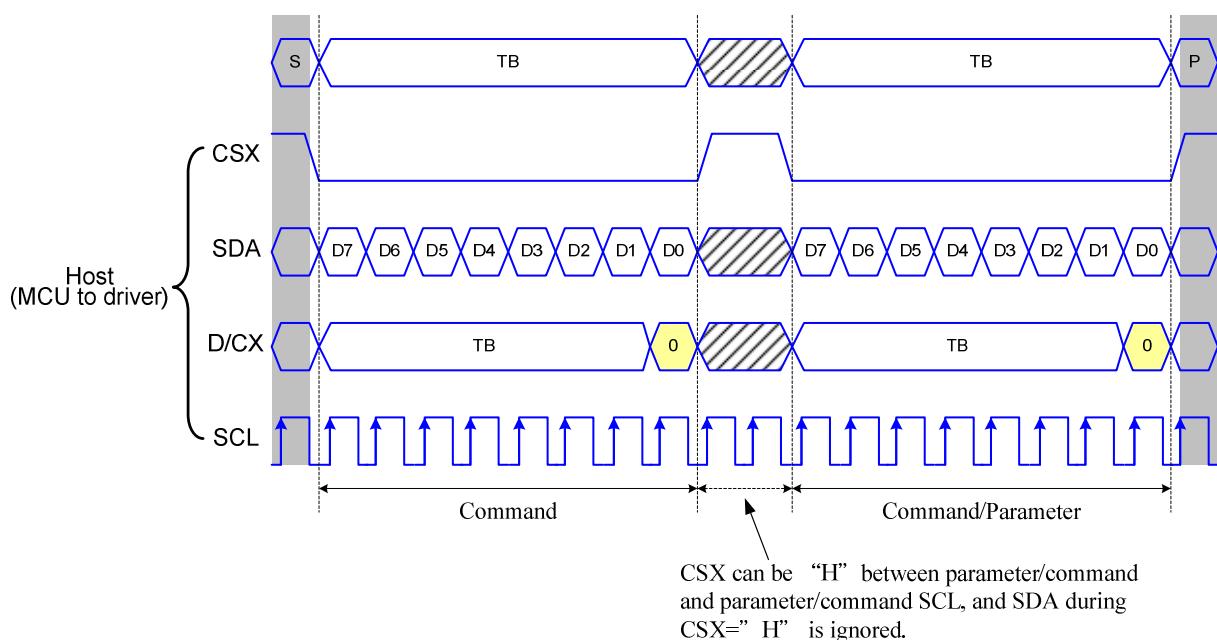


Fig. 9.3.3 4-line serial interface write protocol (write to register with control bit in transmission)

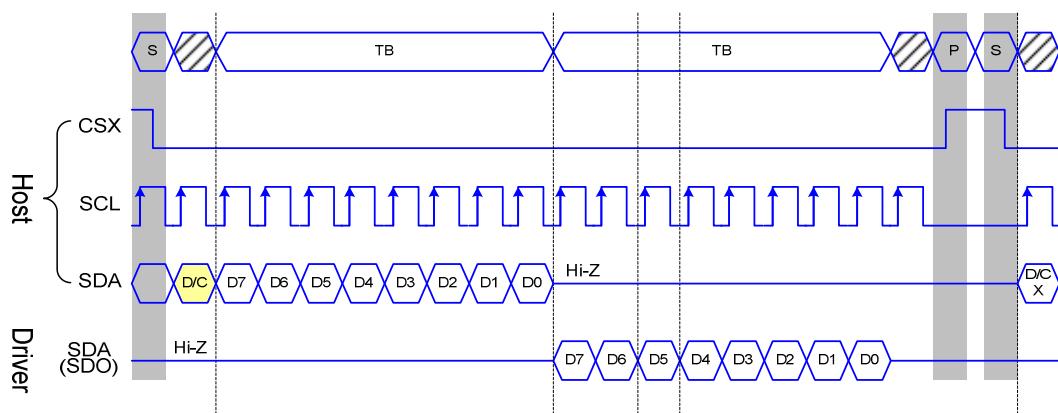
9.3.2 Read Functions

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

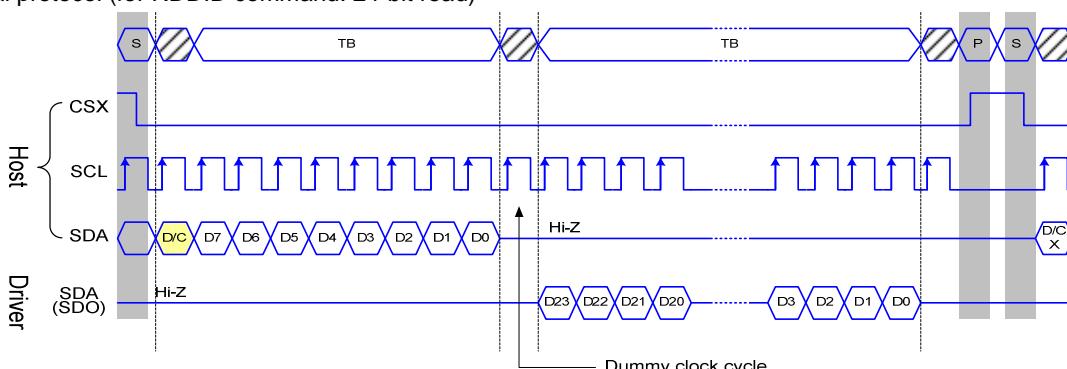
After the read status command has been sent, the SDA line must be set to tri-state no later than at the falling edge of SCL of the last bit.

9.3.3 3-line serial protocol

3-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



3-line serial protocol (for RDDID command: 24-bit read)



3-line Serial Protocol (for RDDST command: 32-bit read)

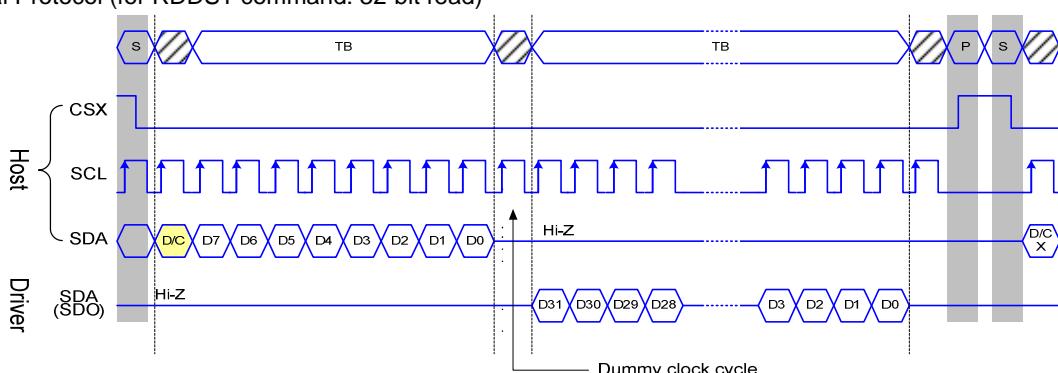
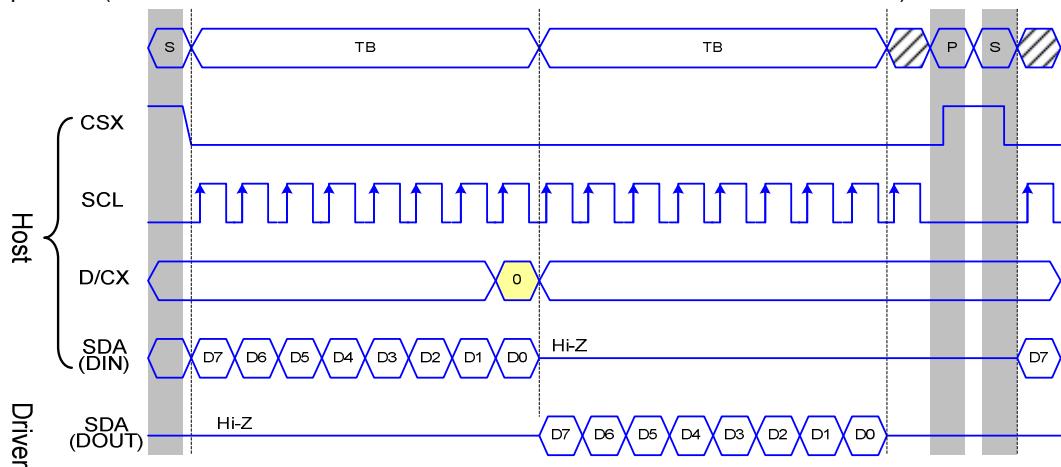


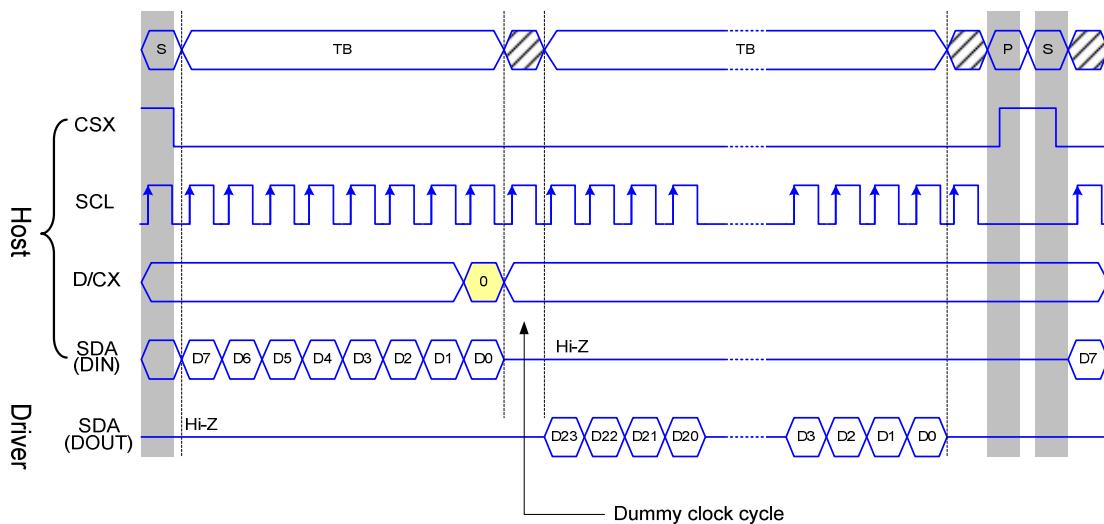
Fig. 9.3.4 3-line serial interface read protocol

9.3.4 4-line serial protocol

4-line serial protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read):



4-line serial protocol (for RDDID command: 24-bit read)



4-line Serial Protocol (for RDDST command: 32-bit read)

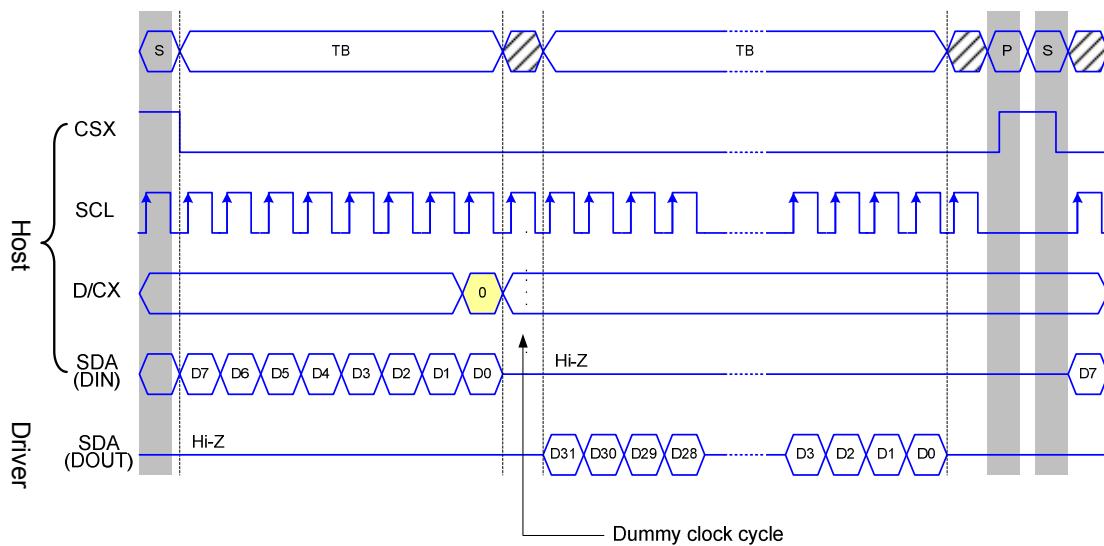


Fig. 9.3.5 4-line serial interface read protocol

9.4 Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been HIGH state. See the following example

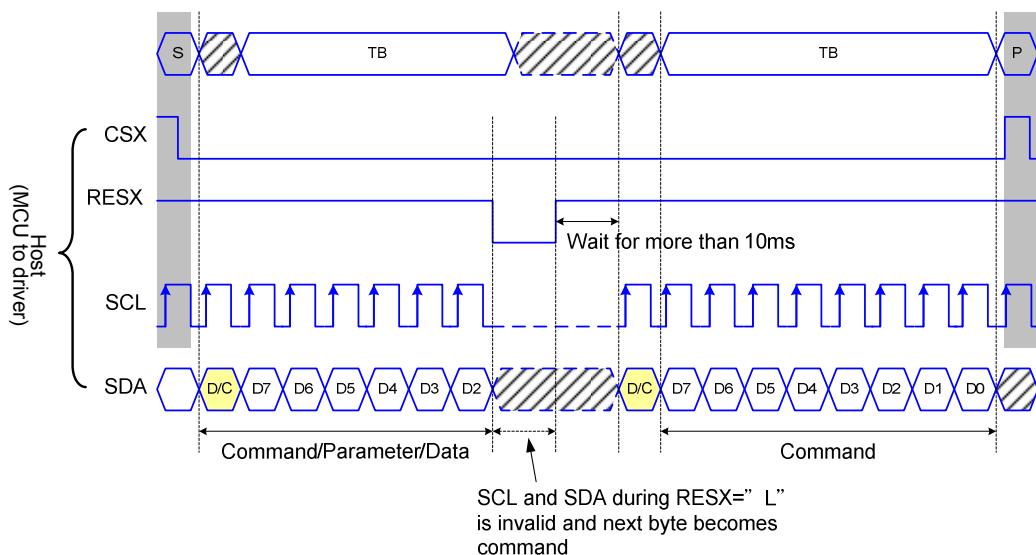


Fig. 9.4.1 Serial bus protocol, write mode – interrupted by RESX

If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example

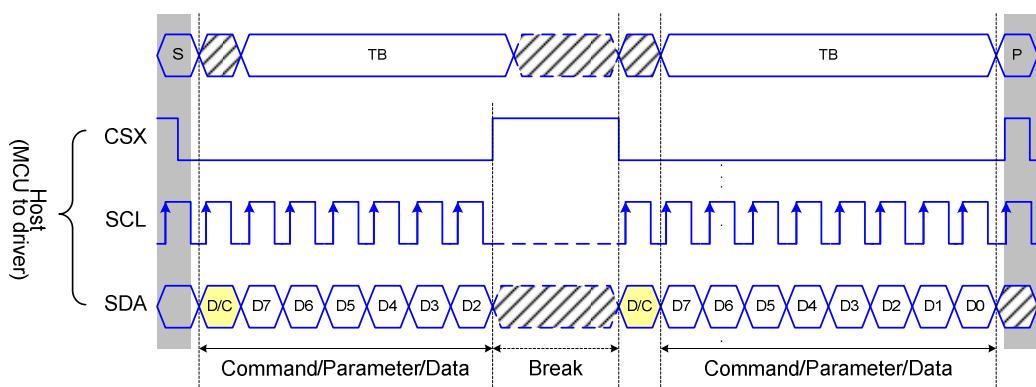


Fig. 9.4.2 Serial bus protocol, write mode – interrupted by CSX

If 1, 2 or more parameter commands are being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

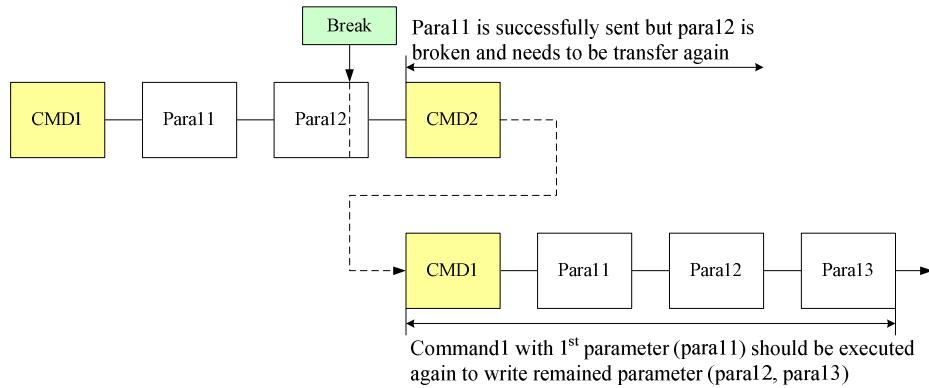


Fig. 9.4.3 Write interrupts recovery (serial interface)

If a 2 or more parameter commands are being sent and a break occurs by the other command before the last one is sent, then the parameters that were successfully sent are stored and the other parameter of that command remains previous value.

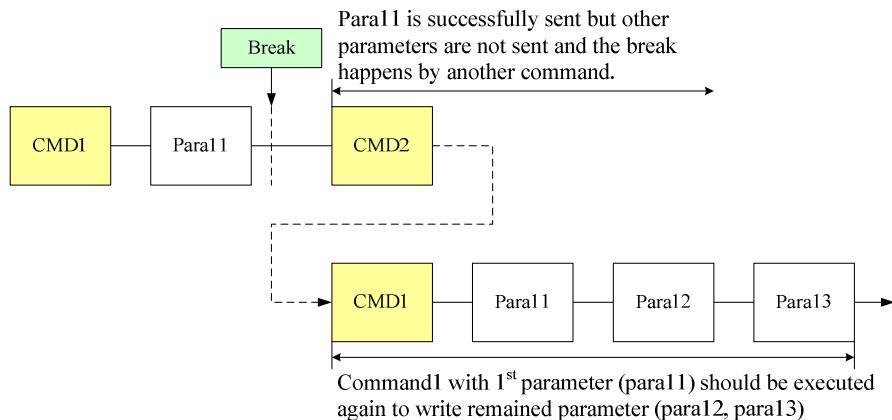


Fig. 9.4.4 Write interrupts recovery (both serial and parallel Interface)

9.5 Data transfer pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select line is released after a whole byte of a frame memory data or multiple parameter data has been completed, then driver will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select Line is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select line is next enabled as shown below.

This applies to the following 4 conditions:

- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter

9.5.1 Serial interface pause

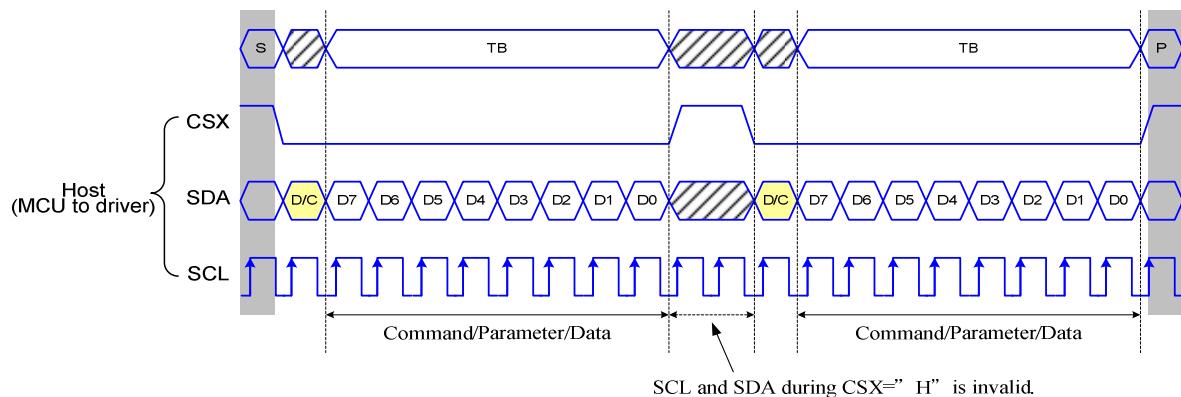


Fig. 9.5.1 Serial interface pause protocol (pause by CSX)

9.5.2 Parallel interface pause

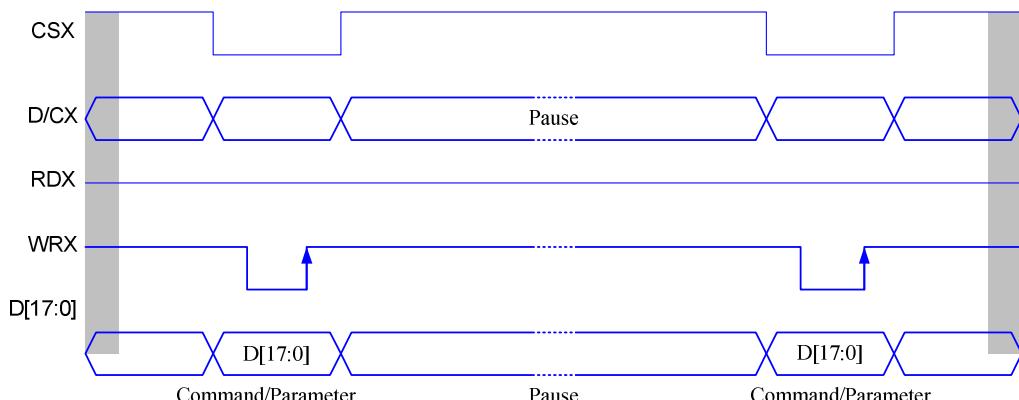


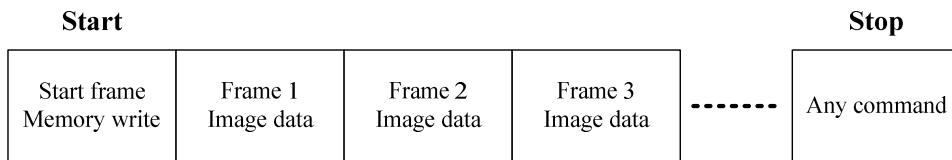
Fig. 9.5.2 Parallel bus pause protocol (paused by CSX)

9.6 Data Transfer Modes

The module has three kinds color modes for transferring data to the display RAM. These are 12-bit color per pixel, 16-bit color per pixel and 18-bit color per pixel. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

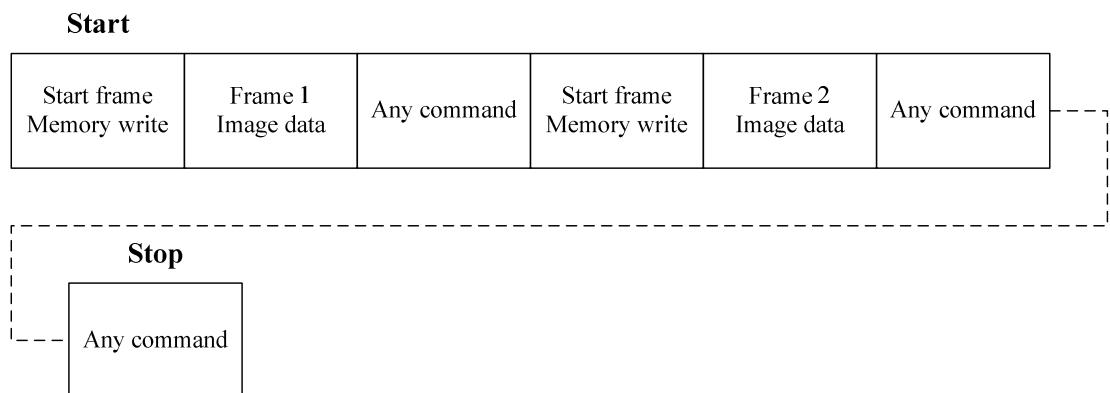
9.6.1 Method 1

The image data is sent to the frame memory in successive frame writes, each time the frame memory is filled, the frame memory pointer is reset to the start point and the next frame is written.



9.6.2 Method 2

The image data is sent and at the end of each frame memory download, a command is sent to stop frame memory write. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These apply to all data transfer Color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

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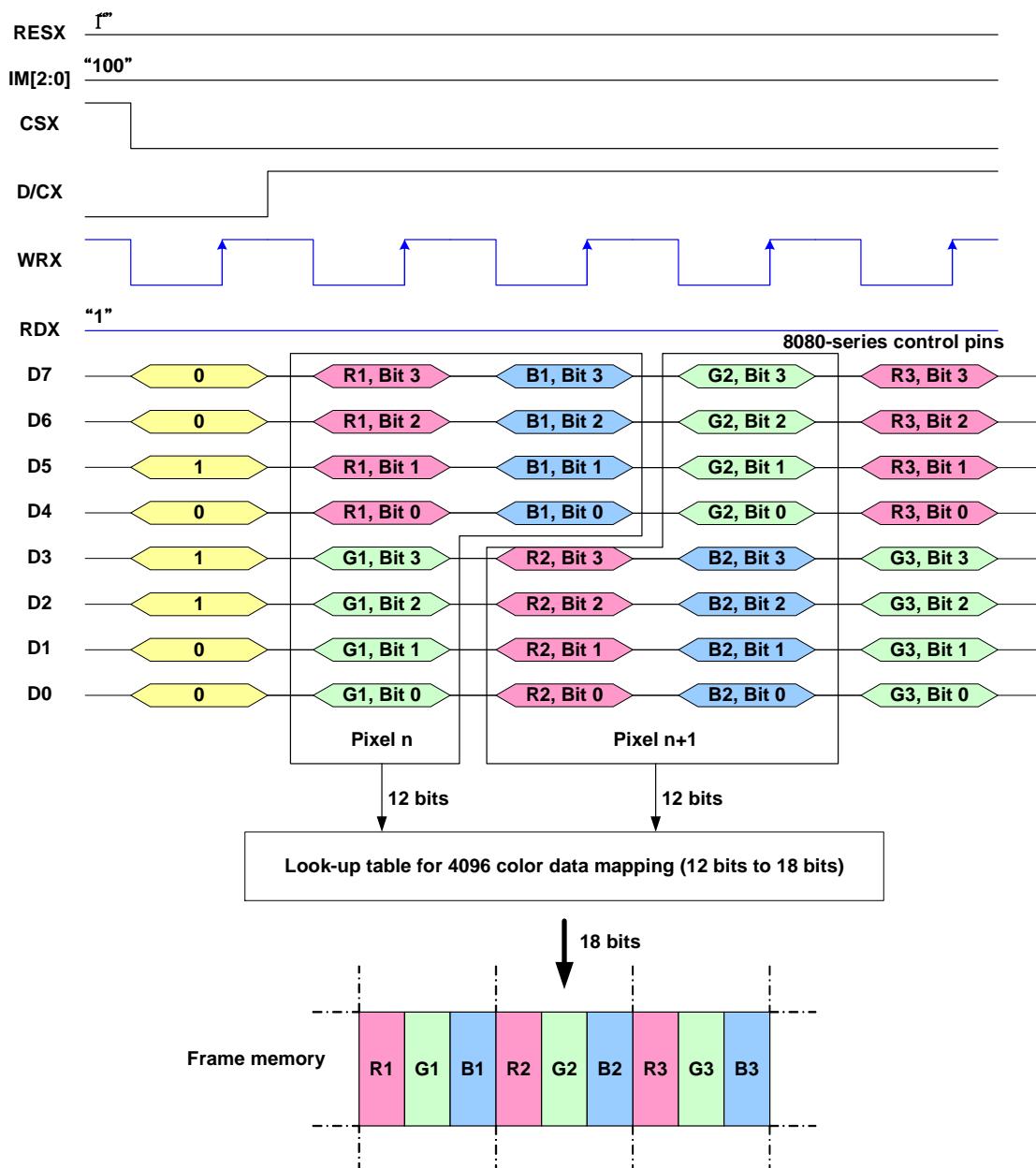
9.7 Data Color Coding

9.7.1 8-bit Parallel Interface (IM2, IM1, IM0= "100")

Different display data formats are available for three Colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input.
- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

9.7.2 8-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= "03h"



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

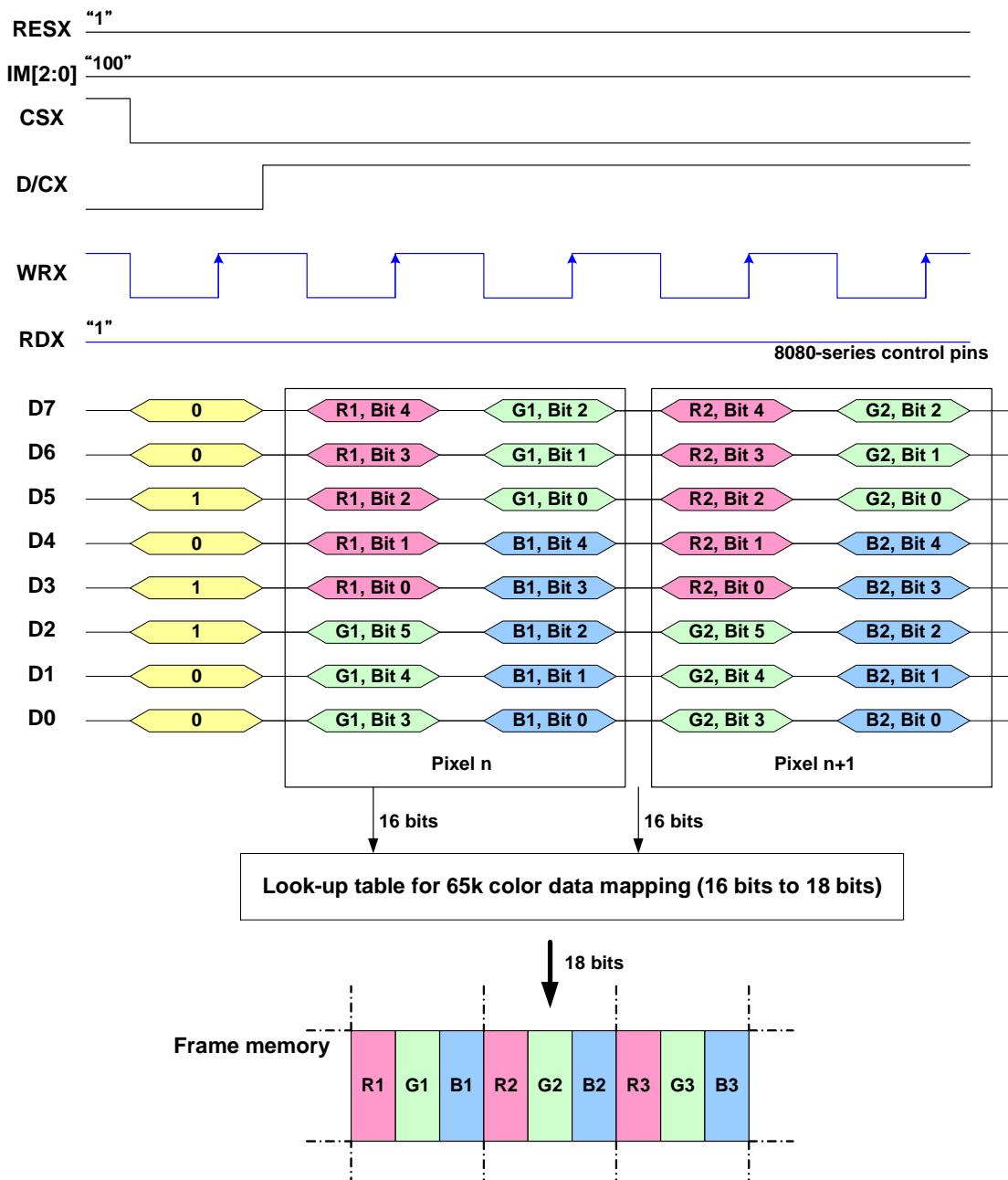
Note 2: 3-time transfer is used to transmit 1 pixel data with the 12-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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9.7.3 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 2-byte



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

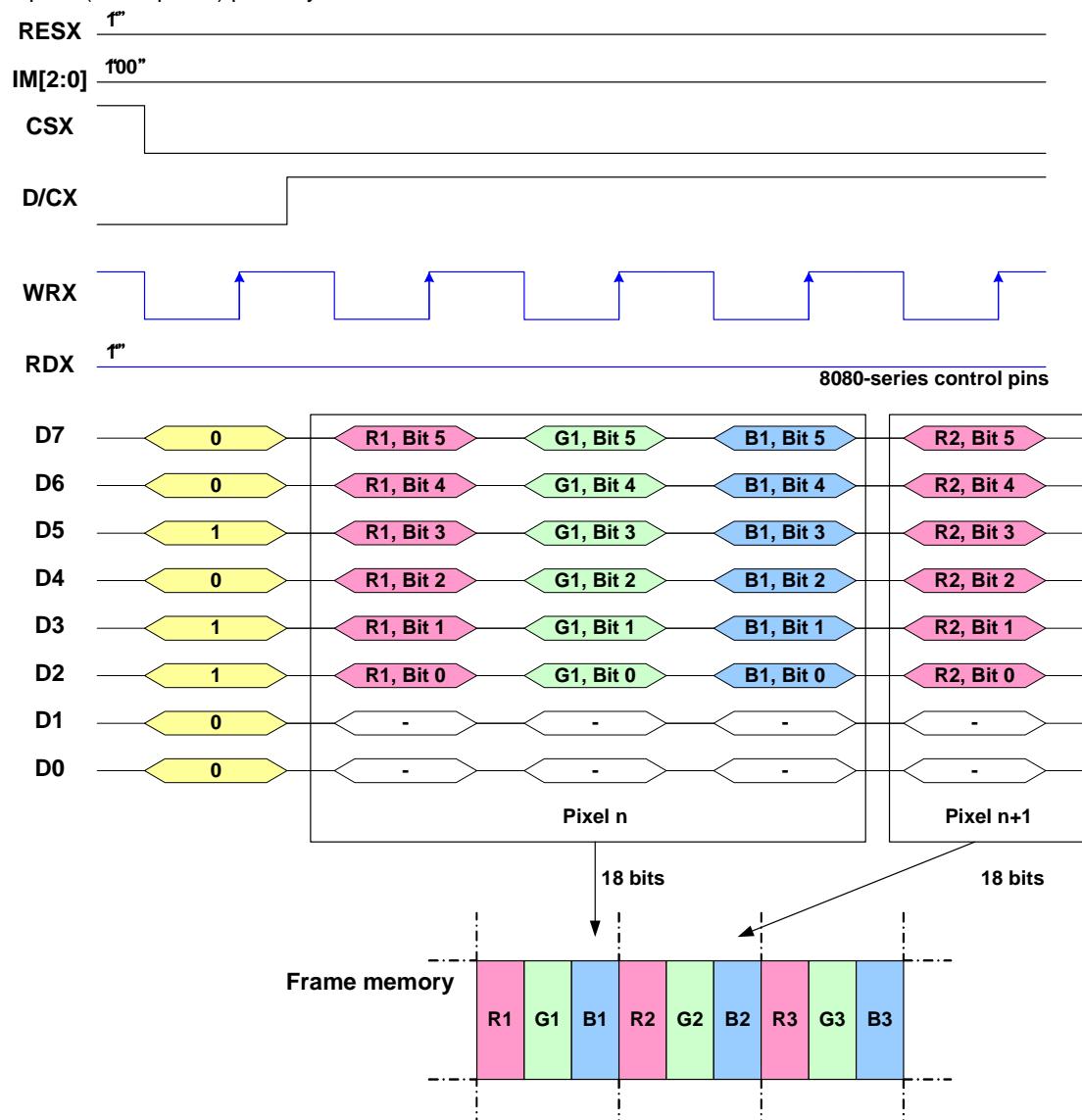
Note 2: 2-times transfer is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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9.7.4 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= "06h"

There is 1 pixel (3 sub-pixels) per 3-bytes.



Note 1: The data order is as follows, MSB=D7, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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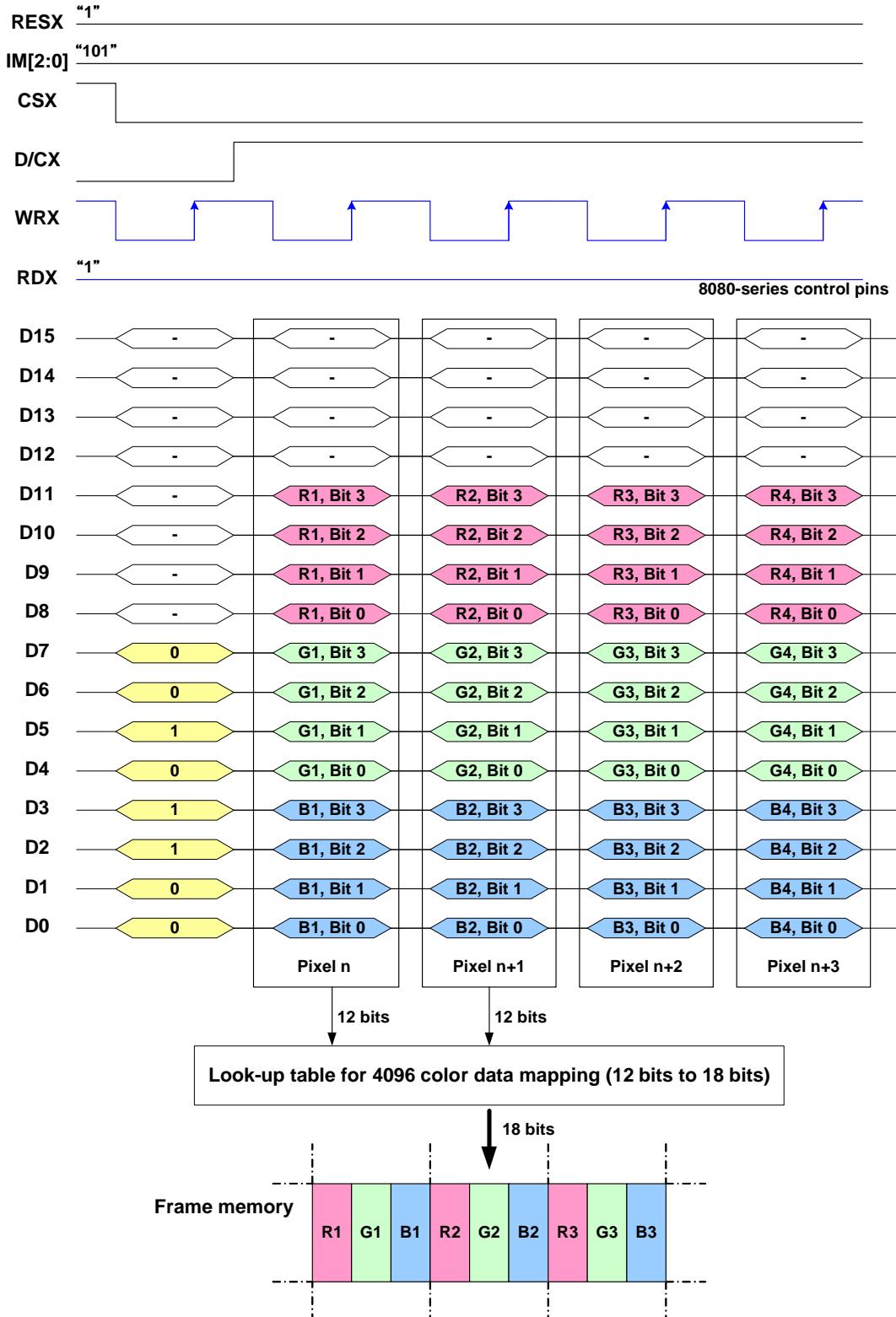
9.7.5 16-Bit Parallel Interface (IM2,IM1, IM0= "101")

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input

9.7.6 16-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH= "03h"

There is 1 pixel (3 sub-pixels) per 1 byte



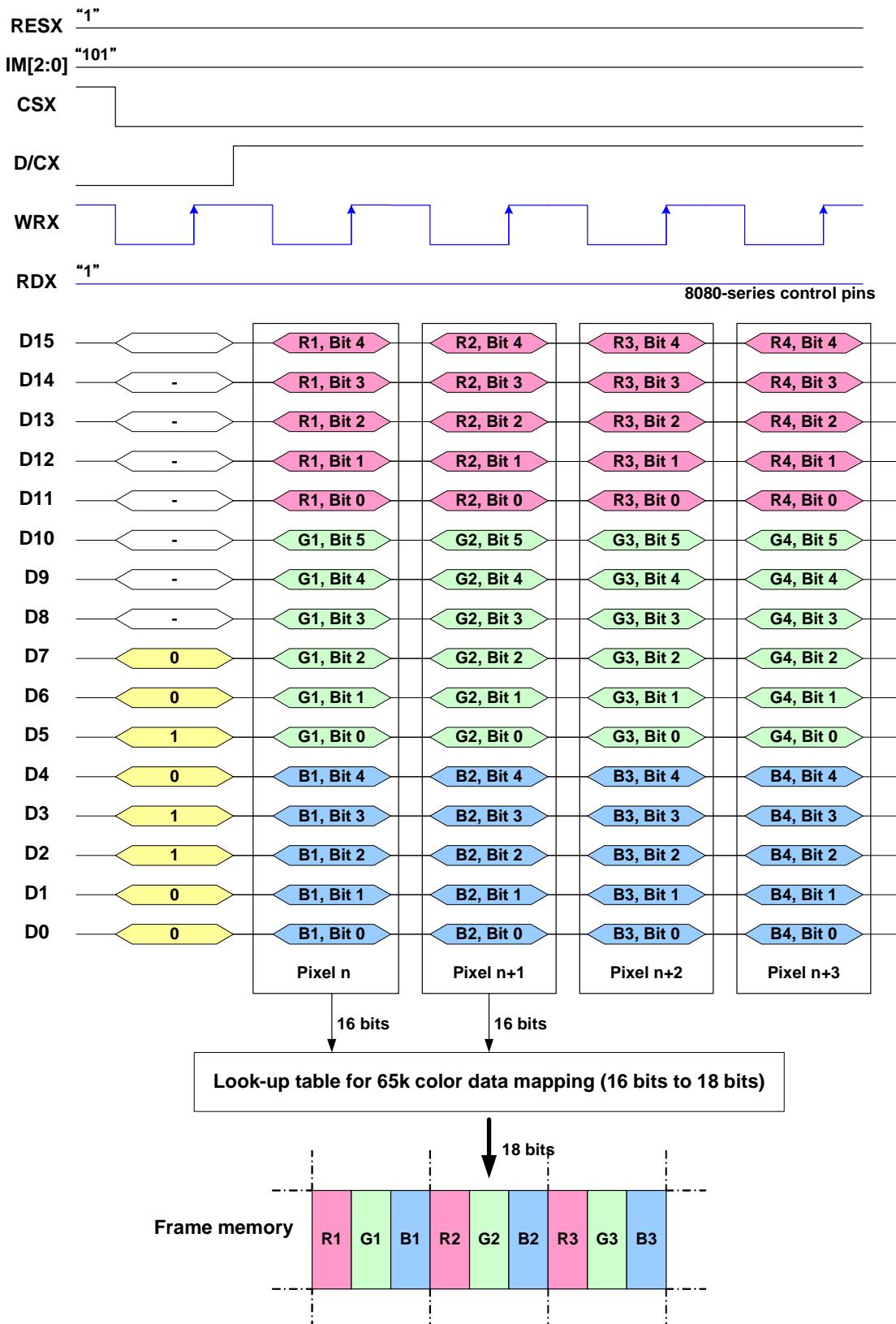
Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer (D11 to D0) is used to transmit 1 pixel data with the 12-bit color depth information.

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9.7.7 16-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH= "05h"

There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

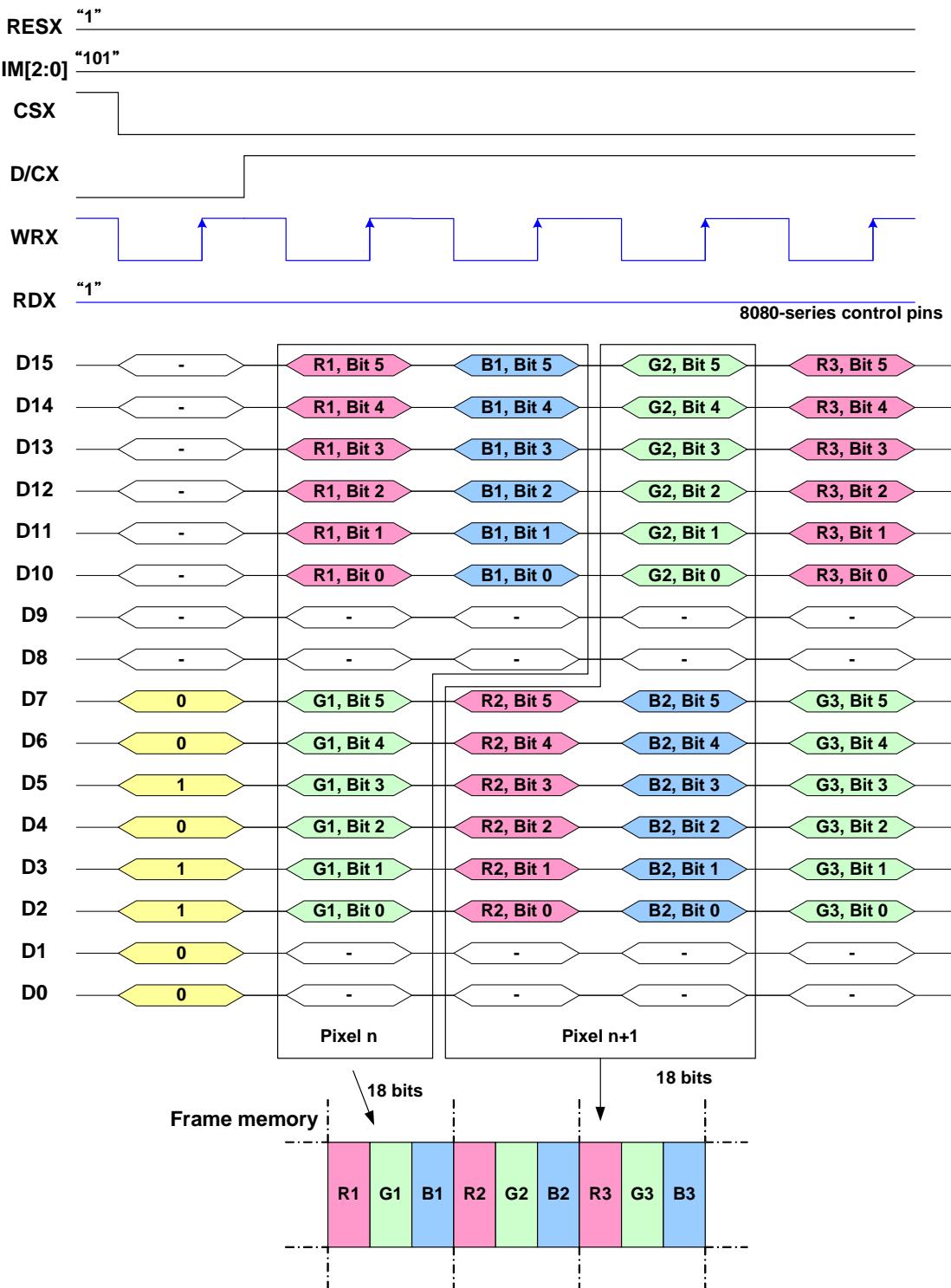
Note 2: 1-times transfer (D15 to D0) is used to transmit 1 pixel data with the 16-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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9.7.8 16-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH= "06h"

There are 2 pixels (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bits 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

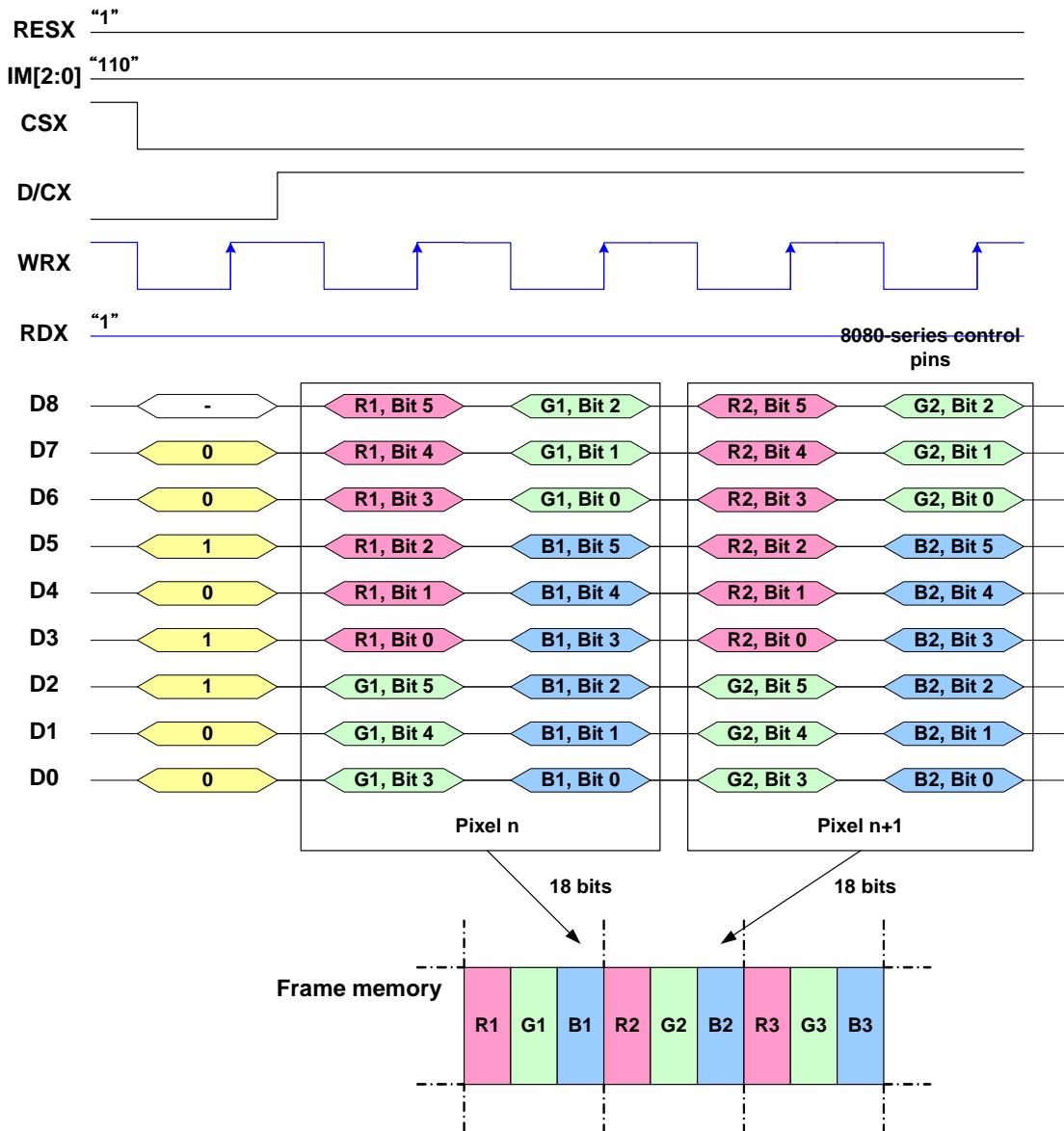
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9.7.9 9-Bit Parallel Interface (IM2, IM1, IM0="110")

Different display data formats are available for three colors depth supported by listed below.
-262k colors, RGB 6,6,6-bit input

9.7.10 Write 9-bit data for RGB 6-6-6-bit input (262k-color)

There is 1 pixel (6 sub-pixels) per 3 bytes



Note 1: The data order is as follows, MSB=D8, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.

Note 3: '-' = Don't care - Can be set to '0' or '1'

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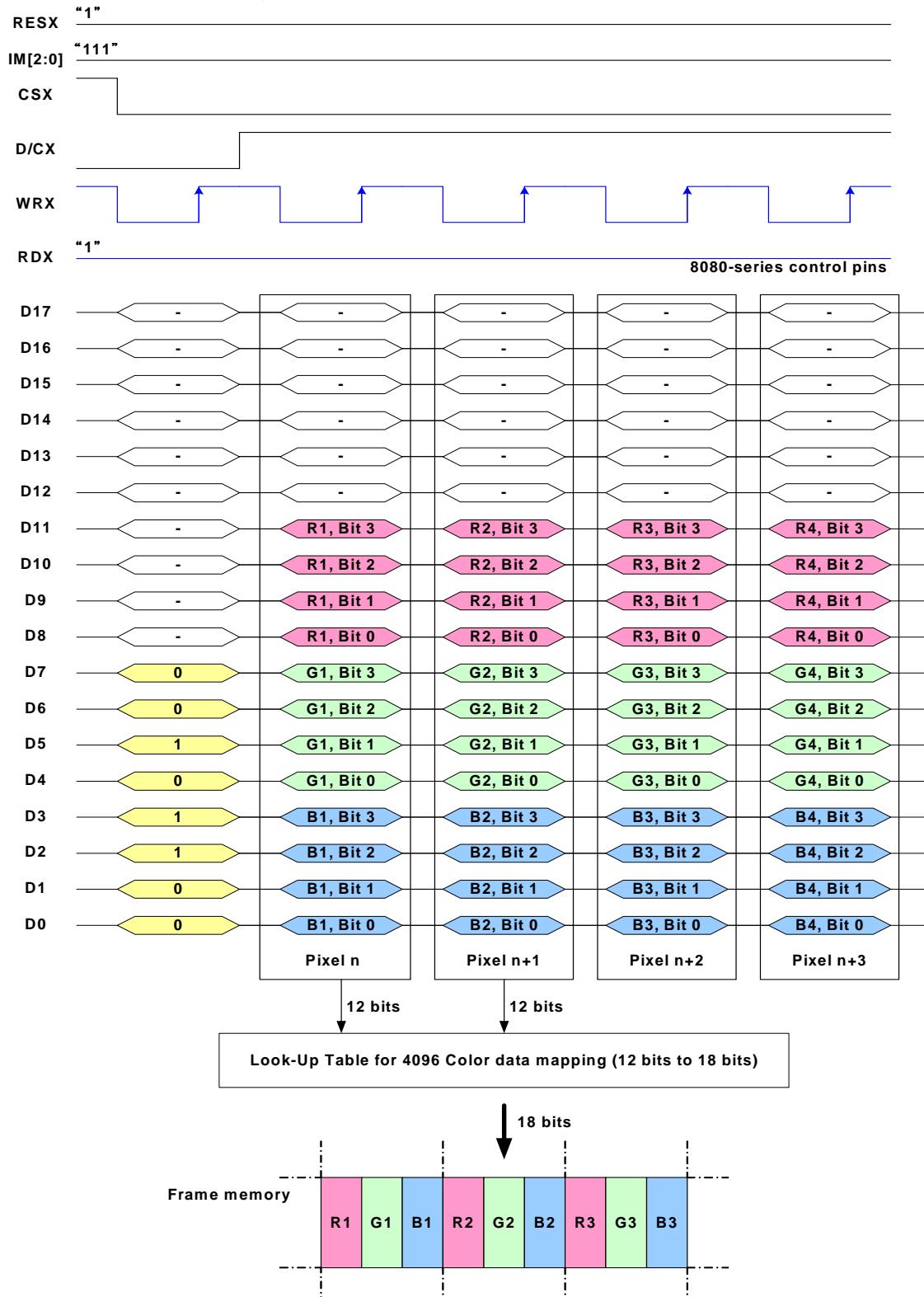
9.7.11 18-Bit Parallel Interface (IM2, IM1, IM0="111")

Different display data formats are available for three colors depth supported by listed below.

- 4k colors, RGB 4,4,4-bit input
- 65k colors, RGB 5,6,5-bit input
- 262k colors, RGB 6,6,6-bit input.

9.7.12 18-bit data bus for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"

There is 1 pixel (3 sub-pixels) per 1 byte



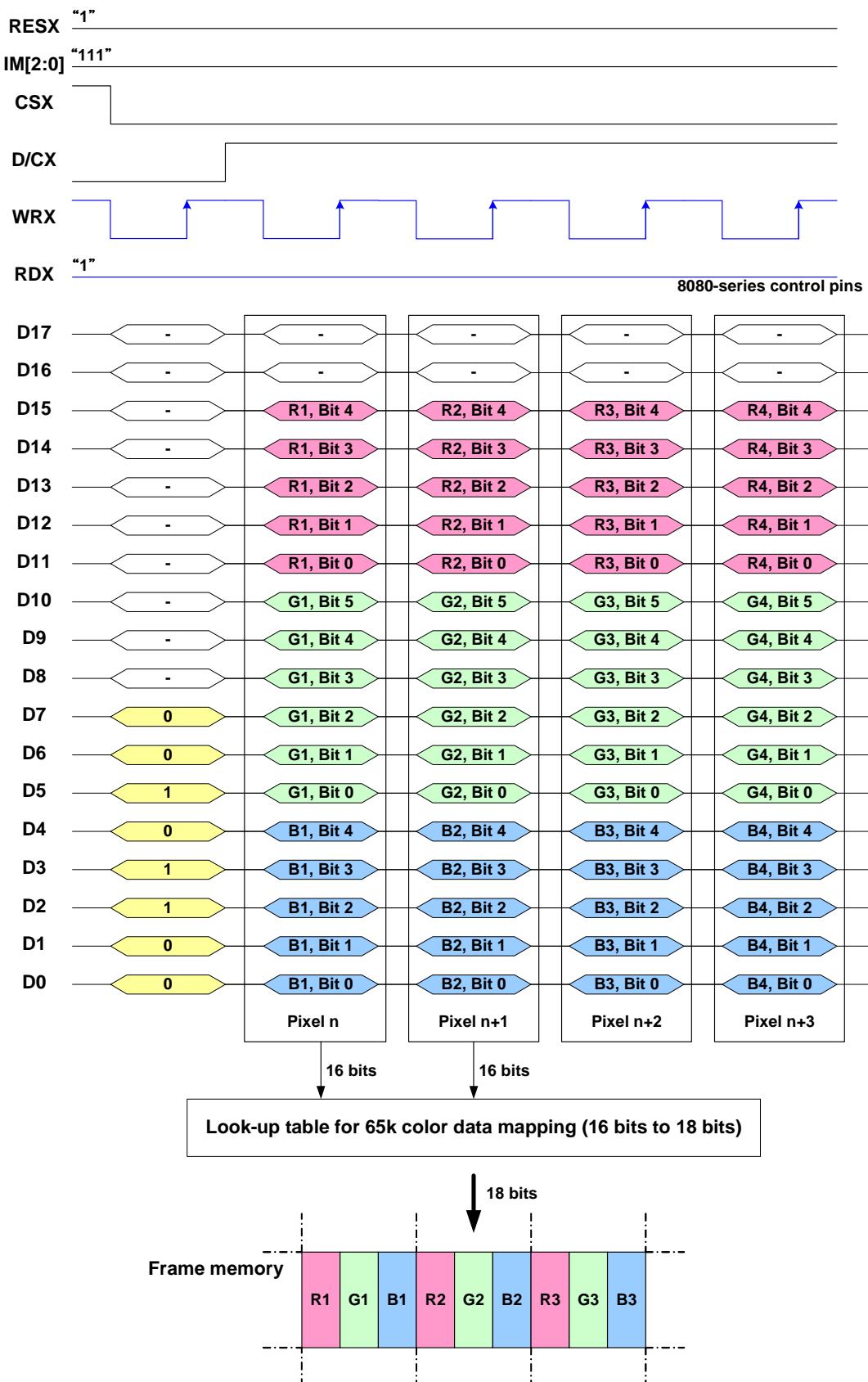
Note 1: The data order is as follows, MSB=D11, LSB=D0 and picture data is MSB=Bit 3, LSB=Bit 0 for Red, Green and Blue data.

Note 2: 1-times transfer is used to transmit 1 pixel data with the 12-bit color depth information.

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9.7.13 18-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"

There is 1 pixel (3 sub-pixels) per 1 byte



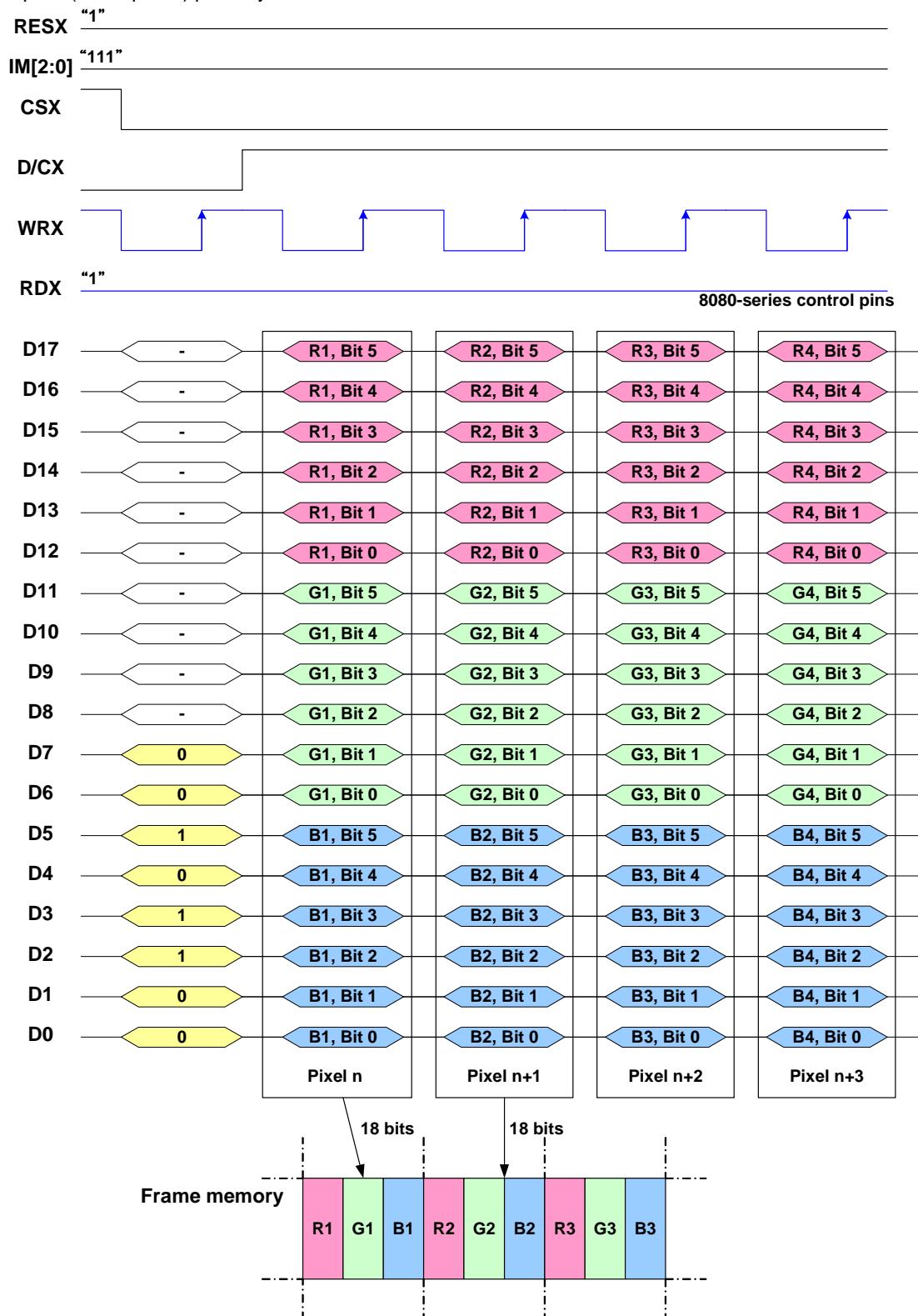
Note 1: The data order is as follows, MSB=D15, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 1-time transfer is used to transmit 1 pixel data with the 16-bit color depth information.

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9.7.14 18-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"

There is 1 pixel (3 sub-pixels) per 1 byte



Note 1: The data order is as follows, MSB=D17, LSB=D0 and picture data is MSB=Bit 5, LSB=Bit 0 for Read, Green and Blue data.

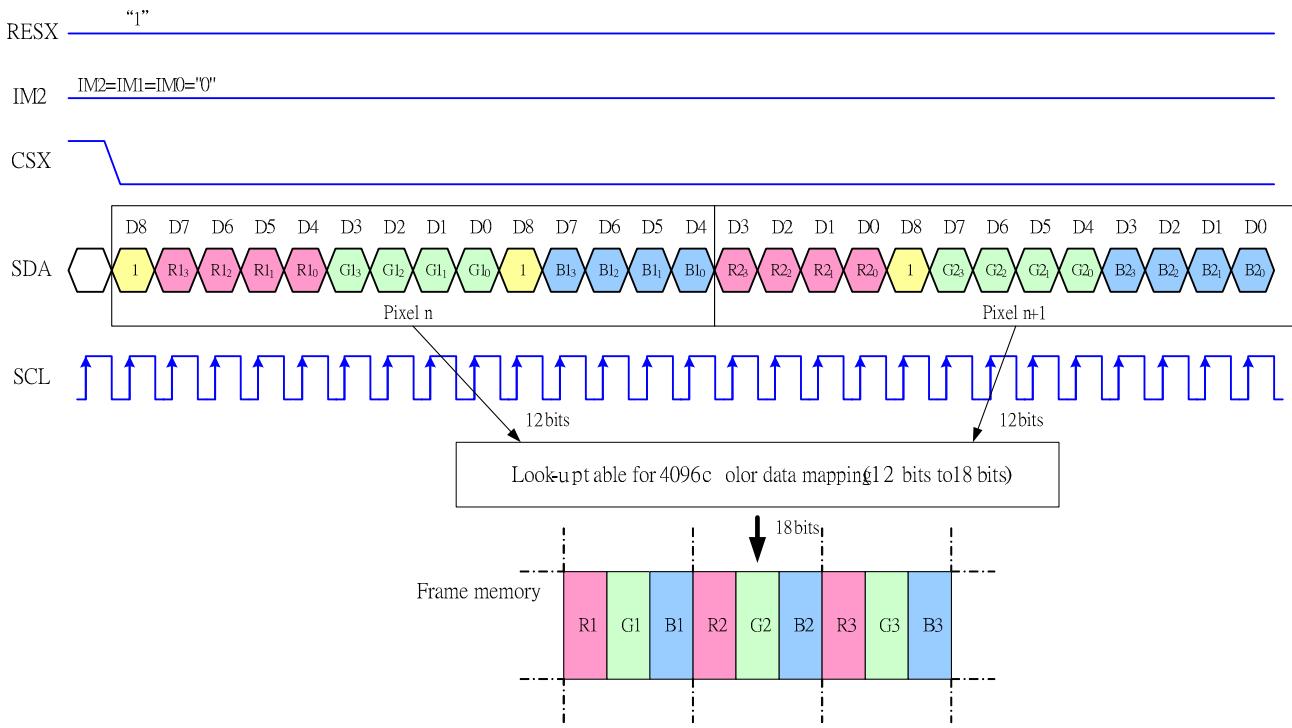
Note 2: 1-times transfer (D17o D0) is used to transmit 1 pixel data with the 18-bit color depth information.

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9.7.15 3-line serial Interface

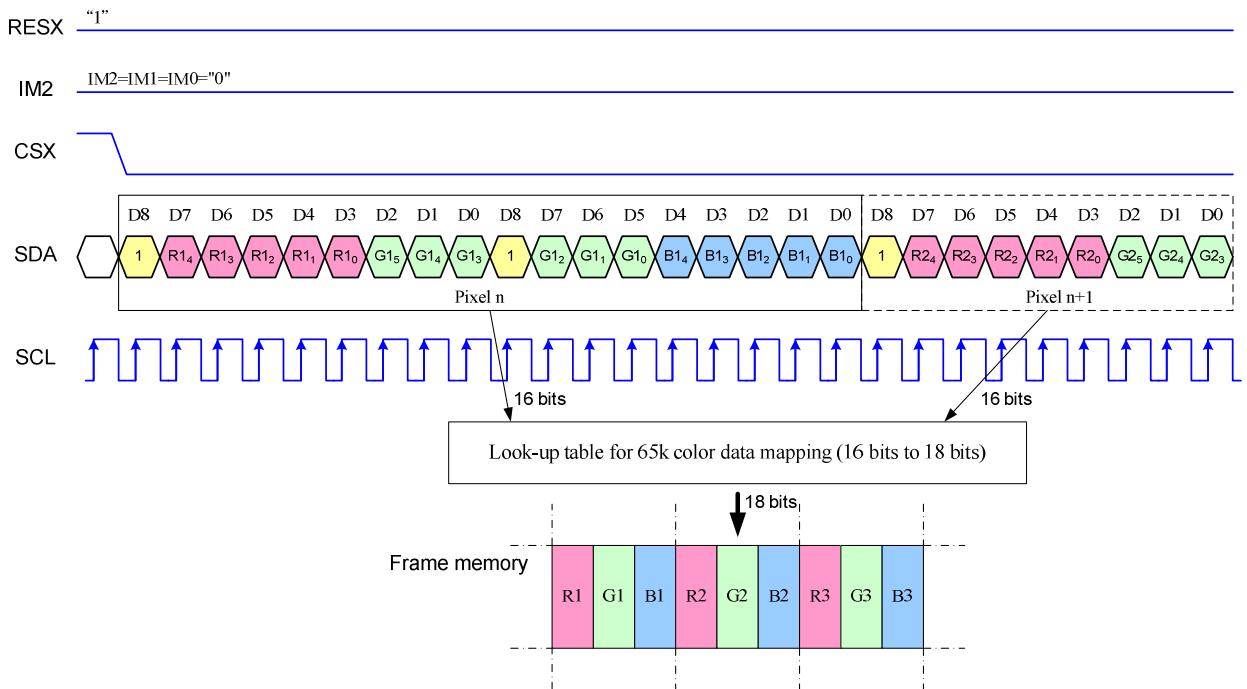
Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.7.16 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



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9.7.17 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



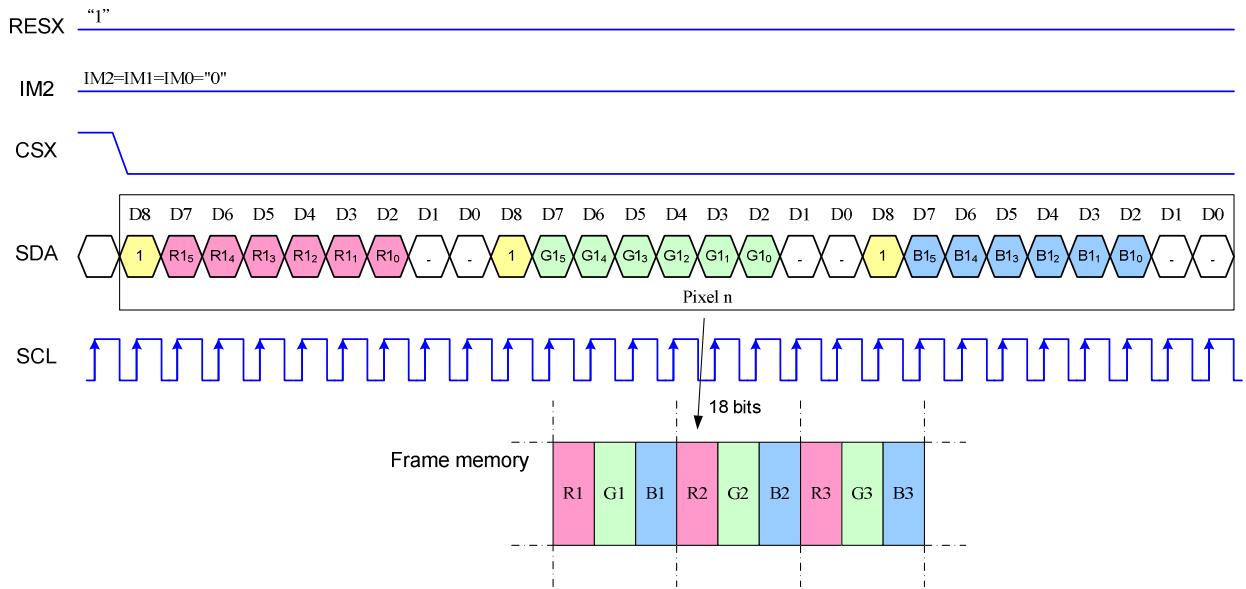
Note 1: Pixel data with the 16-bit color depth information

Note 2: The most significant bits are: Rx4, Gx5 and Bx4

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

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9.7.18 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

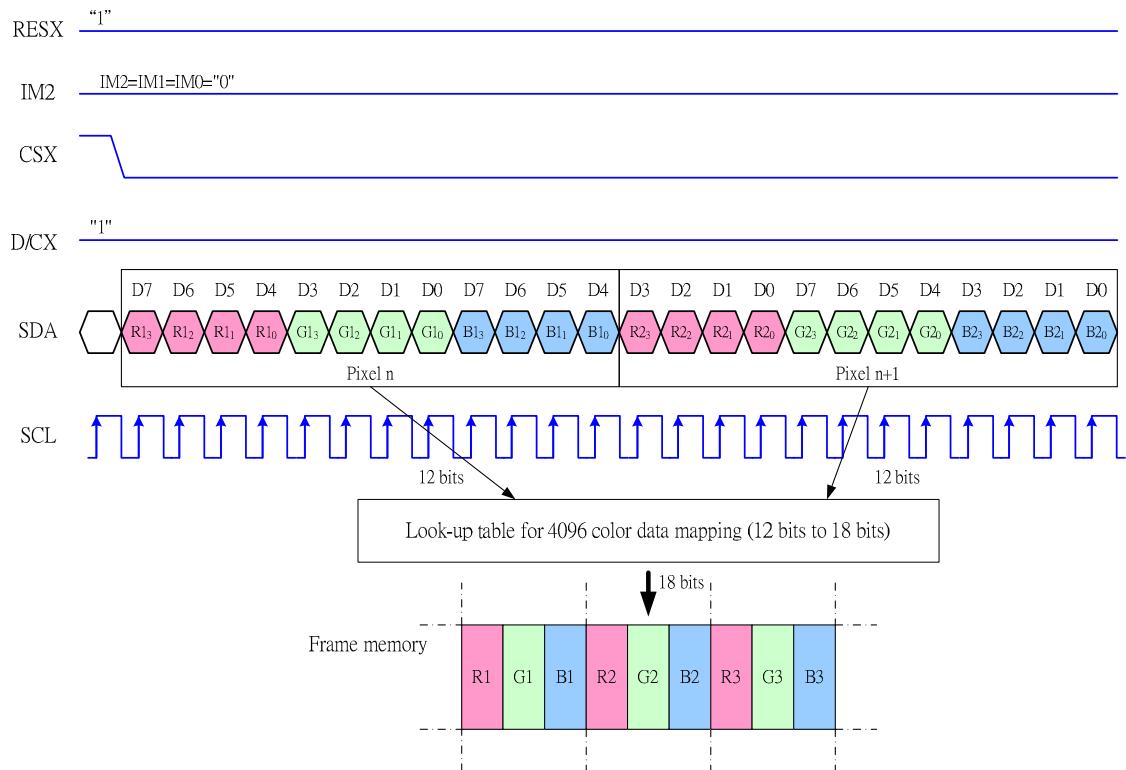
Note 3: The least significant bits are: Rx0, Gx0 and Bx0

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9.7.19 4-line serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.
4k colors, RGB 4-4-4-bit input
65k colors, RGB 5-6-5-bit input
262k colors, RGB 6-6-6-bit input

9.7.20 Write data for 12-bit/pixel (RGB 4-4-4-bit input), 4K-Colors, 3AH="03h"



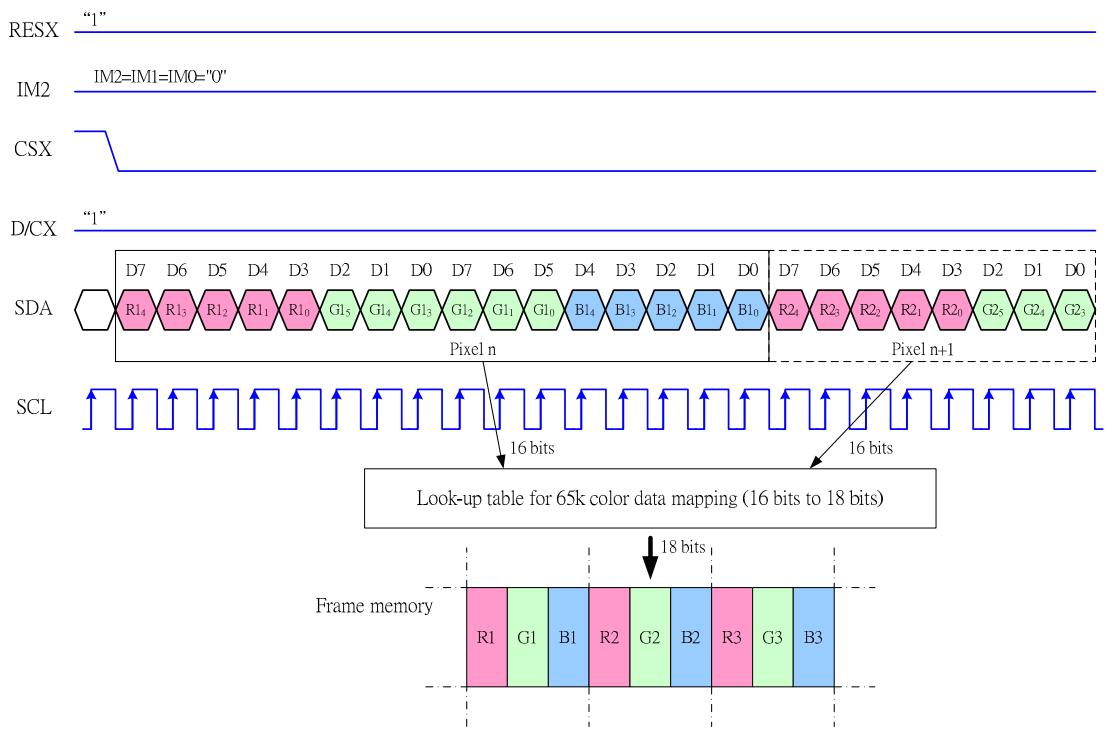
Note 1: Pixel data with the 12-bit color depth information

Note 2: The most significant bits are: Rx3, Gx3 and Bx3

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

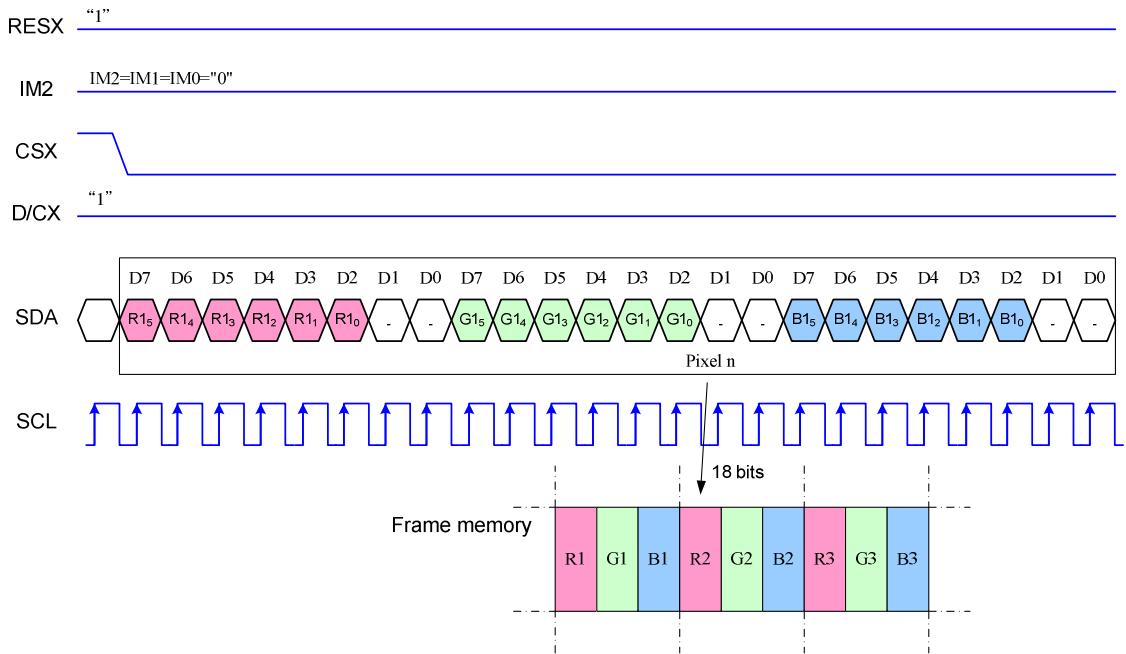
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9.7.21 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3AH="05h"



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9.7.22 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3AH="06h"



Note 1: Pixel data with the 18-bit color depth information

Note 2: The most significant bits are: Rx5, Gx5 and Bx5

Note 3: The least significant bits are: Rx0, Gx0 and Bx0

9.8 Display Data RAM

9.8.1 Configuration (GM[2:0] = "000")

The display module has an integrated 132x162x18-bit graphic type static RAM. This 384,912-bit memory allows storing on-chip a 132xRGBx162 image with an 18-bpp resolution (262K-color). There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.

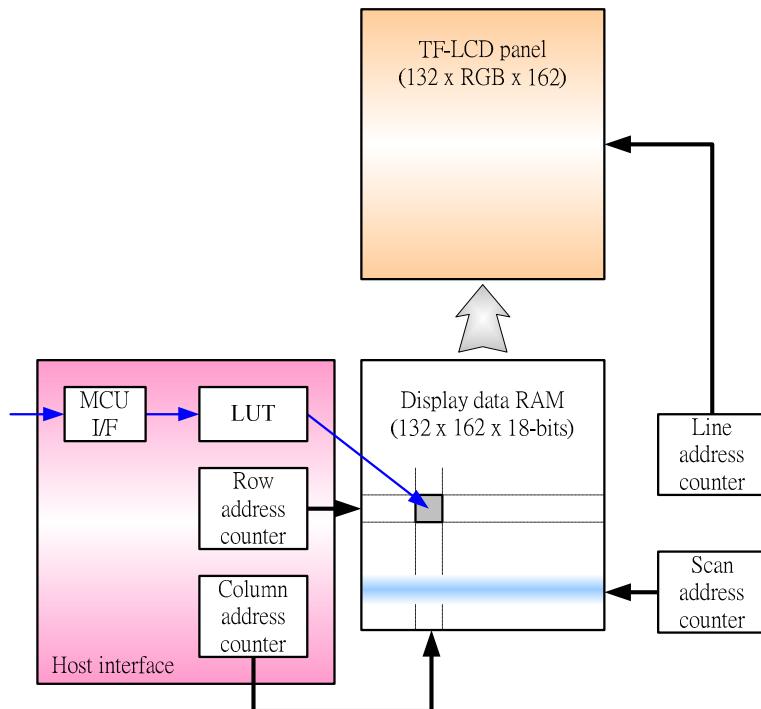


Fig. 9.8.1 Display data RAM organization

9.8.2 Memory to Display Address Mapping

9.8.2.1 When using 128RGB x 160 resolution (GM[2:0] = "011", SMX=SMY=SRGB= '0')

		Pixel 1			Pixel 2			Pixel 127			Pixel 128				
Gate Out	Source Out	S7	S8	S9	S10	S11	S12	-----	S385	S386	S387	S388	S389	S390	
		RA			RGB=0		RGB=1		RGB=0		RGB=1		RGB=0		RGB=1
		MY='0'	MY='1'												
2	0	159	R0	G0	B0	R1	G1	B1	-----	R126	G126	B126	R127	G127	B127
3	1	158													
4	2	157													
5	3	156													
6	4	155													
7	5	154													
8	6	153													
9	7	152													
-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----
154	152	7													
155	153	6													
156	154	5													
157	155	4													
158	156	3													
159	157	2													
160	158	1													
161	159	0													
CA		MX='0'	0		1		-----			126		127			
		MX='1'	127		126		-----			1		0			

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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9.8.2.2 When using 132RGB x 162 resolution (GM[2:0] = "000", SMX=SMY=SRGB='0')

		Pixel 1			Pixel 2			-----			Pixel 131			Pixel 132		
Gate Out	Source Out	S1	S2	S3	S4	S5	S6	-----	S391	S392	S393	S394	S395	S396		
		RA		RGBD		RGBD		RGBD		RGBD		RGBD		SA		
		MY='0' MY='1'		R0 G0 B0		R1 G1 B1		-----		R131 G131 B131		R132 G132 B132		ML='0' ML='1'		
1	0	161	R0	G0	B0	R1	G1	B1	-----	R131	G131	B131	R132	G132	B132	0 161
2	1	160							-----							1 160
3	2	159							-----							2 159
4	3	158							-----							3 158
5	4	157							-----							4 157
6	5	156							-----							5 156
7	6	155							-----							6 155
8	7	154							-----							7 154
1	1	1														1 1
1	1	1														1 1
1	1	1														1 1
1	1	1														1 1
1	1	1														1 1
155	154	7							-----							154 7
156	155	6							-----							155 6
157	156	5							-----							156 5
158	157	4							-----							157 4
159	158	3							-----							158 3
160	159	2							-----							159 2
161	160	1							-----							160 1
162	161	0							-----							161 0
CA		MX='0' 0			1			-----			130			131		
CA		MX='1' 131			130			-----			1			0		

Note

RA = Row Address,

CA = Column Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

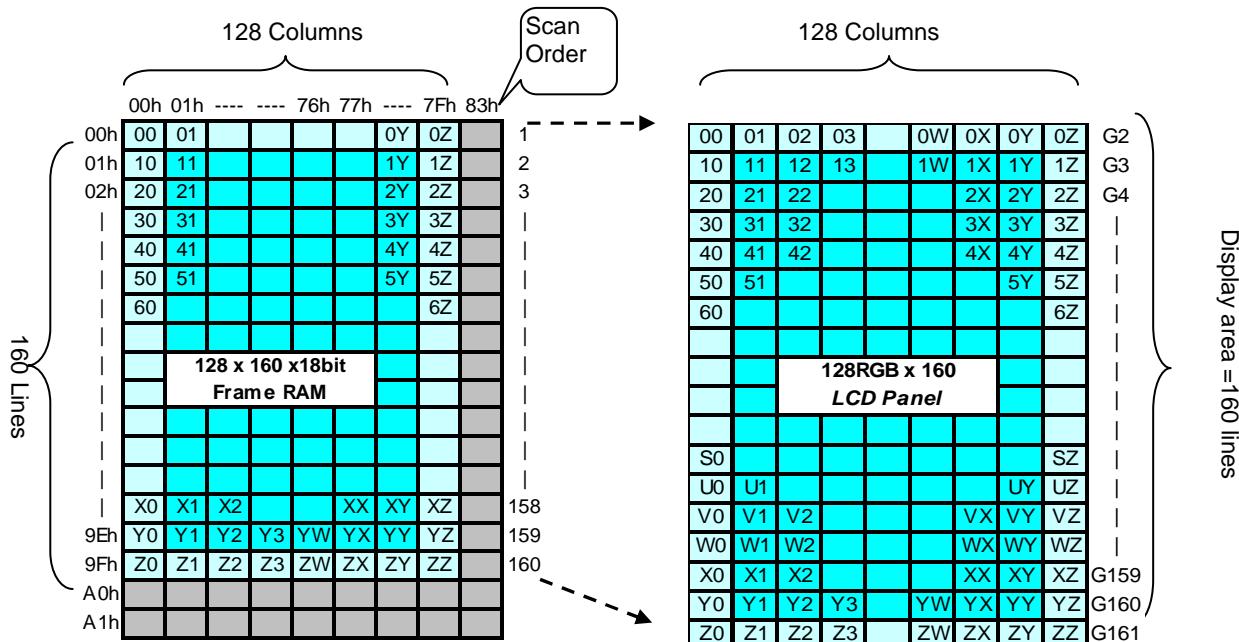
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9.8.3 Normal Display On or Partial Mode On

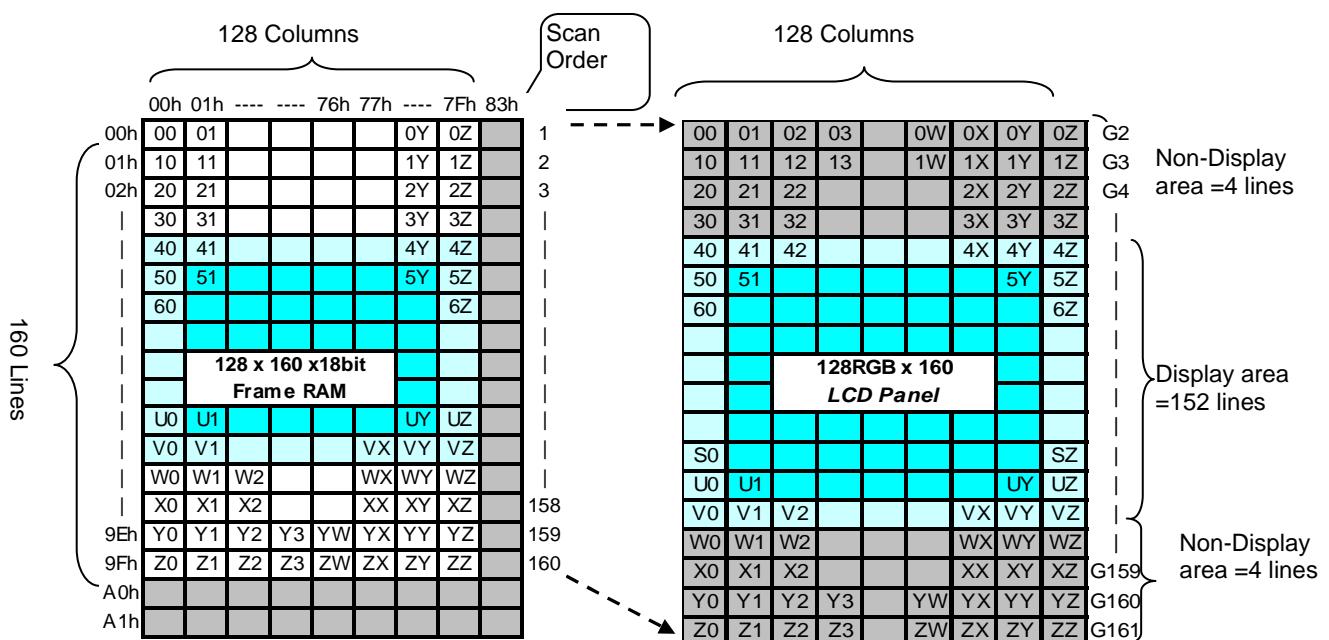
9.8.3.1 When using 128RGB x 160 resolution (GM[2:0] = "011")

In this mode, the content of the frame memory within an area where column pointer is 00h to 7Fh and page pointer is 00h to 9Fh is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0).

- 1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



- 2). Example for Partial Display On (PSL[7:0]=04h, PEL[7:0]=9Bh, MX=MV=ML='0', SMX=SMY='0')

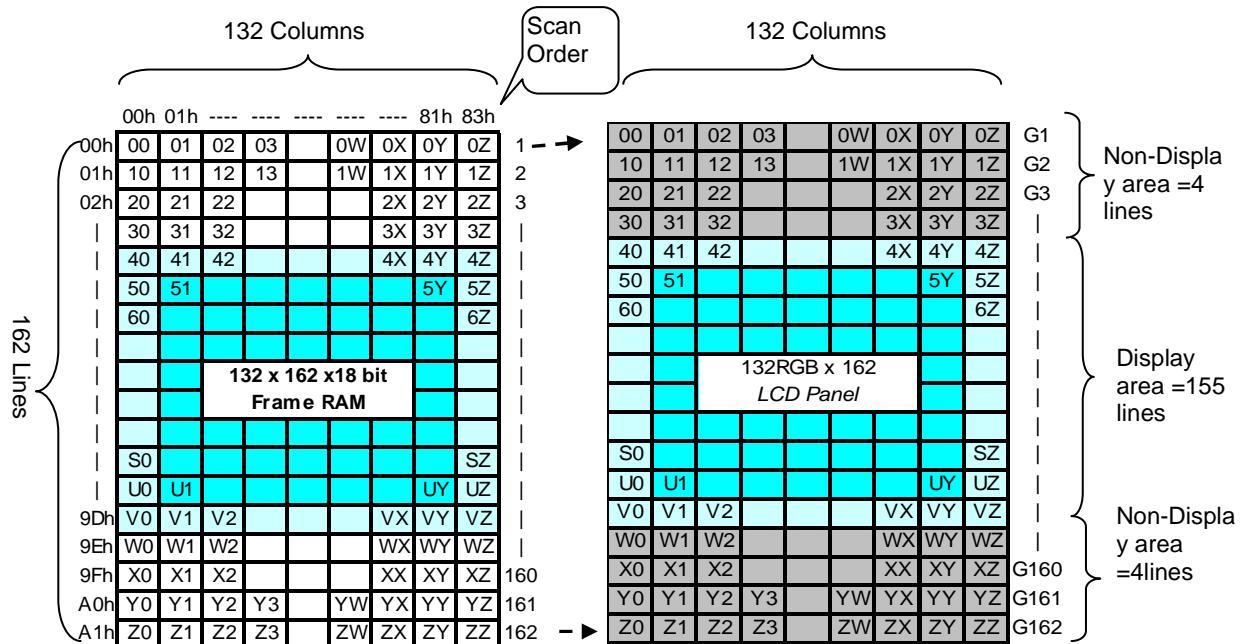


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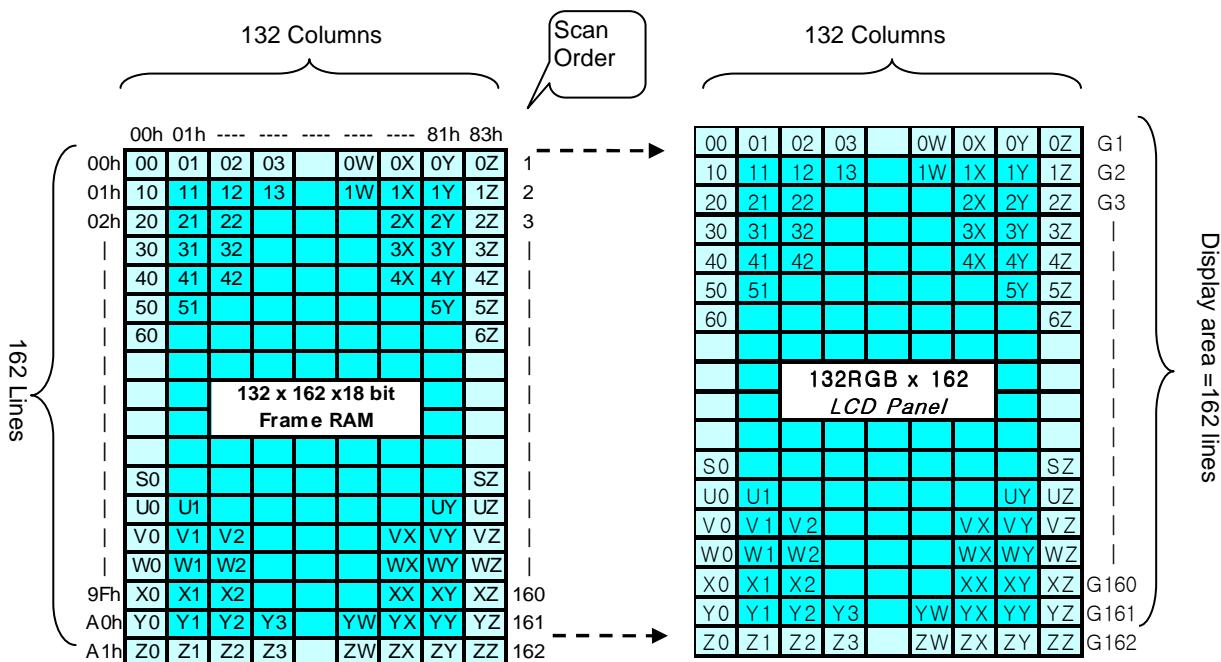
9.8.3.2 When using 132RGB x 162 resolution (GM[2:0] = "000")

In this mode, contents of the frame memory within an area where column pointer is 00h to 83h and page pointer is 00h to A1h is displayed. To display a dot on leftmost top corner, store the dot data at (column pointer, row pointer) = (0, 0)

- 1). Example for Normal Display On (MX=MY=ML='0', SMX=SMY='0')



- 2). Example for Partial Display On (PSL[7:0]=04h, PEL[7:0]=9Dh, MX=MV=ML='0' ,SMX=SMY='0')



9.9 Address Counter

The address counter sets the addresses of the display data RAM for writing and reading.

Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the "Write access" is activated on the RAM. The locations of RAM are addressed by the address pointers. The address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM, a window must be defined that will be written. The window is programmable via the command registers XS, YS designating the start address and XE, YE designating the end address.

For example the whole display contents will be written, the window is defined by the following values: XS=0 (0h) YS=0 (0h) and XE=127 (83h), YE=161 (A1h).

In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address (X=XE), X wraps around to XS and Y increments to address the next row. After the every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands "CASET, RASET and MADCTL" (see section 10 command list), define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Section 9.10 show the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM.

For each image condition, the controls for the column and row counters apply as section 9.10 below

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column (XS)"	Return to "Start Row (YS)"
Complete Pixel Read / Write action	Increment by 1	No change
The Column counter value is larger than "End Column (XE)"	Return to "Start Column (XS)"	Increment by 1
The Column counter value is larger than "End Column (XE)" and the Row counter value is larger than "End Row (YE)"	Return to "Start Column (XS)"	Return to "Start Row (YS)"

9.10 Memory Data Write/ Read Direction

The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, bits B5 (MV), B6 (MX), B7 (MY) as described below.

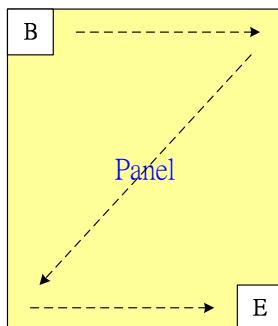


Fig. 9.10.1 Data streaming order

9.10.1 When 128RGBx160 (GM= "011")

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (159-Physical Row Pointer)
0	1	0	Direct to (127-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (127-Physical Column Pointer)	Direct to (159-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (159-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (127-Physical Column Pointer)
1	1	1	Direct to (159-Physical Row Pointer)	Direct to (127-Physical Column Pointer)

9.10.2 When 132RGBx162 (GM= "000")

MV	MX	MY	CASET	RASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Row Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161-Physical Row Pointer)
0	1	0	Direct to (131-Physical Column Pointer)	Direct to Physical Row Pointer
0	1	1	Direct to (131-Physical Column Pointer)	Direct to (161-Physical Row Pointer)
1	0	0	Direct to Physical Row Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161-Physical Row Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Row Pointer	Direct to (131-Physical Column Pointer)
1	1	1	Direct to (161-Physical Row Pointer)	Direct to (131-Physical Column Pointer)

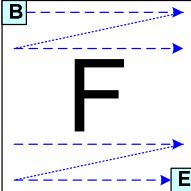
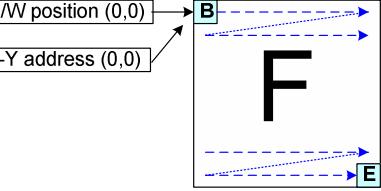
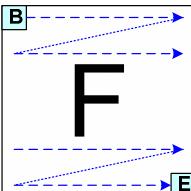
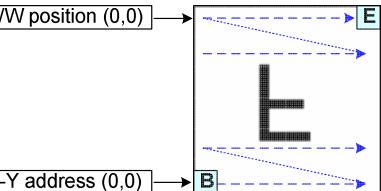
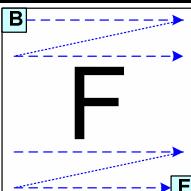
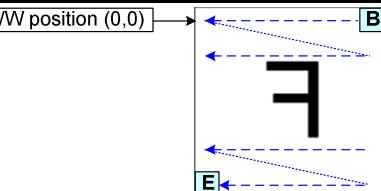
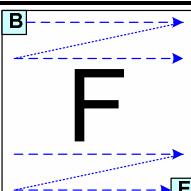
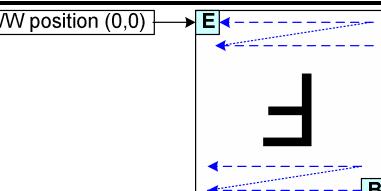
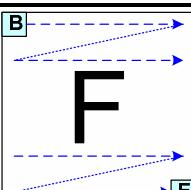
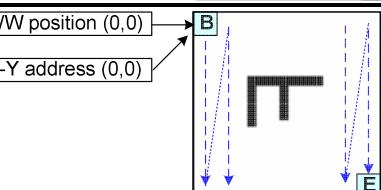
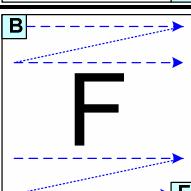
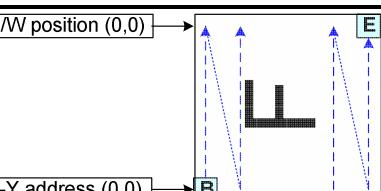
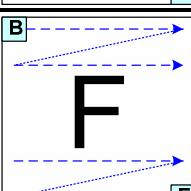
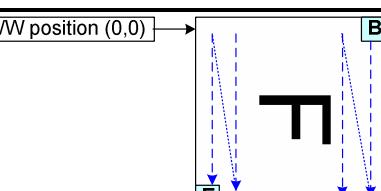
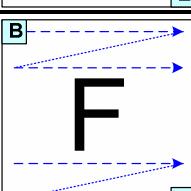
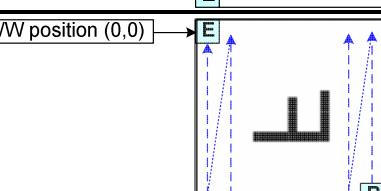
Note: Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7 (MY), B6 (MX), B5 (MV). The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1page counter value on the Frame Memory.

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9.10.3 Frame Data Write Direction According to the MADCTL parameters (MV, MX and MY)

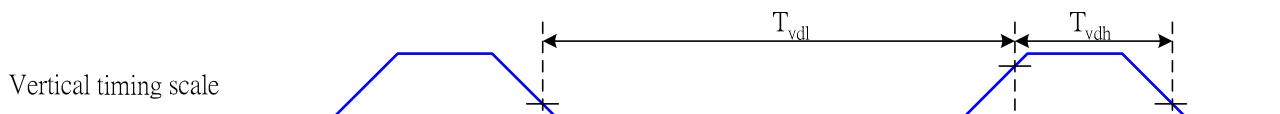
Display Data Direction	MADCTL Parameter			Image in the Host (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		
X-Y Exchange X-Mirror Y-Mirror	1	1	1		

9.11 Tearing Effect Output Line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory Writing when displaying video images.

9.11.1 Tearing Effect Line Modes

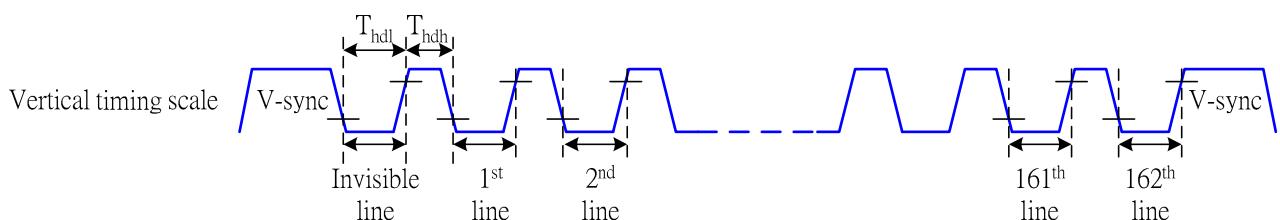
Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:



$tvdh$ = The LCD display is not updated from the Frame Memory

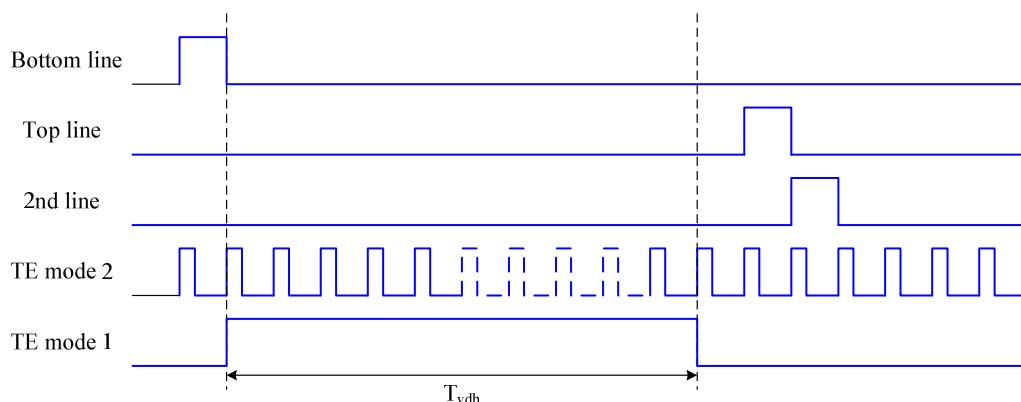
$tvdl$ = The LCD display is updated from the Frame Memory (except Invisible Line – see above)

Mode 2, the Tearing Effect Output signal consists of V-Blanking and H-Blanking Information, there is one V-sync and 162 H-sync pulses per field.



$thdh$ = The LCD display is not updated from the Frame Memory

$thdl$ = The LCD display is updated from the Frame Memory (except Invisible Line – see above)



Note: During Sleep In Mode, the Tearing Output Pin is active Low.

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9.11.2 Tearing Effect Line Timings

The Tearing Effect signal is described below:

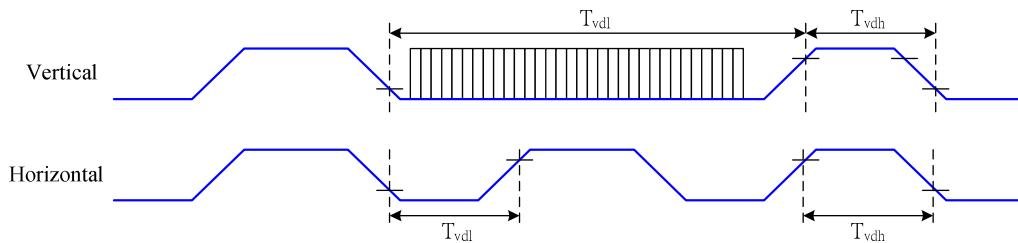
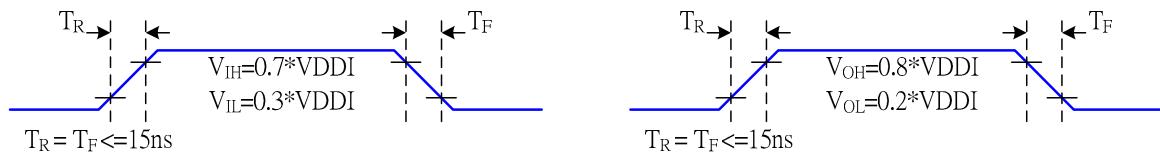


Table 9.11.1 AC characteristics of Tearing Effect Signal Idle Mode Off (Frame Rate = 60 Hz, Ta=25°C)

Symbol	Parameter	min	max	unit	description
tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μs	
thdl	Horizontal Timing Low Duration	33	-	μs	
thdh	Horizontal Timing Low Duration	25	500	μs	

Note: The timings in Table 9.10.1 apply when MADCTL ML=0 and ML=1

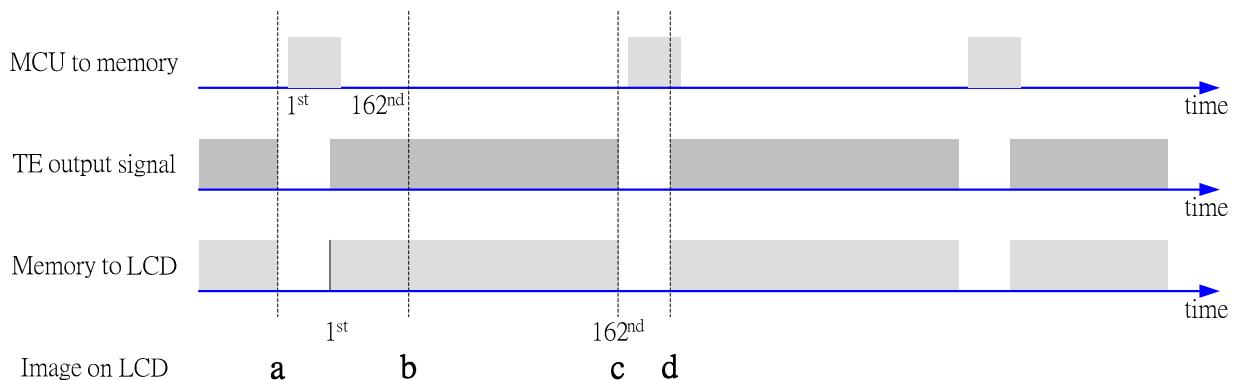
The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



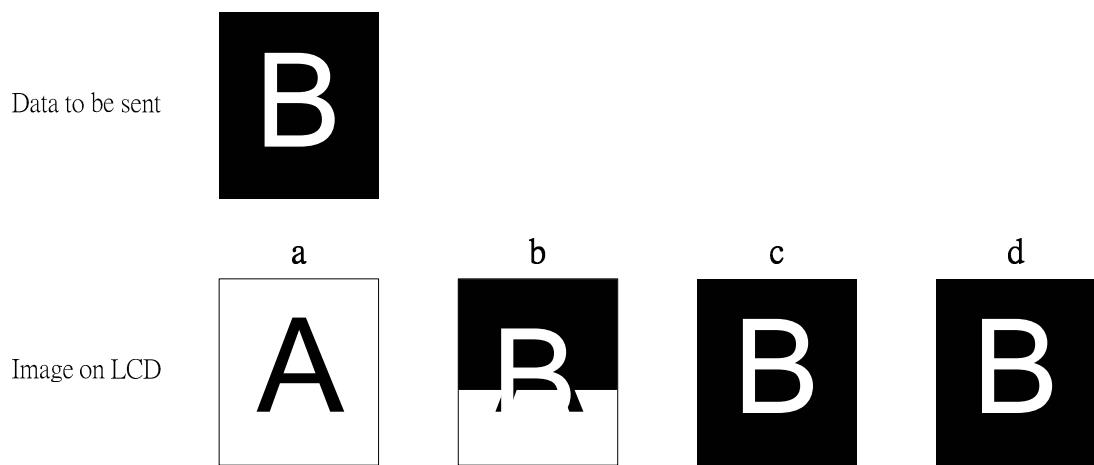
The Tearing Effect Output Line is fed back to the MPU and should be used as shown below to avoid Tearing Effect:

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9.11.3 Example 1: MPU Write is faster than panel read

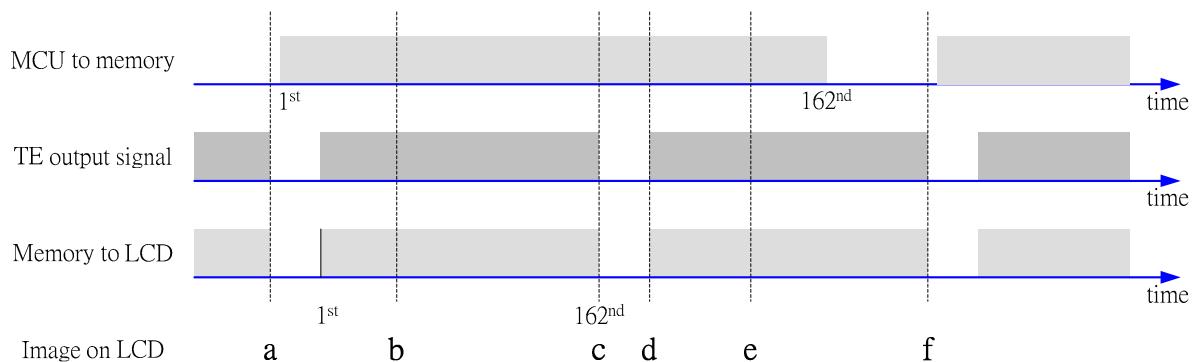


Data write to Frame Memory is now synchronized to the Panel Scan. It should be written during the vertical sync pulse of the Tearing Effect Output Line. This ensures that data is always written ahead of the panel scan and each Panel Frame refresh has a complete new image:

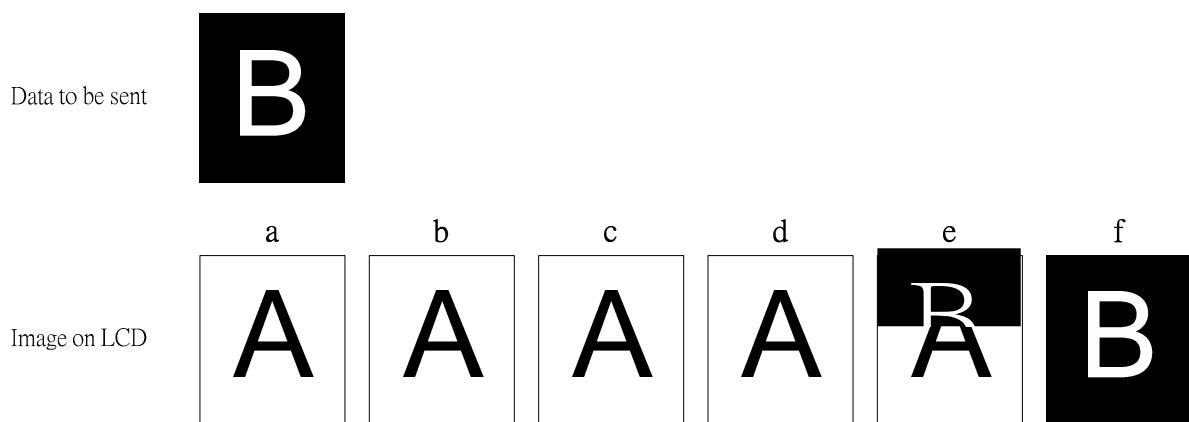


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9.11.4 Example 2: MPU write is slower than panel read



The MPU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer "catches" the MPU to Frame memory write position.



9.12 Power ON/OFF Sequence

VDD must be powered on before the VDDI.

VDDI must be powered off before the VDD.

During power off, if LCD is in the Sleep Out mode, VDD and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VDD can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

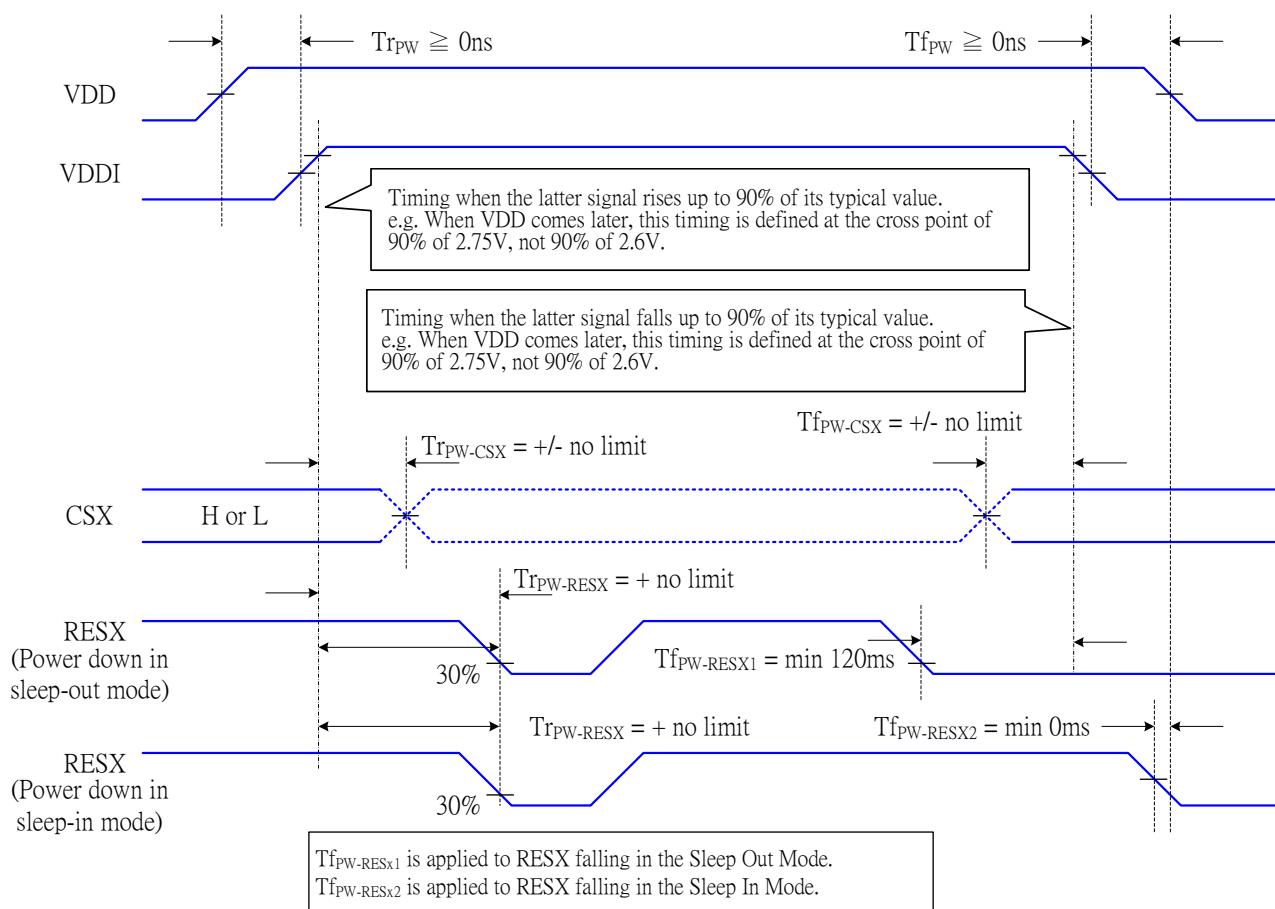
Note 1: There will be no damage to the display module if the power sequences are not met.

Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



9.12.1 Uncontrolled Power Off

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until "Power On Sequence" powers it up.

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9.13 Power Level Definition

9.13.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode

In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

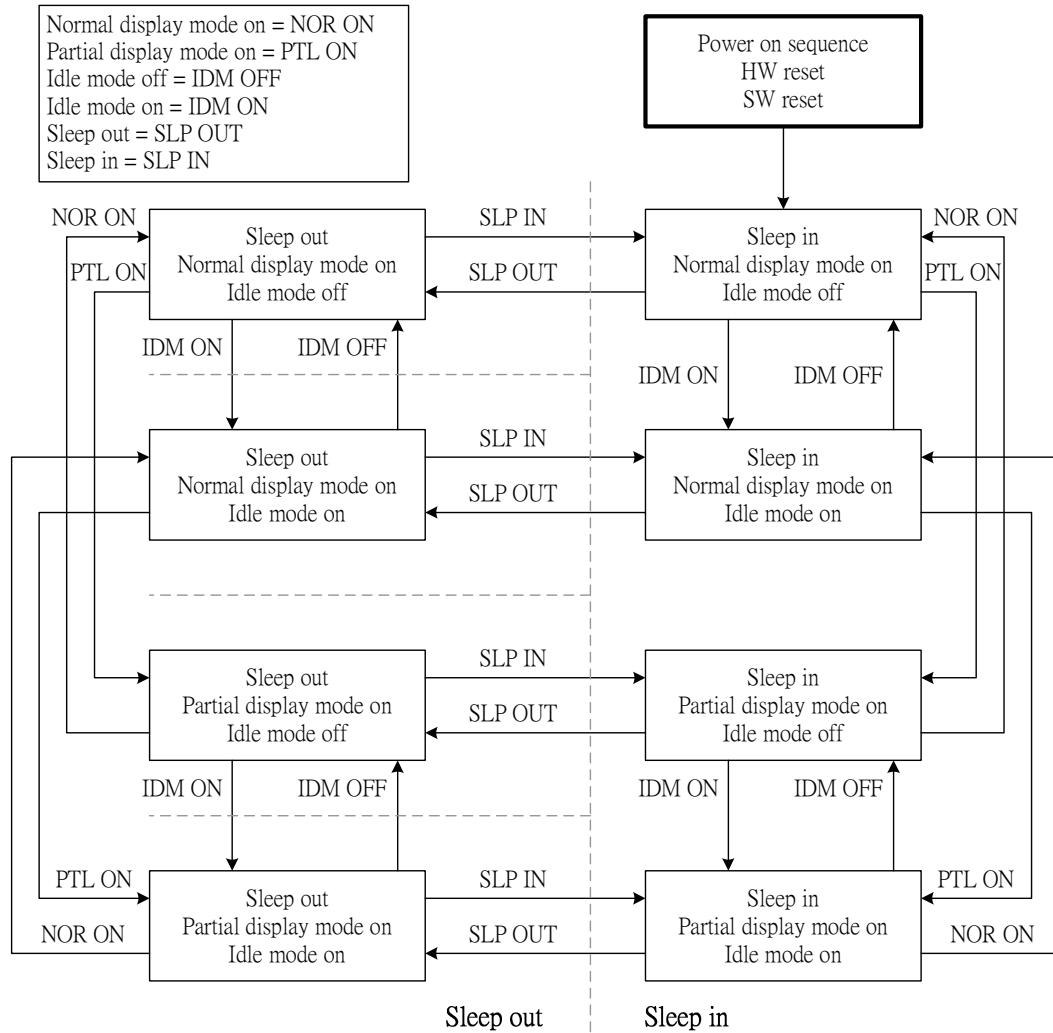
6. Power Off Mode

In this mode, both VDD and VDDI are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

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9.13.2 Power Flow Chart



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9.14 Reset Table

9.14.1 Reset Table (Default Value, GM[2:0] = "011", 128RGB x 160)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	007Fh	007Fh	007Fh (127d) (when MV=0) 009Fh (159d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	009Fh	009Fh	009Fh (159d) (when MV=0) 007Fh (127d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	See Section 9.17	See Section 9.17	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	009Fh	009Fh	009Fh
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0/0	0/0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

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9.14.2 Reset Table (GM[2:0]= “000”, 132RGB x 162)

Item	After Power On	After H/W Reset	After S/W Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode (normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column: Start Address (XS)	0000h	0000h	0000h
Column: End Address (XE)	0083h	0083h	0083h (131d) (when MV=0) 00A1h (161d) (when MV=1)
Row: Start Address (YS)	0000h	0000h	0000h
Row: End Address (YE)	00A1h	00A1h	00A1h (161d) (when MV=0) 0083h (131d) (when MV=1)
Gamma setting	GC0	GC0	GC0
RGB for 4k and 65k Color Mode	See Section 9.17	See Section 9.17	No Change
Partial: Start Address (PSL)	0000h	0000h	0000h
Partial: End Address (PEL)	00A1h	00A1h	00A1h
Tearing: On/Off	Off	Off	Off
Tearing Effect Mode (*1)	0 (Mode1)	0 (Mode1)	0 (Mode1)
Memory Data Access Control (MY/MX/MV/ML/RGB)	0/0/0/0	0/0/0/0	No Change
Interface Pixel Color Format	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDPM	08h	08h	08h
RDDMADCTL	00h	00h	No Change
RDDCOLMOD	6 (18-Bit/Pixel)	6 (18-Bit/Pixel)	No Change
RDDIM	00h	00h	00h
RDDSM	00h	00h	00h
RDDSDR	00h	00h	00h
ID2	NV value	NV value	NV value
ID3	NV value	NV value	NV value

Note: TE Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only

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9.15 Module Input/Output Pins

9.15.1 Output or Bi-directional (I/O) Pins

Output or Bi-directional pins	After Power On	After Hardware Reset	After Software Reset
TE	Low	Low	Low
D7 to D0 (Output driver)	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Input pins	During Power On Process	After Power On	After Hardware Reset	After Software Reset	During Power Off Process
RESX	See 9.14	Input valid	Input valid	Input valid	See 9.14
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D7 to D0	Input invalid	Input valid	Input valid	Input valid	Input invalid

Note: There will be no output from D7-D0 during Power On/Off sequence, Hardware Reset and Software Reset.

9.16 Reset Timing

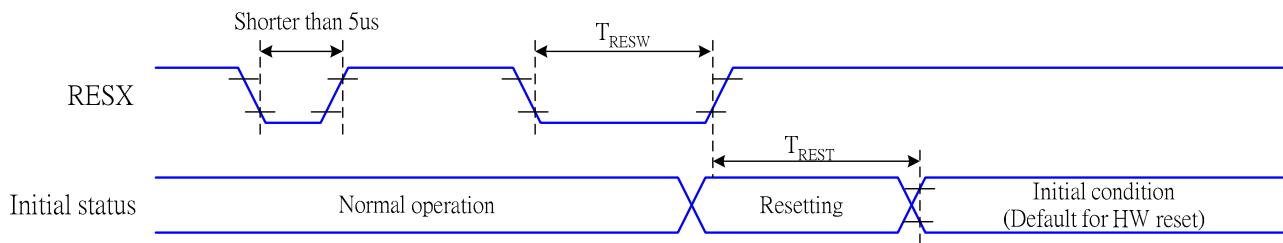


Table 9.16.1 Reset timing

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	tRESW	Reset pulse duration	10	-	us
	tREST	Reset cancel	-	5	ms
				120	ms

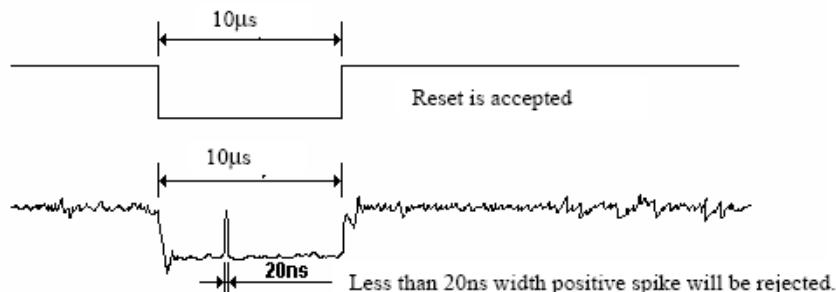
Notes:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (t_{RT}) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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9.17 Color Depth Conversion Look Up Tables

9.17.1 65536 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data
				65k Color (5-bits)
RED	R005 R004 R003 R002 R001 R000	000000	1	00000
	R015 R014 R013 R012 R011 R010	000010	2	00001
	R025 R024 R023 R022 R021 R020	000100	3	00010
	R035 R034 R033 R032 R031 R030	000110	4	00011
	R045 R044 R043 R042 R041 R040	001000	5	00100
	R055 R054 R053 R052 R051 R050	001010	6	00101
	R065 R064 R063 R062 R061 R060	001100	7	00110
	R075 R074 R073 R072 R071 R070	001110	8	00111
	R085 R084 R083 R082 R081 R080	010000	9	01000
	R095 R094 R093 R092 R091 R090	010010	10	01001
	R105 R104 R103 R102 R101 R100	010100	11	01010
	R115 R114 R113 R112 R111 R110	010110	12	01011
	R125 R124 R123 R122 R121 R120	011000	13	01100
	R135 R134 R133 R132 R131 R130	011010	14	01101
	R145 R144 R143 R142 R141 R140	011100	15	01110
	R155 R154 R153 R152 R151 R150	011110	16	01111
	R165 R164 R163 R162 R161 R160	100001	17	10000
	R175 R174 R173 R172 R171 R170	100011	18	10001
	R185 R184 R183 R182 R181 R180	100101	19	10010
	R195 R194 R193 R192 R191 R190	100111	20	10011
	R205 R204 R203 R202 R201 R200	101001	21	10100
	R215 R214 R213 R212 R211 R210	101011	22	10101
	R225 R224 R223 R222 R221 R220	101101	23	10110
	R235 R234 R233 R232 R231 R230	101111	24	10111
	R245 R244 R243 R242 R241 R240	110001	25	11000
	R255 R254 R253 R252 R251 R250	110011	26	11001
	R265 R264 R263 R262 R261 R260	110101	27	11010
	R275 R274 R273 R272 R271 R270	110111	28	11011
	R285 R284 R283 R282 R281 R280	111001	29	11100
	R295 R294 R293 R292 R291 R290	111011	30	11101
	R305 R304 R303 R302 R301 R300	111101	31	11110
	R315 R314 R313 R312 R311 R310	111111	32	11111

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data
				65k Color (5-bits)
GREEN	G005 G004 G003 G002 G001 G000	000000	33	00000
	G015 G014 G013 G012 G011 G010	000001	34	000001
	G025 G024 G023 G022 G021 G020	000010	35	000010
	G035 G034 G033 G032 G031 G030	000011	36	000011
	G045 G044 G043 G042 G041 G040	000100	37	000100
	G055 G054 G053 G052 G051 G050	000101	38	000101
	G065 G064 G063 G062 G061 G060	000110	39	000110
	G075 G074 G073 G072 G071 G070	000111	40	000111
	G085 G084 G083 G082 G081 G080	001000	41	001000
	G095 G094 G093 G092 G091 G090	001001	42	001001
	G105 G104 G103 G102 G101 G100	001010	43	001010
	G115 G114 G113 G112 G111 G110	001011	44	001011
	G125 G124 G123 G122 G121 G120	001100	45	001100
	G135 G134 G133 G132 G131 G130	001101	46	001101
	G145 G144 G143 G142 G141 G140	001110	47	001110
	G155 G154 G153 G152 G151 G150	001111	48	001111
	G165 G164 G163 G162 G161 G160	010000	49	010000
	G175 G174 G173 G172 G171 G170	010001	50	010001
	G185 G184 G183 G182 G181 G180	010010	51	010010
	G195 G194 G193 G192 G191 G190	010011	52	010011
	G205 G204 G203 G202 G201 G200	010100	53	010100

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G215 G214 G213 G212 G211 G210	010101	54	010101
G225 G224 G223 G222 G221 G220	010110	55	010110
G235 G234 G233 G232 G231 G230	010111	56	010111
G245 G244 G243 G242 G241 G240	011000	57	011000
G255 G254 G253 G252 G251 G250	011001	58	011001
G265 G264 G263 G262 G261 G260	011010	59	011010
G275 G 274 G273 G272 G271 G270	011011	60	011011
G285 G 284 G283 G282 G281 G280	011100	61	011100
G295 G 294 G293 G292 G291 G290	011101	62	011101
G305 G 304 G303 G302 G301 G300	011110	63	011110
G315 G 314 G313 G312 G311 G310	011111	64	011111
G325 G324 G323 G322 G321 G320	100000	65	100000
G335 G334 G333 G332 G331 G330	100001	66	100001
G345 G344 G343 G342 G341 G340	100010	67	100010
G355 G354 G353 G352 G351 G350	100011	68	100011
G365 G364 G363 G362 G361 G360	100100	69	100100
G375 G374 G373 G372 G371 G370	100101	70	100101
G385 G384 G383 G382 G381 G380	100110	71	100110
G395 G394 G393 G392 G391 G390	100111	72	100111
G405 G404 G403 G402 G401 G400	101000	73	101000
G415 G414 G413 G412 G411 G410	101001	74	101001
G425 G424 G423 G422 G421 G420	101010	75	101010
G435 G434 G433 G432 G431 G430	101011	76	101011
G445 G444 G443 G442 G441 G440	101100	77	101100
G455 G454 G453 G452 G451 G450	101101	78	101101
G465 G464 G463 G462 G461 G460	101110	79	101110
G475 G474 G473 G472 G471 G470	101111	80	101111
G485 G484 G483 G482 G481 G480	110000	81	110000
G495 G494 G493 G492 G491 G490	110001	82	110001
G505 G504 G503 G502 G501 G500	110010	83	110010
G515 G514 G513 G512 G511 G510	110011	84	110011
G525 G524 G523 G522 G521 G520	110100	85	110100
G535 G534 G533 G532 G531 G530	110101	86	110101
G545 G544 G543 G542 G541 G540	110110	87	110110
G555 G554 G553 G552 G551 G550	110111	88	110111
G565 G564 G563 G562 G561 G560	111000	89	111000
G575 G574 G573 G572 G571 G570	111001	90	111001
G585 G584 G583 G582 G581 G580	111010	91	111010
G595 G594 G593 G592 G591 G590	111011	92	111011
G605 G604 G603 G602 G601 G600	111100	93	111100
G615 G614 G613 G612 G611 G610	111101	94	111101
G625 G624 G623 G622 G621 G620	111110	95	111110
G635 G634 G633 G632 G631 G630	111111	96	111111

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data
				65k Color (5-bits)
BLUE	B005 B004 B003 B002 B001 B000	000000	97	00000
	B015 B014 B013 B012 B011 B010	000010	98	00001
	B025 B024 B023 B022 B021 B020	000100	99	00010
	B035 B034 B033 B032 B031 B030	000110	100	00011
	B045 B044 B043 B042 B041 B040	001000	101	00100
	B055 B054 B053 B052 B051 B050	001010	102	00101
	B065 B064 B063 B062 B061 B060	001100	103	00110
	B075 B074 B073 B072 B071 B070	001110	104	00111
	B085 B084 B083 B082 B081 B080	010000	105	01000
	B095 B094 B093 B092 B091 B090	010010	106	01001
	B105 B104 B103 B102 B101 B100	010100	107	01010
	B115 B114 B113 B112 B111 B110	010110	108	01011
	B125 B124 B123 B122 B121 B120	011000	109	01100
	B135 B134 B133 B132 B131 B130	011010	110	01101
	B145 B144 B143 B142 B141 B140	011100	111	01110
	B155 B154 B153 B152 B151 B150	011110	112	01111
	B165 B164 B163 B162 B161 B160	100001	113	10000

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B175 B174 B173 B172 B171 B170	100011	114	10001
B185 B184 B183 B182 B181 B180	100101	115	10010
B195 B194 B193 B192 B191 B190	100111	116	10011
B205 B204 B203 B202 B201 B200	101001	117	10100
B215 B214 B213 B212 B211 B210	101011	118	10101
B225 B224 B223 B222 B221 B220	101101	119	10110
B235 B234 B233 B232 B231 B230	101111	120	10111
B245 B244 B243 B242 B241 B240	110001	121	11000
B255 B254 B253 B252 B251 B250	110011	122	11001
B265 B264 B263 B262 B261 B260	110101	123	11010
B275 B274 B273 B272 B271 B270	110111	124	11011
B285 B284 B283 B282 B281 B280	111001	125	11100
B295 B294 B293 B292 B291 B290	111011	126	11101
B305 B304 B303 B302 B301 B300	111101	127	11110
B315 B314 B313 B312 B311 B310	111111	128	11111

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9.17.2 4096 Color to 262,144 Color

Color	Look Up Table Output Frame Memory Data (6-bits)	Default value after H/W Reset	RGBSET Parameter	Look Up Table Input Data
				4k Color (4-bits)
RED	R005 R004 R003 R002 R001 R000	000000	1	0000
	R015 R014 R013 R012 R011 R010	000100	2	0001
	R025 R024 R023 R022 R021 R020	001000	3	0010
	R035 R034 R033 R032 R031 R030	001100	4	0011
	R045 R044 R043 R042 R041 R040	010001	5	0100
	R055 R054 R053 R052 R051 R050	010101	6	0101
	R065 R064 R063 R062 R061 R060	011001	7	0110
	R075 R074 R073 R072 R071 R070	011101	8	0111
	R085 R084 R083 R082 R081 R080	100010	9	1000
	R095 R094 R093 R092 R091 R090	100110	10	1001
	R105 R104 R103 R102 R101 R100	101010	11	1010
	R115 R114 R113 R112 R111 R110	101110	12	1011
	R125 R124 R123 R122 R121 R120	110011	13	1100
	R135 R134 R133 R132 R131 R130	110111	14	1101
	R145 R144 R143 R142 R141 R140	111011	15	1110
	R155 R154 R153 R152 R151 R150	111111	16	1111
	R165 R164 R163 R162 R161 R160	-----	17	Not used
	R315 R314 R313 R312 R311 R310	-----	32	
GREEN	G005 G004 G003 G002 G001 G000	000000	33	0000
	G015 G014 G013 G012 G011 G010	000100	34	0001
	G025 G024 G023 G022 G021 G020	001000	35	0010
	G035 G034 G033 G032 G031 G030	001100	36	0011
	G045 G044 G043 G042 G041 G040	010001	37	0100
	G055 G054 G053 G052 G051 G050	010101	38	0101
	G065 G064 G063 G062 G061 G060	011001	39	0110
	G075 G074 G073 G072 G071 G070	011101	40	0111
	G085 G084 G083 G082 G081 G080	100010	41	1000
	G095 G094 G093 G092 G091 G090	100110	42	1001
	G105 G104 G103 G102 G101 G100	101010	43	1010
	G115 G114 G113 G112 G111 G110	101110	44	1011
	G125 G124 G123 G122 G121 G120	110011	45	1100
	G135 G134 G133 G132 G131 G130	110111	46	1101
	G145 G144 G143 G142 G141 G140	111011	47	1110
	G155 G154 G153 G152 G151 G150	111111	48	1111
	G165 G164 G163 G162 G161 G160	-----	49	Not used
	G635 G634 G633 G632 G631 G630	-----	96	
BLUE	B005 B004 B003 B002 B001 B000	000000	97	0000
	B015 B014 B013 B012 B011 B010	000100	98	0001
	B025 B024 B023 B022 B021 B020	001000	99	0010
	B035 B034 B033 B032 B031 B030	001100	100	0011
	B045 B044 B043 B042 B041 B040	010001	101	0100
	B055 B054 B053 B052 B051 B050	010101	102	0101
	B065 B064 B063 B062 B061 B060	011001	103	0110
	B075 B074 B073 B072 B071 B070	011101	104	0111
	B085 B084 B083 B082 B081 B080	100010	105	1000
	B095 B094 B093 B092 B091 B090	100110	106	1001
	B105 B104 B103 B102 B101 B100	101010	107	1010
	B115 B114 B113 B112 B111 B110	101110	108	1011
	B125 B124 B123 B122 B121 B120	110011	109	1100
	B135 B134 B133 B132 B131 B130	110111	110	1101
	B145 B144 B143 B142 B141 B140	111011	111	1110
	B155 B154 B153 B152 B151 B150	111111	112	1111
	B165 B164 B163 B162 B161 B160	-----	113	Not used
	B315 B314 B313 B312 B311 B310	-----	128	

10 Command

10.1 System function Command List and Description

Table 10.1.1 System Function command List (1)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	10.1.10		↑	1	-	0	0	0	0	0	0	0	0	(00h)	No Operation
SWRESET	10.1.20		↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	10.1.31	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read Display ID
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	-	ID1 read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20	-	ID2 read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	-	ID3 read
RDDST	10.1.4	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read Display Status
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24	-	-
		1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON	-	-
		1	1	↑	-	VSSON	ST14	INVON	ST12	ST11	DISON	TEON	GCS2	-	-
RDDPM	10.1.5	1	1	↑	-	GCS1	GCS0	TELOM	ST4	ST3	ST2	ST1	ST0	-	-
		0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read Display Power
		1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	-	-	-	Dummy read
RDD MADCTL	10.1.6	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read Display
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	MY	MX	MV	ML	RGB	MH	-	-	-	-
RDD COLMOD	10.1.7	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read Display Pixel
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0	-	-
RDDIM	10.1.8	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read Display Image
		1	1	↑	-	-	-	-	-	-	-	-	-	-	Dummy read
		1	1	↑	-	VSSON	D6	INVON	-	-	GCS2	GCS1	GCS0	-	-
RDDSM	10.1.9	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read Display Signal
		1	1	↑	-	TEON	TELOM	-	-	-	-	-	-	-	Dummy read

"-": Don't care

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Table 10.1.2 System Function command List (2)

Instruction	Refer	D/C	WR	RDX	D17-	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
SLPIN	10.1.10	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in & booster off
SLPOUT	10.1.11	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out & booster on
PTLON	10.1.12	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	10.1.13	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	10.1.14	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	10.1.15	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	10.1.16	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)	Gamma curve select
		1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0		-
DISPOFF	10.1.17	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	10.1.18	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	10.1.19	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
		1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start: $0 \leq XS \leq X$
		1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		
		1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address end: $S \leq XE \leq X$
		1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		
RASET	10.1.20	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
		1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start: $0 \leq YS \leq Y$
		1	↑	1	-	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		
		1	↑	1	-	YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address end: $S \leq YE \leq Y$
		1	↑	1	-	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		
RAMWR	10.1.21	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
		1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0		Write data
RAMRD	10.1.22	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read
		1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	D7	D6	D5	D4	D3	D2	D1	D0		Read data

"-": Don't care

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Table 10.1.3 System Function command List (3)

Instruction	Refer	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
PTLAR	10.1.23	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial start/end address set
		1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address (0,1,2,..P)
		1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
		1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0,1,2,.., P)
		1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
TEOFF	10.1.24	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	10.1.25	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect mode set & on
		1	↑	1	-	-	-	-	-	-	-	-	TELOM		Mode1: TELOM="0" Mode2: TELOM="1"
MADCTL	10.1.26	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
		1	↑	1	-	MY	MX	MV	ML	RGB	MH	-	-		
IDMOFF	10.1.27	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	10.1.28	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on
COLMOD	10.1.29	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
		1	↑	1	-	-	-	-	-	-	IFPF2	IFPF1	IFPF0		Interface format
RDID1	10.1.30	0	↑	1	-	1	1	0	1	1	0	1	0	(DAh)	Read ID1
		1	↑	-	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	10.1.31	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
		1	↑	-	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	10.1.32	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3
		1	↑	-	-	-	-	-	-	-	-	-	-		Dummy read
		1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

"-": Don't care

Note 1: After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer "RESET TABLE" section)

Note 2: Undefined commands are treated as NOP (00 h) command.

Note 3: B0 to D9 and DA to F are for factory use of driver supplier.

Note 4: Commands 10h, 12h, 13h, 20h, 21h, 26h, 28h, 29h, 30h, 33h, 36h (ML parameter only), 37h, 38h and 39h are updated during V-sync when Module is in Sleep Out Mode to avoid abnormal visual effects. During Sleep In mode, these commands are updated immediately. Read status (09h), Read Display Power Mode (0Ah), Read Display MADCTL (0Bh), Read Display Pixel Format (0Ch), Read Display Image Mode (0Dh), Read Display Signal Mode (0Eh).

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10.1.1 NOP (00h)

NOP (No Operation)													
00H	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)
Parameter	No Parameter												
Description	This command is empty command.												

"_" Don't care

10.1.2 SWRESET (01h): Software Reset

SWRESET (Software Reset)													
01H	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(01h)
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	-
Parameter	No Parameter												
Description	<p>“-“ Don't care</p> <p>-If Software Reset is applied during Sleep In mode, it will be necessary to wait 120msec before sending next command.</p> <p>-The display module loads all default values to the registers during 120msec.</p> <p>-If Software Reset is applied during Sleep Out or Display On Mode, it will be necessary to wait 120msec before sending next command.</p>												
Flow Chart	<pre> graph TD SWRESET[SWRESET] --> DisplayBlank[Display whole blank screen] DisplayBlank --> SetCommands{Set Commands to S/W Default Value} SetCommands --> SleepInMode[Sleep In Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

10.1.3 RDDID (04h): Read Display ID

04H		RDDID (Read Display ID)																															
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)																				
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																				
2 nd parameter	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10																					
3 rd parameter	1	1	↑	-	1	ID26	ID25	ID24	ID23	ID22	ID21	ID20																					
4 th parameter	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30																					
Description	<ul style="list-style-type: none"> -This read byte returns 24-bit display identification information. -The 1st parameter is dummy data -The 2nd parameter (ID17 to ID10): LCD module's manufacturer ID. -The 3rd parameter (ID26 to ID20): LCD module/driver version ID -The 4th parameter (ID37 to UD30): LCD module/driver ID. -Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 2,3,4 of the command 04h, respectively. "-" Don't care 																																
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Status</th><th colspan="3">Default Value</th></tr> <tr> <th></th><th>ID1</th><th>ID2</th><th>ID3</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>-</td><td>NV Value</td><td>NV Value</td></tr> <tr> <td>S/W Reset</td><td>-</td><td>NV Value</td><td>NV Value</td></tr> <tr> <td>H/W Reset</td><td>-</td><td>NV Value</td><td>NV Value</td></tr> </tbody> </table>													Status	Default Value				ID1	ID2	ID3	Power On Sequence	-	NV Value	NV Value	S/W Reset	-	NV Value	NV Value	H/W Reset	-	NV Value	NV Value
Status	Default Value																																
	ID1	ID2	ID3																														
Power On Sequence	-	NV Value	NV Value																														
S/W Reset	-	NV Value	NV Value																														
H/W Reset	-	NV Value	NV Value																														
Flow Chart	<pre> graph TD Start[Read 04h] --> S_DummyClock[Dummy Clock] Start --> P_DummyRead[Dummy Read] S_DummyClock --> S_Send2[Send 2nd parameter] S_Send2 --> S_Send3[Send 3rd parameter] S_Send3 --> S_Send4[Send 4th parameter] P_DummyRead --> P_Send2[Send 2nd parameter] P_Send2 --> P_Send3[Send 3rd parameter] P_Send3 --> P_Send4[Send 4th parameter] subgraph Legend [Legend] Command[Command] Parameter[Parameter] Display[Display] Action[Action] Mode[Mode] Sequential[Sequential transfer] end </pre>																																

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10.1.4 RDDST (09h): Read Display Status

09H		RDDST (Read Display Status)												
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-	
2 nd parameter	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		
3 rd parameter	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		
4 th parameter	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		
5 th parameter	1	1	↑	-	GCS1	GCS0	TELOM	ST4	ST3	ST2	ST1	ST0		
Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description				Value								
	BSTON	Booster Voltage Status				'1' =Booster on, '0' =Booster off								
	MY	Row Address Order (MY)				'1' =Decrement, (Bottom to Top, when MADCTL (36h) D7='1') '0' =Increment, (Top to Bottom, when MADCTL (36h) D7='0')								
	MX	Column Address Order (MX)				'1' =Decrement, (Right to Left, when MADCTL (36h) D6='1') '0' =Increment, (Left to Right, when MADCTL (36h) D6='1')								
	MV	Row/Column Exchange (MV)				'1' = Row/column exchange, (when MADCTL (36h) D5='1') '0' = Normal, (when MADCTL (36h) D5='0')								
	ML	Scan Address Order (ML)				'0' =Decrement, (LCD refresh Top to Bottom, when MADCTL (36h) D4='0') '1'=Increment, (LCD refresh Bottom to Top, when MADCTL (36h) D4='1')								
	RGB	RGB/ BGR Order (RGB)				'1' =BGR, (When MADCTL (36h) D3='1') '0' =RGB, (When MADCTL (36h) D3='0')								
	MH	Horizontal Order				'0' =Decrement, (LCD refresh Left to Right, when MADCTL (36h) D2='0') '1' =Increment, (LCD refresh Right to Left, when MADCTL (36h) D2='1')								
	ST24	For Future Use				'0'								
	ST23	For Future Use				'0'								
	IFPF2	Interface Color Pixel Format Definition				"011" = 12-bit / pixel, "101" = 16-bit / pixel,								
	IFPF1					"110" = 18-bit / pixel, others are no define								
	IFPF0													
	IDMON	Idle Mode On/Off				'1' = On, "0" = Off								
	PTLON	Partial Mode On/Off				'1' = On, "0" = Off								
	SLPOUT	Sleep In/Out				'1' = Out, "0" = In								
	NORON	Display Normal Mode On/Off				'1' = Normal Display, '0' = Partial Display								
	ST15					'1' = Scroll on,"0" = Scroll off								
	ST14	Horizontal Scroll Status (Not Used)				'0'								
	INVON	Inversion Status				'1' = On, "0" = Off								
	ST12	All Pixels On (Not Used)				'0'								

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	DISON	Display On/Off	'1' = On, "0" = Off						
	TEON	Tearing effect line on/off	'1' = On, "0" = Off						
	GCSEL2	Gamma Curve Selection	"000" = GC0						
	GCSEL1		"001" = GC1						
			"010" = GC2						
	GCSEL0		"011" = GC3 "100" to "111" = Not defined						
	TELOM	Tearing effect line mode	'0' = mode1, '1' = mode2						
	ST4	For Future Use	'0'						
	ST3	For Future Use	'0'						
	ST2	For Future Use	'0'						
	ST1	For Future Use	'0'						
	ST0	For Future Use	'0'						
	"-- Don't care								
Default	Status		Default Value (ST31 to ST0)						
			ST[31-24]	ST[23-16]	ST[15-8]	ST[7-0]			
	Power On Sequence		0000-0000	0110-0001	0000-0000	0000-0000			
	S/W Reset		0xxx0xx00	0xxx-0001	0000-0000	0000-0000			
	H/W Reset		0000-0000	0110-0001	0000-0000	0000-0000			
Flow Chart	<p style="text-align: center;">Serial I/F Mode</p> <pre> graph TD A[RDDST 09h] --> B{Dummy Clock} B --> C[Send 2nd parameter] C --> D[Send 3rd parameter] D --> E[Send 4th parameter] E --> F[Send 5th parameter] </pre>								
	<p style="text-align: center;">Parallel I/F Mode</p> <pre> graph TD A[RDDST 09h] --> B{Dummy Read} B --> C[Send 2nd parameter] C --> D[Send 3rd parameter] D --> E[Send 4th parameter] E --> F[Send nth parameter] </pre>								
	<table border="1"> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>			Command	Parameter	Display	Action	Mode	Sequential transfer
Command									
Parameter									
Display									
Action									
Mode									
Sequential transfer									

10.1.5 RDDPM (0Ah): Read Display Power Mode

RDDPM (Read Display Power Mode)																																							
0AH	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																										
Inst / Para																																							
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)																										
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-																										
2 nd parameter	1	1	↑		BSTON	IDMON	PTLON	SLPON	NORON	DISON	D1	D0																											
Description	This command indicates the current status of the display as described in the table below:																																						
	“-“ Don’t care																																						
	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>BSTON</td><td>Booster Voltage Status</td><td>'1' =Booster on, '0' =Booster off</td></tr> <tr> <td>IDMON</td><td>Idle Mode On/Off</td><td>'1' = Idle Mode On, '0' = Idle Mode Off</td></tr> <tr> <td>PTLON</td><td>Partial Mode On/Off</td><td>'1' = Partial Mode On, '0' = Partial Mode Off</td></tr> <tr> <td>SLPON</td><td>Sleep In/Out</td><td>'1' = Sleep Out, '0' = Sleep In</td></tr> <tr> <td>NORON</td><td>Display Normal ModemOn/Off</td><td>'1' = Normal Display, '0' = Partial Display</td></tr> <tr> <td>DISON</td><td>Display On/Off</td><td>'1' = Display On, '0' = Display Off</td></tr> <tr> <td>D1</td><td>Not Used</td><td>'0'</td></tr> <tr> <td>D0</td><td>Not Used</td><td>'0'</td></tr> </tbody> </table>													Bit	Description	Value	BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off	IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off	PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off	SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In	NORON	Display Normal ModemOn/Off	'1' = Normal Display, '0' = Partial Display	DISON	Display On/Off	'1' = Display On, '0' = Display Off	D1	Not Used	'0'	D0	Not Used
Bit	Description	Value																																					
BSTON	Booster Voltage Status	'1' =Booster on, '0' =Booster off																																					
IDMON	Idle Mode On/Off	'1' = Idle Mode On, '0' = Idle Mode Off																																					
PTLON	Partial Mode On/Off	'1' = Partial Mode On, '0' = Partial Mode Off																																					
SLPON	Sleep In/Out	'1' = Sleep Out, '0' = Sleep In																																					
NORON	Display Normal ModemOn/Off	'1' = Normal Display, '0' = Partial Display																																					
DISON	Display On/Off	'1' = Display On, '0' = Display Off																																					
D1	Not Used	'0'																																					
D0	Not Used	'0'																																					
<table border="1"> <tr> <td>Status</td><td>Default Value (D7 to D0)</td></tr> <tr> <td>Power On Sequence</td><td>0000_1000(08h)</td></tr> <tr> <td>S/W Reset</td><td>0000_1000(08h)</td></tr> <tr> <td>H/W Reset</td><td>0000_1000(08h)</td></tr> </table>													Status	Default Value (D7 to D0)	Power On Sequence	0000_1000(08h)	S/W Reset	0000_1000(08h)	H/W Reset	0000_1000(08h)																			
Status	Default Value (D7 to D0)																																						
Power On Sequence	0000_1000(08h)																																						
S/W Reset	0000_1000(08h)																																						
H/W Reset	0000_1000(08h)																																						
<pre> graph TD Start[RDDPM 0Ah] --> S[Send 2nd parameter] Start[Parallel I/F Mode] --> P[Dummy Read] P --> S[Parallel I/F Mode] S --> End[Sequential transfer] </pre>																																							
<pre> graph TD Start[Command] --> P[Parameter] P --> D[Display] D --> A[Action] A --> M[Mode] M --> ST[Sequential transfer] </pre>																																							

10.1.6 RDDMADCTL (0Bh): Read Display MADCTL

0BH	RDDMADCTL (Read Display MADCTL)												HEX								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
RDDMADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)								
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-								
2 nd parameter	1	1	↑		MY	MX	MV	ML	RGB	MH	D1	D0									
Description	This command indicates the current status of the display as described in the table below:																				
	"-“ Don’t care																				
	Bit	Description				Value															
	MX	Column Address Order				'1' = Right to Left (When MADCTL B6='1') '0' = Left to Right (When MADCTL B6='0')															
	MY	Row Address Order				'1' = Bottom to Top (When MADCTL B7='1') '0' = Top to Bottom (When MADCTL B7='0')															
	MV	Row/Column Order (MV)				'1' = Row/column exchange (MV=1) '0' = Normal (MV=0)															
	ML	Vertical Refresh Order				'1' =LCD Refresh Bottom to Top '0' =LCD Refresh Top to Bottom															
	RGB	RGB/BGR Order				'1' =BGR, "0"=RGB															
	MH	Horizontal Refresh Order				LCD horizontal refresh direction control '0' = LCD horizontal refresh Left to right '1' = LCD horizontal refresh right to left															
Default	D1	Not Used				'0'															
	D0	Not Used				'0'															
Flow Chart	<table border="1"> <tr> <td>Status</td> <td>Default Value (D7 to D0)</td> </tr> <tr> <td>Power On Sequence</td> <td>0000_0000 (00h)</td> </tr> <tr> <td>S/W Reset</td> <td>No change</td> </tr> <tr> <td>H/W Reset</td> <td>0000_0000 (00h)</td> </tr> </table>												Status	Default Value (D7 to D0)	Power On Sequence	0000_0000 (00h)	S/W Reset	No change	H/W Reset	0000_0000 (00h)	
Status	Default Value (D7 to D0)																				
Power On Sequence	0000_0000 (00h)																				
S/W Reset	No change																				
H/W Reset	0000_0000 (00h)																				
<p>Serial I/F Mode</p> <pre> graph TD Start[RDDMADCTL 0Bh] --> Send2nd[Send 2nd parameter] </pre> <p>Parallel I/F Mode</p> <pre> graph TD Start[RDDMADCTL 0Bh] --> DummyRead[Dummy Read] DummyRead --> Send2nd[Send 2nd parameter] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																					

10.1.7 RDDCOLMOD (0Ch): Read Display Pixel Format

RDDCOLMOD (Read Display Pixel Format)														
0Ch	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Inst / Para														
RDDCOLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-	
2 nd parameter	1	1	↑	-	0	0	0	0	-	IFPF2	IFPF1	IFPF0		
Description	This command indicates the current status of the display as described in the table below:													
	IFPF[2:0]		MCU Interface Color Format											
	011		12-bit/pixel											
	101		16-bit/pixel											
	110		18-bit/pixel											
	111		No used											
Others are no define and invalid														
"-“ Don't care														
Default	Status				Default Value									
					IFPF[2:0]									
	Power On Sequence				0110 (18 bits/pixel)									
	S/W Reset				No Change									
	H/W Reset				0110 (18 bits/pixel)									
Flow Chart	<pre> graph TD Start((RDDCOLMOD 0Ch)) --> Serial[/Send 2nd parameter/] Start --> Parallel[/Dummy Read/] Serial --> End[/Send 2nd parameter/] Parallel --> End </pre> <p>The flowchart illustrates the execution of the RDDCOLMOD command. In Serial I/F Mode, the process starts with the command (RDDCOLMOD 0Ch), followed by sending the 2nd parameter, and ends with another send of the 2nd parameter. In Parallel I/F Mode, the process starts with the command (RDDCOLMOD 0Ch), followed by a dummy read from the display, and ends with sending the 2nd parameter.</p>													
	<table border="1"> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table> <p>The legend defines the symbols used in the flowchart: Command (rectangle), Parameter (parallelogram), Display (oval), Action (hexagon), Mode (elliptical), and Sequential transfer (wavy line).</p>		Command	Parameter	Display	Action	Mode	Sequential transfer						
Command														
Parameter														
Display														
Action														
Mode														
Sequential transfer														

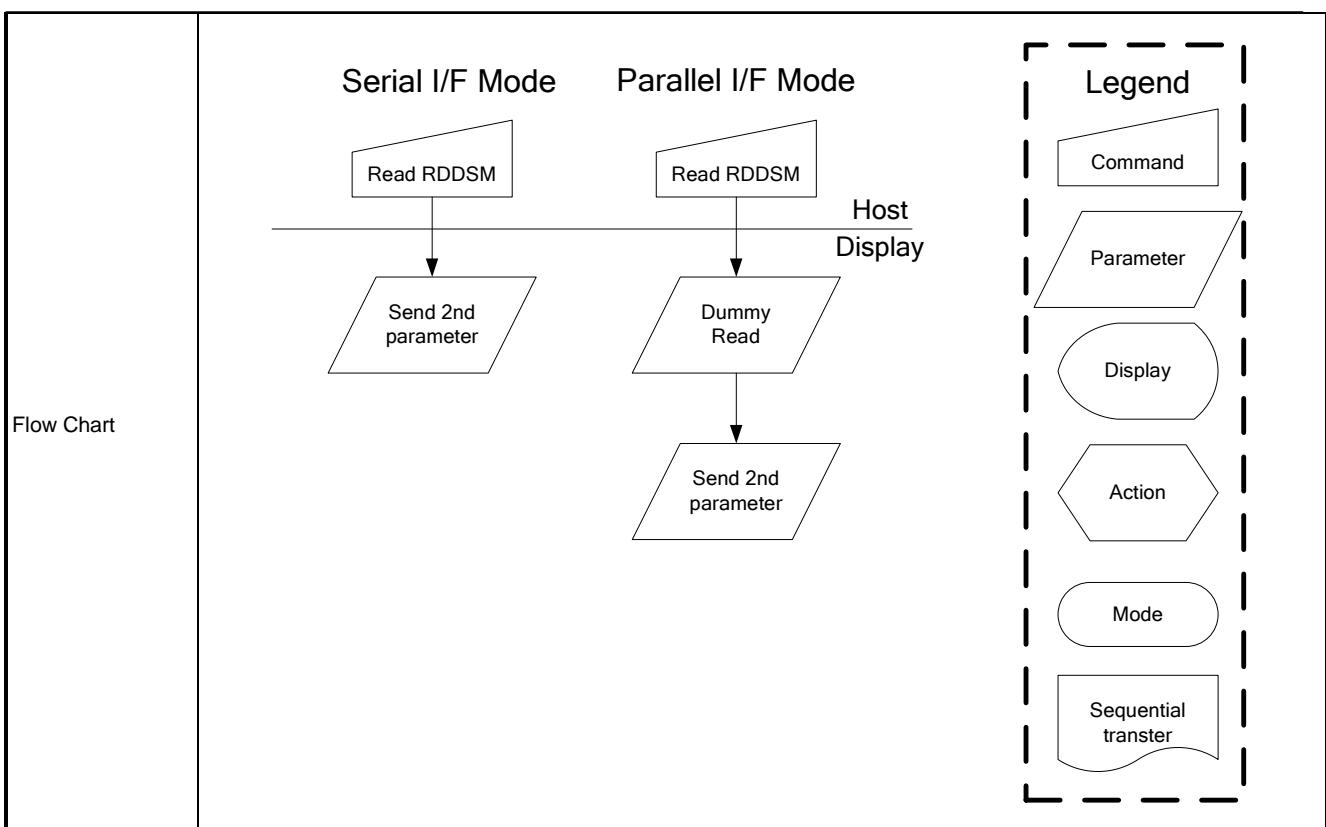
10.1.8 RDDIM (0Dh): Read Display Image Mode

RDDIM (0Dh): Read Display Image Mode																				
0DH	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(0Dh)							
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)							
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-							
2 nd parameter	1	1	↑	-	VSSON	D6	INVON	D4	D3	GCS2	GCS1	GCS0								
Description	This command indicates the current status of the display as described in the table below: “-” Don't care																			
	Bit	Description			Value															
	VSSON	Reversed			“0”															
	D6	Reversed			“0”															
	INVON	Inversion On/Off			“1” = Inversion is On, “0” = Inversion is Off															
	D4	All Pixels On			“0” (Not used)															
	D3	All Pixels Off			“0” (Not used)															
	GCS2				“000” = GC0, “001” = GC1, “010” = GC2, “011” = GC3, “100” to “111” = Not defined															
Default	Status	Default Value(D7 to D0)																		
	Power On Sequence	0000_0000 (00h)																		
	S/W Reset	0000_0000 (00h)																		
	H/W Reset	0000_0000 (00h)																		
Flow Chart	<pre> graph TD Start((RDDIM 0Dh)) --> SIF[Serial I/F Mode] Start --> PIF[Parallel I/F Mode] SIF --> S2P{Send 2nd parameter} PIF --> DR{Dummy Read} DR --> S2P S2P --> End(((Sequential transfer))) </pre>																			
	<table border="1"> <tr> <td>Legend</td> </tr> <tr> <td>Command</td> </tr> <tr> <td>Parameter</td> </tr> <tr> <td>Display</td> </tr> <tr> <td>Action</td> </tr> <tr> <td>Mode</td> </tr> <tr> <td>Sequential transfer</td> </tr> </table>		Legend	Command	Parameter	Display	Action	Mode	Sequential transfer											
Legend																				
Command																				
Parameter																				
Display																				
Action																				
Mode																				
Sequential transfer																				

10.1.9 RDDSM (0Eh): Read Display Signal Mode

RDDSM (0Eh): Read Display Signal Mode																		
0EH	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX					
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(0Eh)					
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)					
1 st parameter	1	1	↑	-	-	-	-	-	-	-	-	-	-					
2 nd parameter	1	1	↑	-	TEON	TELOM	D5	D4	D3	D2	D1	D0						
Description	This command indicates the current status of the display as described in the table below: “-“ Don't care																	
	Bit	Description						Value										
	TEON	Tearing Effect Line On/Off						“1” = On, “0” = Off										
	TELOM	Tearing effect line mode						“1” = mode2, “0” = mode1										
	D5	Not Used						“1” = On, “0” = Off										
	D4	Not Used						“1” = On, “0” = Off										
	D3	Not Used						“1” = On, “0” = Off										
	D2	Not Used						“1” = On, “0” = Off										
	D1	Not Used						“1” = On, “0” = Off										
	D0	Not Used						“1” = On, “0” = Off										
Default	Status				Default Value(D7~D0)													
	Power On Sequence				0000_0000 (00h)													
	S/W Reset				0000_0000 (00h)													
	H/W Reset				0000_0000 (00h)													

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10.1.10 SLPIN (10h): Sleep In

SLPIN (Sleep In)																				
10H	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(10h)							
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)							
Parameter	No Parameter												-							
Description	<p>-This command causes the LCD module to enter the minimum power consumption mode.</p> <p>-In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.</p>																			
Restriction	<p>-This command has no effect when module is already in Sleep In mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).</p> <p>-When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.</p>																			
Default	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </table>												Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode
Status	Default Value																			
Power On Sequence	Sleep in mode																			
S/W Reset	Sleep in mode																			
H/W Reset	Sleep in mode																			
Flow Chart	<p>The flowchart shows the sequence of events for the SLPIN command:</p> <ul style="list-style-type: none"> The process begins with the SLPIN command. It then displays a Display whole blank screen (Automatic No effect to DISP ON/OFF Commands). Finally, it performs Drain Charge From LCD Panel. <p>Legend:</p> <ul style="list-style-type: none"> Command: Rectangle Parameter: Parallelogram Display: Oval Action: Hexagon Mode: Hexagon Sequential transfer: Wavy line 																			

10.1.11 SLPOUT (11h): Sleep Out

SLPOUT (Sleep Out)																					
11H	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(11h)								
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	-								
Parameter	No Parameter																				
Description	<p>-This command turns off sleep mode.</p> <p>-In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started.</p>																				
Restriction	<p>-This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h).</p> <p>-When IC is in Sleep In mode, it is necessary to wait 120msec before sending next command because of the stabilization timing for the supply voltages and clock circuits.</p> <p>-When IC is in Sleep Out or Display On mode, it is necessary to wait 120msec before sending next command due to the download of default value of registers and the execution of self-diagnostic function.</p>																				
Default	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>Power On Sequence</td> <td>Sleep in mode</td> </tr> <tr> <td>S/W Reset</td> <td>Sleep in mode</td> </tr> <tr> <td>H/W Reset</td> <td>Sleep in mode</td> </tr> </table>													Status	Default Value	Power On Sequence	Sleep in mode	S/W Reset	Sleep in mode	H/W Reset	Sleep in mode
Status	Default Value																				
Power On Sequence	Sleep in mode																				
S/W Reset	Sleep in mode																				
H/W Reset	Sleep in mode																				
Flow Chart	<pre> graph TD SLPOUT[SLPOUT] --> StartOsc{Start Internal Oscillator} StartOsc --> StartDCDC{Start up DC:DC Converter} StartDCDC --> ChargeOffset{Charge Offset voltage for LCD Panel} ChargeOffset --> Parallel[Parallel] Parallel --> SleepOut{Sleep Out mode} subgraph Parallel [Parallel] direction TB P1((Display whole blank screen for 2 frames Automatic No effect to DISP ON/OFF Commands)) --> P2((Display Memory contents In accordance with the current command table settings)) P2 --> SleepOut end </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																				

10.1.12 PTLON (12h): Partial Display Mode On

12H	PTLON (12h): Partial Display Mode On																			
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0								
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0								
Parameter	No Parameter																			
Description	<p>-This command turns on Partial mode. The partial mode window is described by the Partial Area command (30h)</p> <p>-To leave Partial mode, the Normal Display Mode On command (13h) should be written.</p> <p>"-" Don't care</p>																			
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></tbody></table>												Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On
Status	Default Value																			
Power On Sequence	Normal Mode On																			
S/W Reset	Normal Mode On																			
H/W Reset	Normal Mode On																			
Flow Chart	See Partial Area (30h)																			

10.1.13 NORON (13h): Normal Display Mode On

13H	NORON (Normal Display Mode On)												HEX							
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(13h)							
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)							
Parameter	No Parameter												-							
Description	<p>-This command returns the display to normal mode.</p> <p>-Normal display mode on means Partial mode off.</p> <p>-Exit from NORON by the Partial mode On command (12h)</p> <p>"-" Don't care</p>																			
Default	<table border="1"><thead><tr><th>Status</th><th>Default Value</th></tr></thead><tbody><tr><td>Power On Sequence</td><td>Normal Mode On</td></tr><tr><td>S/W Reset</td><td>Normal Mode On</td></tr><tr><td>H/W Reset</td><td>Normal Mode On</td></tr></tbody></table>												Status	Default Value	Power On Sequence	Normal Mode On	S/W Reset	Normal Mode On	H/W Reset	Normal Mode On
Status	Default Value																			
Power On Sequence	Normal Mode On																			
S/W Reset	Normal Mode On																			
H/W Reset	Normal Mode On																			
Flow Chart	See Partial Area Definition Descriptions for details of when to use this command																			

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10.1.14 INVOFF (20h): Display Inversion Off

10.1.15 INVON (21h): Display Inversion On

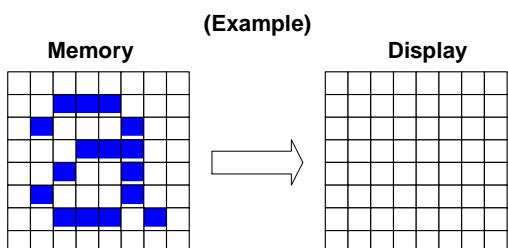
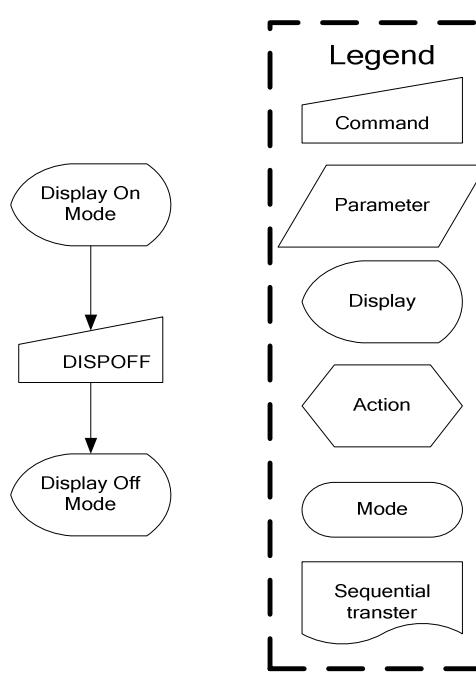
IVNOFF (Display Inversion On)																				
21H	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Inst / Para	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)							
Parameter	No Parameter												-							
Description	<p>-This command is used to enter into display inversion mode</p> <p>-To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.</p> <p>"-" Don't care</p> <p>(Example)</p>																			
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>Display Inversion off</td></tr> <tr> <td>S/W Reset</td><td>Display Inversion off</td></tr> <tr> <td>H/W Reset</td><td>Display Inversion off</td></tr> </tbody> </table>												Status	Default Value	Power On Sequence	Display Inversion off	S/W Reset	Display Inversion off	H/W Reset	Display Inversion off
Status	Default Value																			
Power On Sequence	Display Inversion off																			
S/W Reset	Display Inversion off																			
H/W Reset	Display Inversion off																			
Flow Chart	<pre> graph TD A((Display Inversion OFF Mode)) --> B[INVON (21h)] B --> C((Display Inversion ON Mode)) style B fill:#fff,stroke:#000,stroke-width:1px </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																			

ST7735

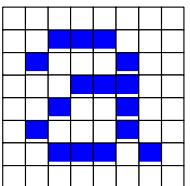
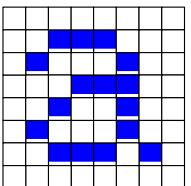
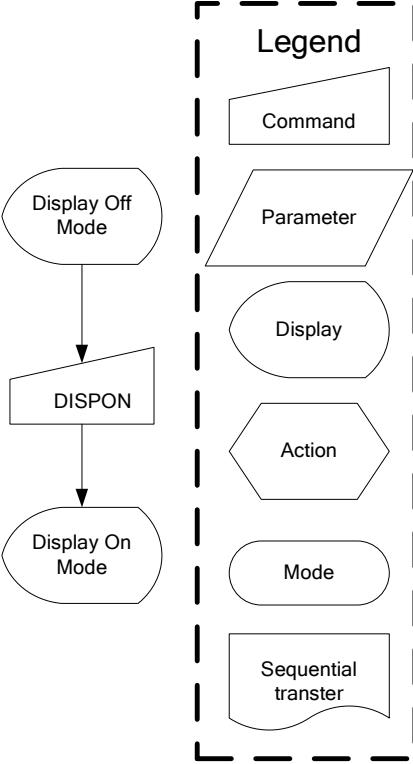
10.1.16 GAMSET (26h): Gamma Set

26H		GAMSET (Gamma Set)																																			
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
GAMSET	0	↑	1	-	0	0	1	0	0	1	1	0	(26h)																								
Parameter	1	↑	1	-	-	-	-	-	GC3	GC2	GC1	GC0																									
Description	<p>-This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.</p> <table border="1"> <thead> <tr> <th>GC [7:0]</th><th>Parameter</th><th>Curve Selected</th><th></th></tr> </thead> <tbody> <tr> <td></td><td></td><td>GS=1</td><td>GS=0</td></tr> <tr> <td>01h</td><td>GC0</td><td>Gamma Curve 1 (G2.2)</td><td>Gamma Curve 1 (G1.0)</td></tr> <tr> <td>02h</td><td>GC1</td><td>Gamma Curve 2 (G1.8)</td><td>Gamma Curve 2 (G2.5)</td></tr> <tr> <td>04h</td><td>GC2</td><td>Gamma Curve 3 (G2.5)</td><td>Gamma Curve 3 (G2.2)</td></tr> <tr> <td>08h</td><td>GC3</td><td>Gamma Curve 4 (G1.0)</td><td>Gamma Curve 4 (G1.8)</td></tr> </tbody> </table> <p>Note: All other values are undefined.</p>												GC [7:0]	Parameter	Curve Selected				GS=1	GS=0	01h	GC0	Gamma Curve 1 (G2.2)	Gamma Curve 1 (G1.0)	02h	GC1	Gamma Curve 2 (G1.8)	Gamma Curve 2 (G2.5)	04h	GC2	Gamma Curve 3 (G2.5)	Gamma Curve 3 (G2.2)	08h	GC3	Gamma Curve 4 (G1.0)	Gamma Curve 4 (G1.8)	
GC [7:0]	Parameter	Curve Selected																																			
		GS=1	GS=0																																		
01h	GC0	Gamma Curve 1 (G2.2)	Gamma Curve 1 (G1.0)																																		
02h	GC1	Gamma Curve 2 (G1.8)	Gamma Curve 2 (G2.5)																																		
04h	GC2	Gamma Curve 3 (G2.5)	Gamma Curve 3 (G2.2)																																		
08h	GC3	Gamma Curve 4 (G1.0)	Gamma Curve 4 (G1.8)																																		
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>01h</td></tr> <tr> <td>S/W Reset</td><td>01h</td></tr> <tr> <td>H/W Reset</td><td>01h</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	01h	S/W Reset	01h	H/W Reset	01h																
Status	Default Value																																				
Power On Sequence	01h																																				
S/W Reset	01h																																				
H/W Reset	01h																																				
Flow Chart	<pre> graph TD Command[GAMSET (26h)] --> Parameter{1st parameter: GC[7:0]} Parameter --> Action{New Gamma Curve Loaded} </pre> <p>The flowchart illustrates the sequence of events for the GAMSET command. It begins with the 'Command' (GAMSET (26h)), followed by the 'Parameter' (GC[7:0]). This leads to the 'Action' (New Gamma Curve Loaded).</p> <p>A legend on the right side defines the symbols used in the flowchart:</p> <ul style="list-style-type: none"> Legend: A dashed rectangular border. Command: A parallelogram shape. Parameter: A rounded rectangle. Display: An oval shape. Action: A hexagon shape. Mode: An oval shape. Sequential transfer: A rounded rectangle with a wavy bottom edge. 																																				

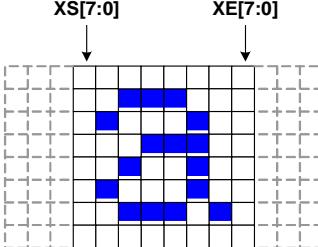
10.1.17 DISPOFF (28h): Display Off

DISPOFF (Display Off)																				
28H	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	(28h)							
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)							
Parameter	No Parameter												-							
Description	<ul style="list-style-type: none"> - This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. - This command makes no change of contents of frame memory. - This command does not change any other status. - There will be no abnormal visible effect on the display. - Exit from this command by Display On (29h) - The delay time between DISPON and DISPOFF needs 120ms at least. <p style="text-align: center;">(Example)</p>  <p>Note1: Complete 1 frame display (ex: continue 2-falling edges of VS) Note2: Please use command 28h (display off) combined with command 10h (sleep in) to make module into display off status. Please check the application note of ST7735 when using display off function.</p>																			
Default	<table border="1"> <tr> <td>Status</td> <td>Default Value</td> </tr> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </table>												Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																			
Power On Sequence	Display off																			
S/W Reset	Display off																			
H/W Reset	Display off																			
Flow Chart	 <pre> graph TD A([Display On Mode]) --> B[DISPOFF] B --> C([Display Off Mode]) </pre>																			

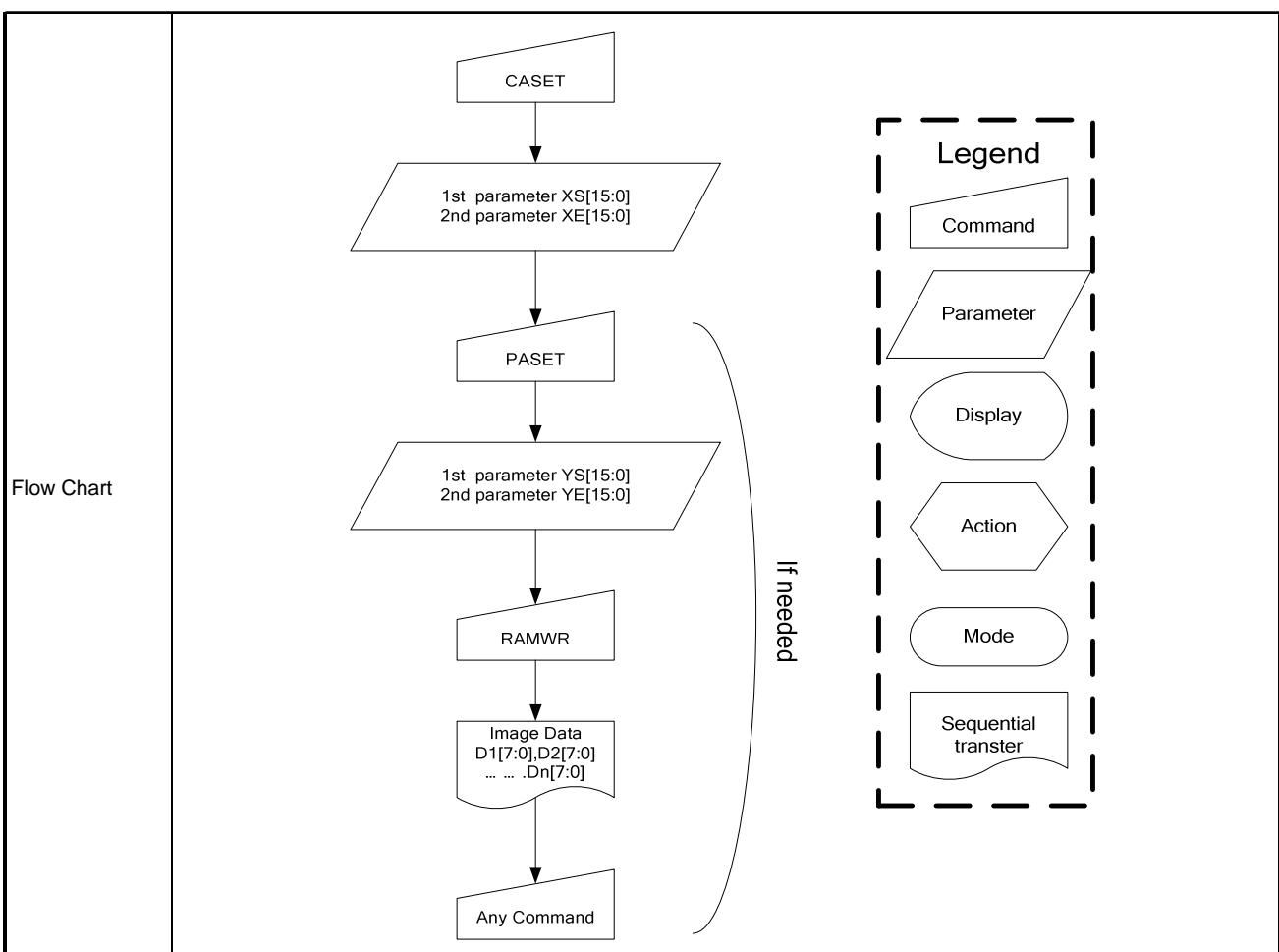
10.1.18 DISPON (29h): Display On

DISPON (Display On)																					
29H	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)								
Parameter	No Parameter																				
<ul style="list-style-type: none"> - This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. - This command makes no change of contents of frame memory. - This command does not change any other status. - The delay time between DISPON and DISPOFF needs 120ms at least 																					
Description	<p style="text-align: center;">(Example)</p> <div style="display: flex; justify-content: space-around;"> <div style="text-align: center;"> Memory  </div> <div style="text-align: center;">  </div> <div style="text-align: center;"> Display  </div> </div>																				
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display off</td> </tr> <tr> <td>S/W Reset</td> <td>Display off</td> </tr> <tr> <td>H/W Reset</td> <td>Display off</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display off	S/W Reset	Display off	H/W Reset	Display off
Status	Default Value																				
Power On Sequence	Display off																				
S/W Reset	Display off																				
H/W Reset	Display off																				
Flow Chart	 <pre> graph TD A([Display Off Mode]) --> B[/DISPON/] B --> C([Display On Mode]) </pre>																				

10.1.19 CASET (2Ah): Column Address Set

2AH		CASET(Column Address Set)...																																													
Inst / Para	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																		
CASET(2Ah)	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)																																		
1 st parameter	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8																																			
2 nd parameter	1	↑	1	-	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0																																			
3 rd parameter	1	↑	1	-	XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8																																			
4 th parameter	1	↑	1	-	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0																																			
Description	<p>-The value of XS [7:0] and XE [7:0] are referred when RAMWR command comes.</p> <p>-Each value represents one column line in the Frame Memory.</p> 																																														
Restriction	<p>XS [15:0] always must be equal to or less than XE [15:0]</p> <p>When XS [15:0] or XE [15:0] is greater than maximum address like below, data of out of range will be ignored.</p> <ol style="list-style-type: none"> 1. 128X160 memory base (GM = '011') (Parameter range: 0 < XS [15:0] < XE [15:0] < 127 (007Fh)): MV="0" (Parameter range: 0 < XS [15:0] < XE [15:0] < 159 (009Fh)): MV="1" 2. 132X162 memory base (GM = '000') (Parameter range: 0 < XS [15:0] < XE [15:0] < 131 (0083h)): MV="0" (Parameter range: 0 < XS [15:0] < XE [15:0] < 161 (00A1h)): MV="1" 																																														
Default	<table border="1"> <thead> <tr> <th rowspan="2">GM Status</th> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>XS [7:0]</th> <th>XE [7:0] (MV='0')</th> <th>XE [7:0] (MV='1')</th> </tr> </thead> <tbody> <tr> <td rowspan="3">GM='011' (128x160 memory base)</td> <td>Power On Sequence</td> <td>0000h</td> <td colspan="2">007Fh (127)</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> <td>007Fh (127)</td> <td>009Fh (159)</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> <td colspan="2">007Fh (127)</td> </tr> <tr> <td rowspan="3">GM='000' (132x162 memory base)</td> <td>Power On Sequence</td> <td>0000h</td> <td colspan="2">0083h (131)</td> </tr> <tr> <td>S/W Reset</td> <td>0000h</td> <td>0083h (131)</td> <td>00A1h (161)</td> </tr> <tr> <td>H/W Reset</td> <td>0000h</td> <td colspan="2">0083h (131)</td> </tr> </tbody> </table>													GM Status	Status	Default Value			XS [7:0]	XE [7:0] (MV='0')	XE [7:0] (MV='1')	GM='011' (128x160 memory base)	Power On Sequence	0000h	007Fh (127)		S/W Reset	0000h	007Fh (127)	009Fh (159)	H/W Reset	0000h	007Fh (127)		GM='000' (132x162 memory base)	Power On Sequence	0000h	0083h (131)		S/W Reset	0000h	0083h (131)	00A1h (161)	H/W Reset	0000h	0083h (131)	
GM Status	Status	Default Value																																													
		XS [7:0]	XE [7:0] (MV='0')	XE [7:0] (MV='1')																																											
GM='011' (128x160 memory base)	Power On Sequence	0000h	007Fh (127)																																												
	S/W Reset	0000h	007Fh (127)	009Fh (159)																																											
	H/W Reset	0000h	007Fh (127)																																												
GM='000' (132x162 memory base)	Power On Sequence	0000h	0083h (131)																																												
	S/W Reset	0000h	0083h (131)	00A1h (161)																																											
	H/W Reset	0000h	0083h (131)																																												

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9.3. Hoja de datos de CFAP128296C0-0290



ePAPER DISPLAY MODULE DATASHEET



Datasheet Release 2017-08-14
for
CFAP128296C0-0290

Crystalfontz America, Inc.

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1. General Information

Datasheet Revision History

Datasheet Release Date: **2017-08-14**

Datasheet for the CFAP128296C0-0290 ePaper display module.

Product Change Notifications

You can check for or subscribe to [Part Change Notices](#) for this display module on our website.

Variations

Slight variations between lots are normal (e.g., contrast, color, or intensity).

Volatility

This display module has volatile memory.

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2. Description Overview

This ePaper display is a TFT active matrix electrophoretic display with interface and a reference system design. The 2.9" active area contains 296x128 pixels and has 1-bit white/black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

3. Features

- High contrast
- High reflectance
- Ultra-wide viewing angle
- Ultra-low power consumption
- Pure reflective mode
- Bi-Stable Display
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On-chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating V_{COM}, Gate and source driving voltage
- I²C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 280um

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	inch	
Display Resolution	296 × 128	pixel	dpi: 112
Active Area	66.9 × 29.06	mm	
Pixel Pitch	0.227 × 0.226	mm	
Pixel Configuration	Square		
Outline Dimension	79.0 (H) × 36.7 (W) × 1.18 (D)	mm	
Weight (Typical)	4±0.5	g	

5. Input/Output Terminals

5.1. Pin Out List

Pin #	Type	Single	Description	Remark
1	-	NC	No Connection and Do Not Connect with Other NC Pins	Keep Open
2	O	GDR	N-Channel MOSFET Gate Drive Control	-
3	O	RESE	Current Sense Input for the Control Loop	-
4	C	VGL	Negative Gate Driving Voltage	-
5	C	VGH	Positive Gate Driving Voltage	-
6	O	TSCL	I ² C Interface to Digital Temperature Sensor Clock Pin	-
7	I/O	TSDA	I ² C Interface to Digital Temperature Sensor Data Pin	-
8	I	BS1	Bus Selection Pin	Note 5-5
9	O	BUSY	Busy State Output Pin	Note 5-4
10	I	RES #	Reset	Note 5-3
11	I	D/C #	Data /Command Control Pin	Note 5-2
12	I	CS #	Chip Select Input Pin	Note 5-1
13	I/O	D0	Serial Clock Pin (SPI)	-
14	I/O	D1	Serial Data Pin (SPI)	-
15	I	VDDIO	Power for Interface Logic Pins	-
16	I	VCI	Power Supply Pin for the Chip	-
17	-	VSS	Ground	-
18	C	VDD	Core Logic Power Pin	-
19	C	VPP	Power Supply for OTP Programming	-
20	C	VSH	Positive Source Driving Voltage	-
21	C	PREVGH	Power Supply Pin for VGH and VSH	-
22	C	VSL	Negative Source Driving Voltage	-
23	C	PREVGL	Power Supply Pin for VCOM, VGL, and VSL	-
24	C	VCOM	VCOM Driving Voltage	-

Note (5-1): This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note (5-2): This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note (5-3): This pin (RES#) is reset signal input. The Reset is active Low.

Note (5-4): This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and no commands should be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting Display Waveform; or
- Programming with OTP
- Communicating with Digital Temperature Sensor

Note (5-5): This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is "Low", 4-line SPI is selected. When it is "High", 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Bus Interface Selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

6. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD, SHL,SHD_N,RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN,VDG_EN	03h
		0	1	-	-	-	-	-	#	#	#	VCOM_HV,VGHL_LV[1:0]	00h
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OF	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
9	Display Start Transmission 1(DTM1, white/black data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W Pixel Data (160x296)	10h
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00h
		0	1
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00h
10	Data Stop	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-		00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	VCOM LUT (LUTC) (45-byte command, structure of bytes 2~7 repeated)	0	0	0	0	1	0	0	0	0	0		20h
13	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
14	B2W LUT (LUTBW / LUTR) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	1	0		22h
15	W2B LUT (LUTWB / LUTW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	1	1		23h
16	B2B LUT (LUTBB / LUTB) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	0		24h
17	PLL Control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0],N[2:0]	3Ch
18	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	LM[10:3]/TSR[7:0]	00h
		1	1	#	#	#	-	-	-	-	-	LM[2:0]/-	00h
19	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	#	#	#	#	TSE,TO[3:0]	00h
20	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h
21	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
22	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[1:0],DDX[1:0],CDI[3:0]	D7h
23	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	-	-	-	-	-	-	#	LPD	01h
24	TCON Setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
25	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00h
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
26	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	#	#	#	#	#	#	#	PTL_FLAG,I ² C_BUSY,DATA_FLAG,PON,POF,BUSY	02h
27	Auto Measurement V _{COM}	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV, AMVE	10h
28	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00h
29	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00h
30	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90h
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00h
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07h
		0	1	-	-	-	-	-	-	-	#	VRST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	-	#	VRED[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	-	#	PT_SCAN	01h
31	Partial In (PTIN)		0	0	1	0	0	1	0	0	0	1	91h
32	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
33	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0		A0h
		0	1	1	0	1	0	0	1	0	1	Check Code = A5h	A5h
34	Active Programming (APG)	0	0	1	0	1	0	0	0	0	1		A1h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
35	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	-	-	-	-	-	-	-	-	Read Dummy	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = 000h	N/A
		1	1	N/A
		1	1	#	#	#	#	#	#	#	#	Data of Address = n	N/A
36	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0],SD_W[3:0]	00h

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the Panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	REG_EN	BWR	UD	SHL	SHD_N	RST_N

RES [1:0]: Display Resolution setting (source x gate)

- 00b: 96x230 (Default) Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.
- 01b: 96x252. Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.
- 10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.
- 11b: 160x296 Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.

REG_EN: LUT selection

- 0: LUT from OTP. (Default)
- 1: LUT from register.

BWR: Black / White / Red

- 0: Pixel with B/W/Red. (Default)
- 1: Pixel with B/W.

UD: Gate Scan Direction

- 0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 → ... → G0
- 1: Scan up. (Default) First line to last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift direction

- 0: Shift left. First data to last data: Sn-1 → Sn-2 → Sn-3 → ... → S0
- 1: Shift right. (Default) First data to last data: S0 → S1 → S2 → ... → Sn-1

SHD_N: Booster Switch

- 0: Booster OFF, register data are kept and SEG/BG/VCOM are kept 0V or floating.
- 1: Booster ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD_N may have two conditions: 0v or floating.

RST_N: Soft Reset

- 1: No effect (Default). Booster OFF, register data are set to their default values, and SEG/BG/VCOM: 0V

When RST_N become LOW, the driver will be reset; all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1		
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN		
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]			
	0	1	-	-	VDH[5:0]							
	0	1	-	-	VDL[5:0]							
	0	1	-	-	VDHR[5:0]							

VDS_EN: Source power selection

- 0: External source power from VDH/VDL pins
- 1: Internal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection

- 0: External gate power from VGH/VGL pins

1: Internal DC/DC function for generating VGH/VGL

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC

1: VCOML=VGH, VCOML=VGL

VGHL_LV [1:0]: VGH / VGL Voltage Level selection

VGHL_LV	VGHL voltage level
00(Default)	VGH=16V, VGL= -16V
01	VGH=15V, VGL= -15V
10	VGH=14V, VGL= -14V
11	VGH=13V, VGL= -13V

VDH [5:0]: Internal VDH power selection for B/W pixel. (Default value: 100110b)

VDH	VDH_V	VDH	VDH_V
000000	2.4V
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

VDL [5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-2.4V
000001	-2.6V	100110	-10.0V
000010	-2.8V	100111	-10.2V
000011	-3.0V	101000	-10.4V
000100	-3.2V	101001	-10.6V
000101	-3.4V	101010	-10.8V
000110	-3.6V	101011	-11.0V
000111	-3.8V	(others)	-11.0V

VDHR [5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR	VDHR_V	VDHR	VDHR_V
000000	2.4V
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

(3) Power OFF (PWR) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off following the Power Off Sequence. This command will turn off charge pump, T-con, source driver, gate driver, V_{COM}, and temperature sensor, but register data will be kept until VDD becomes OFF. Source Driver output and V_{COM} will remain as previous condition, which may have 2 conditions: 0V or floating.

(4) Power off sequence setting (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]	-	-	-	-	-

T_VDS_OFF [1:0]: Power OFF Sequence of VDH and VDL.

00b: 1frame (Default) 01b: 2 frames 10b: 3frames 11b:4 frame

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence. Refer to the Power ON Sequence section. In the sequence, temperature sensor will be activated for one-time sensing before enabling booster.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Measure	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting Data Transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA 7	BT_PHA 6	BT_PHA 5	BT_PHA 4	BT_PHA 3	BT_PHA 2	BT_PHA 1	BT_PHA 0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA [7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA [5:3]: Driving strength of phase A.

000b: strength 001b: strength 2 **010b: strength 3**

011b: strength 4 100b: strength 5 101b: strength 6

110b: strength 7 111b: strength 8 (strongest)

BTPHA [2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS

100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB [7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB [5:3]: Driving strength of phase B
 000b: strength 1 001b: strength 2 **010b: strength 3**
 011b: strength 4 100b: strength 5 101b: strength 6
 110b: strength 7 111b: strength 8 (strongest)

BTPHB [2:0]: Minimum OFF time setting of GDR in phase B
 000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC [5:3]: Driving strength of phase C
 000b: strength 1 001b: strength 2 **010b: strength 3**
 011b: strength 4 100b: strength 5 101b: strength 6
 110b: strength 7 111b: strength 8 (strongest)

BTPHC [2:0]: Minimum OFF time setting of GDR in phase C
 000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS
 100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	1	1
Deep Sleep	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel 1	Pixel 2	Pixel 3	Pixel 4	Pixel 5	Pixel 6	Pixel 7	Pixel 8
	0	1
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and writes them into SRAM. To complete data transmission, command DSP (Data Transmission Stop) must be issued. Then the chip will start to send data/V_{COM} for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping Data Transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY signal will become “0”.

(11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/V_{COM}) according to SRAM data and LUT. After Display Refresh command, BUSY signal will become "0" and the refreshing of panel starts.

(12) VCOM LUT (LUTC) (R20H)

This command builds Look-up Table for V_{COM}

(13) W2W LUT (LUTWW) (R21H)

This command builds Look-up Table for White-to-White

(14) B2W LUT (LUTBW/LUTR) (R22H)

This command builds Look-up Table for Black-to-White

(15) W2B LUT (LUTWB/LUTW) (R23H)

This command builds Look-up Table for White - to- Black

(16) B2B LUT (LUTBB / LUTB) (R24H)

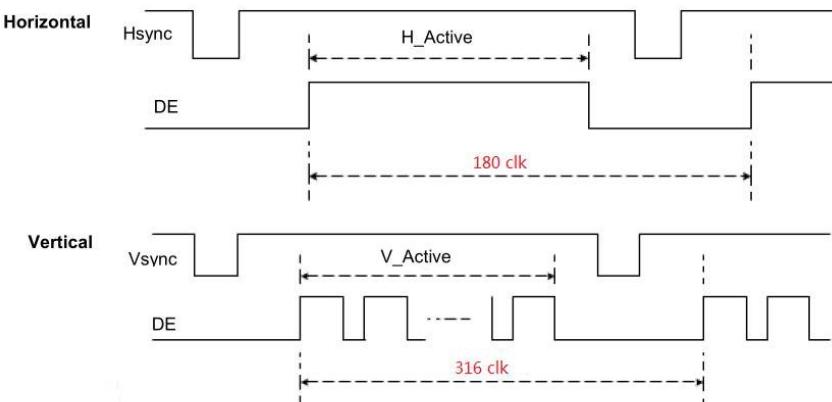
This command builds Look-up Table for Black - to- Black

(17) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]				N[2:0]	

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame Rate									
1	1	29 Hz	3	1	86 Hz	5	1	150 Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	72 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	7 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	6 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	5 Hz		6	14 Hz		6	24 Hz		6	33Hz
	7	4 Hz		7	12Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



(18) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS [7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D [10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS [7:0]/D [10:3]	Temperature (°C)	TS [7:0]/D [10:3]	Temperature (°C)	TS [7:0]/D [10:3]	Temperature (°C)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

(19) Temperature Sensor Enable (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature Sensor/Offset	0	0	0	1	0	0	0	0	0	1
	0	1	TSE	-	-	-				TO[3:0]

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default)

1: Disable; using external sensor.

TO [3:0]: Temperature offset.

TO [3:0]	Calculation	TO [3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
...
0110	6	1110	-2
0111	7	1111	-1

(20) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1								WATTR[7:0]
	0	1								WMSB[7:0]
	0	0								WLSB[7:0]

This command reads the temperature sensed by the temperature sensor.

WATTR: D [7:6]: I²C Write Byte Number

00b: 1 byte (head byte only)

01b: 2 bytes (head byte + pointer)

10b: 3 bytes (head byte + pointer + 1st parameter)

11b: 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D [5:3]: User-defined address bits (A2, A1, A0)

D [2:0]: Pointer setting

WMSB [7:0]: MSByte of write-data to external temperature sensor.

WLSB [7:0]: LSByte of write-data to external temperature sensor.

(21) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1								RMSB[7:0]
	1	1								RLSB[7:0]

This command reads the temperature sensed by the temperature sensor.

RMSB [7:0]: MSByte read data from external temperature sensor.

RLSB [7:0]: LSByte read data from external temperature sensor.

(22) V_{COM} and Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between V _{COM} and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of V_{COM} and data output. When setting the vertical back porch, the total blanking will be kept (20 HSYNC).

VBD [1:0]: Border Data Selection

B/W/Red mode (BWR=0)

DDX [0]	VBD [1:0]	LUT	DDX [0]	VBD [1:0]	LUT
0	00	Floating	1(Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11	Floating

B/W mode (BWR=1)

DDX [0]	VBD [1:0]	LUT	DDX [0]	VBD [1:0]	LUT
0	00	Floating	1(Default)	00	Floating
	01	LUTBW (1→0)		01	LUTWB (1→0)
	10	LUTWB (0→1)		10	LUTBW (0→1)
	11	Floating		11	Floating

DDX [1:0]: Data Polarity.

DDX [1] for RED data, DDX [0] for BW data in the B/W/Red mode

DDX [0] for B/W mode

B/W/Red mode (BWR=0)

DDX [1:0]	Data {Red, B/W}	LUT	DDX [1:0]	Data {Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB
01(Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

B/W mode (BWR=1)

DDX [0]	Data {New, Old}	LUT	DDX [0]	Data {New, Old}	LUT
0	00	LUTWW (0→0)	1(Default)	00	LUTBB (0→0)
	01	LUTBW (1→0)		01	LUTWB (0→1)
	10	LUTWB (0→1)		10	LUTBW (1→0)
	11	LUTBB (1→1)		11	LUTWW (1→1)

CDI [3:0]: V_{COM} and Data Interval

CDI [3:0]	V _{COM} and Data Interval	CDI [3:0]	V _{COM} and Data Interval
0000 b	17 H _{SYNC}	0110	11
0001	16	0111	10 (Default)
0010	15
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2

(23) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Interval Low Power Detection Flag

0: Low power input (V_{DD} < 2.5V)

1: Normal status (default)

(24) TCON Setting (TCON) (R60H)

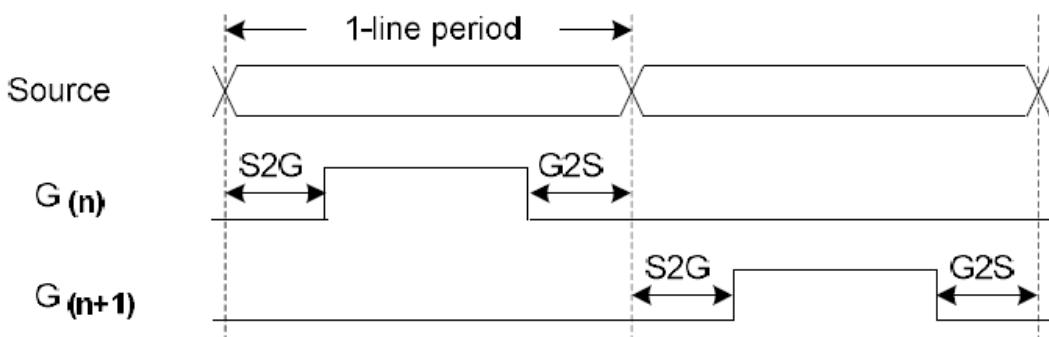
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-Overlap Period	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G [3:0] or G2S [3:0]: Source to Gate / Gate to Source Non-overlap period

S2G [3:0] or G2S [3:0]	Period		S2G [3:0] or G2S [3:0]	Period
0000b	4	
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(25) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:3]			0			0	0
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	0	VRES[7:0]							

This command defines alternative resolution and this setting is of higher priority than the RES [1:0] in R00H (PSR).

HRES [7:3]: Horizontal Display Resolution

VRES [8:0]: Vertical Display Resolution

Active Channel Calculation:

GD: First active gate = G0 (Fixed); LAST active gate = VRES [8:0] - 1

SD: First active source = S0 (Fixed); LAST active source = HRES [7:3]*8 - 1

(26) Get Status (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	PTL_flag	I ² C_ERR	I ² C_BUSY	data_flag	PON	POF	BUSY

This command reads the IC status.

PTL_FLAG: Partial display status (high: partial mode)

I²C_ERR: I²C master error status

I²C_BUSY: I²C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

(27) Auto Measure V_{COM} (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically Measure V _{COM}	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]	XON	AMVS	AMV	AMVE	

This command reads the IC status.

AMVT [1:0]: Auto Measure V_{COM} Time

00b: 3s 01b: 5s (Default)

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scans during Auto Measure V_{COM} period. (Default)

1: All Gate ON during Auto Measure V_{COM} period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure V_{COM} period. (Default)

1: Source output VDHR during Auto Measure V_{COM} period.

AMV: Analog signal

0: Get V_{COM} value with the VV command (R81h) (Default)

1: Get V_{COM} value in analog signal. (External analog to digital converter)

AMVE: Auto Measure V_{COM} Enable (/Disable)

- 0: No effect
- 1: Trigger auto V_{COM} sensing.

(28) Vcom Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV [5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(29) VCM_DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS [5:0]: VCOM_DC Setting

VDCS [5:0]	Vcom value
00 0000b	-0.10 V (default)
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(30) Partial Window (PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Window	0	0	1	0	0	1	0	0	0	0
	0	1	HRST[7:3]						0	0
	0	1	HRED[7:3]						1	1
	0	1	-	-	-	-	-	-	-	VRST[8]
	0	1	VRST[7:0]							
	0	1	-	-	-	-	-	-	-	VRED[8]
	0	1	VRED[7:0]							
	0	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST [7:3]: Horizontal start channel bank. (Value 00h~13h)

HRED [7:3]: Horizontal end channel bank. (Value 00h~13h). HRED must be greater than HRST.

VRST [8:0]: Vertical start line. (Value 000h~127h)

VRED [8:0]: Vertical end line. (Value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (Default)

(31) Partial In (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(32) Partial Out (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	1	0

This command makes the display exit partial mode and enter normal mode.

(33) Program Mode (PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Mode	0	0	1	0	1	0	0	0	0	0
Program	0	1	1	0	1	0	0	1	0	1

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(34) Active Program (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is transmitted, the programming state machine would be activated.

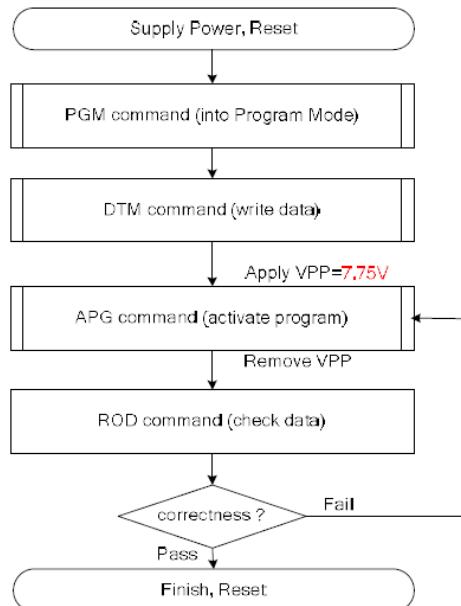
The BUSY flag would fall to 0 until the programming is completed.

(35) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP Data for Check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFFF.

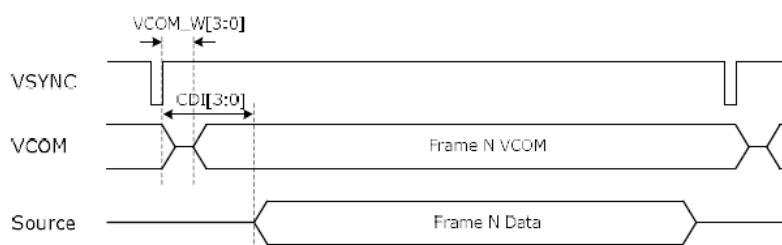


(36) Power Saving (PWS) (RE3H)

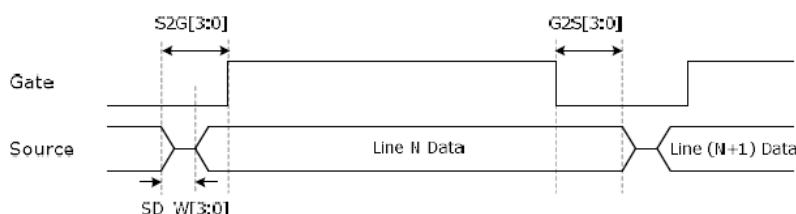
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for VCOM & Source	0	0	1	1	1	0	0	0	1	1
	0	1		VCOM W[3:0]					SD W[3:0]	

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W [3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



7. Electrical Characteristics

7.1. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V _{CI}	-0.3 to +6.0	V
Logic Input Voltage	V _{IN}	-0.3 to V _{CI} +2.4	V
Operating Temp. range	T _{OPR}	0 to +50	°C
Storage Temp. range	T _{STG}	-25 to +70	°C
Humidity Range	RH	40~70	%

IMPORTANT: It is recommended that you use a UV protective film when operating the module in direct sunlight.

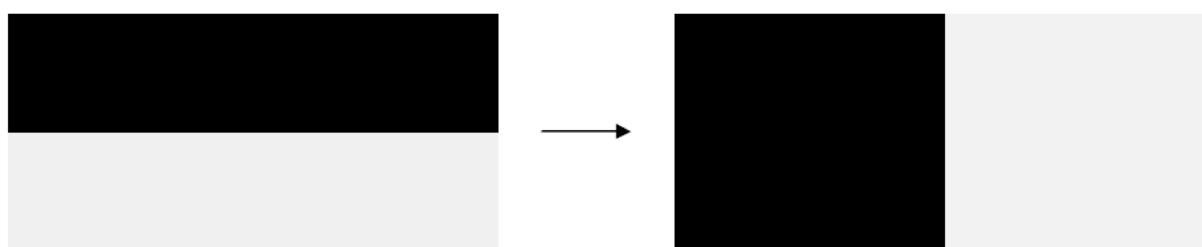
7.2. Panel DC Characteristics

The following specifications apply for: V_{SS} = 0V, V_{CI} = 3.3V, TA = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V _{SS}	-	-	0	-	V
Logic Supply Voltage	V _{CI}	-	2.3	3.3	3.6	V
High level input voltage	V _{IH}	Digital Input Pins	0.7V _{CI}	-	V _{CI}	V
Low level input voltage	V _{IL}	Digital Input Pins	0	-	0.3V _{CI}	V
High level output voltage	V _{OH}	Digital Input Pins, I _{OH} = 400uA	V _{CI} -0.4	-	-	V
Low level output voltage	V _{OL}	Digital Input Pins, I _{OL} = -400uA	0	-	0.4	V
Image update current	I _{UPDATE}	-	-	8	10	mA
Standby panel current	I _{STANDBY}	-	-	-	5	uA
Power panel update)	P _{UPDATE}	-	-	26.4	40	mW
Standby power panel	P _{STBY}	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	50	°C
Storage temperature	-	-	-25	-	70	°C
Image update Time at 25°C	-	-	-	6	8	Sec
Deep Sleep Mode Current	I _{VCI}	DC/DC Off No Clock No Input Load Ram Data Not Retained	-	2	5	uA
Sleep Mode Current	I _{VCI}	DC/DC Off No Clock No Input Load Ram Data Retained	-	35	50	uA

The typical power consumption is measured with the following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern, shown below.

Note: The standby power is the consumed power when the panel controller is in standby mode. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Crystalfontz. Vcom is recommended to be set in the range of assigned value $\pm 0.1V$.



8. Panel AC Characteristics

8.1. Oscillator Frequency

The following specifications apply for: $V_{SS} = 0V$, $V_{Cl} = 3.3V$, $T_A = 25^\circ C$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator Frequency	F_{osc}	$V_{Cl}=2.3 \text{ to } 3.6V$	-	1.625	-	MHz

8.2. MCU Interface

8.2.1. MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is "Low", 4-wire SPI is selected. When it is "High", 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

MCU Interface Assignment Under Different Bus Interface Mode

Note: "L" is connected to V_{SS} . "H" is connected to V_{Cl} .

8.2.2. MCU Serial Interface (4-Wire SPI)

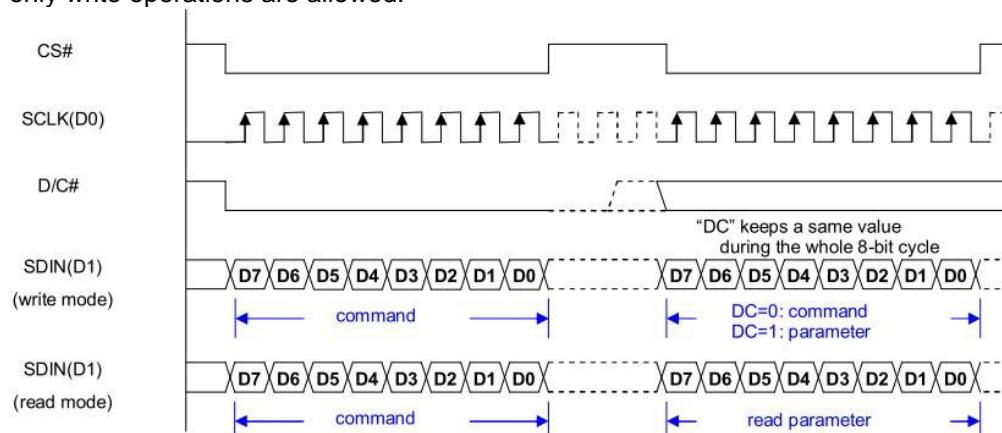
The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Control Pins of 4-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.



Write procedure in 4-wire Serial Peripheral Interface mode

8.2.3. MCU Serial Interface (3-Wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

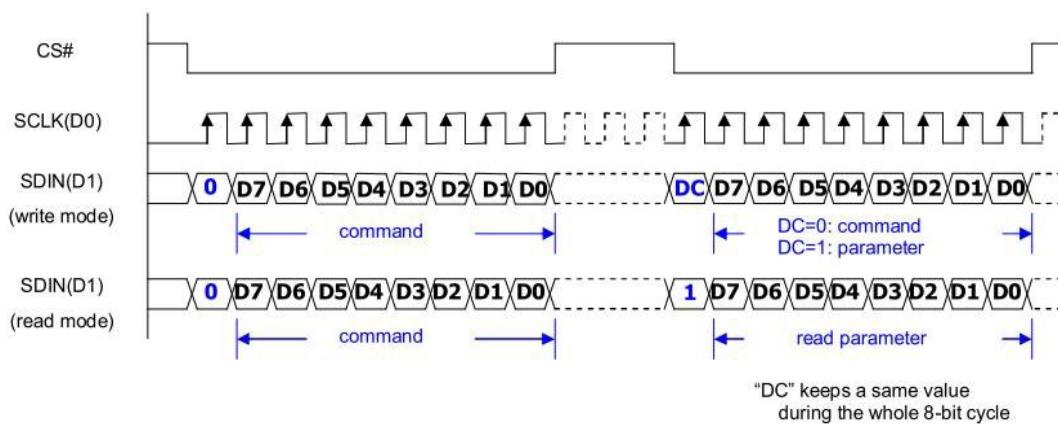
In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

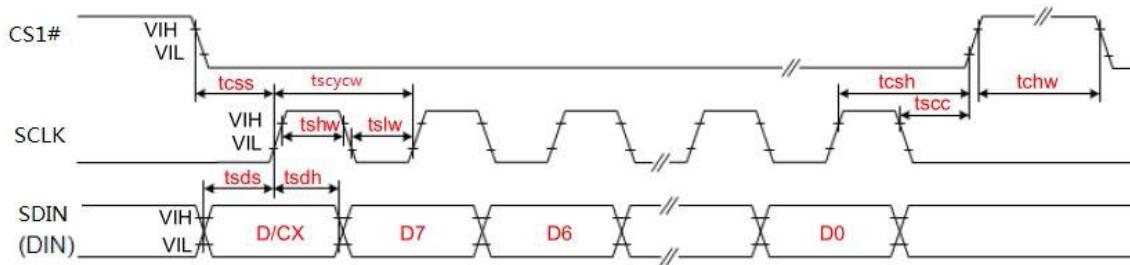
Control Pins of 3-Wire Serial Peripheral Interface

Note: ↑stands for rising edge of signal

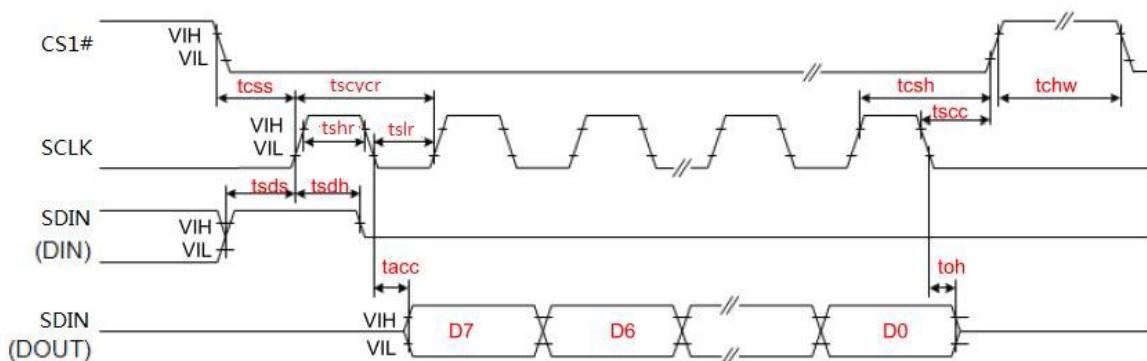


Write Procedure in 3-Wire Serial Peripheral Interface Mode

9. Timing Characteristics of Series Interface



3-wire Serial Interface – Write



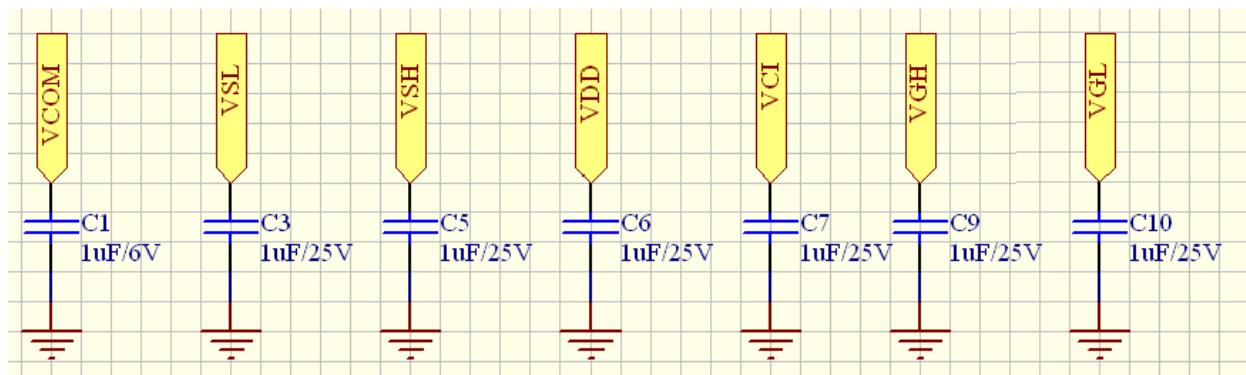
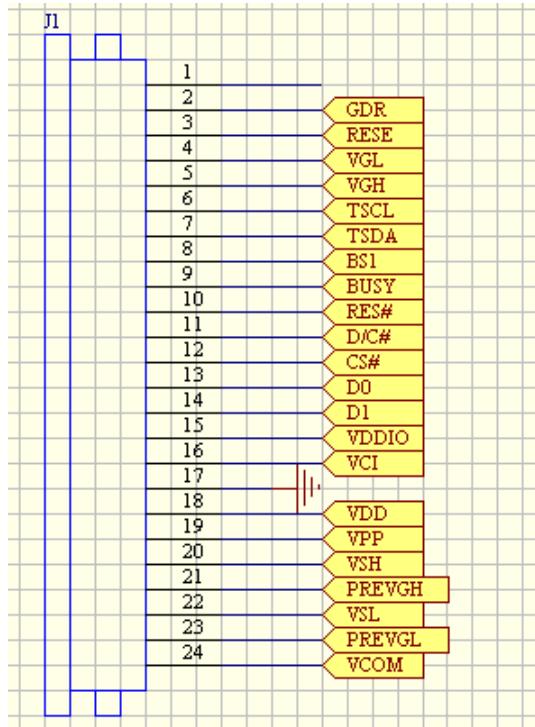
3-wire Serial Interface – Read

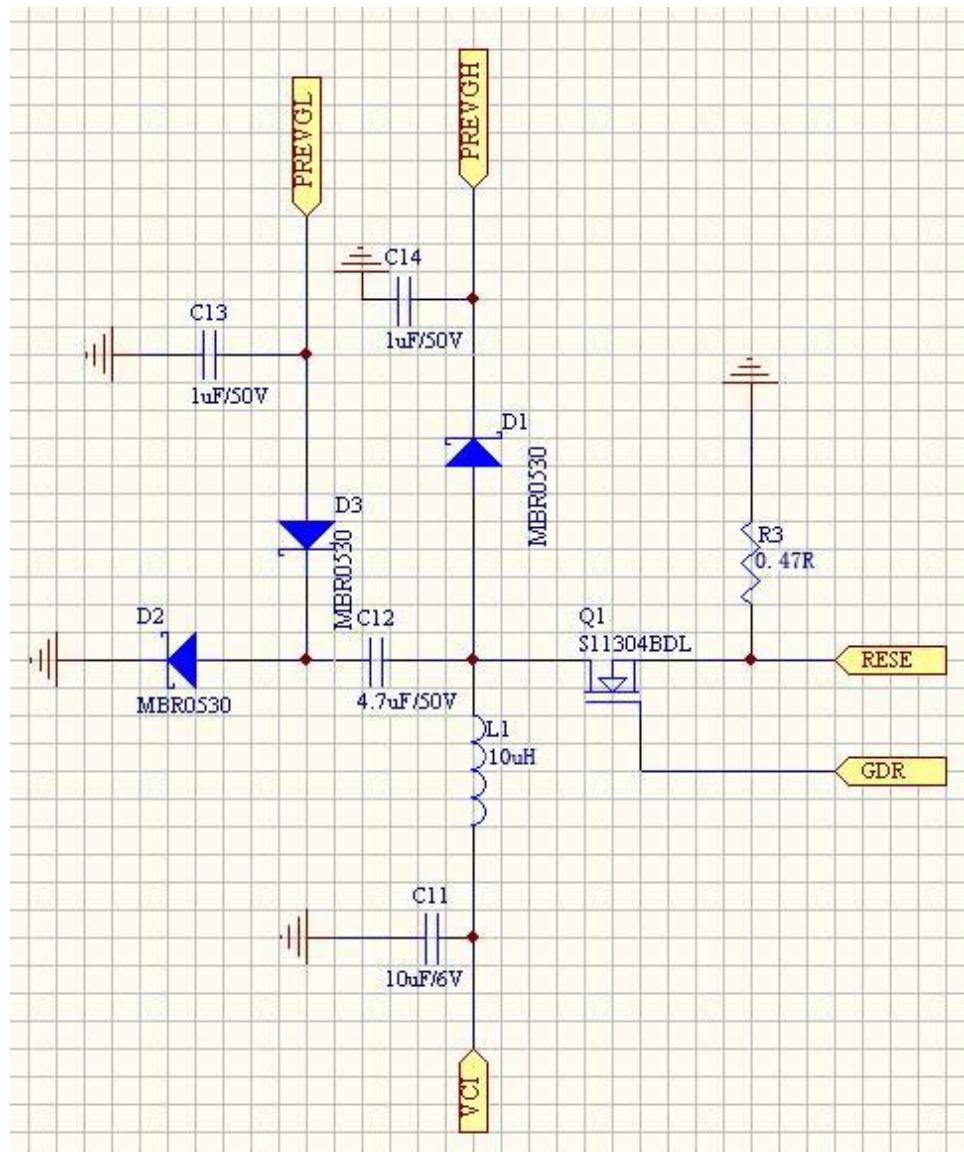
Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsch		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchew		Chip Select Setup Time	40	-	-	ns
tscycw	SCLK	Serial clock cycle (write)	100	-	-	ns
tshw		SCL "H" pulse width (write)	35	-	-	ns
tslw		SCL "L" pulse width (write)	35	-	-	ns
tscvcvr		Serial clock cycle (Read)	150	-	-	ns
tshw		SCL "H" pulse width (Read)	60	-	-	ns
tslr		SCL "L" pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	-	-	10	ns
toh		Output disable time	15	-	-	ns

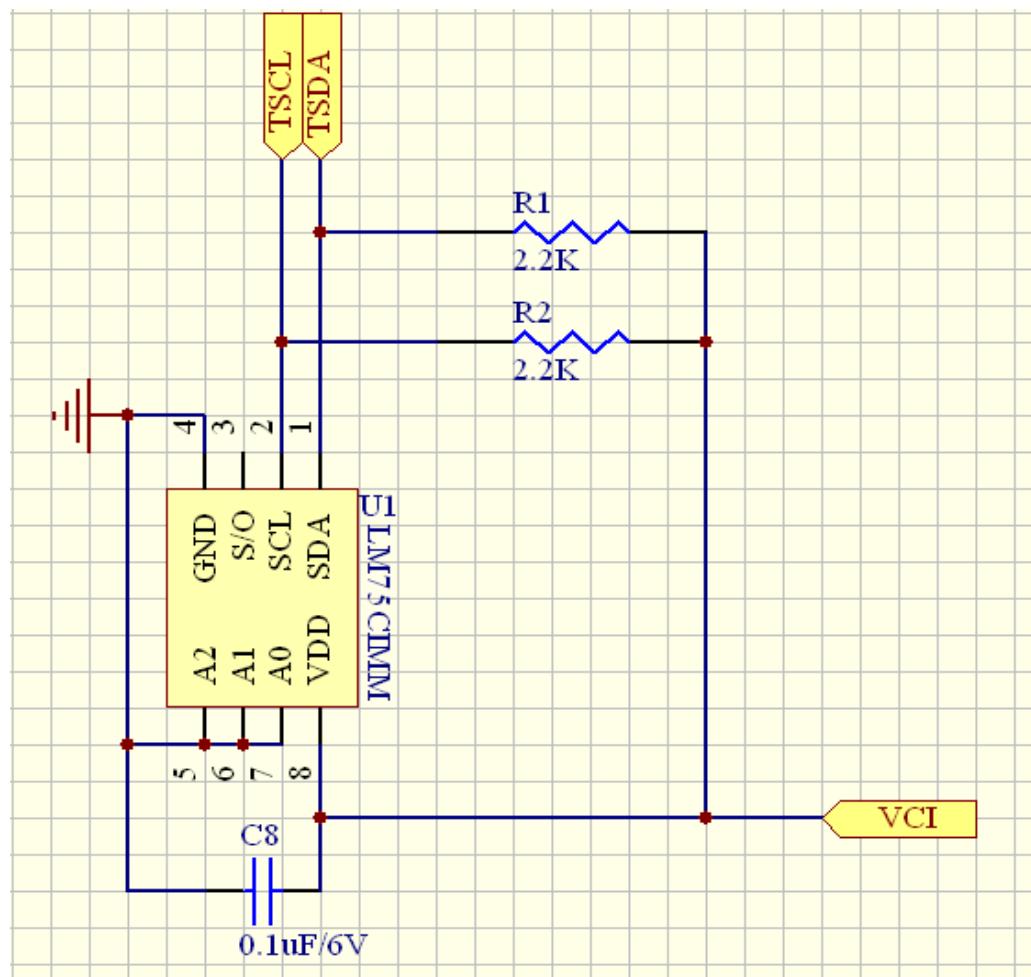
10. Power Consumption

Parameter	Symbol	Conditions	Typ	Max	Unit	Remark
Panel power consumption during update	-	25°C	26.4	40	mW	-
Power consumption in standby mode	-	25°C	-	0.0165	mW	-

11. Reference Circuit

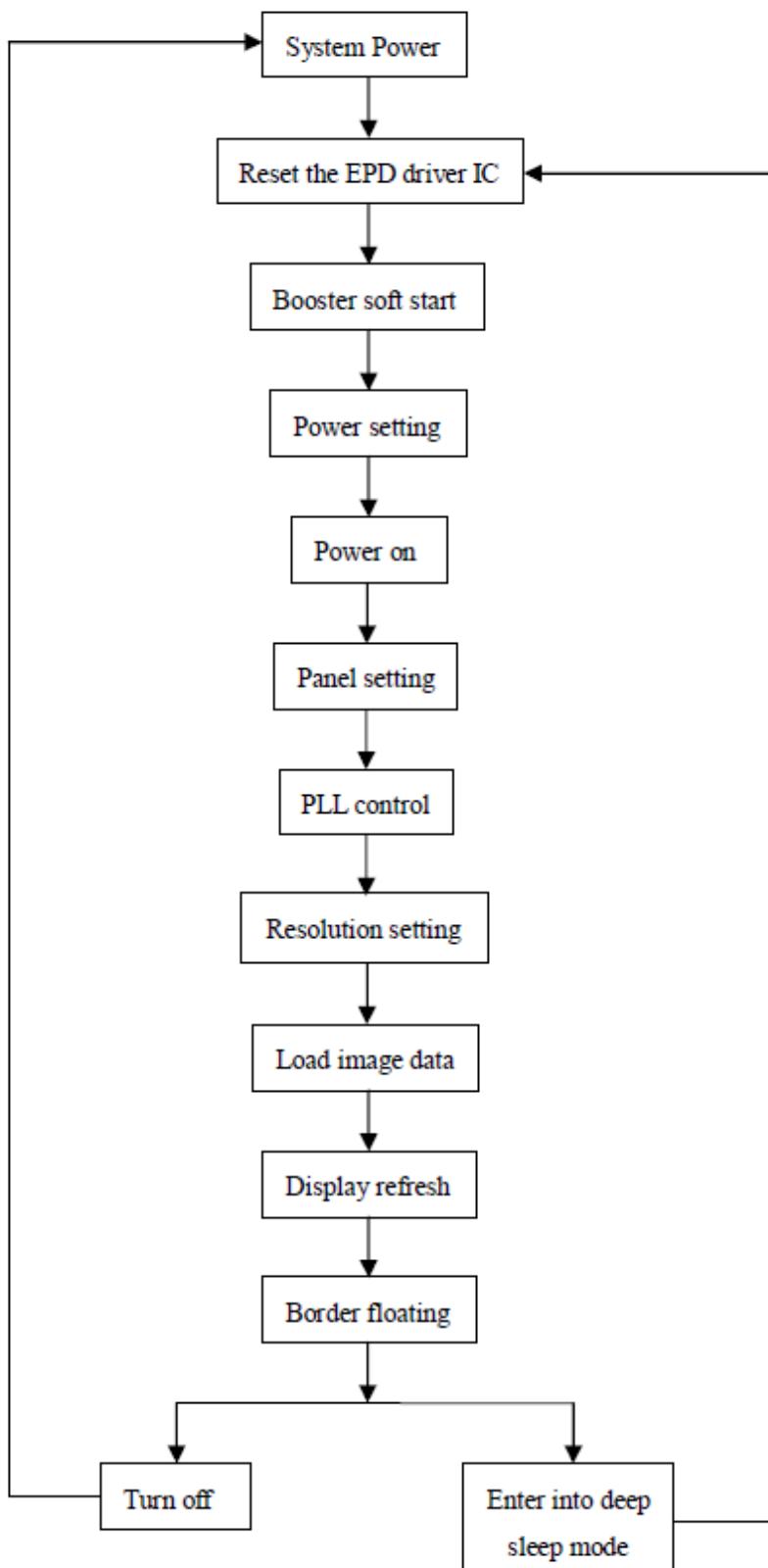




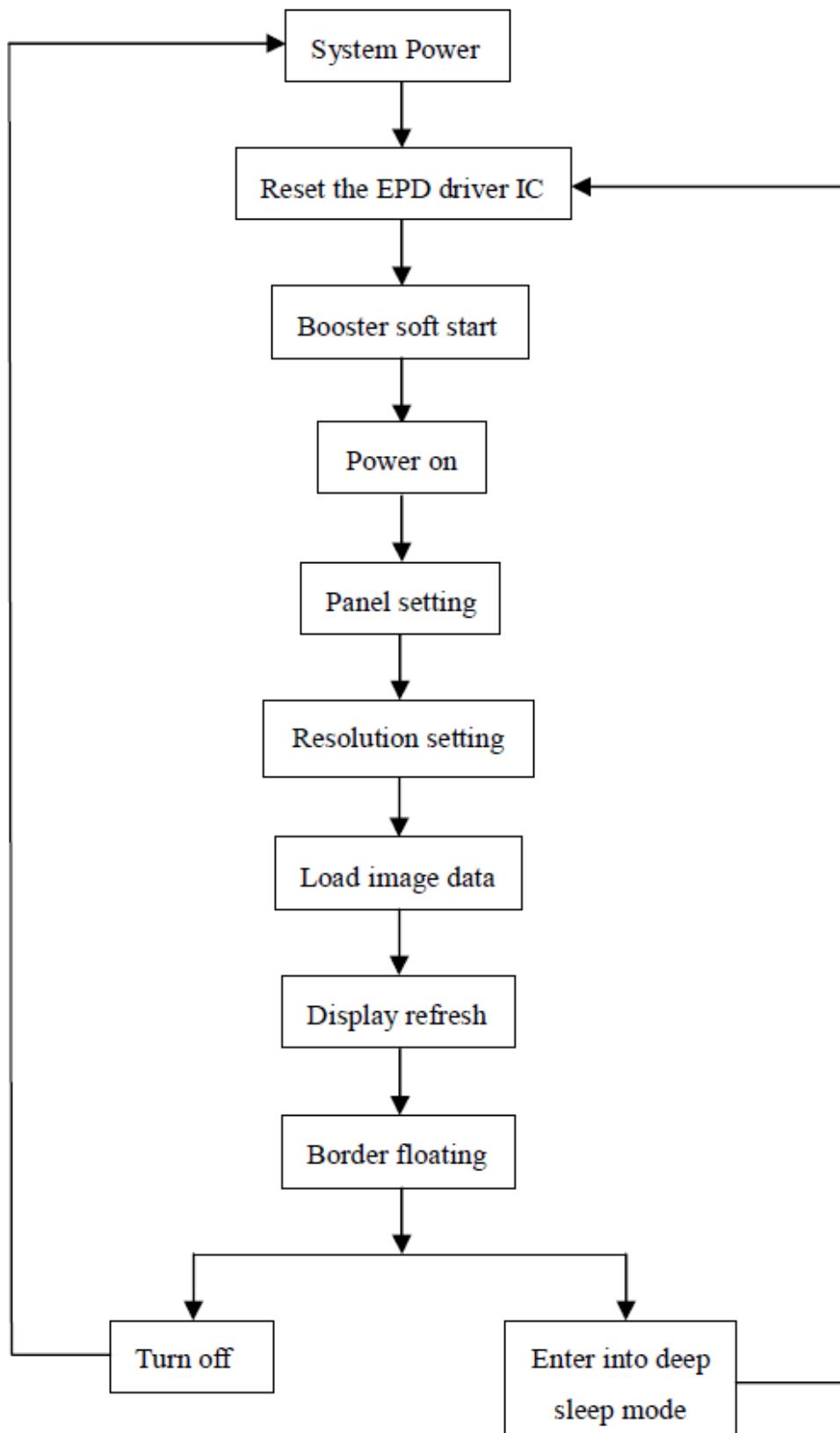


12. Typical Operating Sequence

12.1. BWR Mode & LUT from Register (Normal Operation Flow)

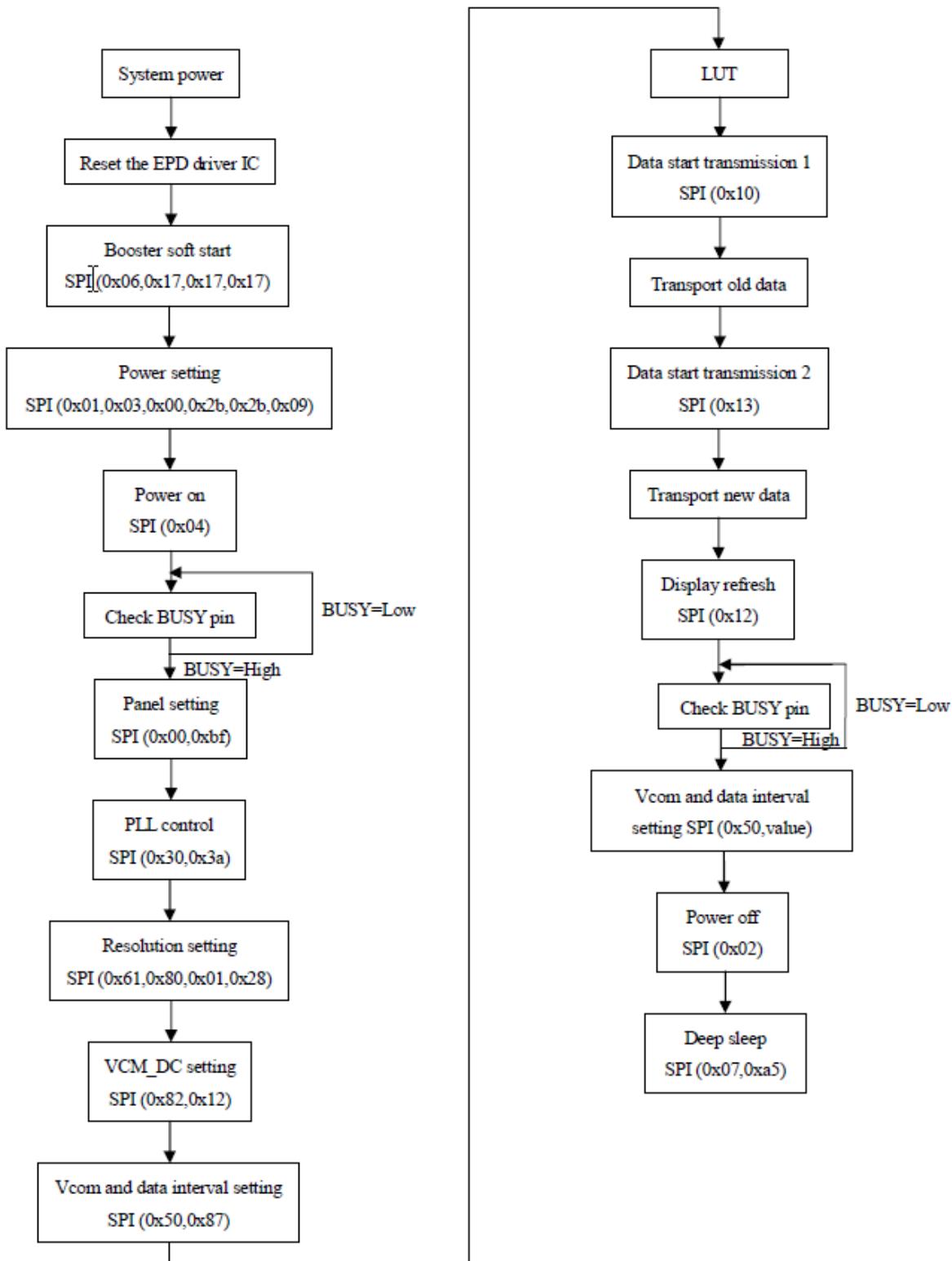


12.2. BWR Mode & LUT from OTP

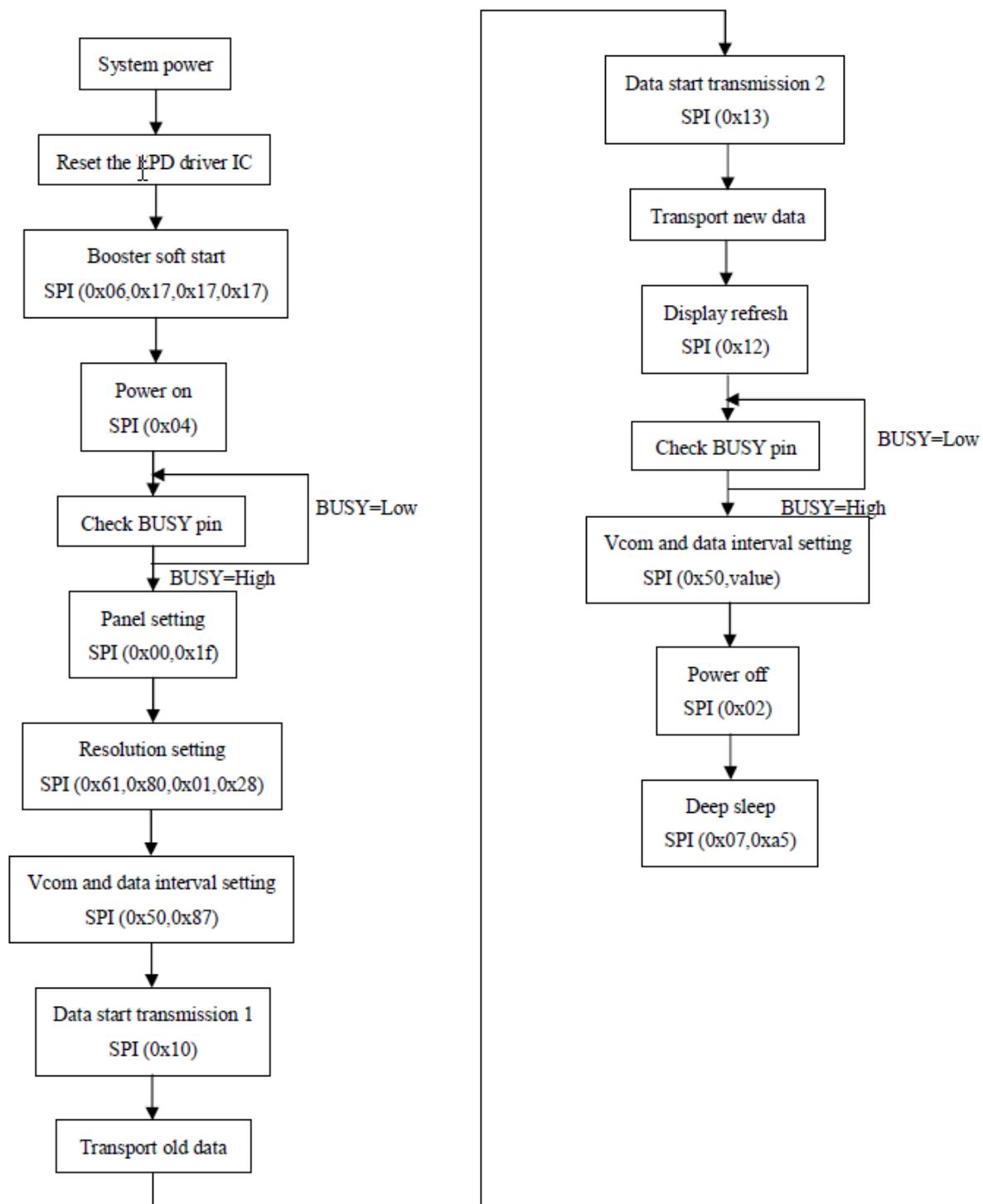


13. Reference Program Code

13.1. BWR Mode & LUT from Register



13.2. BWR Mode & LUT from OTP



14. Optical Characteristics

14.1. Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25°C

Symbol	Parameter	Conditions	Min	Typical	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 14-1
Gn	2Gray Level	-	-	DS+(WS-DS) × n(m-1)	-	L*	-
CR	Contrast Ratio	Indoor	8		-	-	-
Panel Life		0°C ~50°C		1000000 times or 5 years			Note 14-2

WS: White State, DS: Dark State

Gray State from Dark to White: DS、 WS

m: 2

Note (14-1): Luminance meter: Eye – One Pro Spectrophotometer

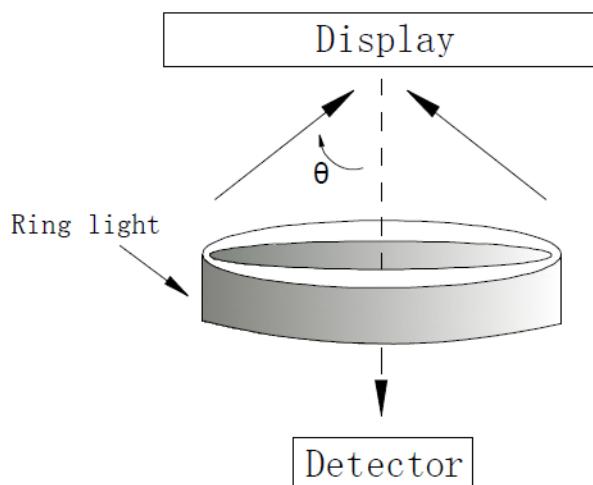
Note (14-2): Panel life is not guaranteed when worked in temperatures below 0 degrees or above 50 degrees. Each update interval time should be at a minimum of 180 seconds.

14.2. Definition of Contrast Ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd) ():

R1: White Reflectance Rd: Dark Reflectance

$$CR = R1/Rd$$

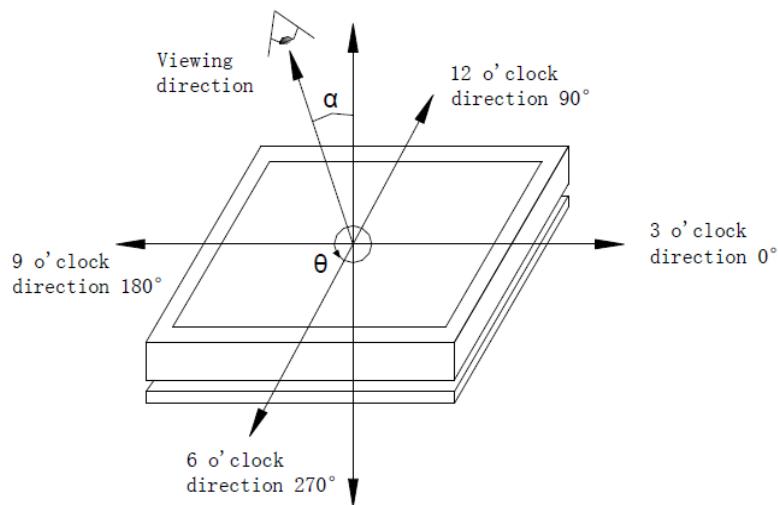


14.3. Reflection Ratio

The reflection ratio is expressed as:

$$R = \text{Reflectance Factor WHITE BOARD} \times (L_{\text{CENTER}} / L_{\text{WHITE BOARD}})$$

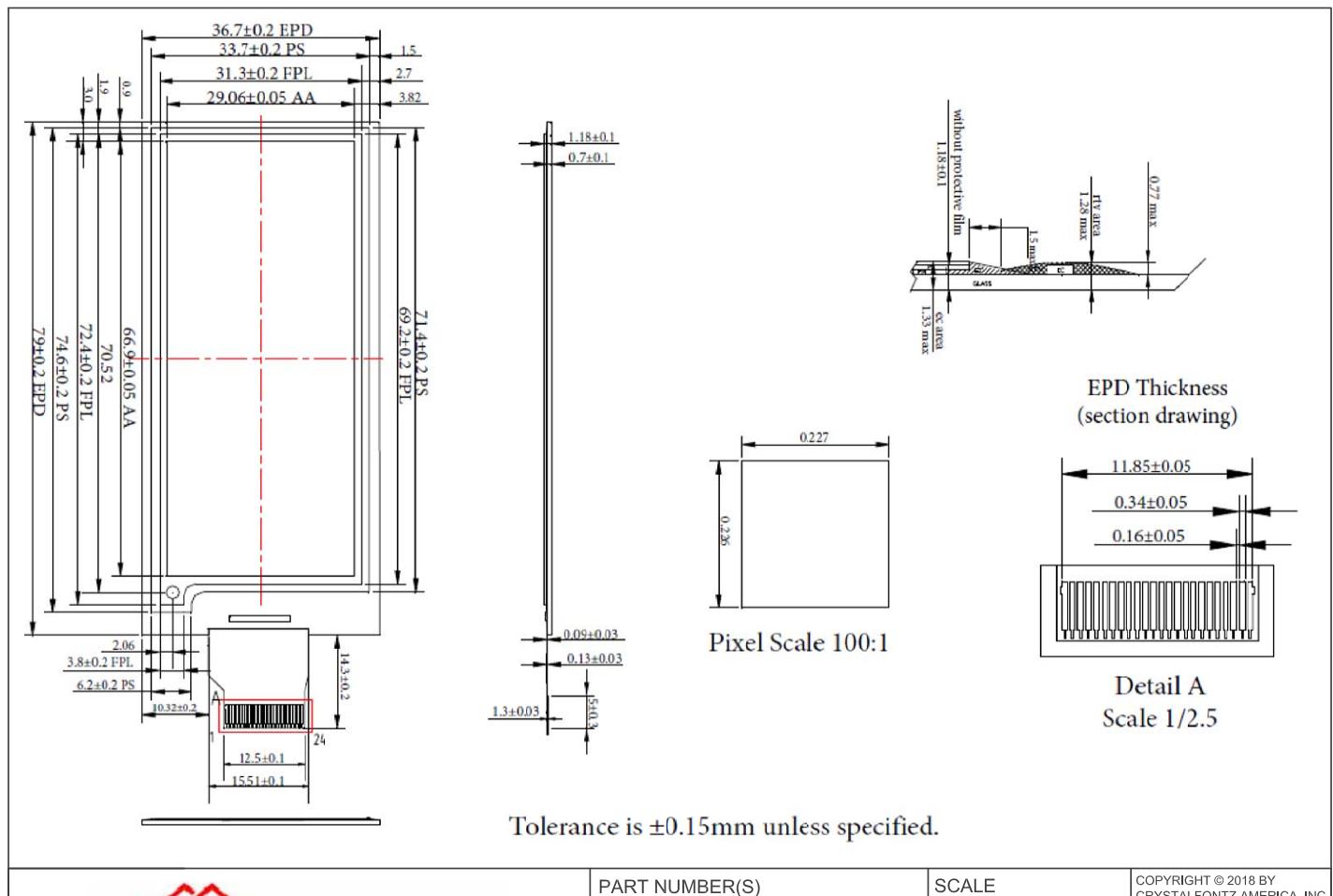
L_{CENTER} is the luminance measured at center in a white area ($R=G=B=1$). $L_{\text{WHITE BOARD}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



14.4. Bi-Stability

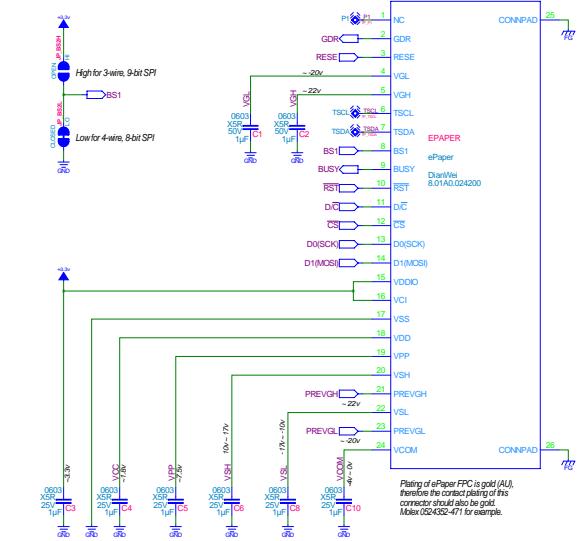
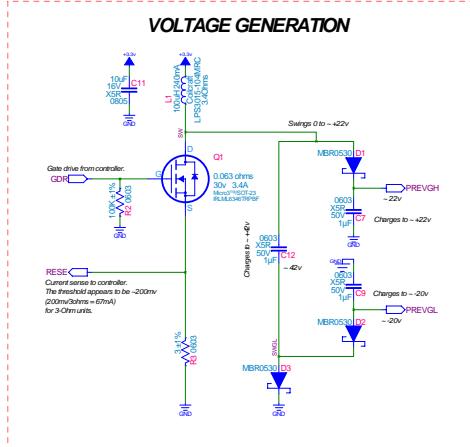
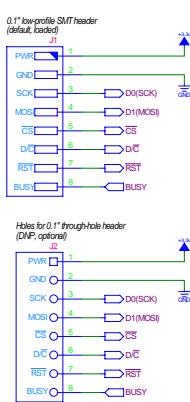
The Bi-Stability standard is as follows:

Bi-Stability	Result		
		AVG	MAX
24-Hour Luminance Drift	White state ΔL^*	-	3
	Black state ΔL^*	-	3



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	CFAP128296C0-0290	Not to Scale	
DRAWING NUMBER	UNITS	DATE	
CFAP128296C0-0290 master	Millimeters	2018-07-03	

REV	ENGINEER	DATE	REMARKS
0.0	BAC	2018-04-04	Initial Creation
0.1	BAC	2018-05-17	Ind val, C12 val, JP_0P47 open, CN FPC
-	-	-	-
-	-	-	-
-	-	-	-



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CFA-10084: ePaper Adapter Board 24-pin (3-ohm)		
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PRODUCT NAME:	PRODUCT REVISION:	PCB NUMBER:

CFA-10084

0v1

PCB-10084

0v1