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IE-0624: Laboratorio de Microcontroladores

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Laboratorio # 4

STM32: GPIO, ADC, comunicaciones, IoT

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1. Introducción

Repository de GitHub <https://github.com/ErickMaRi/Laboratorios-Grupales-IE0624>

En este laboratorio, se desarrolló un sismógrafo digital utilizando la placa STM32F429 Discovery y la biblioteca libopencm3. El objetivo principal fue registrar y analizar oscilaciones mecánicas con un sensor MEMS, usando el sistema diseñado, para proporcionar datos precisos y en tiempo real que luego puedan ser estudiados.

Este informe detalla las especificaciones técnicas como:

- Hardware utilizado
- La configuración del software
- El desarrollo del circuito
- Las pruebas realizadas
- Los resultados obtenidos

2. Nota Teórica

2.1. STM32F429 Discovery Kit

El STM32F429 Discovery Kit es una placa de desarrollo avanzada basada en el microcontrolador STM32F429ZIT6, perteneciente a la familia de microcontroladores ARM Cortex-M4 de STMicroelectronics [1]. Este microcontrolador combina un alto rendimiento y características avanzadas, lo que lo hace ideal para aplicaciones exigentes en tiempo real.

El STM32F429 ofrece una frecuencia de operación de hasta 180 MHz, integrando 2 MB de memoria Flash y 256 KB de SRAM, lo que proporciona un amplio espacio para el desarrollo de aplicaciones complejas [5]. Además, cuenta con una unidad de punto flotante (FPU) de precisión simple, lo que mejora el rendimiento en cálculos matemáticos intensivos.

Entre los periféricos integrados destacan:

- **Convertidores ADC y DAC:** Permiten la conversión de señales analógicas a digitales y viceversa, esenciales para aplicaciones de procesamiento de señales.
- **Interfaces de comunicación:** Incluye múltiples interfaces como UART, SPI, I2C, USB OTG (On-The-Go), CAN y Ethernet, facilitando la comunicación con una variedad de dispositivos y redes.
- **Controladores de pantalla:** Soporta pantallas TFT-LCD con controlador integrado, permitiendo el desarrollo de interfaces de usuario gráficas avanzadas.
- **GPIOs de alta velocidad:** Ofrece numerosos pines de entrada/salida de propósito general, configurables y con capacidades de interrupción.

El kit también incorpora sensores y periféricos adicionales, como acelerómetros, giroscopios y micrófonos digitales, ampliando su funcionalidad y aplicaciones posibles [6].

2.1.1. Diagrama de pines

Los diagramas de pines proporcionan una referencia visual de la disposición física de los pines en la placa, facilitando la conexión de periféricos externos y la asignación de funciones a los GPIOs.

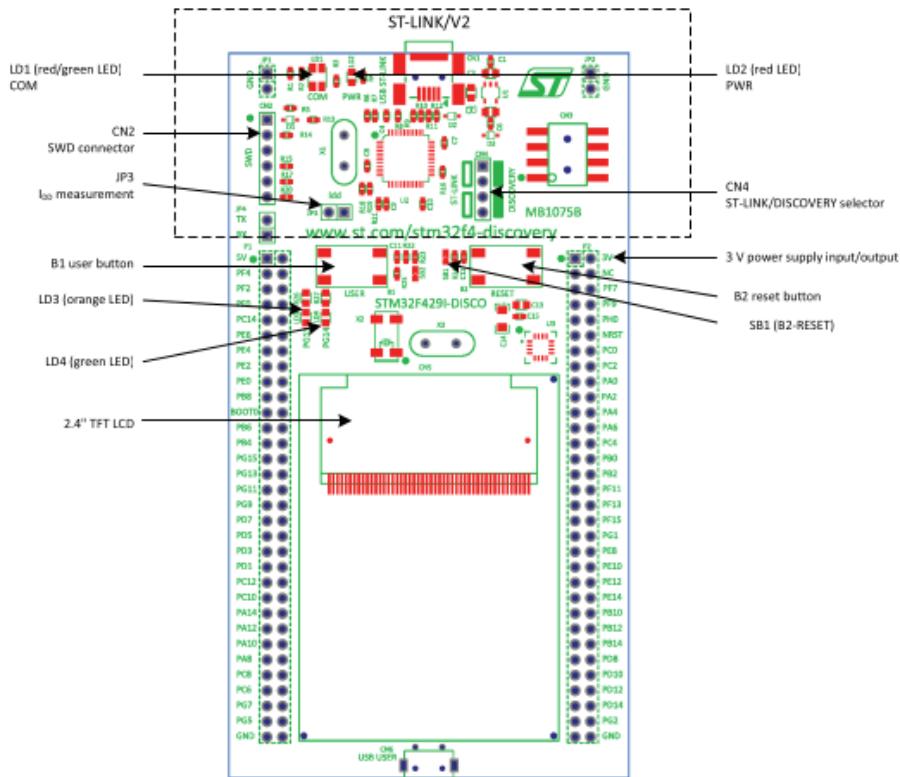


Figura 1: Diagrama de pines superior de STM32F429 Discovery [6]

En la figura 3, se muestra el diagrama de pines correspondiente a la parte superior de la placa. Se pueden identificar los pines asociados a los buses de comunicación, pines de alimentación y tierra, y otros pines funcionales.

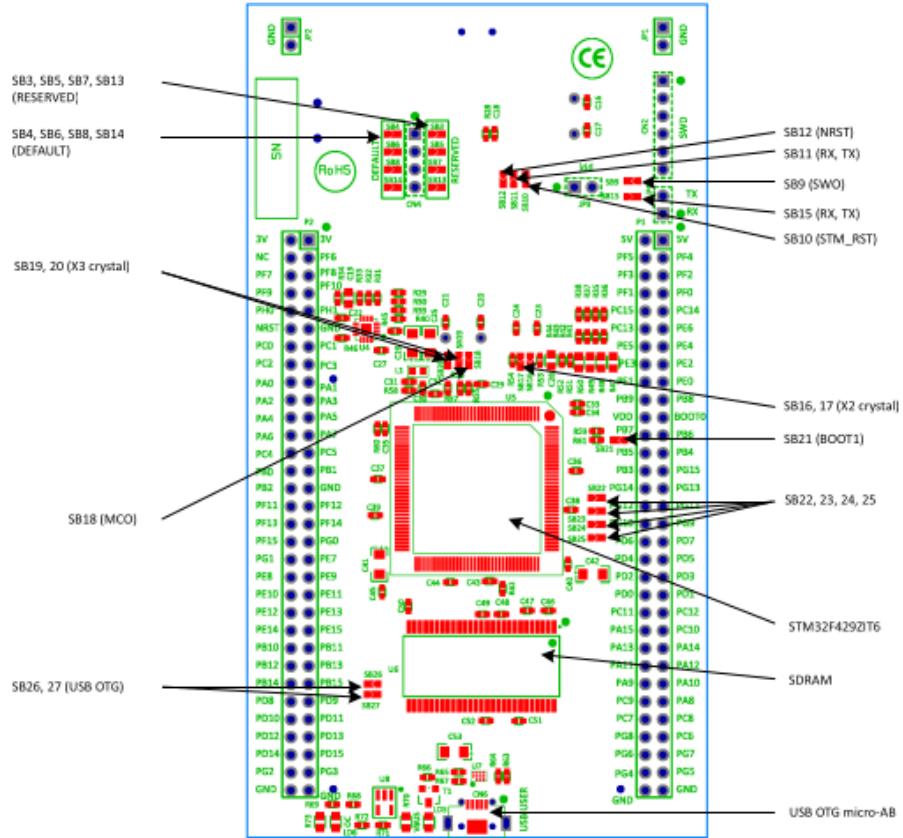


Figura 2: Diagrama de pines inferior de STM32F429 Discovery [6]

La figura 3 presenta el diagrama de pines de la parte inferior de la placa, complementando la información y permitiendo una visión completa de las posibilidades de conexión.

2.1.2. Diagrama de bloques

El diagrama de bloques es una representación simplificada que muestra los principales componentes y su interconexión dentro del sistema.

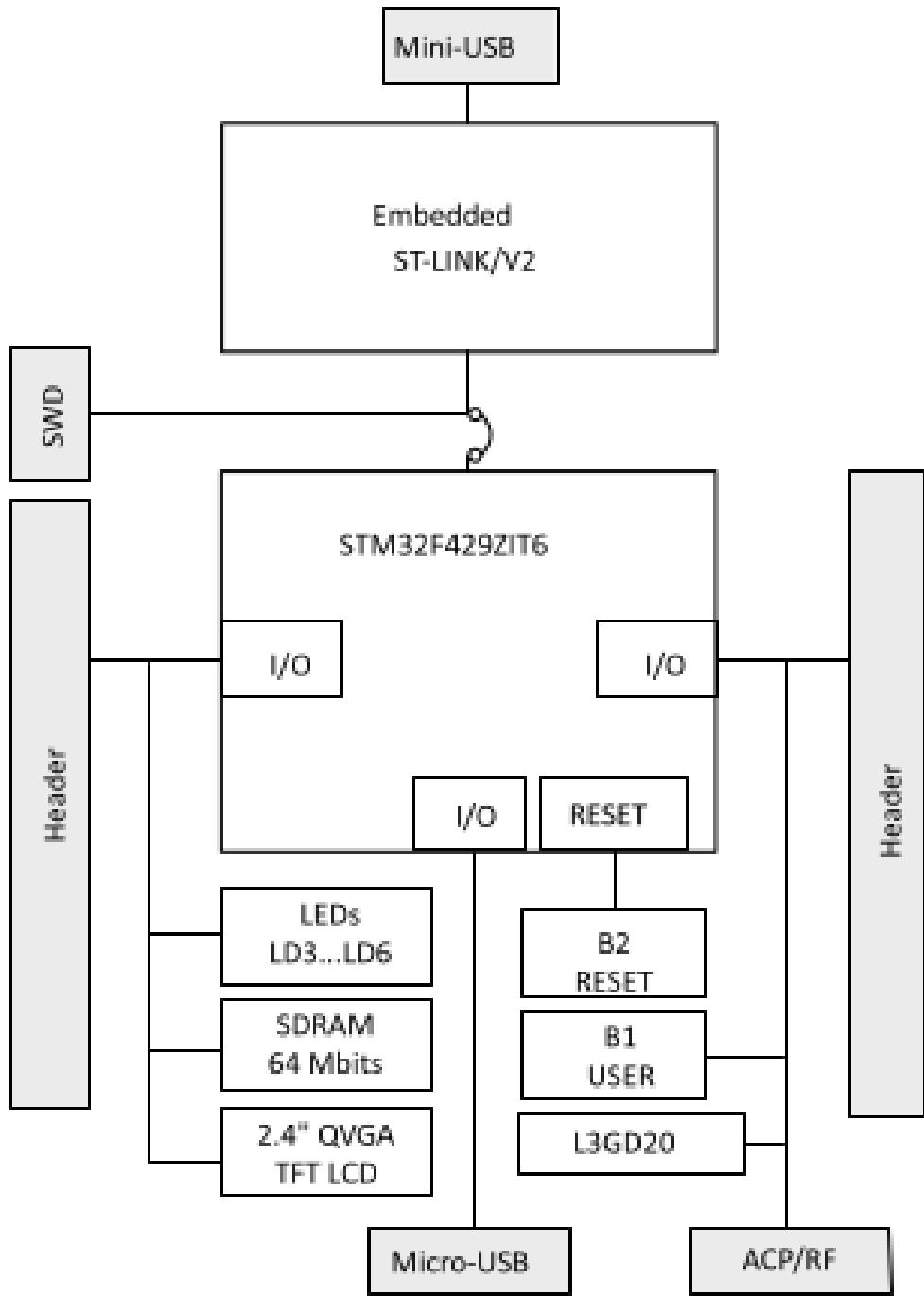


Figura 3: Diagrama de bloques de STM32F429 Discovery [6]

En la figura 3, se observa cómo el microcontrolador central se comunica con los periféricos integrados y externos, incluyendo la memoria, interfaces de comunicación y dispositivos de entrada/salida. Este diagrama es esencial para comprender la arquitectura del sistema y planificar su uso en proyectos específicos.

2.2. Biblioteca libopencm3

libopencm3 es una biblioteca de código abierto que proporciona un acceso de bajo nivel y multiplataforma a los periféricos de los microcontroladores ARM Cortex-M [2]. Diseñada para simplificar el desarrollo de firmware, abstrae las complejidades asociadas con la configuración directa de registros de hardware.

Entre sus características principales se incluyen:

- **Acceso uniforme a periféricos:** Ofrece una interfaz consistente para controlar periféricos como GPIO, ADC, UART, SPI e I2C, independientemente del fabricante del microcontrolador.
- **Abstracción de hardware:** Elimina la necesidad de manipular registros manualmente, reduciendo errores y acelerando el desarrollo.
- **Licencia permisiva:** Distribuida bajo GPL v3 o posterior, permite su uso en proyectos comerciales y no comerciales con pocas restricciones.
- **Documentación y comunidad activa:** Cuenta con una documentación extensa y una comunidad activa que contribuye al la robustez de la librería por su soporte activo.

2.3. Giroscopio L3GD20

El giroscopio L3GD20 es un sensor MEMS (Micro Electro Mechanical Systems) de tres ejes que se encuentra integrado en la placa STM32F429 Discovery [6]. Este dispositivo es capaz de medir la velocidad angular alrededor de los ejes X, Y y Z, lo que permite detectar movimientos y rotaciones en el espacio tridimensional.

Características principales del L3GD20:

- **Rango de medida ajustable:** Permite seleccionar entre ± 250 , ± 500 y ± 2000 grados por segundo, adaptándose a diferentes necesidades de precisión y rango.
- **Comunicación SPI:** Se comunica con el microcontrolador a través de la interfaz SPI, permitiendo transferencias de datos rápidas y eficientes.
- **Bajo consumo de energía:** Diseñado para aplicaciones portátiles y de bajo consumo.

2.4. ADC (Convertidor Analógico a Digital)

El Convertidor Analógico a Digital (ADC) es un periférico que permite la conversión de señales analógicas en valores digitales procesables por el microcontrolador [5]. En este proyecto, el ADC se utiliza para monitorear el nivel de voltaje de la batería:

- **Resolución de 12 bits:** Proporciona una alta precisión en la conversión de señales analógicas.
- **Velocidad de conversión:** Soporta altas tasas de muestreo, adecuadas para aplicaciones de tiempo real.
- **Multiplexación de canales:** Permite la lectura de múltiples señales analógicas a través de canales independientes.
- **Modos de operación flexibles:** Incluye modos de escaneo, inyección y discontinuo, adaptándose a diferentes requisitos de aplicación.

2.5. Comunicación USART/USB

La comunicación es un aspecto esencial en sistemas embebidos, permitiendo la interacción con otros dispositivos y la transferencia de datos. El STM32F429 incorpora múltiples interfaces de comunicación, destacando USART y USB.

2.5.1. USART (Universal Synchronous/Asynchronous Receiver/Transmitter)

La interfaz USART es ampliamente utilizada para la comunicación serial tanto síncrona como asíncrona [5]. Es esencial para transmitir y recibir datos entre el microcontrolador y otros dispositivos como computadoras, sensores y módulos de comunicación.

Características clave:

- **Velocidades de transmisión configurables:** Soporta una amplia gama de baudios.
- **Modos de operación:** Compatible con protocolos estándar como RS-232 y RS-485.
- **Interrupciones y DMA:** Soporta el uso de interrupciones y acceso directo a memoria para mejorar la eficiencia.

2.5.2. USB (Universal Serial Bus)

La interfaz USB proporciona una conexión rápida y versátil para la transferencia de datos [5]. El STM32F429 soporta USB OTG, permitiendo que el dispositivo actúe como host o como dispositivo.

Beneficios del uso de USB:

- **Alta velocidad de transferencia:** Ideal para aplicaciones que requieren transmitir grandes cantidades de datos.
- **Compatibilidad universal:** Fácil integración con computadoras y otros dispositivos USB.
- **Soporte para HID y CDC:** Permite implementar dispositivos de interfaz humana y comunicaciones de dispositivos de clase.

La utilización de estas interfaces facilita la integración con plataformas IoT como ThingsBoard, permitiendo la transmisión eficiente de datos para su procesamiento y visualización.

2.6. Plataforma IoT ThingsBoard

ThingsBoard es una plataforma IoT de código abierto diseñada para facilitar la recolección, el procesamiento y la visualización de datos provenientes de dispositivos conectados [4]. Ofrece una arquitectura escalable y robusta, adecuada tanto para proyectos pequeños como para implementaciones industriales a gran escala.

Características destacadas:

- **Dashboards personalizables:** Permite crear paneles de control interactivos con una variedad de widgets para visualizar datos en tiempo real, la amplia variedad de widgets se adaptan a casi cualquier proyecto con una amplia selección de tablas, mapas e indicadores.
- **Gestión de dispositivos y usuarios:** Facilita la administración centralizada de múltiples dispositivos y la asignación de permisos a diferentes usuarios. Esto nos permitió trabajar de manera separada y siempre poder registrar las salidas del sistema en el table-ro, en un instante.
- **Procesamiento de reglas:** Incluye un motor de reglas para procesar y reaccionar a eventos y condiciones específicas. Lo que nos permitió configurar una alarma para la batería

En resumidas cuentas, ThingsBoard se utilizó para recibir los datos del sismógrafo digital, permitir su análisis y proporcionar alertas o visualizaciones necesarias para los usuarios finales.

2.7. Componentes

Para el desarrollo del circuito son necesarios los componentes listados a continuación. Estos pueden ser adquiridos en la bodega de la escuela de Ingeniería Eléctrica o en sitios de venta de componentes electrónicos, como MicroJPM y Mouser.

Cabe destacar que el potenciómetro se utiliza para simular la descarga de la batería, por lo que sustituye a la resistencia de $1k\Omega$.

Componente	Cantidad	Precio por unidad
Resistencia $1k\Omega$	1	₡26
Resistencia 820Ω	1	₡26
Potenciómetro $1k\Omega$	1	₡26
STM32F429I-DISC1	1	₡18 723
Batería 9V	1	₡1 841
Paquete de jumper	1	₡1 176
Breadboard	1	₡5 599

Tabla 1: Componentes utilizados

3. Desarrollo

3.1. Configuración de Hardware

3.1.1. Ajuste del voltaje a un rango entre 0V y 5V

Debido a que el rango de voltajes de entrada para el ADC de la placa es de 0V a 5V, tuvimos que encontrar un circuito que ajusta el rango de voltajes que vienen de la batería (9 Voltios máximo) a uno compatible con nuestro sistema. Tras investigar configuraciones comúnmente usadas se decidió utilizar un divisor de tensión para ajustar con una ganancia de cinco novenos.

$$V_{out} = \frac{R_2}{R_1 + R_2} \quad (1)$$

Lo que nos permite determinar los dos valores eligiendo arbitrariamente uno de los disponibles en el laboratorio.

$$R_2 = 1k\Omega$$

$$R_1 = 820\Omega$$

Para efectos del desarrollo del proyecto, con el objetivo de simular el comportamiento de la batería se usó un potenciómetro en el lugar de R_2 para variar la entrada al pin analógico.

3.1.2. Configuración del Giroscopio

El giroscopio L3GD20 se comunica con el microcontrolador STM32F429 mediante la interfaz SPI5. Se configuró el giroscopio para operar en modo normal, habilitando los ejes X, Y y Z, y estableciendo una escala de sensibilidad adecuada para la detección de oscilaciones.

3.1.3. Monitoreo del Nivel de Batería

Para monitorear el nivel de la batería, se utilizó uno de los canales del ADC del microcontrolador. Se implementó un divisor de voltaje para adaptar el rango de voltaje de la batería

([0, 9]V) al rango de entrada del ADC ([0, 3.3]V). De esta manera, se puede medir el voltaje de la batería y activar una alerta cuando el voltaje cae por debajo de 7V.

3.1.4. Integración de la Pantalla LCD

La pantalla LCD se conectó al microcontrolador utilizando la interfaz SPI. Se utilizaron las librerías gráficas para inicializar la pantalla y mostrar en tiempo real el nivel de batería y los valores de los ejes X, Y y Z del giroscopio.

3.2. Implementación del Software

3.2.1. Inicialización de Periféricos

Se desarrollaron funciones en lenguaje C utilizando la biblioteca libopencm3 para inicializar y configurar los periféricos necesarios, incluyendo GPIOs, SPI, USART, ADC y la pantalla LCD.

Listing 1: Configuración del SPI5 para el giroscopio

```
static void setup_spi(void)
{
    rcc_periph_clock_enable(RCC_SPI5);
    rcc_periph_clock_enable(RCC_GPIOC);
    rcc_periph_clock_enable(RCC_GPIOF);

    gpio_mode_setup(GPIOC, GPIO_MODE_OUTPUT, GPIO_PUPD_NONE, GPIO1);
    gpio_set(GPIOC, GPIO1); // Establecer el pin GPIOC1 en alto
    gpio_mode_setup(GPIOF, GPIO_MODE_AF, GPIO_PUPD_NONE, GPIO7 | GPIO8 | GPIO9);
    gpio_set_af(GPIOF, GPIO_AF5, GPIO7 | GPIO8 | GPIO9);

    spi_set_master_mode(SPI5);
    spi_set_baudrate_prescaler(SPI5, SPI_CR1_BR_FPCLK_DIV_64);
    spi_set_clock_polarity_0(SPI5);
    spi_set_clock_phase_0(SPI5);
    spi_set_full_duplex_mode(SPI5);
    spi_set_unidirectional_mode(SPI5);
    spi_enable_software_slave_management(SPI5);
    spi_send_msb_first(SPI5);
    spi_set_nss_high(SPI5);
    SPI_I2SCFGR(SPI5) &= ~SPI_I2SCFGR_I2SMOD;
    spi_enable(SPI5);

    write_reg(GYR_CTRL_REG1, GYR_CTRL_REG1_PD | GYR_CTRL_REG1_XEN |
              GYR_CTRL_REG1_YEN | GYR_CTRL_REG1_ZEN | (3 << GYR_CTRL_REG1_BW_SHIFT));
    write_reg(GYR_CTRL_REG4, (1 << GYR_CTRL_REG4_FS_SHIFT));
}
```

3.2.2. Lectura de Datos del Giroscopio

Se implementó una función para leer los datos del giroscopio a través del SPI. Los valores de los ejes X, Y y Z se obtienen y se procesan para ser mostrados en la pantalla LCD.

Listing 2: Lectura de los ejes X, Y, Z del giroscopio

```

void read_xyz(int16_t vecs[3])
{
    read_reg(GYR_WHO_AM_I | 0x80);
    read_reg(GYR_STATUS_REG | GYR_RNW);

    vecs[0] = read_reg(GYR_OUT_X_L | GYR_RNW) | read_reg(GYR_OUT_X_H | GYR_RNW) <<
        8;
    vecs[1] = read_reg(GYR_OUT_Y_L | GYR_RNW) | read_reg(GYR_OUT_Y_H | GYR_RNW) <<
        8;
    vecs[2] = read_reg(GYR_OUT_Z_L | GYR_RNW) | read_reg(GYR_OUT_Z_H | GYR_RNW) <<
        8;
}

```

3.2.3. Control de Comunicaciones USART/USB

Se configuró un botón para habilitar y deshabilitar las comunicaciones USART/USB. Cuando las comunicaciones están habilitadas, un LED indicador parpadea para señalar que la transmisión de datos está activa.

Listing 3: Control de comunicaciones con botón

```

if (gpio_get(GPIOA, GPIO0)) {
    usart_enabled = !usart_enabled; // Cambia el estado de la bandera
    msleep(300); // Retardo para evitar rebotes
}
if (usart_enabled) {
    gpio_toggle(GPIOG, GPIO13); // Enciende y apaga el LED
    msleep(500);
} else {
    gpio_clear(GPIOG, GPIO13); // Se asegura de que el LED se encuentra apagado
}

```

3.2.4. Monitoreo del Nivel de Batería

Se implementó la lectura del nivel de batería utilizando el ADC. Si el voltaje cae por debajo de 7V, se activa un LED de alarma y se muestra una alerta en la pantalla LCD.

Listing 4: Monitoreo del nivel de batería

```

input_adc3 = read_adc_naive(3);
float temp = input_adc3 * 9.0f / 4095.0f;
if (temp < 7.0f) {
    gpio_toggle(GPIOG, GPIO14); // Activar LED de alarma
}

```

3.2.5. Visualización en Pantalla LCD

Se diseñó una interfaz sencilla en la pantalla LCD para mostrar el título "Sismógrafo", los valores de los ejes X, Y, Z y el voltaje de la batería en tiempo real.

Listing 5: Función para actualizar la pantalla LCD

```

void lcd_main_structure(void)

```

```

{
    gfx_init(lcd_draw_pixel, 240, 320);
    gfx_fillScreen(LCD_WHITE);
    gfx_setTextSize(2.5);
    gfx_setCursor(15, 25);
    gfx_puts("Sismografo");
    gfx_setTextSize(2);
    gfx_setCursor(15, 49);
    gfx_puts("X:");
    gfx_setCursor(15, 73);
    gfx_puts("Y:");
    gfx_setCursor(15, 97);
    gfx_puts("Z:");
    gfx_setCursor(15, 121);
    gfx_puts("V:");
}

```

En el ciclo principal del programa, se actualizan los valores y se muestran en la pantalla.

Listing 6: Actualización de valores en la pantalla LCD

```

lcd_main_structure();
gfx_setTextSize(2);
gfx_setCursor(40, 49);
gfx_puts(char_X);
gfx_setCursor(40, 73);
gfx_puts(char_Y);
gfx_setCursor(40, 97);
gfx_puts(char_Z);
gfx_setCursor(40, 121);
gfx_puts(volt);
lcd_show_frame();

```

3.3. Pruebas y Resultados

Se realizaron pruebas para verificar el correcto funcionamiento del sistema. Se confirmó que los valores de los ejes X, Y y Z del giroscopio se actualizan en tiempo real en la pantalla LCD al mover la placa. También se verificó que el nivel de voltaje de la batería se muestra correctamente y que el LED de alarma se activa cuando el voltaje cae por debajo del umbral establecido.

Para demostrar la funcionalidad de la placa se grabó un video disponible en youtube a través del enlace:

Link del video: Labo 4 IE-0624 Laboratorio de Microcontroladores

3.3.1. Visualización de Valores en la Pantalla LCD

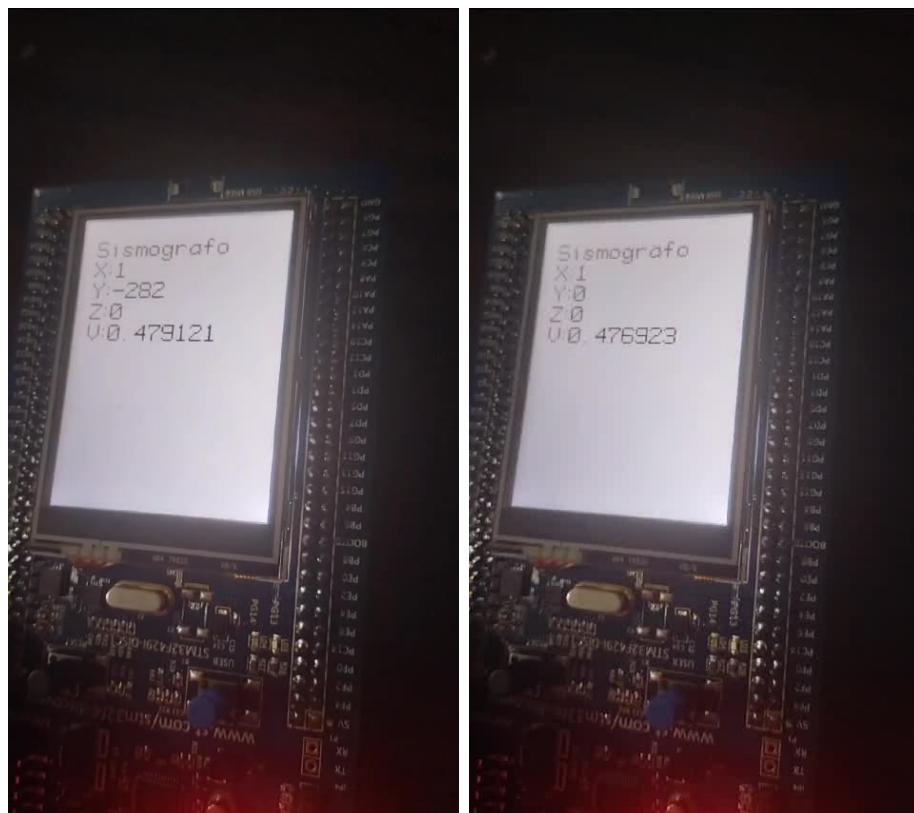


Figura 4: Valores del giroscopio y voltaje en la pantalla LCD al moverla y dejarla descansar.

La Figura 4 muestra los datos en la pantalla LCD. Los valores cambian dinámicamente al mover la placa y con el ruido ambiental, indicando que el giroscopio funciona.

3.3.2. Activación del LED de Alarma por Batería Baja

Se simularon condiciones de batería baja reduciendo el voltaje de entrada. Al caer por debajo de 7V, el LED de alarma comenzó a parpadear, y en la pantalla LCD se mostró una alerta, confirmando que el monitoreo del nivel de batería funciona adecuadamente.

3.4. Integración con ThingsBoard

Logramos comunicar la tarjeta con el Thingsboard para producir series de tiempo de los valores del giroscopio:



Figura 5: Serie de tiempo de valores del giroscopio capturada en thingsboard.

Las señales se muestran junto con un indicador de batería:

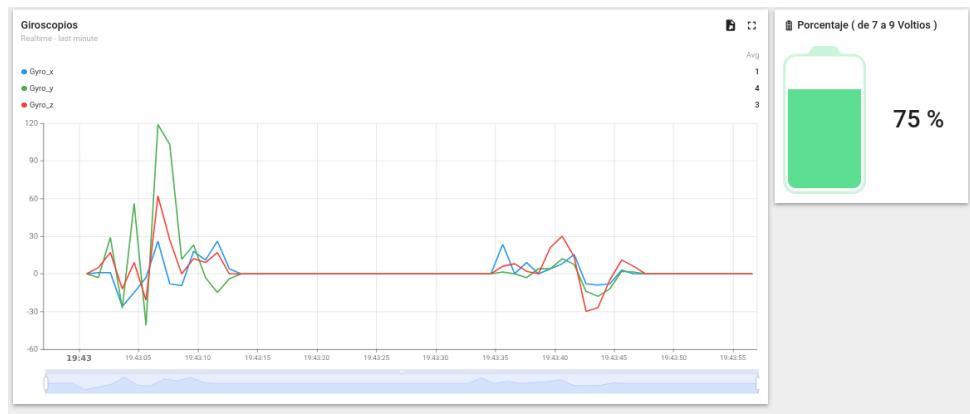


Figura 6: Widgets del tablero.

Y usando una Rule Chain revisamos que el valor porcentual de la batería sea positivo para la alarma de baja batería:

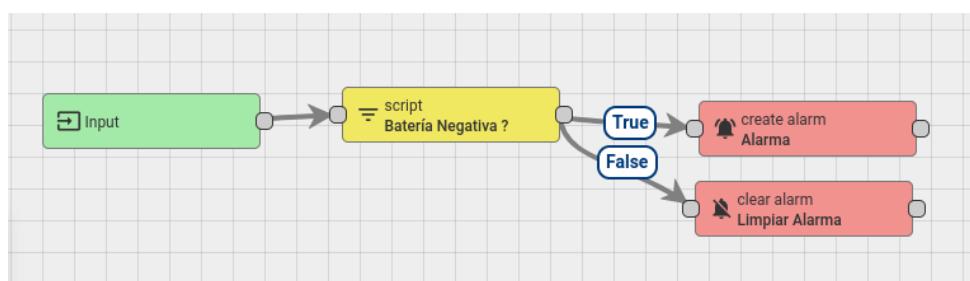


Figura 7: Rulechain usado para la alarma de batería.

4. Conclusiones y Recomendaciones

- Se logró desarrollar un sismógrafo digital funcional utilizando la placa STM32F429 Discovery y la biblioteca libopencm3, cumpliendo con los requisitos establecidos.

- La lectura y visualización en tiempo real de los datos del giroscopio y el nivel de batería se implementaron exitosamente, permitiéndonos mostrar los valores en la pantalla LCD y activando alertas cuando es necesario desde la plataforma de ThingsBoard.
- La implementación del control de comunicaciones mediante un botón y la indicación mediante LEDs proporcionan una interfaz de usuario inmediata y útil para verificar de un vistazo el funcionamiento del sistema.
- La plataforma de ThingsBoard es versátil y fácil de usar a la hora de configurar los dispositivos, de forma en la que si se trabaja con varios dispositivos similares, configurar el tablero no es tan complejo gracias al sistema de perfiles que estos tienen.

Referencias

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5. Anexos

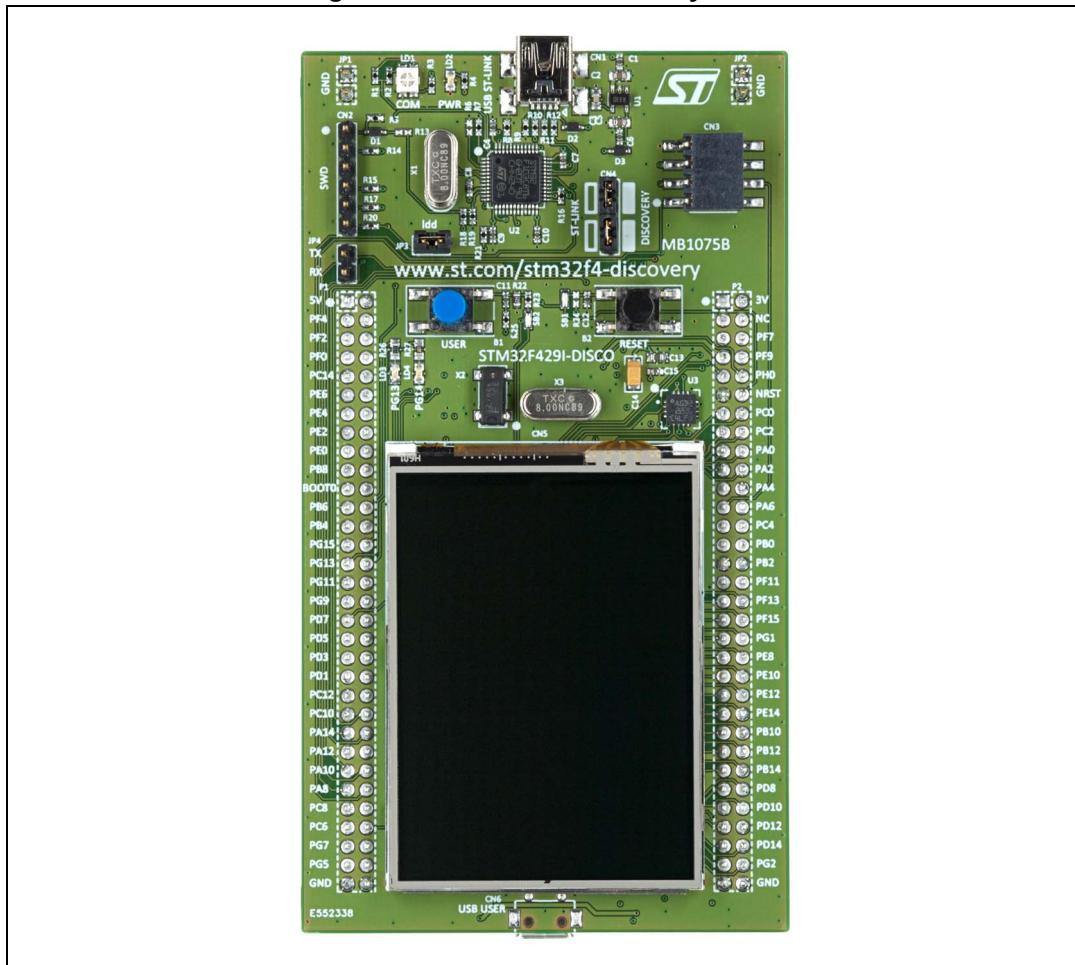
5.1. Hoja de datos del STM32F429 Discovery kit

Discovery kit for STM32F429/439 lines

Introduction

The STM32F429 Discovery kit (32F429IDISCOVERY) helps you to discover the high performance of the STM32F4 series and to develop your applications. It is based on an STM32F429ZIT6 and includes an ST-LINK/V2 embedded debug tool interface, 2.4" TFT LCD, SDRAM 64 Mbits, Gyroscope ST MEMS, LEDs, pushbuttons and a USB OTG micro-B connector.

Figure 1. STM32F429 Discovery board



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1 Conventions

Table 1 provides the definition of some conventions used in the present document.

Table 1. ON/OFF conventions

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Solder bridge SBx ON	SBx connections closed by solder
Solder bridge SBx OFF	SBx connections left open

2 Quick start

The STM32F429 Discovery is a low-cost and easy-to-use development kit to quickly evaluate and start a development with an STM32F4 series microcontroller.

Before installing and using the product, please accept the Evaluation Product License Agreement from www.st.com/stm32f4-discovery.

For more information on the STM32F429 Discovery board and for demonstration software, visit www.st.com/stm32f4-discovery.

2.1 Getting started

Follow the sequence below to configure the STM32F429 Discovery board and launch the DISCOVER application:

1. Ensure that the jumpers JP3 and CN4 are set to "on" (Discovery mode).
2. Connect the STM32F429 Discovery board to a PC using a USB cable type A/mini-B through the USB ST-LINK connector CN1, to power the board. The LEDs LD2 (PWR) and LD1 (COM).
3. The following applications are available on the screen:
 - Clock/Calendar and Game
 - Video Player and Image Browser (play videos and view images from the USB mass storage connected to CN6)
 - Performance monitor (watch the CPU load and run a graphical benchmark)
 - System Info
4. The demo software, as well as other software examples that allow you to discover the STM32 F4 series features, are available on www.st.com/stm32f4-discovery.
5. Develop your own applications starting from the examples.

2.2 System requirements

- Windows PC (XP, Vista, 7)
- USB type A to mini-B cable

2.3 Development toolchain supporting the STM32F429 Discovery kit

- Altium: TASKING™ VX-Toolset
- Atollic: TrueSTUDIO
- IAR: EWARM
- Keil™: MDK-ARM

2.4 Order code

To order the STM32F429 Discovery kit, use the STM32F429I-DISCO order code.

3 Features

The STM32F429 Discovery board offers the following features:

- STM32F429ZIT6 microcontroller featuring 2 MB of Flash memory, 256 KB of RAM in an LQFP144 package
- On-board ST-LINK/V2 with selection mode switch to use the kit as a standalone ST-LINK/V2 (with SWD connector for programming and debugging)
- Board power supply: through the USB bus or from an external 3 V or 5 V supply voltage
- L3GD20, ST MEMS motion sensor, 3-axis digital output gyroscope
- TFT LCD (Thin-film-transistor liquid-crystal display) 2.4", 262K colors RGB, 240 x 320 dots
- SDRAM 64 Mbits (1 Mbit x 16-bit x 4-bank) including an AUTO REFRESH MODE, and a power-saving
- Six LEDs:
 - LD1 (red/green) for USB communication
 - LD2 (red) for 3.3 V power-on
 - Two user LEDs:
LD3 (green), LD4 (red)
 - Two USB OTG LEDs:
LD5 (green) VBUS and LD6 (red) OC (over-current)
- Two pushbuttons (user and reset)
- USB OTG with micro-AB connector
- Extension header for LQFP144 I/Os for a quick connection to the prototyping board and an easy probing

4 Hardware layout

The STM32F429 Discovery board has been designed around the STM32F429ZIT6 microcontroller in a 144-pin LQFP package.

Figure 1 illustrates the connections between the STM32F429ZIT6 and its peripherals (ST-LINK/V2, pushbutton, LED, USB OTG, Gyroscope ST MEMS, Accelerometer + Magnetometer ST MEMS, and connectors).

Figure 2 and *Figure 3* help you to locate these features on the STM32F429 Discovery board.

Figure 1. Hardware block diagram

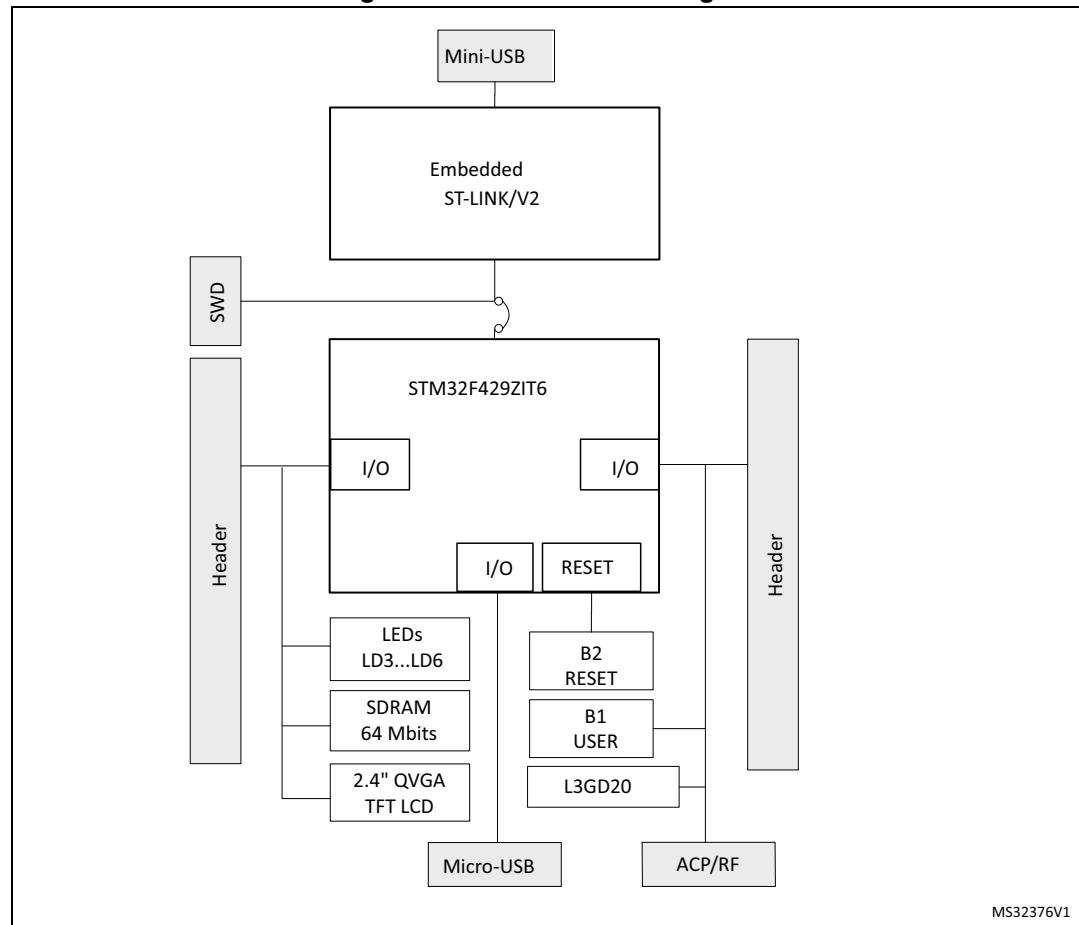


Figure 2. Top layout

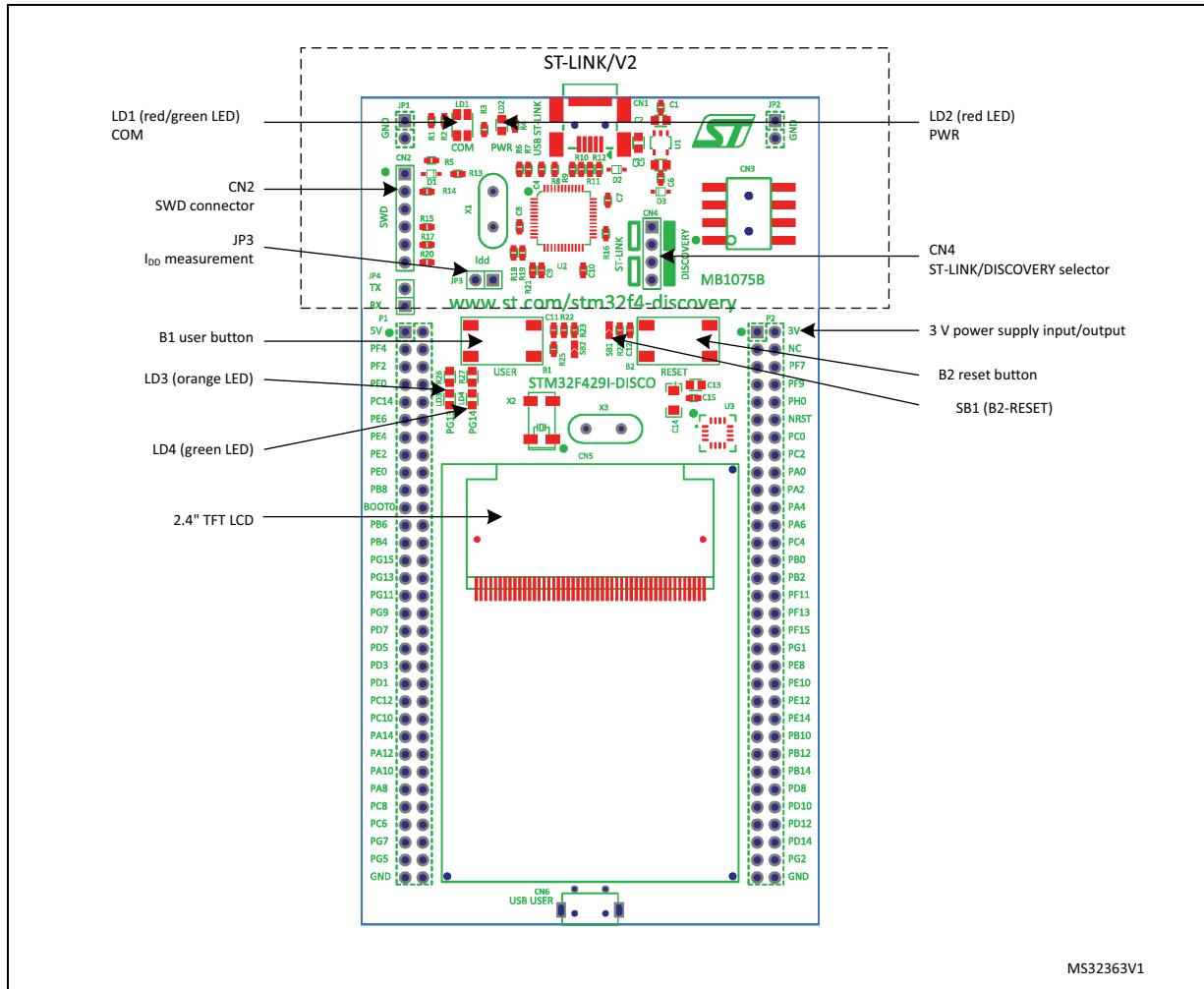
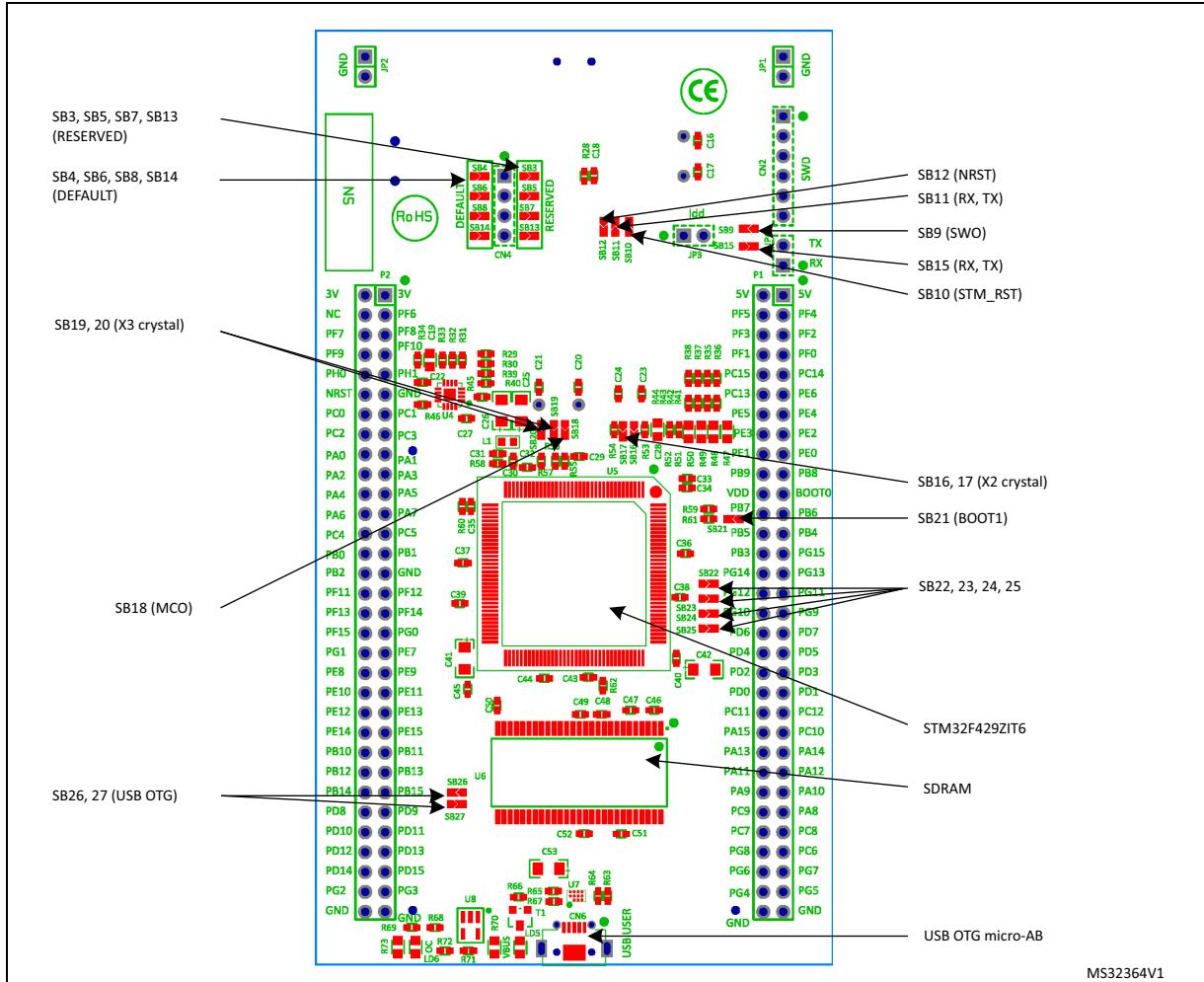


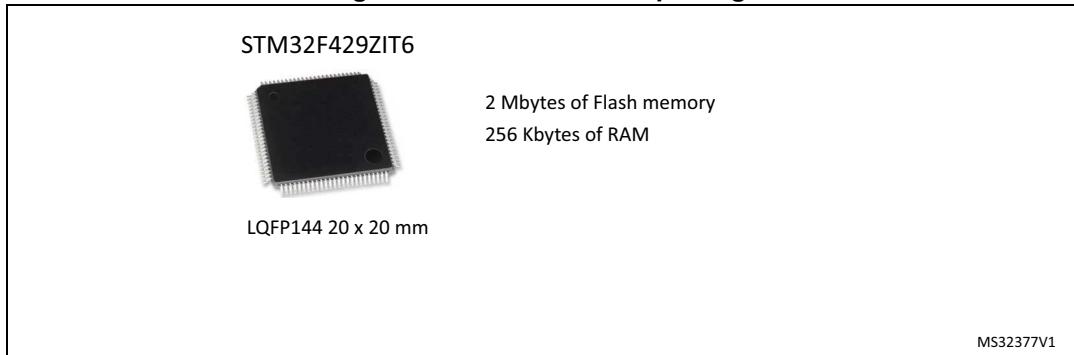
Figure 3. Bottom layout



4.1 STM32F429ZIT6 microcontroller

This ARM Cortex-M4 32-bit MCU with FPU has 225 DMIPS, up to 2 MB Flash/256 + 4 KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 20 comm. interfaces, a camera and an LCD-TFT, 1.7-3.6 V operation.

Figure 4. STM32F429ZIT6 package



This device provides the following benefits (see [Table 2](#)).

Table 2. Features and benefits

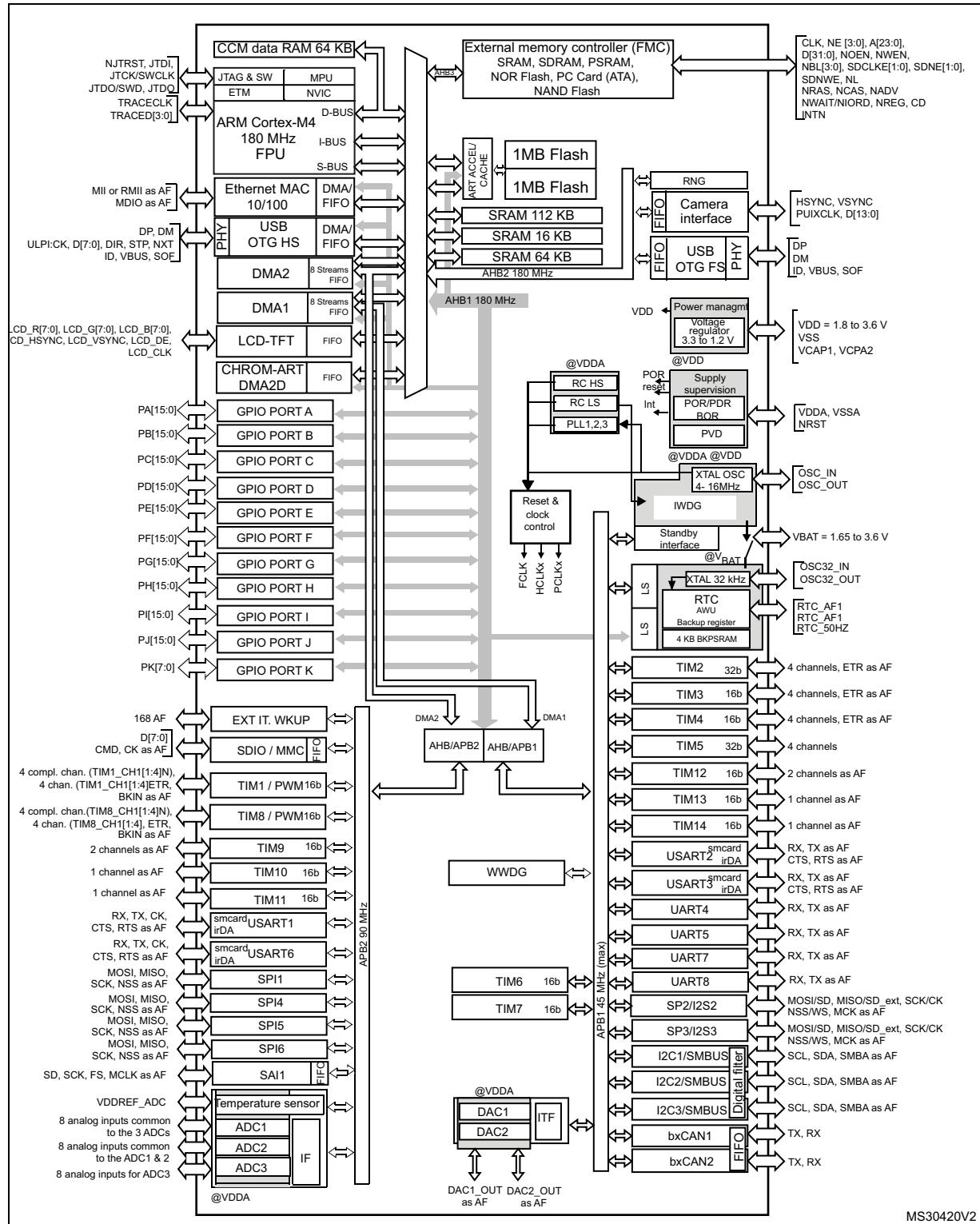
Features	Benefits
High performance <ul style="list-style-type: none"> – Up to 180 MHz/225 DMIPS Cortex-M4 with single cycle DSP MAC and floating point unit – CoreMark score: 608 at 180 MHz – CoreMark/MHz: 3.37 	<ul style="list-style-type: none"> – Boosted execution of control algorithms – More features for your applications – Ease of use – Better code efficiency – Faster time to market – Elimination of scaling and saturation – Easier support for meta-language tools
Maximum integration <ul style="list-style-type: none"> – Up to 2 Mbytes of on-chip dual bank Flash memory, up to 256 Kbytes of SRAM, reset circuit, internal RCs, PLLs, ultra-small packages (WLCSP) 	<ul style="list-style-type: none"> – Read while write operations support – More features in space-constrained applications – Use of high-level languages: Java, .Net
Designed for high performance and ultra-fast data transfers <ul style="list-style-type: none"> – ART Accelerator™: memory accelerator – Chrom-ART Accelerator™: graphic accelerator (rectangle filling, rectangle copy with pixel format conversion and blending) 	<ul style="list-style-type: none"> – Performance equivalent to zero-wait execution from Flash – Graphic content is created twice as fast and independently from the CPU
<ul style="list-style-type: none"> – 32-bit, 7-layer AHB bus matrix with up to 10 masters and 8 slaves including 3 blocks of SRAM – Multi DMA controllers: 2 general-purpose, 1 for USB HS, one for Ethernet 	Concurrent execution and data transfer
<ul style="list-style-type: none"> – One 4th SRAM block dedicated to the core 	Simplified resource allocation
<ul style="list-style-type: none"> – Flexible memory interface with SDRAM support: up to 90 MHz, 32-bit parallel 	<ul style="list-style-type: none"> – High bandwidth for external memories – Cost-effective external RAM

Table 2. Features and benefits (continued)

Features	Benefits
Outstanding power efficiency <ul style="list-style-type: none"> – Ultra-low dynamic power in Run mode: 260 μA/MHz at 180 MHz running CoreMark benchmark from Flash memory (peripherals off) – RTC <1 μA typ in V_{BAT} mode – Down to 100 μA typ in Stop mode – 3.6 V down to 1.7 V V_{DD} – 1.2 V voltage regulator with power scaling capability 	Extra flexibility to reduce power consumption for applications requiring both high-processing and low-power performance when running at low voltage or on a rechargeable battery
Superior and innovative peripherals and connectivity <ul style="list-style-type: none"> – Connectivity: camera interface, crypto/hash HW processor with AES GCM and CCM support, and SHA-256 – Ethernet MAC10/100 with IEEE 1588 v2 support, 2 USB OTG (one with HS support) – Up to 20 communication interfaces (including 4x USART + 4x UART, 6x SPI, 3x I²C with digital filter, 2x CAN, SDIO) – USART at 11.25 Mbit/s; SPI at 45 Mbit/s 	New possibilities to connect and communicate high-speed data
Audio: <ul style="list-style-type: none"> – dedicated audio PLL, 2x I²S and 1x SAI with TDM⁽¹⁾ support 	High-quality multi-channel audio support
<ul style="list-style-type: none"> – LCD TFT controller – Up to SVGA format (800 x 600) – Up to 24-bit RGB parallel pixel output – 2-layer support with blending 	Support for cost-effective standard displays
Analog: <ul style="list-style-type: none"> – 2x 12-bit DACs, 3x 12-bit ADCs reaching 7.2 MSPS in interleaved mode – Up to 17 timers: 16 and 32 bits running up to 180 MHz 	More precision thanks to high resolution
High integration <ul style="list-style-type: none"> – WLCSP143 4.5 x 5.5 mm, 2-Mbyte Flash/256-Kbyte SRAM) 	Smaller board space allowing for smaller applications
Extensive tools and software solutions <ul style="list-style-type: none"> – Hardware sector protection with execute only access – Various IDE, starter kits, libraries, RTOS and stacks, either open source or provided by ST or 3rd parties, including the ARM CMSIS DSP library optimized for Cortex-M4 instructions 	<ul style="list-style-type: none"> – Software IP protection – A wide choice within the STM32 ecosystem to develop your applications

1. TDM: time division multiplex

Figure 5. STM32F429ZIT6 block diagram



MS30420V2

4.2 Embedded ST-LINK/V2

The ST-LINK/V2 programming and debugging tool is integrated on the STM32F429 Discovery board. The embedded ST-LINK/V2 can be used in 2 different ways according to the jumper states (see [Table 3](#)):

- Program/debug the MCU on board,
- Program/debug an MCU in an external application board using a cable connected to SWD connector CN3.

The embedded ST-LINK/V2 supports only SWD for STM32 devices. For information about debugging and programming features, refer to user manual UM1075 (ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32) which describes in detail all the ST-LINK/V2 features.

Figure 6. Typical configuration

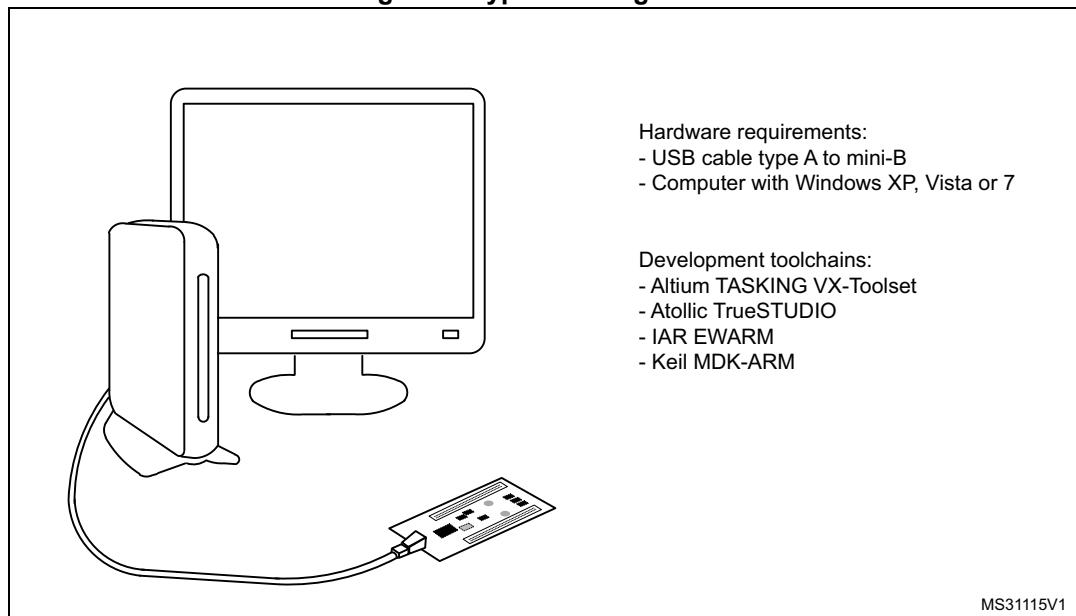


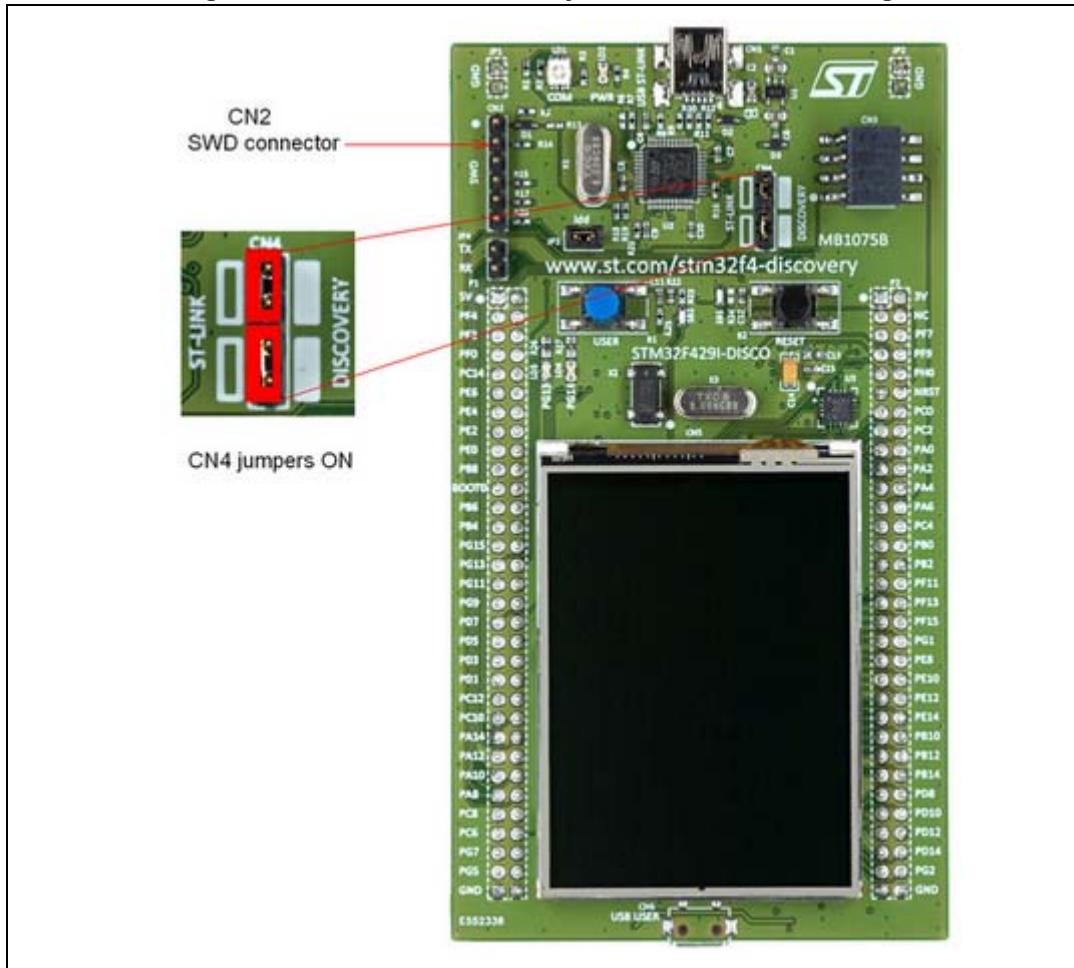
Table 3. Jumper states

Jumper state	Description
Both CN4 jumpers ON	ST-LINK/V2 functions enabled for on-board programming (default)
Both CN4 jumpers OFF	ST-LINK/V2 functions enabled for application through external CN3 connector (SWD supported)

4.2.1 Using ST-LINK/V2 to program/debug the STM32F429ZIT6 on board

To program the STM32F429ZIT6 on board, simply plug in the two jumpers on CN4, as shown in *Figure 7* in red, but do not use the CN3 connector as that could disturb the communication with the STM32F429ZIT6 of the STM32F429 Discovery board.

Figure 7. STM32F429 Discovery board connections image



4.2.2 Using ST-LINK/V2 to program/debug an external STM32 application

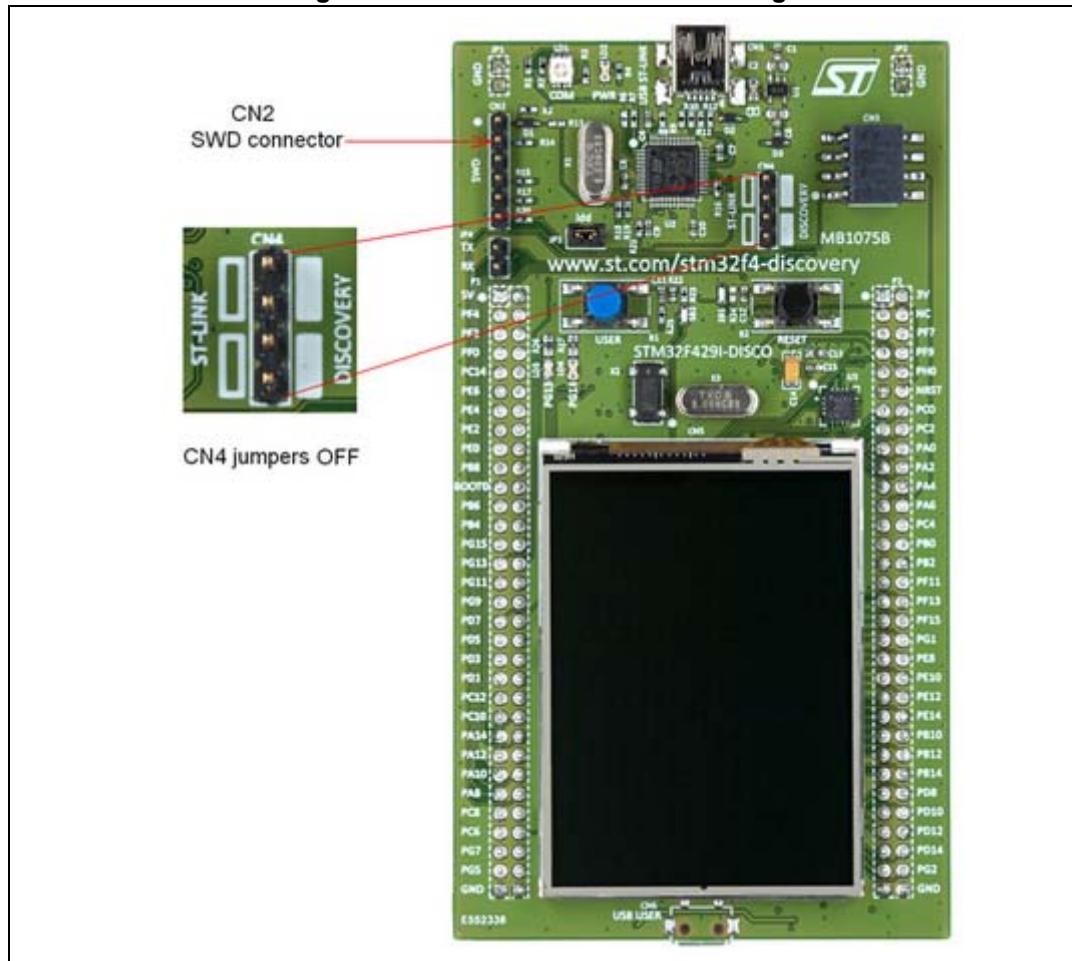
It is very easy to use the ST-LINK/V2 to program the STM32 on an external application. Simply remove the two jumpers from CN4 as shown in [Figure 8](#), and connect your application to the CN3 debug connector according to [Table 4](#).

Note: SB7 must be OFF if you use CN2 pin 5 in your external application.

Table 4. Debug connector CN2 (SWD)

Pin	CN2	Designation
1	VDD_TARGET	VDD from application
2	SWCLK	SWD clock
3	GND	Ground
4	SWDIO	SWD data input/output
5	NRST	RESET of target MCU
6	SWO	Reserved

Figure 8. ST-LINK/V2 connections image



4.3 Power supply and power selection

The power supply is provided either by the host PC through the USB cable, or by an external 5 V power supply.

The D1 and D2 diodes protect the 5 V and 3 V pins from external power supplies:

- 5 V and 3 V can be used as output power supplies when another application board is connected to pins P1 and P2.

In this case, the 5 V and 3 V pins deliver a 5 V or 3 V power supply and the power consumption must be lower than 100 mA.

- 5 V and 3 V can also be used as input power supplies, e.g. when the USB connectors are not connected to the PC.

In this case, the STM32F429 Discovery board must be powered by a power supply unit or by an auxiliary equipment complying with standard EN-60950-1: 2006+A11/2009, and must be Safety Extra Low Voltage (SELV) with limited power capability.

Note: *The board can also be powered through the USB USER connector and is protected by D4 and D5 diodes when both USBs are connected (in which case, the 5 V power is around 4.4 volts).*

4.4 LEDs

- LD1 COM:
LD1 default status is red. LD1 turns to green to indicate that communications are in progress between the PC and the ST-LINK/V2.
- LD2 PWR:
The red LED indicates that the board is powered.
- User LD3:
The green LED is a user LED connected to the I/O PG13 of the STM32F429ZIT6.
- User LD4:
The red LED is a user LED connected to the I/O PG14 of the STM32F429ZIT6.
- User LD5:
The green LED indicates when VBUS is present on CN6 and is connected to PB13 of the STM32F429ZIT6.
- User LD6:
The red LED indicates an overcurrent from VBUS of CN6 and is connected to the I/O PC5 of the STM32F429ZIT6.

4.5 Pushbuttons

- B1 USER:
User and Wake-Up button connected to the I/O PA0 of the STM32F429ZIT6.
- B2 RESET:
The pushbutton connected to NRST is used to RESET the STM32F429ZIT6.

4.6 USB OTG supported

The STM32F429ZIT6 is used to drive only USB OTG full speed on this board. The USB micro-AB connector (CN6) allows the user to connect a host or device component, such as a USB key, mouse, and so on.

Two LEDs are dedicated to this module:

- LD5 (green LED) indicates when VBUS is active
- LD6 (red LED) indicates an overcurrent from a connected device.

4.7 Gyroscope MEMS (ST MEMS L3GD20)

The L3GD20 is an ultra-compact, low-power, three-axis angular rate sensor. It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through the I2C/SPI serial interface.

The L3GD20 has dynamically user-selectable full scales of ± 250 dps/ 500 dps/ ± 2000 dps and is capable of measuring rates.

The STM32F429ZIT6 MCU controls this motion sensor through the SPI interface.

4.8 TFT LCD (Thin-film-transistor liquid-crystal display)

The TFT LCD is a 2.41" display of 262 K colors. Its definition is QVGA (240 x 320 dots) and is directly driven by the STM32F429ZIT6 using the RGB protocol. It includes the ILI9341 LCD controller and can operate with a 2.8 ± 0.3 V voltage.

The STM32F429ZIT6 MCU controls this motion sensor through the SPI interface.

4.9 64-Mbit SDRAM (1Mbit x 16-bit x 4-bank)

The 64-Mbit SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3 V memory systems containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface. Each 16,777,216-bit bank is organized as 4,096 rows by 256 columns by 16 bits. The 64-Mbit SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK.

The STM32F429ZIT6 MCU reads and writes data at 80 MHz.

4.10 JP3 (Idd)

Jumper JP3, labeled Idd, allows the consumption of STM32F429ZIT6 to be measured by removing the jumper and connecting an ammeter.

- Jumper on: STM32F429ZIT6 is powered (default).
- Jumper off: an ammeter must be connected to measure the STM32F429ZIT6 current, (if there is no ammeter, the STM32F429ZIT6 is not powered).

4.11 OSC clock

4.11.1 OSC clock supply

The following information indicates all configurations for clock supply selection.

- **MCO from ST-LINK** (from MCO of the STM32F429ZIT6)
This frequency cannot be changed, it is fixed at 8 MHz and connected to PH0-OSC_IN of the STM32F429ZIT6. The configuration needed is:
 - SB18 closed, SB19 open, R56 removed
 - SB20, R57, C20, C21, X3 = don't care
- **Oscillator onboard** (from X3 crystal)
For typical frequencies and its capacitors and resistors, please refer to the STM32F429ZIT6 Datasheet. The configuration needed is:
 - SB18, SB19, SB20 open
 - -R56, R57, C20, C21, X3 soldered
- **Oscillator from external PH0** (from external oscillator through pin 10 of the P2 connector)
The configuration needed is:
 - SB19 closed, SB18 open, R56 removed
 - SB20, R57, C20, C21, X3 = don't care
- **No external oscillator** (from Internal oscillator HSI only).
PH0 and PH1 can be used as GPIO. The configuration needed is:
 - SB18 open, SB19 closed, SB20 closed, R56 removed, R57 removed
 - C20, C21, X3 = don't care

4.11.2 OSC 32 KHz clock supply

The following information indicates all configurations for the 32 kHz clock supply selection.

- **Oscillator on board** (from X2 Crystal, not provided).
The configuration needed is:
 - SB16 open, SB17 open.
 - R53, R54, C23, C24, X2 soldered.
- **Oscillator from external PC14** (from external oscillator through pin 9 of P1 connector)
The configuration needed is:
 - SB16 closed, R53 removed
 - SB17, R54, C23, C24, X2 = don't care
- **No external oscillator** (PC14 and PC15 can be used as GPI).
The configuration needed is:
 - SB16 closed, SB17 closed, R53 removed, R54 removed.
 - C23, C24, X2 = don't care.

4.12 Solder bridges

Table 5. Solder bridges

Bridge	State ⁽¹⁾	Description
SB19,20 (X3 crystal)	OFF	X3, C20, C21, R56 and R57 provide a clock. PH0, PH1 are disconnected from P2
	ON	PH0, PH1 are connected to P2. Remove only R56 and R57
SB4,6,8,14 (default)	ON	Reserved, do not modify
SB3,5,7,13 (reserved)	OFF	Reserved, do not modify
SB22,23,24,25	OFF	Reserved, do not modify
SB16,17 (X2 crystal)	OFF	X2, C23, C24, R53 and R54 deliver a 32 KHz clock. PC14, PC15 are not connected to P2
	ON	PC14, PC15 are only connected to P2 Remove only R53 and R54
SB1 (B2-RESET)	ON	B2 Push Button is connected to NRST of STM32F429ZIT6
	OFF	B2 Push Button is not connected to NRST of STM32F429ZIT6
SB2 (B1-USER)	ON	B1 Push Button is connected to PA0
	OFF	B1 Push Button is not connected to PA0
SB11,15 (RX,TX)	OFF	Reserved, do not modify
	ON	Reserved, do not modify
SB12 (NRST)	ON	NRST signal of connector CN2 is connected to NRST of STM32F429ZIT6
	OFF	NRST signal is not connected
SB9 (SWO)	OFF	SWO signal is not connected
	ON	SWO signal of connector CN3 is connected to PB3
SB10 (STM_RST)	OFF	No incidence on NRST signal of STM32F429ZIT6
	ON	NRST signal of STM32F429ZIT6 is connected to GND
SB21 (BOOT0)	ON	BOOT0 signal of STM32F429ZIT6 is at level "0" through 510 Ω pull-down
	OFF	BOOT0 signal of STM32F429ZIT6 is at level "1" through 10 KΩ pull-up (not provided)
SB26,27 (USB OTG)	OFF	PB14 and PB15 are only used for USB OTG and not connected to P2 to avoid noise
	ON	PB14 and PB15 are connected to P2.
SB18 (MCO)	OFF	MCO signal of STM32F429ZIT6 is not used
	ON	MCO clock signal from STM32F429ZIT6 is connected to OSC_IN of STM32F429ZIT6

1. Default SBx state is shown in bold.

4.13 Extension connectors

The male headers P1 and P2 can connect the STM32F429 Discovery board to a standard prototyping/wrapping board. STM32F429ZIT6 GPIOs are available on these connectors. P1 and P2 can also be probed by an oscilloscope, a logical analyzer or a voltmeter.

Table 6. MCU pin description versus board function (page 1 of 7)

MCU pin	Board function																					
	Main function	LQFP144	System	SDRAM	LCD-TFT	LCD-RGB	LCD-SPI	INT1	INT2	USB	LED	Puchbutton	ACP/RF	Touch panel	Free I/O	Power supply	CN2	CN3	CN6	P1	P2	
BOOT0	138	NRST	BOOT0																	21		
NRST	25						RESET		RESET												12	
PA0	34											B1	B2									18
PA1	35																					17
PA2	36																					20
PA3	37					VSYNC	DB3															19
PA4	40					DB6																22
PA5	41					G2	VSYNC	B5														21
PA6	42																					24
PA7	43																					23
PA8	100																		3		53	
PA9	101																					52
PA10	102																					51
PA11	103																					50
PA12	104					R5	R4															49
PA13	105	SWDIO				DB15	DB14															48
										SCL	ACP_RST											

Table 6. MCU pin description versus board function (page 2 of 7)

MCU pin		Board function																	
Main function	LQFP144	SWCLK	System	SDRAM	LCD-TFT	LCD-SPI	LCD-RGB	LED	Puchbutton	ACP/RF	INT	Touch panel	Free I/O	Power supply	CN2	CN3	CN6	P1	P2
PA14	109													2			47		
PA15	110																46		
PB0	46																28		
PB1	47																27		
PB2	48		SWO BOOT1														30		
PB3	133													6			28		
PB4	134																25		
PB5	135			SDNE1 SDCKE1													26		
PB6	136																23		
PB7	137																24		
PB8	139				DB9 DB8 DB5 DB4												19		
PB9	140				G5 G4 B7 B6												20		
PB10	69																48		
PB11	70																47		
PB12	73														4		50		
PB13	74							Green								1		49	
PB14	75														2		52 ⁽¹⁾		
PB15	76														3		51 ⁽²⁾		
PC0	26			SDNWE													14		

Table 6. MCU pin description versus board function (page 3 of 7)

MCU pin		Board function																		
Main function	LQFP144	System	SDRAM	LCD-TFT	LCD-RGB	LCD-SPI	L3GD20	USB	LED	Puchbutton	ACP/RF	Touch panel	Free I/O	Power supply	CN2	CN3	CN6	P1	P2	
PC1	27																		13	
PC2	28					CSX													16	
PC3	29																		15	
PC4	44																		26	
PC5	45																		25	
PC6	96																		57	
PC7	97					DB10	H SYNC												56	
PC8	98																		55	
PC9	99								QC PSO							1		54		
PC10	111					DB12													45	
PC11	112																		44	
PC12	113																		43	
PC13	7																		12	
PC14	8	OSC32_OUT	OSC32_IN																	9
PC15	9																			10
PD0	114		D3 D2																	42
PD1	115		D3																	41
PD2	116																			40
PD3	117					DB11														39
PD4	118																			38
PD5	119																			37

Table 6. MCU pin description versus board function (page 4 of 7)

MCU pin		Board function														
Main function	LQFP144	System	SDRAM													
PD6	122							DB0	LCD-TFT							36
PD7	123								B2	LCD-RGB						35
PD8	77			D15	D14	D13										54
PD9	78															53
PD10	79															56
PD11	80															55
PD12	81															58
PD13	82															57
PD14	85															60
PD15	86															59
PE0	141		NBL1	NBL0	D1	D0										17
PE1	142															18
PE2	1															15
PE3	2															16
PE4	3															13
PE5	4															14
PE6	5															11
PE7	58															37
PE8	59															40
PE9	60															39
PE10	63															42
PE11	64															41
PE12	65															44
PE13	66															43
PE14	67															46

Table 6. MCU pin description versus board function (page 5 of 7)

MCU pin		Board function																													
Main function	LQFP144	System		SDRAM		LCD-TFT		LCD-RGB		LED		Pushbutton		ACP/RF		Touch panel		Free I/O		Power supply		CN2		CN3		CN6		P1		P2	
PE15	68																											45			
PF0	10																											7			
PF1	11																											8			
PF2	12																											5			
PF3	13					A5	A4	A3	A2	A1	A0	D12														6					
PF4	14																											3			
PF5	15																											4			
PF6	18																											3			
PF7	19							DCX																				6			
PF8	20																											5			
PF9	21							SDA																				8			
PF10	22							DE																				7			
PF11	49																											32			
PF12	50																											31			
PF13	53																											34			
PF14	54																											33			
PF15	55																											36			
PG0	56																											35			
PG1	57																											38			
PG2	87																											62			
PG3	88																											61			
PG4	89																											62			
PG5	90																											61			

Table 6. MCU pin description versus board function (page 6 of 7)

MCU pin		Board function																	
Main function	LQFP144	System	SDRAM	SDCLK	DOTCLK	DB17	LCD-TFT	LCD-RGB	LCD-SPI	Pushbutton	ACP/RF	Touch panel	Free I/O	Power supply	CN2	CN3	CN6	P1	P2
PG6	91																	60	
PG7	92																	59	
PG8	93																	58	
PG9	124																	33	
PG10	125																	34	
PG11	126																	31	
PG12	127																	32	
PG13	128																	29	
PG14	129																	30	
PG15	132																	27	
PH0	23	OSC_IN	OSC_OUT	OSC_IN															10
PH1	24																		9
																		22	
																		5	
																			1
																			2
																		8	
																		1	
																		2	
														GND	5 V	3 V	VDD		
														3	7	5	63	11	

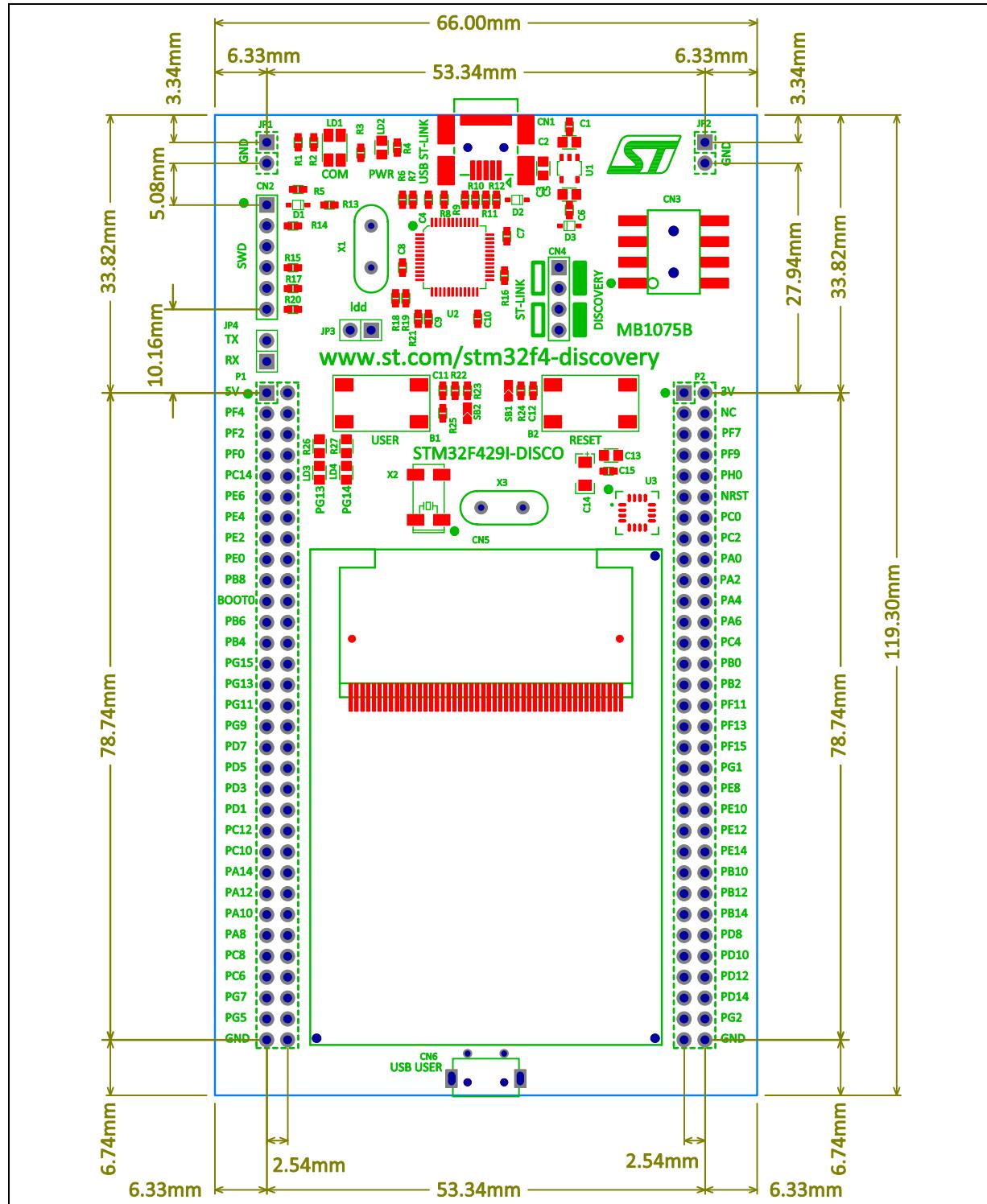
Table 6. MCU pin description versus board function (page 7 of 7)

MCU pin		Board function																	
Main function	LQFP144	System	SDRAM	LCD-TFT	LCD-RGB	LCD-SPI	L3GD20	USB	LED	Pushbutton	ACP/RF	Touch panel	Free I/O	Power supply	CN2	CN3	CN6	P1	P2
																	64	29	
																		63	
																		64	

1. If SB27 is On.
2. If SB26 is On.

5 Mechanical drawing

Figure 9. STM32F429 Discovery board mechanical drawing



6 Electrical schematics

Figure 10. STM32F429 Discovery board

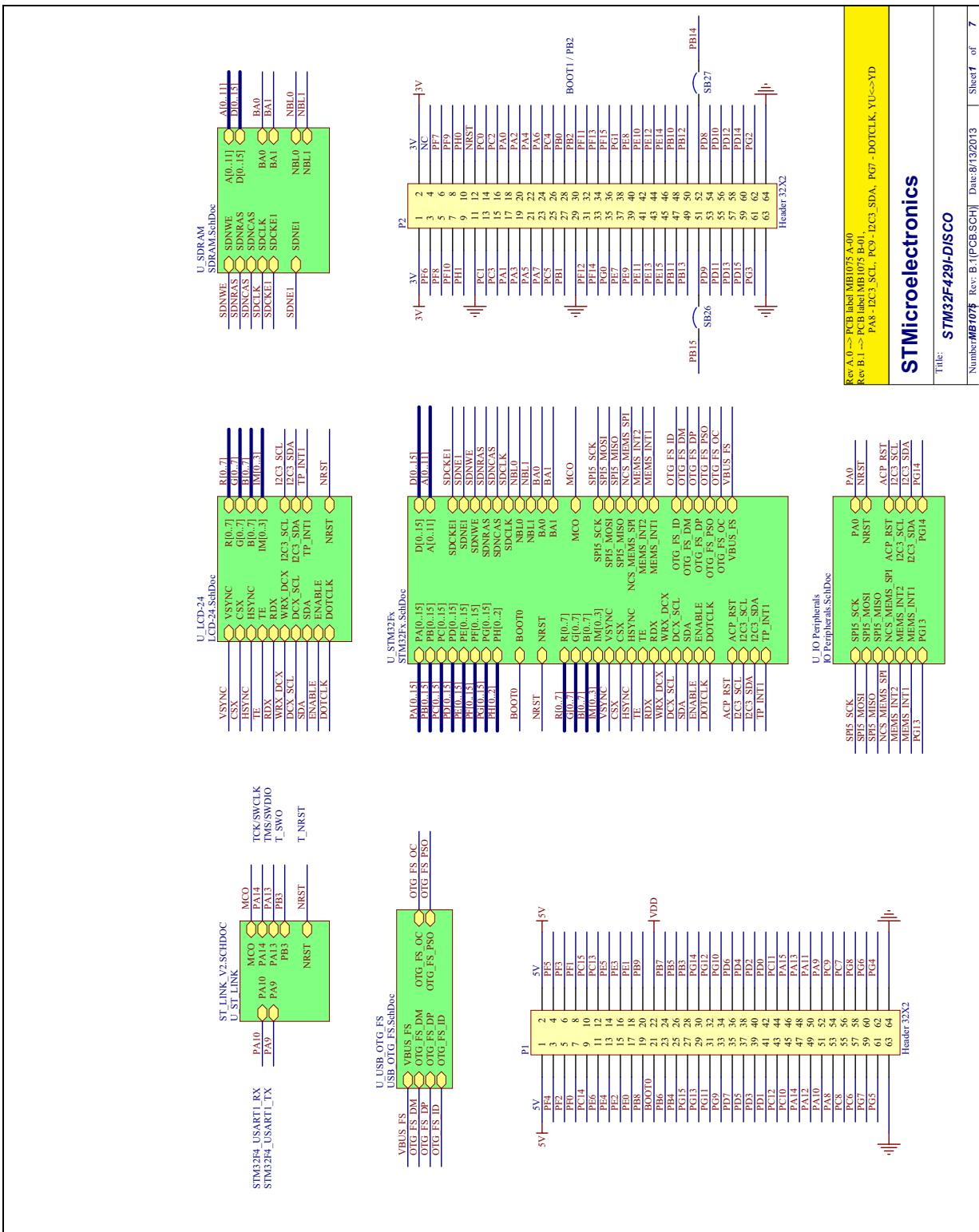


Figure 11. ST-LINK/V2 (SWD only)

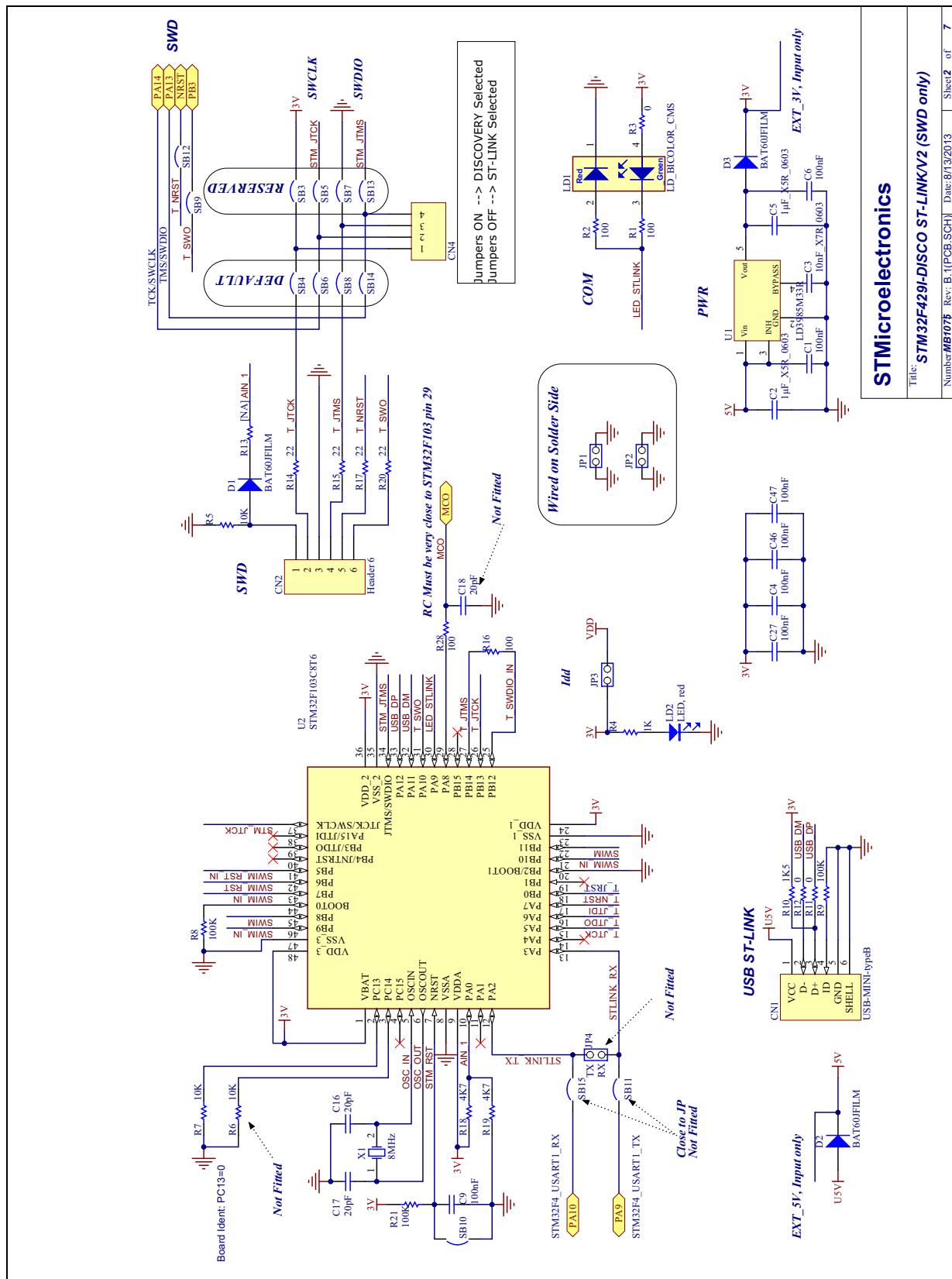


Figure 12. USB OTG_FS

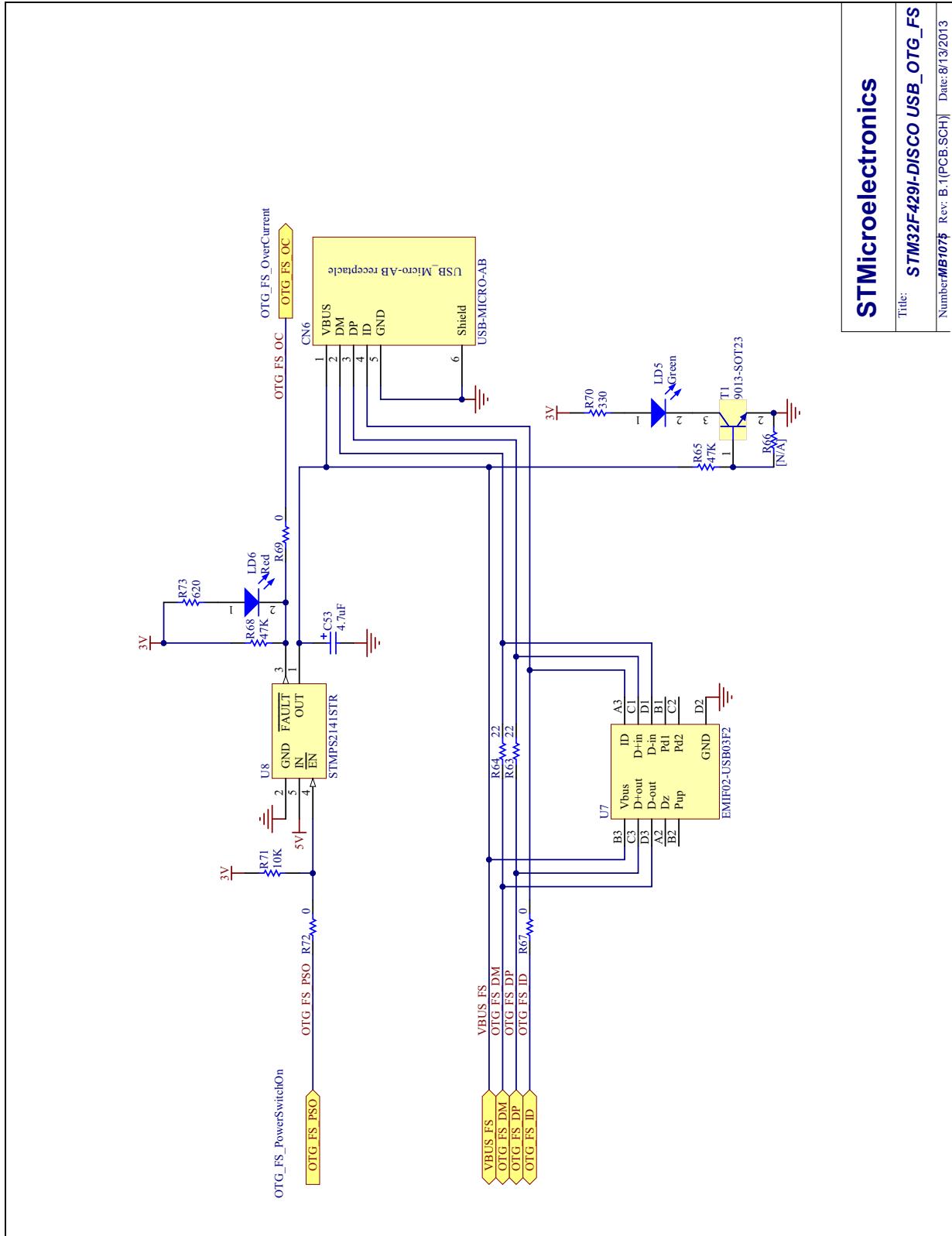


Figure 13. SDRAM 64 Mbits

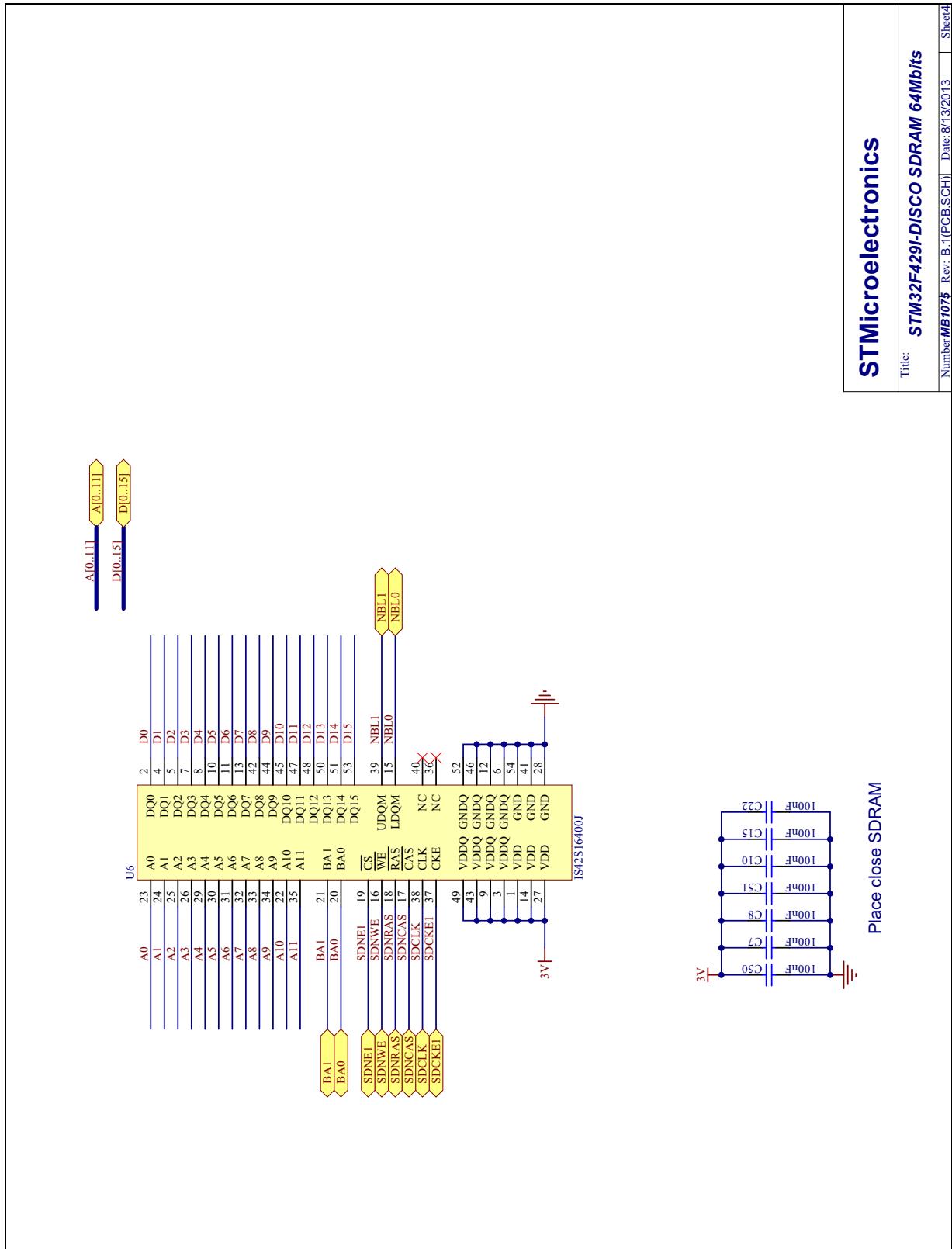


Figure 14. STM32F429ZIT6 MCU

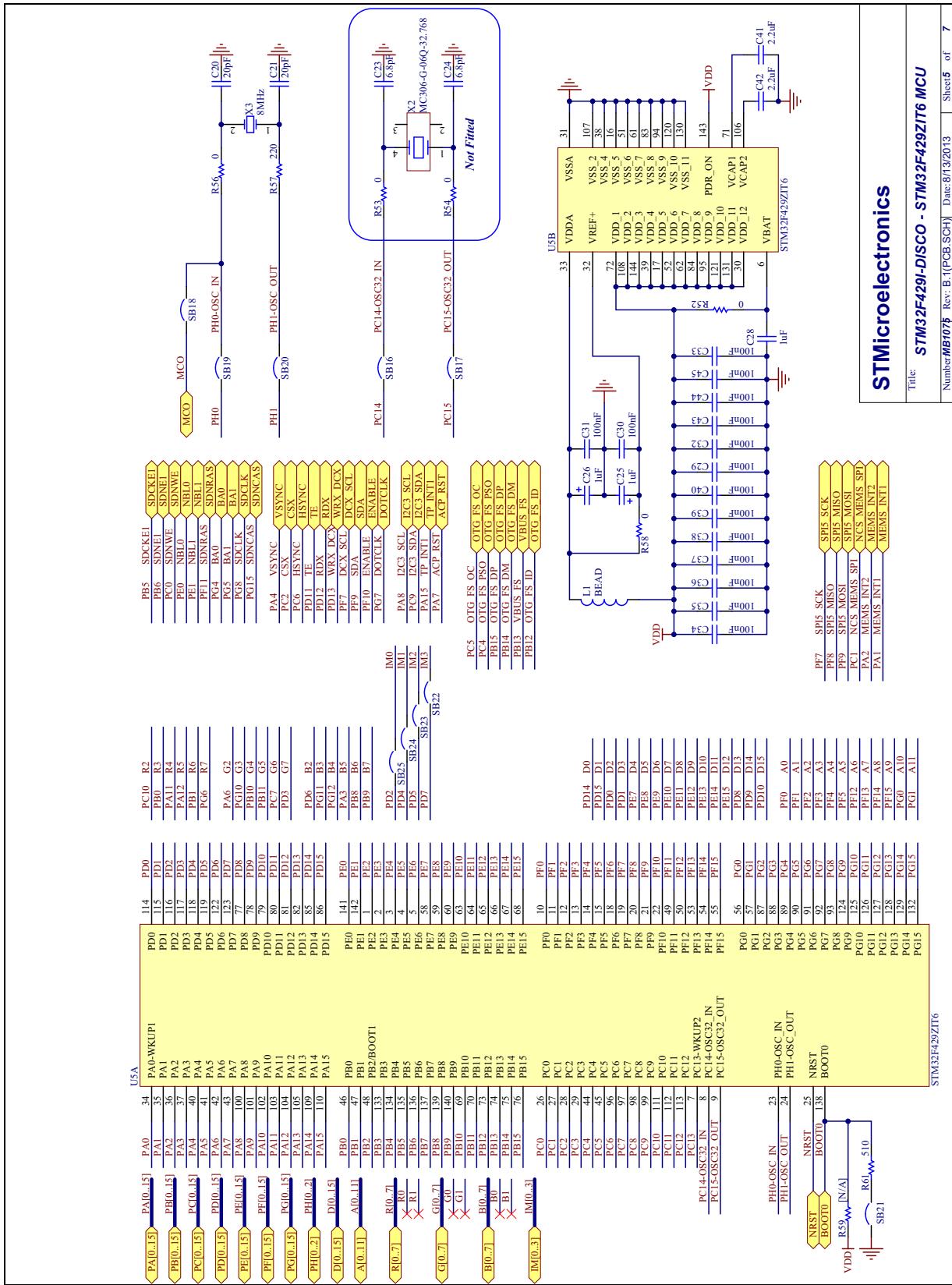


Figure 15. Peripherals

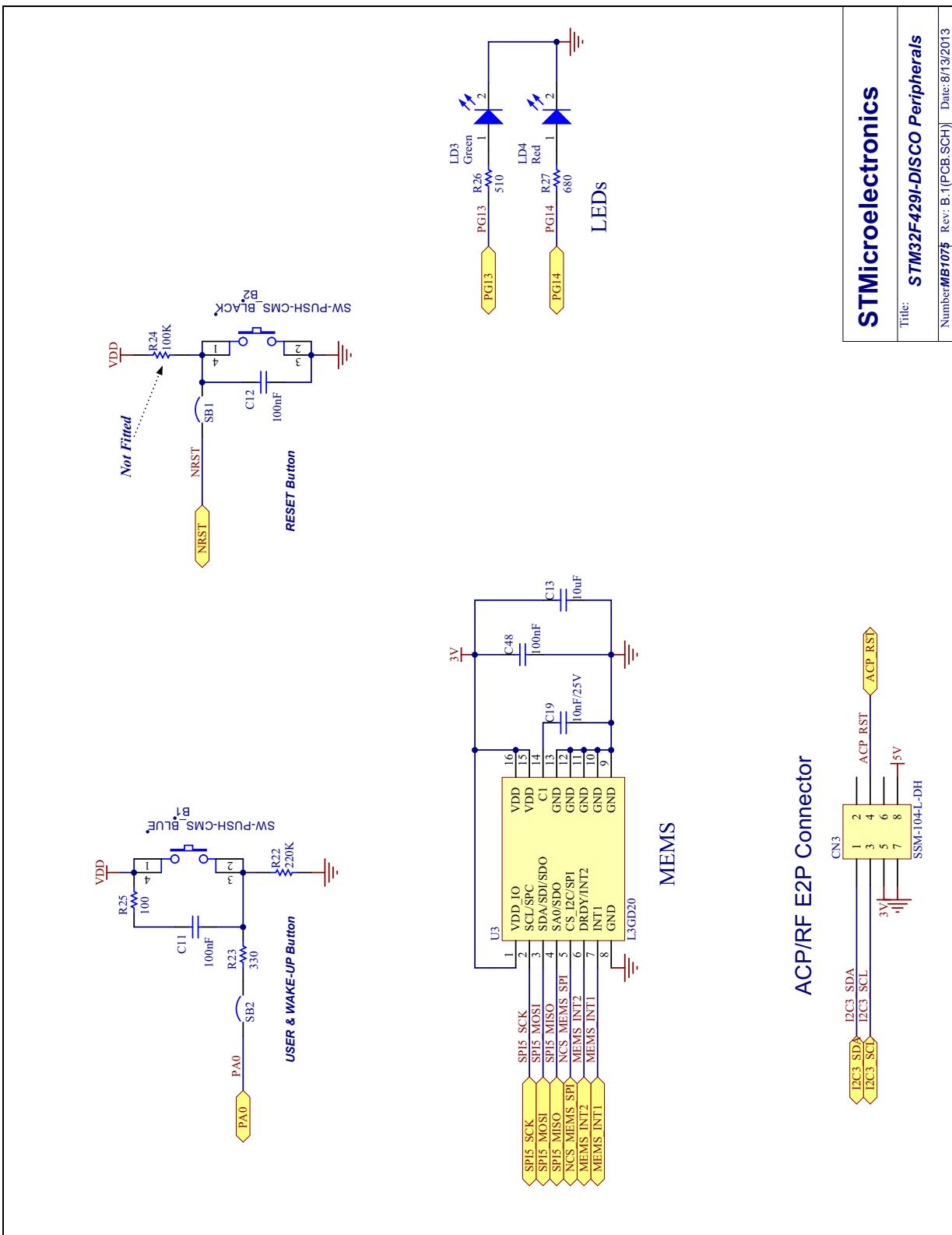
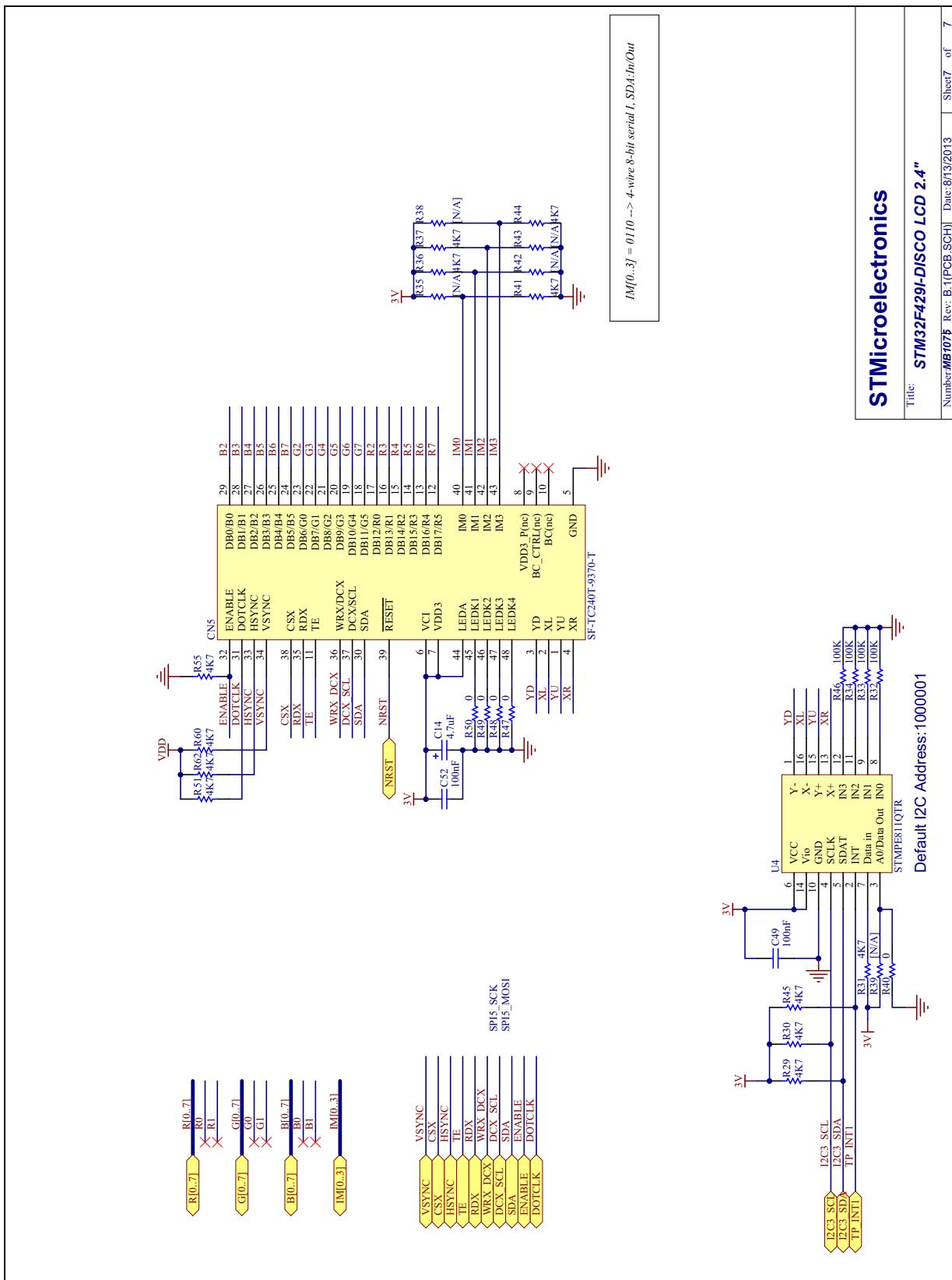


Figure 16. LCD 2.4"



7 Revision history

Table 7. Document revision history

Date	Revision	Changes
10-Sep-2013	1	Initial release.

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5.2. Hoja de datos del ILI4391

**a-Si TFT LCD Single Chip Driver
240RGBx320 Resolution and 262K color**

Specification

Version: V1.11
Document No.: ILI9341_DS_V1.11.pdf

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1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

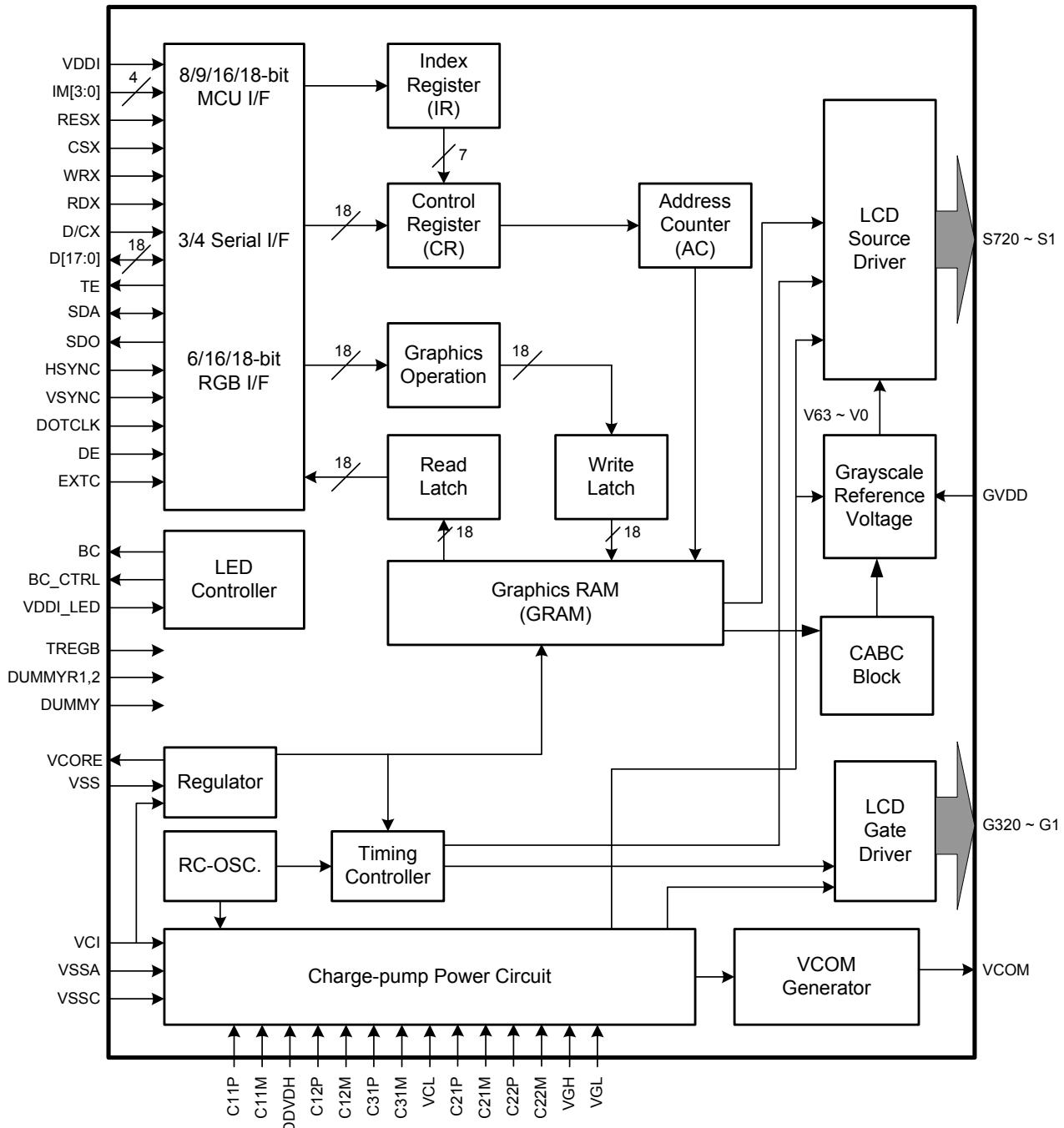
ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- ◆ Display resolution: [240xRGB](H) x 320(V)
- ◆ Output:
 - 720 source outputs
 - 320 gate outputs
 - Common electrode output (VCOM)
- ◆ a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- ◆ System Interface
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
 - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
 - 3-line / 4-line serial interface
- ◆ Display mode:
 - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
 - Reduce color mode (Idle mode ON): 8-color
- ◆ Power saving mode:
 - Sleep mode
- ◆ On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
 - 1 preset Gamma curve with separate RGB Gamma correction
- ◆ Content Adaptive Brightness Control
- ◆ MTP (3 times):
 - 8-bits for ID1, ID2, ID3
 - 7-bits for VCOM adjustment

- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3V (logic)
 - **VCI = 2.5V ~ 3.3V** (analog)
 - ◆ LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 5.8V
 - VCL - GND = -1.5V ~ -2.5V
 - Gate driver output voltage
 - VGH - GND = 10.0V ~ 18.0V
 - VGL - GND = -5.0V ~ -10.0V
 - VGH - VGL \leq 28V
 - VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH – 0.2)V
 - VCOML = (VCL+0.2)V ~ 0V
 - VCOMH - VCOML \leq 6.0V
 - ◆ Operate temperature range: -40°C to 85°C
 - ◆ a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDDI	I	P	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VDDI_LED	I		Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
Vcore	O	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I	I/O Ground	System ground level for I/O circuits.
VSS	I	Digital Ground	System ground level for logic blocks
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

Interface Logic Signals									
Pin Name	I/O	Type	Descriptions						
IM[3:0]	I	(VDDI/VSS)	- Select the MCU interface mode						
			IM3	IM2	IM1	IM0	MCU-Interface Mode		
			0	0	0	0	80 MCU 8-bit bus interface I		
			0	0	0	1	80 MCU 16-bit bus interface I		
			0	0	1	0	80 MCU 9-bit bus interface I		
			0	0	1	1	80 MCU 18-bit bus interface I		
			0	1	0	1	3-wire 9-bit data serial interface I		
			0	1	1	0	4-wire 8-bit data serial interface I		
			1	0	0	0	80 MCU 16-bit bus interface II		
			1	0	0	1	80 MCU 8-bit bus interface II		
			1	0	1	0	80 MCU 18-bit bus interface II		
			1	0	1	1	80 MCU 9-bit bus interface II		
			1	1	0	1	3-wire 9-bit data serial interface II		
			1	1	1	0	4-wire 8-bit data serial interface II		
MPU Parallel interface bus and serial interface select					SDI: In	SDO: Out			
If use RGB Interface must select serial interface.					SDI: In	SDO: Out			
* : Fix this pin at VDDI or VSS.									

RESX	I	MCU (VDDI/VSS)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
EXTC	I	MCU (VDDI/VSS)	Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted. Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2
D/CX (SCL)	I	MCU (VDDI/VSS)	This pin is used to select "Data or Command" in the parallel interface or 4-wire 8-bit serial data interface. When DCX = '1', data is selected. When DCX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSS.
RDX	I	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.
WRX (D/CX)	I	MCU (VDDI/VSS)	- 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use
SDI/SDA	I/O	MCU (VDDI/VSS)	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
SDO	O	MCU (VDDI/VSS)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/VSS)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.

Note.

1. If CSX is connected to VSS in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.
2. When CSX='1', there is no influence to the parallel and serial interface.

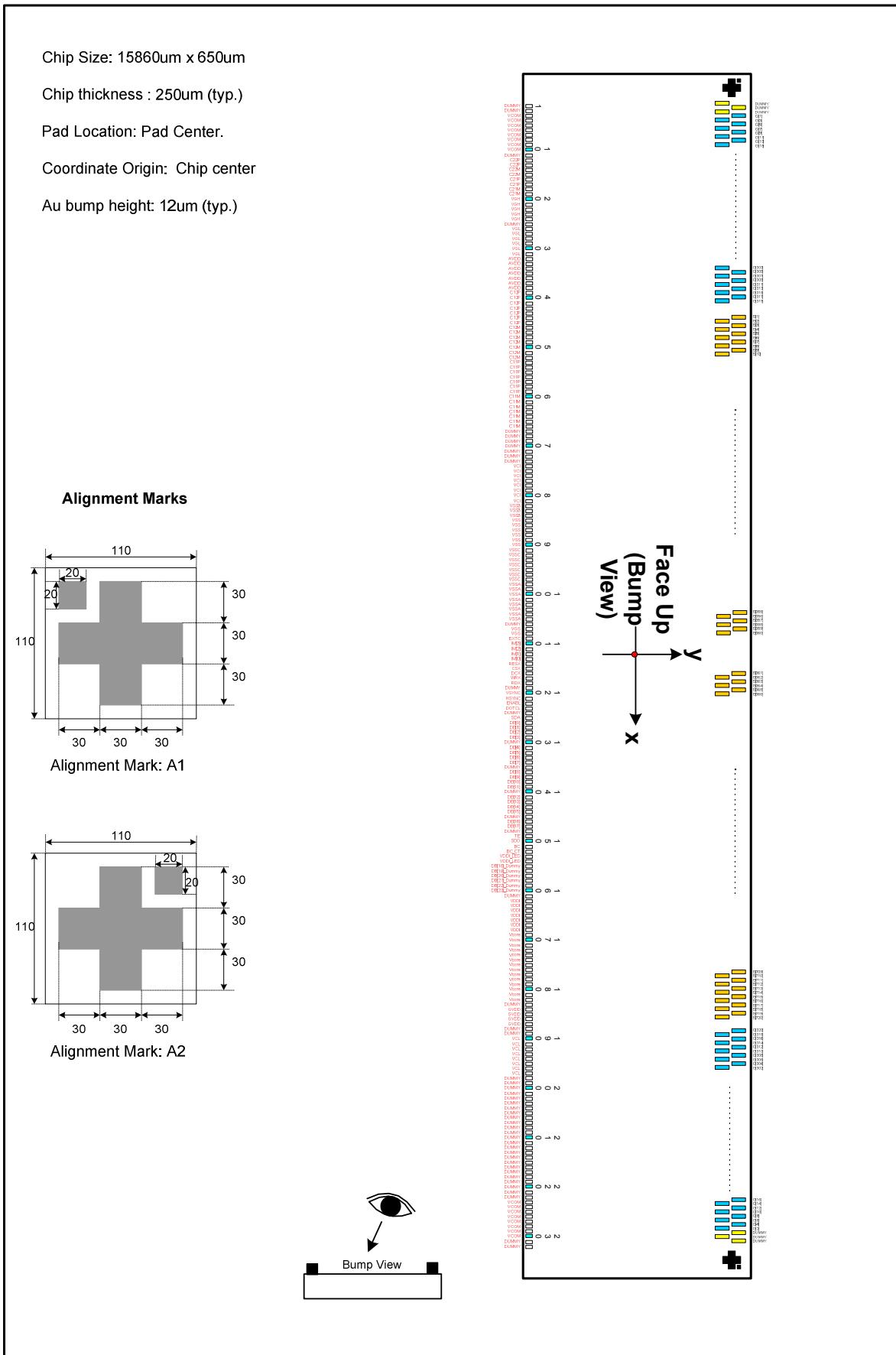
LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S720~S1	O	Source	Source output signals.. <i>Leave the pin to open when not in use.</i>
G320~G1	O	Gate	Gate output signals. <i>Leave the pin to open when not in use.</i>
DDVDH	O	Power Stabilizing capacitor	Output voltage of 1st step up circuit (2 x VCI). Input voltage to 2nd step up circuit. Generated power output pad for source driver block. Connect this pad to the capacitor for stabilization.
VGH	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGH level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VGL	O	Power Stabilizing capacitor	Power supply for the gate driver. Adjust the VGL level with the BT[2:0] bits. Connect this pad with a stabilizing capacitor.
VCL	O	Power Stabilizing capacitor	Power supply for VCOML. VCL = 0~ - VCI Connect this pad with a stabilizing capacitor.
C11P, C11M C12P, C12M	P	Stabilizing capacitor	Connect the charge-pumping capacitor for generating DDVDH level.
C21P, C21M C22P, C22M	P	Stabilizing capacitor	Connect the charge-pumping capacitor for generating VGH, VGL level.
GVDD	O		High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VCOM	O		Power supply pad for the TFT- display counter electrode. Charge recycling method is used with VCI and VSSA voltage. Connect this pad to the TFT-display counter electrode.
LEDPWM	O		Output pin for PWM (Pulse Width Modulation) signal of LED driving. If not used, open this pad.
LEDON	O		Output pin for enabling LED driving. If not used, open this pad.

Test Pins			
Pin Name	I/O	Type	Descriptions
DUMMY	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.
INT_TEST1 INT_TEST2	-	Open	Input pads used only for test purpose at IC-side. During normal operation, leave these pads open.

Liquid crystal power supply specifications Table

No.	Item	Description
1	TFT Source Driver	720 pins (240 x RGB)
2	TFT Gate Driver	320 pins
3	TFT Display's Capacitor Structure	Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1 ~ S720 V0 ~ V63 grayscales
		G1 ~ G320 VGH - VGL
		VCOM VCOMH - VCOML: Amplitude = electronic volumes
5	Input Voltage	VDDI 1.65V ~ 3.30V
		VCI 2.50V ~ 3.30V
6	Liquid Crystal Drive Voltages	DDVDH 4.5V ~ 5.8V
		VGH 10.0V ~ 18.0V
		VGL -5.0V ~ -10.0V
		VCL -1.5V ~ -2.5V
		VGH - VGL Max. 28.0V
7	Internal Step-up Circuits	DDVDH VCI x2,
		VGH VCI x6, x7
		VGL VCI x-3, x-4,
		VCL VCI x-1

5. Pad Arrangement and Coordination



No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1	DUMMY	-7292.5	-248	51	C12M	-4292.5	-248	101	VSSA	-1292.5	-248	151	LEDPWM	2245	-248
2	DUMMY	-7232.5	-248	52	C12M	-4232.5	-248	102	VSSA	-1232.5	-248	152	LEDON	2330	-248
3	VCOM	-7172.5	-248	53	C11P	-4172.5	-248	103	VSSA	-1172.5	-248	153	VDDI_LED	2402.5	-248
4	VCOM	-7112.5	-248	54	C11P	-4112.5	-248	104	VSSA	-1112.5	-248	154	VDDI_LED	2462.5	-248
5	VCOM	-7052.5	-248	55	C11P	-4052.5	-248	105	VSSA	-1052.5	-248	155	DB[18]_Dummy	2535	-248
6	VCOM	-6992.5	-248	56	C11P	-3992.5	-248	106	DUMMY	-992.5	-248	156	DB[19]_Dummy	2620	-248
7	VCOM	-6932.5	-248	57	C11P	-3932.5	-248	107	VGS	-932.5	-248	157	DB[20]_Dummy	2705	-248
8	VCOM	-6872.5	-248	58	C11P	-3872.5	-248	108	VGS	-872.5	-248	158	DB[21]_Dummy	2790	-248
9	VCOM	-6812.5	-248	59	C11P	-3812.5	-248	109	EXTC	-812.5	-248	159	DB[22]_Dummy	2875	-248
10	VCOM	-6752.5	-248	60	C11M	-3752.5	-248	110	IM<3>	-752.5	-248	160	DB[23]_Dummy	2960	-248
11	DUMMY	-6692.5	-248	61	C11M	-3692.5	-248	111	IM<2>	-692.5	-248	161	DUMMY	3032.5	-248
12	C22P	-6632.5	-248	62	C11M	-3632.5	-248	112	IM<1>	-632.5	-248	162	VDDI	3092.5	-248
13	C22P	-6572.5	-248	63	C11M	-3572.5	-248	113	IM<0>	-572.5	-248	163	VDDI	3152.5	-248
14	C22M	-6512.5	-248	64	C11M	-3512.5	-248	114	RESX	-512.5	-248	164	VDDI	3212.5	-248
15	C22M	-6452.5	-248	65	C11M	-3452.5	-248	115	CSX	-452.5	-248	165	VDDI	3272.5	-248
16	C21P	-6392.5	-248	66	C11M	-3392.5	-248	116	DCX	-392.5	-248	166	VDDI	3332.5	-248
17	C21P	-6332.5	-248	67	(GND)	-3332.5	-248	117	WRX	-332.5	-248	167	VDDI	3392.5	-248
18	C21M	-6272.5	-248	68	(GND)	-3272.5	-248	118	RDX	-272.5	-248	168	VDDI	3452.5	-248
19	C21M	-6212.5	-248	69	(GND)	-3212.5	-248	119	DUMMY	-212.5	-248	169	Vcore	3512.5	-248
20	VGH	-6152.5	-248	70	(GND)	-3152.5	-248	120	VSYNC	-152.5	-248	170	Vcore	3572.5	-248
21	VGH	-6092.5	-248	71	(GND)	-3092.5	-248	121	HSYNC	-92.5	-248	171	Vcore	3632.5	-248
22	VGH	-6032.5	-248	72	(GND)	-3032.5	-248	122	ENABL	-32.5	-248	172	Vcore	3692.5	-248
23	VGH	-5972.5	-248	73	(GND)	-2972.5	-248	123	DOTCLK	27.5	-248	173	Vcore	3752.5	-248
24	VGH	-5912.5	-248	74	VCI	-2912.5	-248	124	DUMMY	87.5	-248	174	Vcore	3812.5	-248
25	DUMMY	-5852.5	-248	75	VCI	-2852.5	-248	125	SDA	160	-248	175	Vcore	3872.5	-248
26	VGL	-5792.5	-248	76	VCI	-2792.5	-248	126	DB[0]	245	-248	176	Vcore	3932.5	-248
27	VGL	-5732.5	-248	77	VCI	-2732.5	-248	127	DB[1]	330	-248	177	Vcore	3992.5	-248
28	VGL	-5672.5	-248	78	VCI	-2672.5	-248	128	DB[2]	415	-248	178	Vcore	4052.5	-248
29	VGL	-5612.5	-248	79	VCI	-2612.5	-248	129	DB[3]	500	-248	179	Vcore	4112.5	-248
30	VGL	-5552.5	-248	80	VCI	-2552.5	-248	130	DUMMY	572.5	-248	180	Vcore	4172.5	-248
31	VGL	-5492.5	-248	81	VCI	-2492.5	-248	131	DB[4]	645	-248	181	Vcore	4232.5	-248
32	DDVDH	-5432.5	-248	82	VSS3	-2432.5	-248	132	DB[5]	730	-248	182	Vcore	4292.5	-248
33	DDVDH	-5372.5	-248	83	VSS3	-2372.5	-248	133	DB[6]	815	-248	183	DUMMY	4352.5	-248
34	DDVDH	-5312.5	-248	84	VSS3	-2312.5	-248	134	DB[7]	900	-248	184	GVDD	4412.5	-248
35	DDVDH	-5252.5	-248	85	VSS	-2252.5	-248	135	DUMMY	972.5	-248	185	GVDD	4472.5	-248
36	DDVDH	-5192.5	-248	86	VSS	-2192.5	-248	136	DB[8]	1045	-248	186	GVDD	4532.5	-248
37	DDVDH	-5132.5	-248	87	VSS	-2132.5	-248	137	DB[9]	1130	-248	187	GVDD	4592.5	-248
38	DDVDH	-5072.5	-248	88	VSS	-2072.5	-248	138	DB[10]	1215	-248	188	DUMMY	4652.5	-248
39	C12P	-5012.5	-248	89	VSS	-2012.5	-248	139	DB[11]	1300	-248	189	DUMMY	4712.5	-248
40	C12P	-4952.5	-248	90	VSS	-1952.5	-248	140	DUMMY	1372.5	-248	190	VCL	4772.5	-248
41	C12P	-4892.5	-248	91	VSSC	-1892.5	-248	141	DB[12]	1445	-248	191	VCL	4832.5	-248
42	C12P	-4832.5	-248	92	VSSC	-1832.5	-248	142	DB[13]	1530	-248	192	VCL	4892.5	-248
43	C12P	-4772.5	-248	93	VSSC	-1772.5	-248	143	DB[14]	1615	-248	193	VCL	4952.5	-248
44	C12P	-4712.5	-248	94	VSSC	-1712.5	-248	144	DB[15]	1700	-248	194	VCL	5012.5	-248
45	C12P	-4652.5	-248	95	VSSC	-1652.5	-248	145	DUMMY	1772.5	-248	195	VCL	5072.5	-248
46	C12M	-4592.5	-248	96	VSSC	-1592.5	-248	146	DB[16]	1845	-248	196	VCL	5132.5	-248
47	C12M	-4532.5	-248	97	VSSC	-1532.5	-248	147	DB[17]	1930	-248	197	VCL	5192.5	-248
48	C12M	-4472.5	-248	98	VSSA	-1472.5	-248	148	DUMMY	2002.5	-248	198	DUMMY	5252.5	-248
49	C12M	-4412.5	-248	99	VSSA	-1412.5	-248	149	TE	2075	-248	199	DUMMY	5312.5	-248
50	C12M	-4352.5	-248	100	VSSA	-1352.5	-248	150	SDO	2160	-248	200	DUMMY	5372.5	-248

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
201	DUMMY	5432.5	-248	251	G32	7147	224	301	G132	6447	224	351	G232	5747	224
202	DUMMY	5492.5	-248	252	G34	7133	93	302	G134	6433	93	352	G234	5733	93
203	DUMMY	5552.5	-248	253	G36	7119	224	303	G136	6419	224	353	G236	5719	224
204	DUMMY	5612.5	-248	254	G38	7105	93	304	G138	6405	93	354	G238	5705	93
205	DUMMY	5672.5	-248	255	G40	7091	224	305	G140	6391	224	355	G240	5691	224
206	(GND)	5732.5	-248	256	G42	7077	93	306	G142	6377	93	356	G242	5677	93
207	(GND)	5792.5	-248	257	G44	7063	224	307	G144	6363	224	357	G244	5663	224
208	(GND)	5852.5	-248	258	G46	7049	93	308	G146	6349	93	358	G246	5649	93
209	(GND)	5912.5	-248	259	G48	7035	224	309	G148	6335	224	359	G248	5635	224
210	(GND)	5972.5	-248	260	G50	7021	93	310	G150	6321	93	360	G250	5621	93
211	(GND)	6032.5	-248	261	G52	7007	224	311	G152	6307	224	361	G252	5607	224
212	(GND)	6092.5	-248	262	G54	6993	93	312	G154	6293	93	362	G254	5593	93
213	(GND)	6152.5	-248	263	G56	6979	224	313	G156	6279	224	363	G256	5579	224
214	DUMMY	6212.5	-248	264	G58	6965	93	314	G158	6265	93	364	G258	5565	93
215	DUMMY	6272.5	-248	265	G60	6951	224	315	G160	6251	224	365	G260	5551	224
216	DUMMY	6332.5	-248	266	G62	6937	93	316	G162	6237	93	366	G262	5537	93
217	DUMMY	6392.5	-248	267	G64	6923	224	317	G164	6223	224	367	G264	5523	224
218	DUMMY	6452.5	-248	268	G66	6909	93	318	G166	6209	93	368	G266	5509	93
219	DUMMY	6512.5	-248	269	G68	6895	224	319	G168	6195	224	369	G268	5495	224
220	DUMMY	6572.5	-248	270	G70	6881	93	320	G170	6181	93	370	G270	5481	93
221	DUMMY	6632.5	-248	271	G72	6867	224	321	G172	6167	224	371	G272	5467	224
222	DUMMY	6692.5	-248	272	G74	6853	93	322	G174	6153	93	372	G274	5453	93
223	VCOM	6752.5	-248	273	G76	6839	224	323	G176	6139	224	373	G276	5439	224
224	VCOM	6812.5	-248	274	G78	6825	93	324	G178	6125	93	374	G278	5425	93
225	VCOM	6872.5	-248	275	G80	6811	224	325	G180	6111	224	375	G280	5411	224
226	VCOM	6932.5	-248	276	G82	6797	93	326	G182	6097	93	376	G282	5397	93
227	VCOM	6992.5	-248	277	G84	6783	224	327	G184	6083	224	377	G284	5383	224
228	VCOM	7052.5	-248	278	G86	6769	93	328	G186	6069	93	378	G286	5369	93
229	VCOM	7112.5	-248	279	G88	6755	224	329	G188	6055	224	379	G288	5355	224
230	VCOM	7172.5	-248	280	G90	6741	93	330	G190	6041	93	380	G290	5341	93
231	INT TEST1	7232.5	-248	281	G92	6727	224	331	G192	6027	224	381	G292	5327	224
232	INT TEST2	7292.5	-248	282	G94	6713	93	332	G194	6013	93	382	G294	5313	93
233	DUMMY	7399	224	283	G96	6699	224	333	G196	5999	224	383	G296	5299	224
234	DUMMY	7385	93	284	G98	6685	93	334	G198	5985	93	384	G298	5285	93
235	DUMMY	7371	224	285	G100	6671	224	335	G200	5971	224	385	G300	5271	224
236	G2	7357	93	286	G102	6657	93	336	G202	5957	93	386	G302	5257	93
237	G4	7343	224	287	G104	6643	224	337	G204	5943	224	387	G304	5243	224
238	G6	7329	93	288	G106	6629	93	338	G206	5929	93	388	G306	5229	93
239	G8	7315	224	289	G108	6615	224	339	G208	5915	224	389	G308	5215	224
240	G10	7301	93	290	G110	6601	93	340	G210	5901	93	390	G310	5201	93
241	G12	7287	224	291	G112	6587	224	341	G212	5887	224	391	G312	5187	224
242	G14	7273	93	292	G114	6573	93	342	G214	5873	93	392	G314	5173	93
243	G16	7259	224	293	G116	6559	224	343	G216	5859	224	393	G316	5159	224
244	G18	7245	93	294	G118	6545	93	344	G218	5845	93	394	G318	5145	93
245	G20	7231	224	295	G120	6531	224	345	G220	5831	224	395	G320	5131	224
246	G22	7217	93	296	G122	6517	93	346	G222	5817	93	396	S720	5075	93
247	G24	7203	224	297	G124	6503	224	347	G224	5803	224	397	S719	5061	224
248	G26	7189	93	298	G126	6489	93	348	G226	5789	93	398	S718	5047	93
249	G28	7175	224	299	G128	6475	224	349	G228	5775	224	399	S717	5033	224
250	G30	7161	93	300	G130	6461	93	350	G230	5761	93	400	S716	5019	93

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
401	S715	5005	224	451	S665	4305	224	501	S615	3605	224	551	S565	2905	224
402	S714	4991	93	452	S664	4291	93	502	S614	3591	93	552	S564	2891	93
403	S713	4977	224	453	S663	4277	224	503	S613	3577	224	553	S563	2877	224
404	S712	4963	93	454	S662	4263	93	504	S612	3563	93	554	S562	2863	93
405	S711	4949	224	455	S661	4249	224	505	S611	3549	224	555	S561	2849	224
406	S710	4935	93	456	S660	4235	93	506	S610	3535	93	556	S560	2835	93
407	S709	4921	224	457	S659	4221	224	507	S609	3521	224	557	S559	2821	224
408	S708	4907	93	458	S658	4207	93	508	S608	3507	93	558	S558	2807	93
409	S707	4893	224	459	S657	4193	224	509	S607	3493	224	559	S557	2793	224
410	S706	4879	93	460	S656	4179	93	510	S606	3479	93	560	S556	2779	93
411	S705	4865	224	461	S655	4165	224	511	S605	3465	224	561	S555	2765	224
412	S704	4851	93	462	S654	4151	93	512	S604	3451	93	562	S554	2751	93
413	S703	4837	224	463	S653	4137	224	513	S603	3437	224	563	S553	2737	224
414	S702	4823	93	464	S652	4123	93	514	S602	3423	93	564	S552	2723	93
415	S701	4809	224	465	S651	4109	224	515	S601	3409	224	565	S551	2709	224
416	S700	4795	93	466	S650	4095	93	516	S600	3395	93	566	S550	2695	93
417	S699	4781	224	467	S649	4081	224	517	S599	3381	224	567	S549	2681	224
418	S698	4767	93	468	S648	4067	93	518	S598	3367	93	568	S548	2667	93
419	S697	4753	224	469	S647	4053	224	519	S597	3353	224	569	S547	2653	224
420	S696	4739	93	470	S646	4039	93	520	S596	3339	93	570	S546	2639	93
421	S695	4725	224	471	S645	4025	224	521	S595	3325	224	571	S545	2625	224
422	S694	4711	93	472	S644	4011	93	522	S594	3311	93	572	S544	2611	93
423	S693	4697	224	473	S643	3997	224	523	S593	3297	224	573	S543	2597	224
424	S692	4683	93	474	S642	3983	93	524	S592	3283	93	574	S542	2583	93
425	S691	4669	224	475	S641	3969	224	525	S591	3269	224	575	S541	2569	224
426	S690	4655	93	476	S640	3955	93	526	S590	3255	93	576	S540	2555	93
427	S689	4641	224	477	S639	3941	224	527	S589	3241	224	577	S539	2541	224
428	S688	4627	93	478	S638	3927	93	528	S588	3227	93	578	S538	2527	93
429	S687	4613	224	479	S637	3913	224	529	S587	3213	224	579	S537	2513	224
430	S686	4599	93	480	S636	3899	93	530	S586	3199	93	580	S536	2499	93
431	S685	4585	224	481	S635	3885	224	531	S585	3185	224	581	S535	2485	224
432	S684	4571	93	482	S634	3871	93	532	S584	3171	93	582	S534	2471	93
433	S683	4557	224	483	S633	3857	224	533	S583	3157	224	583	S533	2457	224
434	S682	4543	93	484	S632	3843	93	534	S582	3143	93	584	S532	2443	93
435	S681	4529	224	485	S631	3829	224	535	S581	3129	224	585	S531	2429	224
436	S680	4515	93	486	S630	3815	93	536	S580	3115	93	586	S530	2415	93
437	S679	4501	224	487	S629	3801	224	537	S579	3101	224	587	S529	2401	224
438	S678	4487	93	488	S628	3787	93	538	S578	3087	93	588	S528	2387	93
439	S677	4473	224	489	S627	3773	224	539	S577	3073	224	589	S527	2373	224
440	S676	4459	93	490	S626	3759	93	540	S576	3059	93	590	S526	2359	93
441	S675	4445	224	491	S625	3745	224	541	S575	3045	224	591	S525	2345	224
442	S674	4431	93	492	S624	3731	93	542	S574	3031	93	592	S524	2331	93
443	S673	4417	224	493	S623	3717	224	543	S573	3017	224	593	S523	2317	224
444	S672	4403	93	494	S622	3703	93	544	S572	3003	93	594	S522	2303	93
445	S671	4389	224	495	S621	3689	224	545	S571	2989	224	595	S521	2289	224
446	S670	4375	93	496	S620	3675	93	546	S570	2975	93	596	S520	2275	93
447	S669	4361	224	497	S619	3661	224	547	S569	2961	224	597	S519	2261	224
448	S668	4347	93	498	S618	3647	93	548	S568	2947	93	598	S518	2247	93
449	S667	4333	224	499	S617	3633	224	549	S567	2933	224	599	S517	2233	224
450	S666	4319	93	500	S616	3619	93	550	S566	2919	93	600	S516	2219	93

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
601	S515	2205	224	651	S465	1505	224	701	S415	805	224	751	S365	105	224
602	S514	2191	93	652	S464	1491	93	702	S414	791	93	752	S364	91	93
603	S513	2177	224	653	S463	1477	224	703	S413	777	224	753	S363	77	224
604	S512	2163	93	654	S462	1463	93	704	S412	763	93	754	S362	63	93
605	S511	2149	224	655	S461	1449	224	705	S411	749	224	755	S361	49	224
606	S510	2135	93	656	S460	1435	93	706	S410	735	93	756	S360	-49	93
607	S509	2121	224	657	S459	1421	224	707	S409	721	224	757	S359	-63	224
608	S508	2107	93	658	S458	1407	93	708	S408	707	93	758	S358	-77	93
609	S507	2093	224	659	S457	1393	224	709	S407	693	224	759	S357	-91	224
610	S506	2079	93	660	S456	1379	93	710	S406	679	93	760	S356	-105	93
611	S505	2065	224	661	S455	1365	224	711	S405	665	224	761	S355	-119	224
612	S504	2051	93	662	S454	1351	93	712	S404	651	93	762	S354	-133	93
613	S503	2037	224	663	S453	1337	224	713	S403	637	224	763	S353	-147	224
614	S502	2023	93	664	S452	1323	93	714	S402	623	93	764	S352	-161	93
615	S501	2009	224	665	S451	1309	224	715	S401	609	224	765	S351	-175	224
616	S500	1995	93	666	S450	1295	93	716	S400	595	93	766	S350	-189	93
617	S499	1981	224	667	S449	1281	224	717	S399	581	224	767	S349	-203	224
618	S498	1967	93	668	S448	1267	93	718	S398	567	93	768	S348	-217	93
619	S497	1953	224	669	S447	1253	224	719	S397	553	224	769	S347	-231	224
620	S496	1939	93	670	S446	1239	93	720	S396	539	93	770	S346	-245	93
621	S495	1925	224	671	S445	1225	224	721	S395	525	224	771	S345	-259	224
622	S494	1911	93	672	S444	1211	93	722	S394	511	93	772	S344	-273	93
623	S493	1897	224	673	S443	1197	224	723	S393	497	224	773	S343	-287	224
624	S492	1883	93	674	S442	1183	93	724	S392	483	93	774	S342	-301	93
625	S491	1869	224	675	S441	1169	224	725	S391	469	224	775	S341	-315	224
626	S490	1855	93	676	S440	1155	93	726	S390	455	93	776	S340	-329	93
627	S489	1841	224	677	S439	1141	224	727	S389	441	224	777	S339	-343	224
628	S488	1827	93	678	S438	1127	93	728	S388	427	93	778	S338	-357	93
629	S487	1813	224	679	S437	1113	224	729	S387	413	224	779	S337	-371	224
630	S486	1799	93	680	S436	1099	93	730	S386	399	93	780	S336	-385	93
631	S485	1785	224	681	S435	1085	224	731	S385	385	224	781	S335	-399	224
632	S484	1771	93	682	S434	1071	93	732	S384	371	93	782	S334	-413	93
633	S483	1757	224	683	S433	1057	224	733	S383	357	224	783	S333	-427	224
634	S482	1743	93	684	S432	1043	93	734	S382	343	93	784	S332	-441	93
635	S481	1729	224	685	S431	1029	224	735	S381	329	224	785	S331	-455	224
636	S480	1715	93	686	S430	1015	93	736	S380	315	93	786	S330	-469	93
637	S479	1701	224	687	S429	1001	224	737	S379	301	224	787	S329	-483	224
638	S478	1687	93	688	S428	987	93	738	S378	287	93	788	S328	-497	93
639	S477	1673	224	689	S427	973	224	739	S377	273	224	789	S327	-511	224
640	S476	1659	93	690	S426	959	93	740	S376	259	93	790	S326	-525	93
641	S475	1645	224	691	S425	945	224	741	S375	245	224	791	S325	-539	224
642	S474	1631	93	692	S424	931	93	742	S374	231	93	792	S324	-553	93
643	S473	1617	224	693	S423	917	224	743	S373	217	224	793	S323	-567	224
644	S472	1603	93	694	S422	903	93	744	S372	203	93	794	S322	-581	93
645	S471	1589	224	695	S421	889	224	745	S371	189	224	795	S321	-595	224
646	S470	1575	93	696	S420	875	93	746	S370	175	93	796	S320	-609	93
647	S469	1561	224	697	S419	861	224	747	S369	161	224	797	S319	-623	224
648	S468	1547	93	698	S418	847	93	748	S368	147	93	798	S318	-637	93
649	S467	1533	224	699	S417	833	224	749	S367	133	224	799	S317	-651	224
650	S466	1519	93	700	S416	819	93	750	S366	119	93	800	S316	-665	93

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No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
801	S315	-679	224	851	S265	-1379	224	901	S215	-2079	224	951	S165	-2779	224
802	S314	-693	93	852	S264	-1393	93	902	S214	-2093	93	952	S164	-2793	93
803	S313	-707	224	853	S263	-1407	224	903	S213	-2107	224	953	S163	-2807	224
804	S312	-721	93	854	S262	-1421	93	904	S212	-2121	93	954	S162	-2821	93
805	S311	-735	224	855	S261	-1435	224	905	S211	-2135	224	955	S161	-2835	224
806	S310	-749	93	856	S260	-1449	93	906	S210	-2149	93	956	S160	-2849	93
807	S309	-763	224	857	S259	-1463	224	907	S209	-2163	224	957	S159	-2863	224
808	S308	-777	93	858	S258	-1477	93	908	S208	-2177	93	958	S158	-2877	93
809	S307	-791	224	859	S257	-1491	224	909	S207	-2191	224	959	S157	-2891	224
810	S306	-805	93	860	S256	-1505	93	910	S206	-2205	93	960	S156	-2905	93
811	S305	-819	224	861	S255	-1519	224	911	S205	-2219	224	961	S155	-2919	224
812	S304	-833	93	862	S254	-1533	93	912	S204	-2233	93	962	S154	-2933	93
813	S303	-847	224	863	S253	-1547	224	913	S203	-2247	224	963	S153	-2947	224
814	S302	-861	93	864	S252	-1561	93	914	S202	-2261	93	964	S152	-2961	93
815	S301	-875	224	865	S251	-1575	224	915	S201	-2275	224	965	S151	-2975	224
816	S300	-889	93	866	S250	-1589	93	916	S200	-2289	93	966	S150	-2989	93
817	S299	-903	224	867	S249	-1603	224	917	S199	-2303	224	967	S149	-3003	224
818	S298	-917	93	868	S248	-1617	93	918	S198	-2317	93	968	S148	-3017	93
819	S297	-931	224	869	S247	-1631	224	919	S197	-2331	224	969	S147	-3031	224
820	S296	-945	93	870	S246	-1645	93	920	S196	-2345	93	970	S146	-3045	93
821	S295	-959	224	871	S245	-1659	224	921	S195	-2359	224	971	S145	-3059	224
822	S294	-973	93	872	S244	-1673	93	922	S194	-2373	93	972	S144	-3073	93
823	S293	-987	224	873	S243	-1687	224	923	S193	-2387	224	973	S143	-3087	224
824	S292	-1001	93	874	S242	-1701	93	924	S192	-2401	93	974	S142	-3101	93
825	S291	-1015	224	875	S241	-1715	224	925	S191	-2415	224	975	S141	-3115	224
826	S290	-1029	93	876	S240	-1729	93	926	S190	-2429	93	976	S140	-3129	93
827	S289	-1043	224	877	S239	-1743	224	927	S189	-2443	224	977	S139	-3143	224
828	S288	-1057	93	878	S238	-1757	93	928	S188	-2457	93	978	S138	-3157	93
829	S287	-1071	224	879	S237	-1771	224	929	S187	-2471	224	979	S137	-3171	224
830	S286	-1085	93	880	S236	-1785	93	930	S186	-2485	93	980	S136	-3185	93
831	S285	-1099	224	881	S235	-1799	224	931	S185	-2499	224	981	S135	-3199	224
832	S284	-1113	93	882	S234	-1813	93	932	S184	-2513	93	982	S134	-3213	93
833	S283	-1127	224	883	S233	-1827	224	933	S183	-2527	224	983	S133	-3227	224
834	S282	-1141	93	884	S232	-1841	93	934	S182	-2541	93	984	S132	-3241	93
835	S281	-1155	224	885	S231	-1855	224	935	S181	-2555	224	985	S131	-3255	224
836	S280	-1169	93	886	S230	-1869	93	936	S180	-2569	93	986	S130	-3269	93
837	S279	-1183	224	887	S229	-1883	224	937	S179	-2583	224	987	S129	-3283	224
838	S278	-1197	93	888	S228	-1897	93	938	S178	-2597	93	988	S128	-3297	93
839	S277	-1211	224	889	S227	-1911	224	939	S177	-2611	224	989	S127	-3311	224
840	S276	-1225	93	890	S226	-1925	93	940	S176	-2625	93	990	S126	-3325	93
841	S275	-1239	224	891	S225	-1939	224	941	S175	-2639	224	991	S125	-3339	224
842	S274	-1253	93	892	S224	-1953	93	942	S174	-2653	93	992	S124	-3353	93
843	S273	-1267	224	893	S223	-1967	224	943	S173	-2667	224	993	S123	-3367	224
844	S272	-1281	93	894	S222	-1981	93	944	S172	-2681	93	994	S122	-3381	93
845	S271	-1295	224	895	S221	-1995	224	945	S171	-2695	224	995	S121	-3395	224
846	S270	-1309	93	896	S220	-2009	93	946	S170	-2709	93	996	S120	-3409	93
847	S269	-1323	224	897	S219	-2023	224	947	S169	-2723	224	997	S119	-3423	224
848	S268	-1337	93	898	S218	-2037	93	948	S168	-2737	93	998	S118	-3437	93
849	S267	-1351	224	899	S217	-2051	224	949	S167	-2751	224	999	S117	-3451	224
850	S266	-1365	93	900	S216	-2065	93	950	S166	-2765	93	1000	S116	-3465	93

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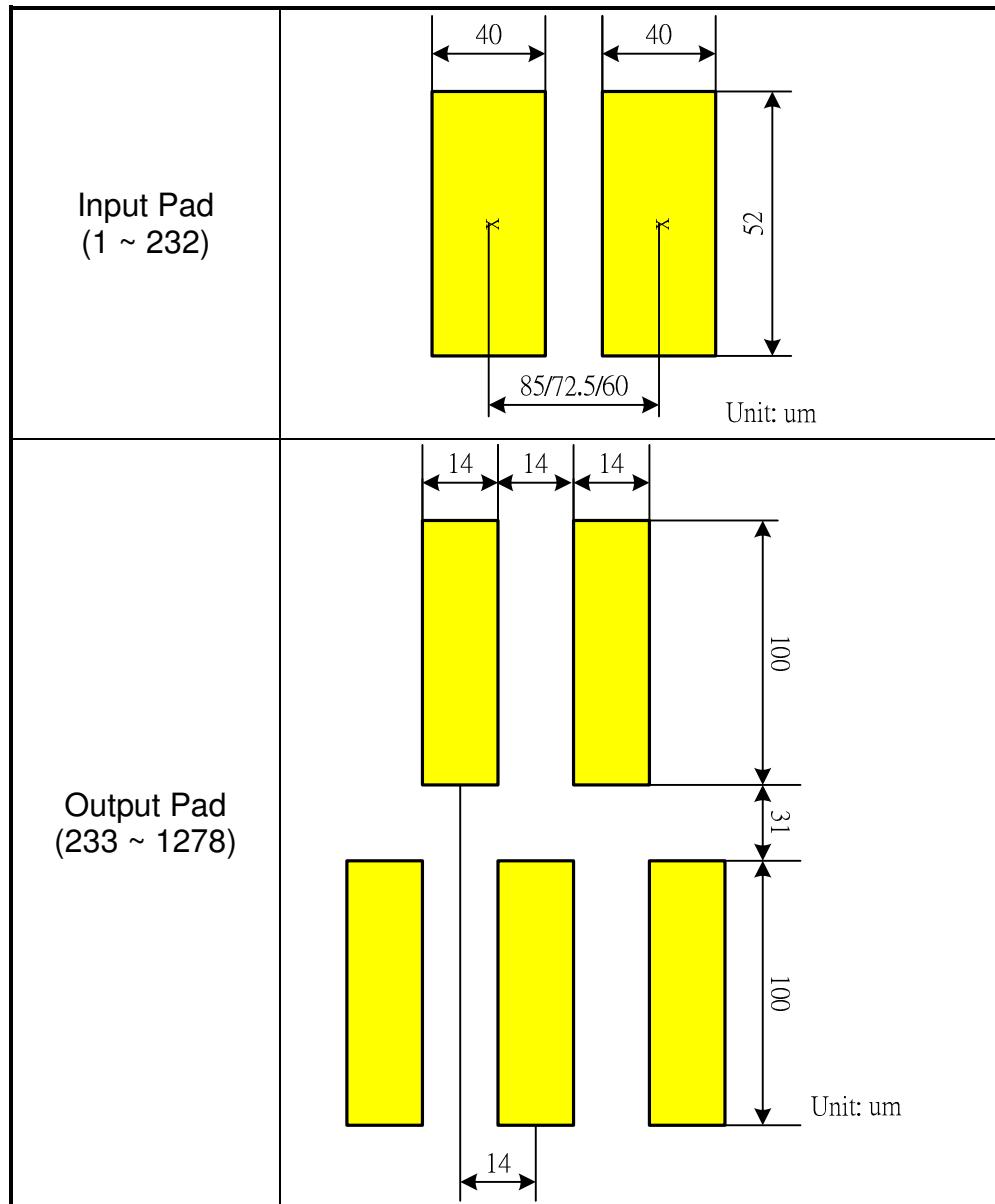
No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y	No.	Pad name	X	Y
1001	S115	-3479	224	1051	S65	-4179	224	1101	S15	-4879	224	1151	G249	-5621	224
1002	S114	-3493	93	1052	S64	-4193	93	1102	S14	-4893	93	1152	G247	-5635	93
1003	S113	-3507	224	1053	S63	-4207	224	1103	S13	-4907	224	1153	G245	-5649	224
1004	S112	-3521	93	1054	S62	-4221	93	1104	S12	-4921	93	1154	G243	-5663	93
1005	S111	-3535	224	1055	S61	-4235	224	1105	S11	-4935	224	1155	G241	-5677	224
1006	S110	-3549	93	1056	S60	-4249	93	1106	S10	-4949	93	1156	G239	-5691	93
1007	S109	-3563	224	1057	S59	-4263	224	1107	S9	-4963	224	1157	G237	-5705	224
1008	S108	-3577	93	1058	S58	-4277	93	1108	S8	-4977	93	1158	G235	-5719	93
1009	S107	-3591	224	1059	S57	-4291	224	1109	S7	-4991	224	1159	G233	-5733	224
1010	S106	-3605	93	1060	S56	-4305	93	1110	S6	-5005	93	1160	G231	-5747	93
1011	S105	-3619	224	1061	S55	-4319	224	1111	S5	-5019	224	1161	G229	-5761	224
1012	S104	-3633	93	1062	S54	-4333	93	1112	S4	-5033	93	1162	G227	-5775	93
1013	S103	-3647	224	1063	S53	-4347	224	1113	S3	-5047	224	1163	G225	-5789	224
1014	S102	-3661	93	1064	S52	-4361	93	1114	S2	-5061	93	1164	G223	-5803	93
1015	S101	-3675	224	1065	S51	-4375	224	1115	S1	-5075	224	1165	G221	-5817	224
1016	S100	-3689	93	1066	S50	-4389	93	1116	G319	-5131	93	1166	G219	-5831	93
1017	S99	-3703	224	1067	S49	-4403	224	1117	G317	-5145	224	1167	G217	-5845	224
1018	S98	-3717	93	1068	S48	-4417	93	1118	G315	-5159	93	1168	G215	-5859	93
1019	S97	-3731	224	1069	S47	-4431	224	1119	G313	-5173	224	1169	G213	-5873	224
1020	S96	-3745	93	1070	S46	-4445	93	1120	G311	-5187	93	1170	G211	-5887	93
1021	S95	-3759	224	1071	S45	-4459	224	1121	G309	-5201	224	1171	G209	-5901	224
1022	S94	-3773	93	1072	S44	-4473	93	1122	G307	-5215	93	1172	G207	-5915	93
1023	S93	-3787	224	1073	S43	-4487	224	1123	G305	-5229	224	1173	G205	-5929	224
1024	S92	-3801	93	1074	S42	-4501	93	1124	G303	-5243	93	1174	G203	-5943	93
1025	S91	-3815	224	1075	S41	-4515	224	1125	G301	-5257	224	1175	G201	-5957	224
1026	S90	-3829	93	1076	S40	-4529	93	1126	G299	-5271	93	1176	G199	-5971	93
1027	S89	-3843	224	1077	S39	-4543	224	1127	G297	-5285	224	1177	G197	-5985	224
1028	S88	-3857	93	1078	S38	-4557	93	1128	G295	-5299	93	1178	G195	-5999	93
1029	S87	-3871	224	1079	S37	-4571	224	1129	G293	-5313	224	1179	G193	-6013	224
1030	S86	-3885	93	1080	S36	-4585	93	1130	G291	-5327	93	1180	G191	-6027	93
1031	S85	-3899	224	1081	S35	-4599	224	1131	G289	-5341	224	1181	G189	-6041	224
1032	S84	-3913	93	1082	S34	-4613	93	1132	G287	-5355	93	1182	G187	-6055	93
1033	S83	-3927	224	1083	S33	-4627	224	1133	G285	-5369	224	1183	G185	-6069	224
1034	S82	-3941	93	1084	S32	-4641	93	1134	G283	-5383	93	1184	G183	-6083	93
1035	S81	-3955	224	1085	S31	-4655	224	1135	G281	-5397	224	1185	G181	-6097	224
1036	S80	-3969	93	1086	S30	-4669	93	1136	G279	-5411	93	1186	G179	-6111	93
1037	S79	-3983	224	1087	S29	-4683	224	1137	G277	-5425	224	1187	G177	-6125	224
1038	S78	-3997	93	1088	S28	-4697	93	1138	G275	-5439	93	1188	G175	-6139	93
1039	S77	-4011	224	1089	S27	-4711	224	1139	G273	-5453	224	1189	G173	-6153	224
1040	S76	-4025	93	1090	S26	-4725	93	1140	G271	-5467	93	1190	G171	-6167	93
1041	S75	-4039	224	1091	S25	-4739	224	1141	G269	-5481	224	1191	G169	-6181	224
1042	S74	-4053	93	1092	S24	-4753	93	1142	G267	-5495	93	1192	G167	-6195	93
1043	S73	-4067	224	1093	S23	-4767	224	1143	G265	-5509	224	1193	G165	-6209	224
1044	S72	-4081	93	1094	S22	-4781	93	1144	G263	-5523	93	1194	G163	-6223	93
1045	S71	-4095	224	1095	S21	-4795	224	1145	G261	-5537	224	1195	G161	-6237	224
1046	S70	-4109	93	1096	S20	-4809	93	1146	G259	-5551	93	1196	G159	-6251	93
1047	S69	-4123	224	1097	S19	-4823	224	1147	G257	-5565	224	1197	G157	-6265	224
1048	S68	-4137	93	1098	S18	-4837	93	1148	G255	-5579	93	1198	G155	-6279	93
1049	S67	-4151	224	1099	S17	-4851	224	1149	G253	-5593	224	1199	G153	-6293	224
1050	S66	-4165	93	1100	S16	-4865	93	1150	G251	-5607	93	1200	G151	-6307	93

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No.	Pad name	X	Y	No.	Pad name	X	Y
1201	G149	-6321	224	1251	G49	-7021	224
1202	G147	-6335	93	1252	G47	-7035	93
1203	G145	-6349	224	1253	G45	-7049	224
1204	G143	-6363	93	1254	G43	-7063	93
1205	G141	-6377	224	1255	G41	-7077	224
1206	G139	-6391	93	1256	G39	-7091	93
1207	G137	-6405	224	1257	G37	-7105	224
1208	G135	-6419	93	1258	G35	-7119	93
1209	G133	-6433	224	1259	G33	-7133	224
1210	G131	-6447	93	1260	G31	-7147	93
1211	G129	-6461	224	1261	G29	-7161	224
1212	G127	-6475	93	1262	G27	-7175	93
1213	G125	-6489	224	1263	G25	-7189	224
1214	G123	-6503	93	1264	G23	-7203	93
1215	G121	-6517	224	1265	G21	-7217	224
1216	G119	-6531	93	1266	G19	-7231	93
1217	G117	-6545	224	1267	G17	-7245	224
1218	G115	-6559	93	1268	G15	-7259	93
1219	G113	-6573	224	1269	G13	-7273	224
1220	G111	-6587	93	1270	G11	-7287	93
1221	G109	-6601	224	1271	G9	-7301	224
1222	G107	-6615	93	1272	G7	-7315	93
1223	G105	-6629	224	1273	G5	-7329	224
1224	G103	-6643	93	1274	G3	-7343	93
1225	G101	-6657	224	1275	G1	-7357	224
1226	G99	-6671	93	1276	DUMMY	-7371	93
1227	G97	-6685	224	1277	DUMMY	-7385	224
1228	G95	-6699	93	1278	DUMMY	-7399	93
1229	G93	-6713	224				
1230	G91	-6727	93				
1231	G89	-6741	224				
1232	G87	-6755	93				
1233	G85	-6769	224				
1234	G83	-6783	93				
1235	G81	-6797	224				
1236	G79	-6811	93				
1237	G77	-6825	224				
1238	G75	-6839	93				
1239	G73	-6853	224				
1240	G71	-6867	93				
1241	G69	-6881	224				
1242	G67	-6895	93				
1243	G65	-6909	224				
1244	G63	-6923	93				
1245	G61	-6937	224				
1246	G59	-6951	93				
1247	G57	-6965	224				
1248	G55	-6979	93				
1249	G53	-6993	224				
1250	G51	-7007	93				

Alignment mark	X	Y
Left COG Align	-7480	225
Right COG Align	7480	225

BUMP Size



6. Block Function Description

MCU System Interface

ILI9341 provides four kinds of MCU system interface with 8080- I /8080- II series parallel interface and 3-/4-line serial interface. The selection of the given interfaces are done by external IM [3:0] pins and shown as below:

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I	SCL,SDA,CSX	
0	1	1	0	4-wire 8-bit data serial interface I	SCL,SDA,D/CX,CSX	
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II	SCL,SDI,SDO, CSX	
1	1	1	0	4-wire 8-bit data serial interface II	SCL,SDI,D/CX,SDO, CSX	

In 8080- I /8080- II series parallel interface, the registers are accessed by the D[17:0] data pins.

8080- I Series				8080- II Series				Operation
CSX	D/CX	RDX	WRX	CSX	D/CX	RDX	WRX	
“L”	“L”	“H”	□	“L”	“L”	“H”	□	Write command
“L”	“H”	□	“H”	“L”	“H”	□	“H”	Read parameter
“L”	“H”	“H”	□	“L”	“H”	“H”	□	Write parameter

Parallel RGB Interface

ILI9341 also supports the RGB interface for displaying a moving picture. When the RGB interface is selected, display operation is synchronized with externally signals, VSYNC, HSYNC, and DOTCLK and input display data is written in synchronization with these signals according to the polarity of enable signal (DE).

Graphic RAM (GRAM)

GRAM is a graphic RAM to store display data. GRAM size is 172,800 bytes with 18 bits per pixel for a maximum 240(RGB) x320 dot graphic display.

Grayscale Voltage Generating Circuit

Grayscale voltage generating circuit generates a liquid crystal drive voltage, which corresponds to grayscale level set in the gamma correction register. ILI9341 can display maximum 262,144 colors.

Power Supply Circuit

The LCD drive power supply circuit generates the voltage levels as GVDD, VGH, VGL and VCOM for driving TFT LCD panel.

Timing controller

The timing controller generates all the timing signals for display and GRAM access.

Oscillator

ILI9341 incorporates RC oscillator circuit and output a stable output frequency for operation.

Panel Driver Circuit

Liquid crystal display driver circuit consists of 720-output source driver (S1~S720), 320-output gate driver (G1~G320), and VCOM signal.

7. Function Description

7.1. MCU interfaces

ILI9341 provides the 8-/9-/16-/18-bit parallel system interface for 8080- I /8080- II series, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [3:0] and the bit formal per pixel color order is selected by DBI [2:0] bits of 3Ah register.

7.1.1. MCU interface selection

The selection of interface is done by setting external pins IM [3:0] as shown in the following table.

IM3	IM2	IM1	IM0	MCU-Interface Mode	Pins in use	
					Register/Content	GRAM
0	0	0	0	8080 MCU 8-bit bus interface I	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	0	1	8080 MCU 16-bit bus interface I	D[7:0]	D[15:0],WRX,RDX,CSX,D/CX
0	0	1	0	8080 MCU 9-bit bus interface I	D[7:0]	D[8:0],WRX,RDX,CSX,D/CX
0	0	1	1	8080 MCU 18-bit bus interface I	D[7:0]	D[17:0],WRX,RDX,CSX,D/CX
0	1	0	1	3-wire 9-bit data serial interface I		SCL,SDA,CSX
0	1	1	0	4-wire 8-bit data serial interface I		SCL,SDA,D/CX,CSX
1	0	0	0	8080 MCU 16-bit bus interface II	D[8:1]	D[17:10],D[8:1],WRX,RDX,CSX,D/CX
1	0	0	1	8080 MCU 8-bit bus interface II	D[17:10]	D[17:10],WRX,RDX,CSX,D/CX
1	0	1	0	8080 MCU 18-bit bus interface II	D[8:1]	D[17:0],WRX,RDX,CSX,D/CX
1	0	1	1	8080 MCU 9-bit bus interface II	D[17:10]	D[17:9],WRX,RDX,CSX,D/CX
1	1	0	1	3-wire 9-bit data serial interface II		SCL,SDI,SDO, CSX
1	1	1	0	4-wire 8-bit data serial interface II		SCL,SDI,D/CX,SDO, CSX

7.1.2. 8080- I Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080- I series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080- I series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080- I Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

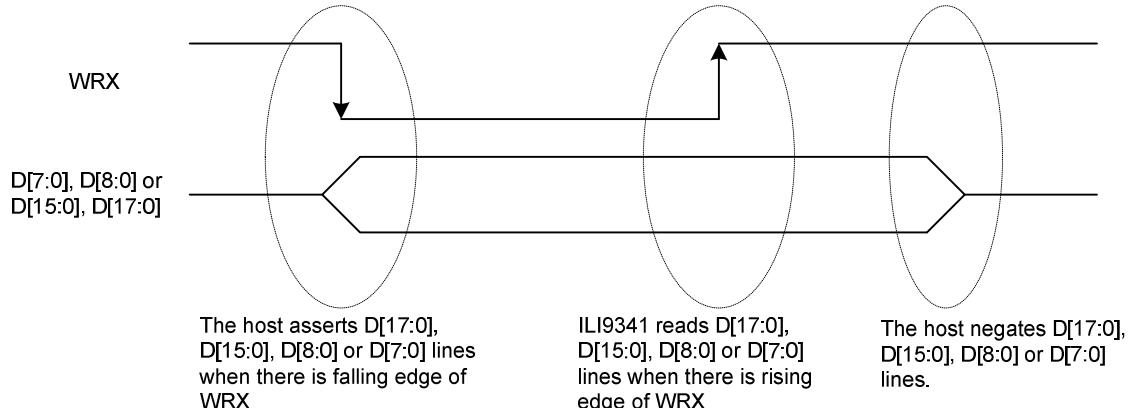
The selection of 8080- I series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IMO	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
0	0	0	0	8080 MCU 8-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
0	0	0	1	8080 MCU 16-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
0	0	1	0	8080 MCU 9-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
0	0	1	1	8080 MCU 18-bit bus interface I	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.

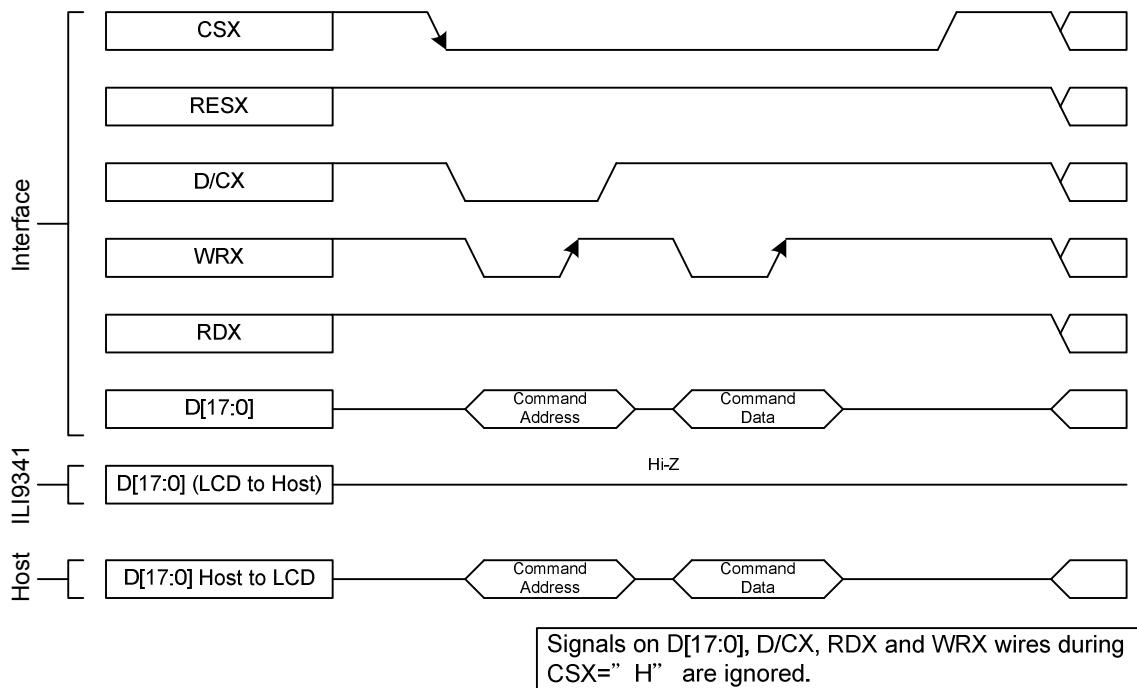
7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- I_MCU interface.



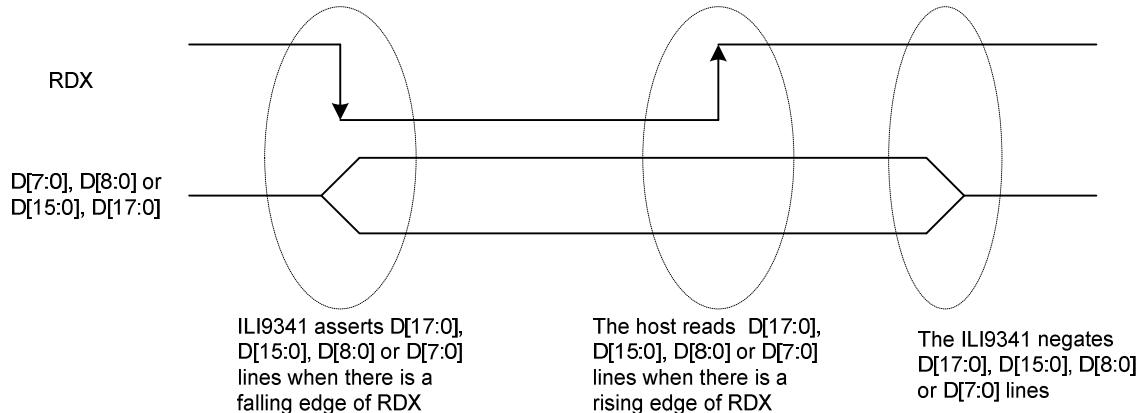
Note: WRX is an unsynchronized signal (It can be stopped)



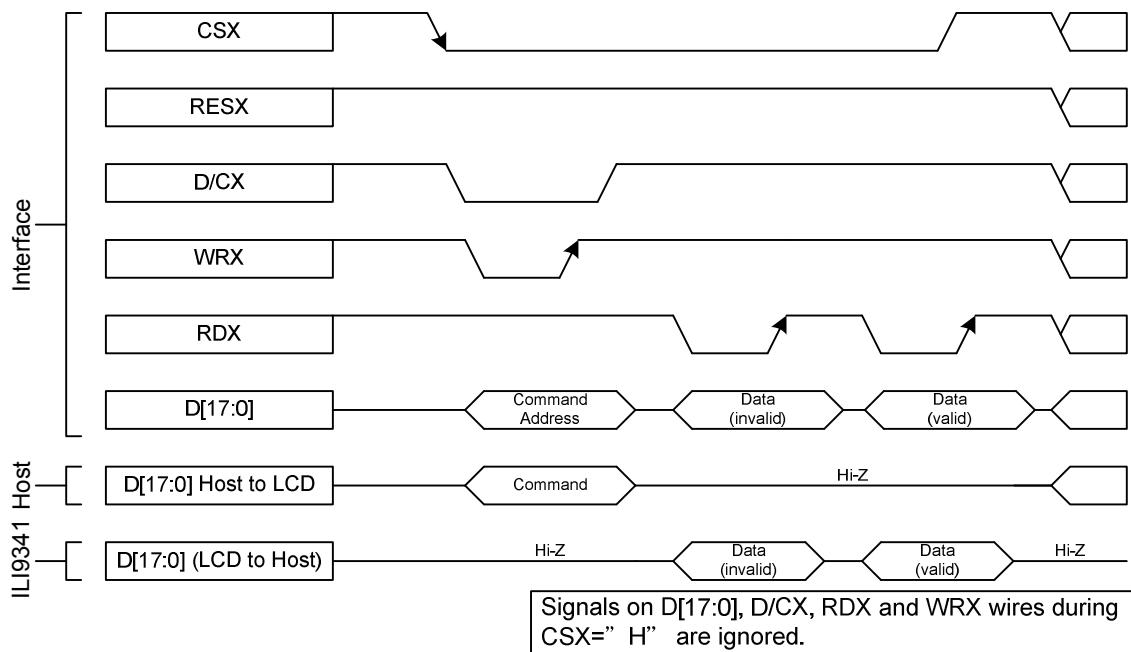
7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- I_MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.5. 8080-II Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080-II series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-II series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-II Interface selection is done when IM3 pin is high state (VDDI level). Interface bus width can be selected by IM [2:0] bits.

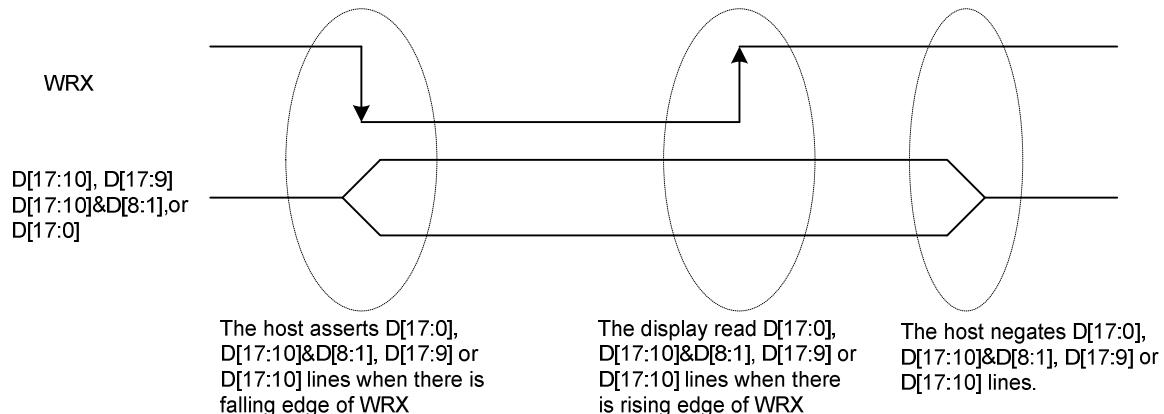
The selection of 8080-II series parallel interface is shown as the table in the following.

IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	WRX	RDX	D/CX	Function
1	0	0	0	8080 MCU 16-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	0	1	8080 MCU 8-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	1	0	8080 MCU 18-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.
1	0	1	1	8080 MCU 9-bit bus interface II	"L"		"H"	"L"	Write command code.
					"L"	"H"		"H"	Read internal status.
					"L"		"H"	"H"	Write parameter or display data.
					"L"	"H"		"H"	Reads parameter or display data.

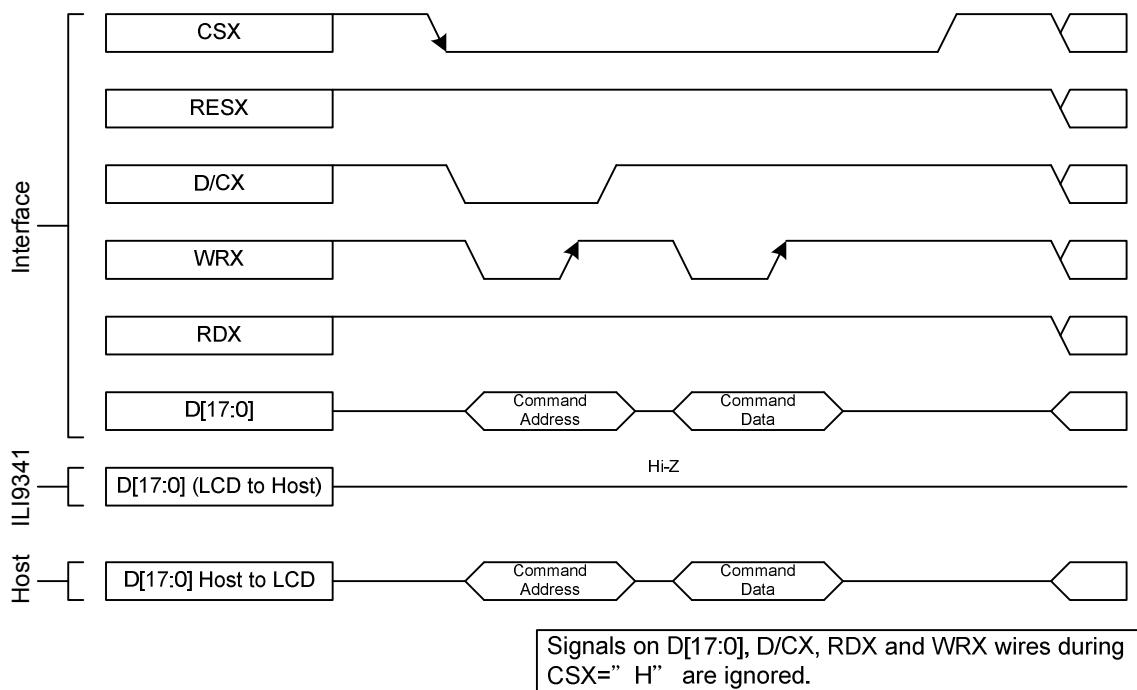
7.1.6. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080-II MCU interface.



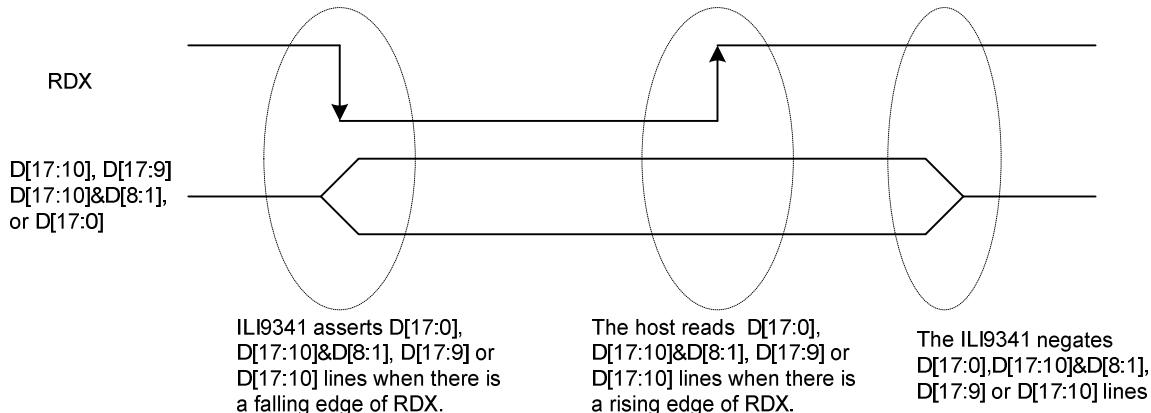
Note: WRX is an unsynchronized signal (It can be stopped)



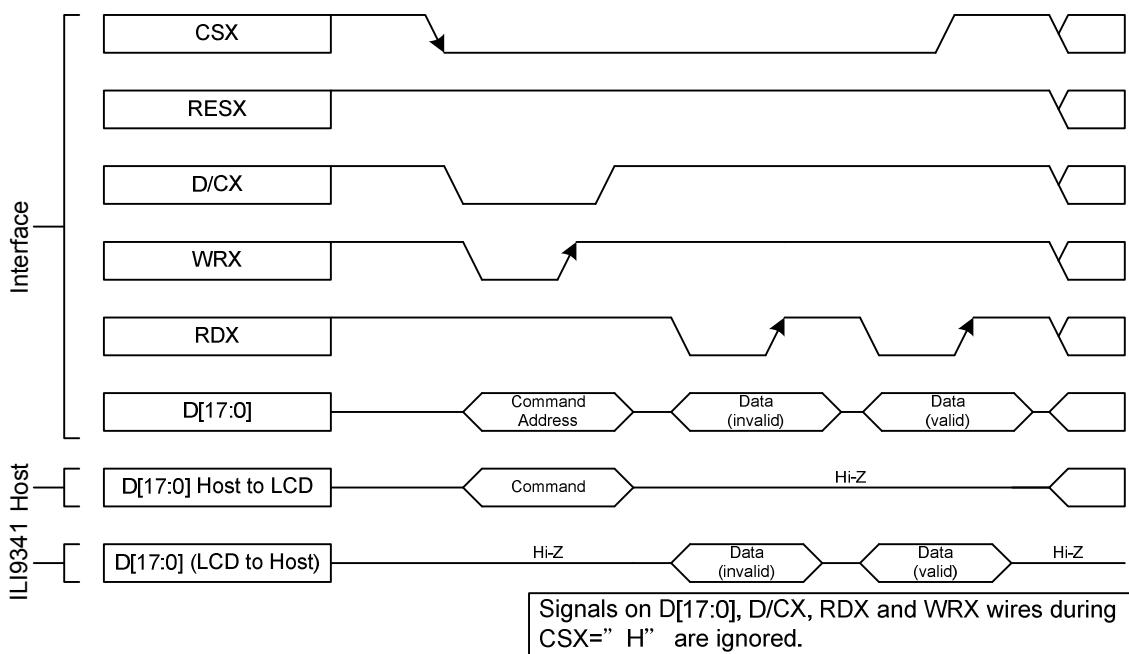
7.1.7. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080-II MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

7.1.8. Serial Interface

The selection of interface is done by IM [3:0] bits. Please refer to the Table in the following.

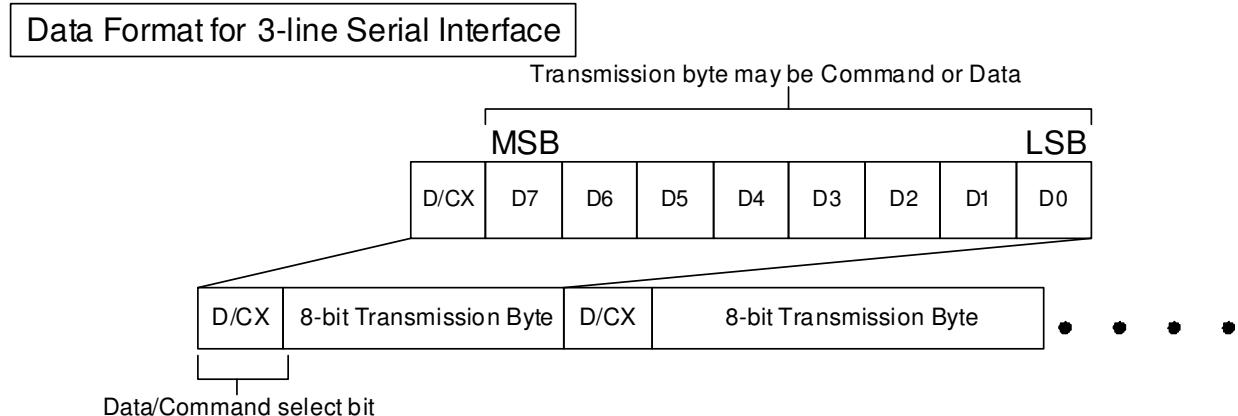
IM3	IM2	IM1	IM0	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	1	0	1	3-line serial interface	"L"	-	↓	Read/Write command, parameter or display data.
0	1	1	0	4-line serial interface	"L"	'H/L"	↓	Read/Write command, parameter or display data.
1	1	0	1	3-line serial interface	"L"	-	↓	Read/Write command, parameter or display data.
1	1	1	0	4-line serial interface	"L"	'H/L"	↓	Read/Write command, parameter or display data.

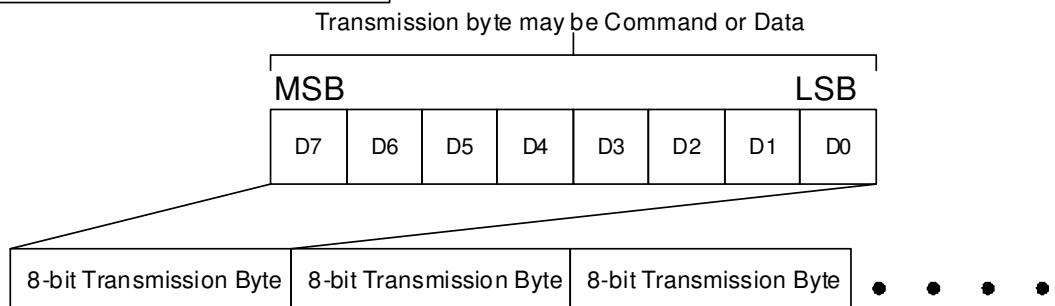
ILI9341 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and ILI9341. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (SDA or SDI/SDO) for data transmission. The data bus (D [17:0]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

7.1.9. Write Cycle Sequence

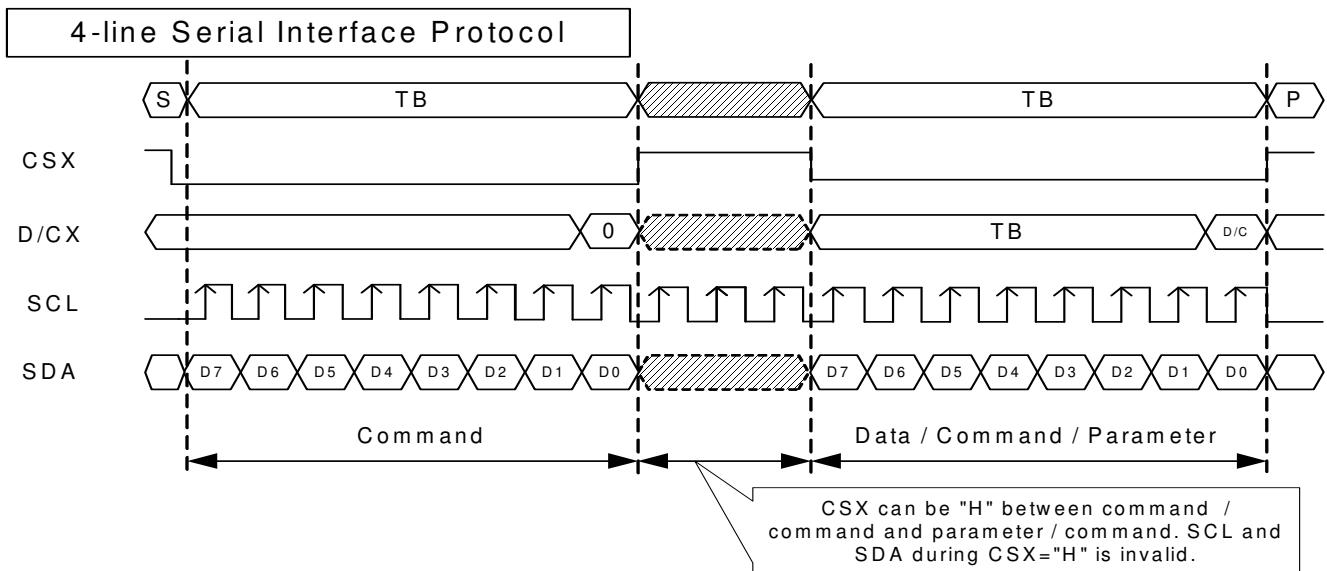
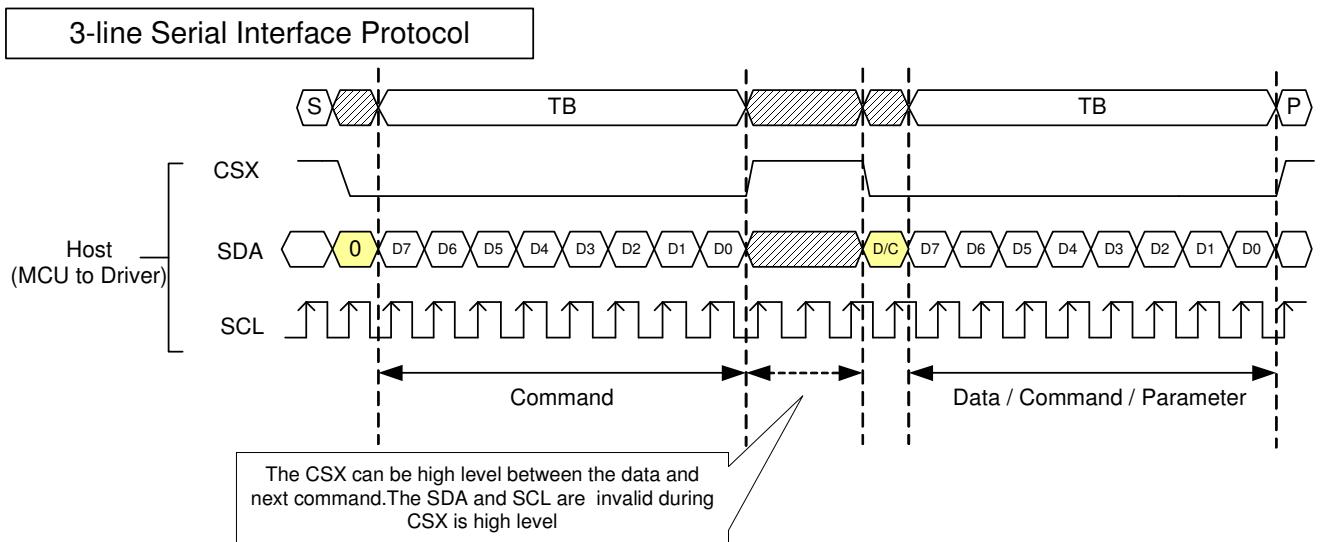
The write mode of the interface means that host writes commands or data to ILI9341. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is "low", the transmission byte is interpreted as a command byte. If the D/CX bit is "high", the transmission byte is stored as the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any order to ILI9341 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.



Data Format for 4-line Serial Interface

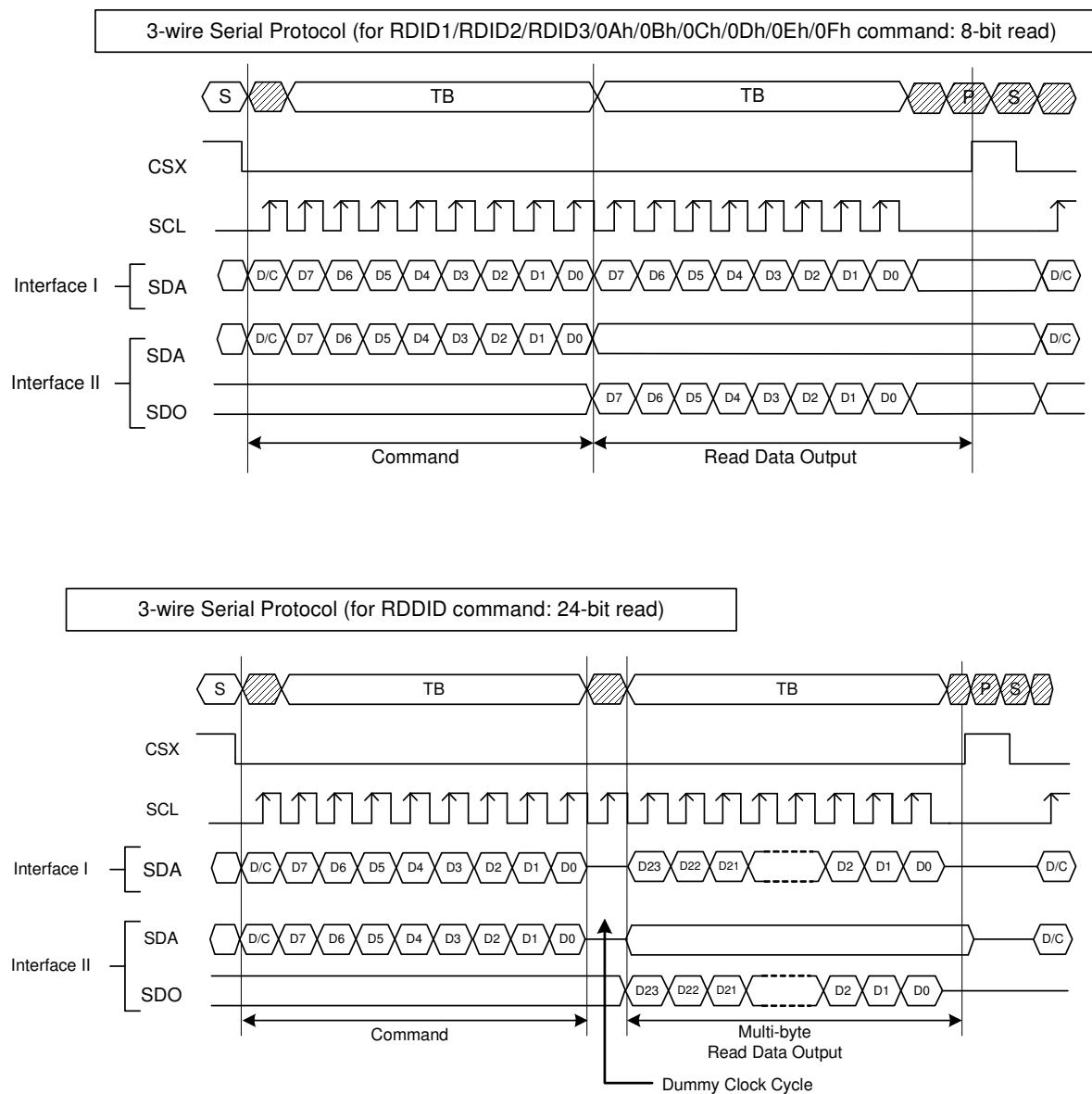
Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by ILI9341 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.

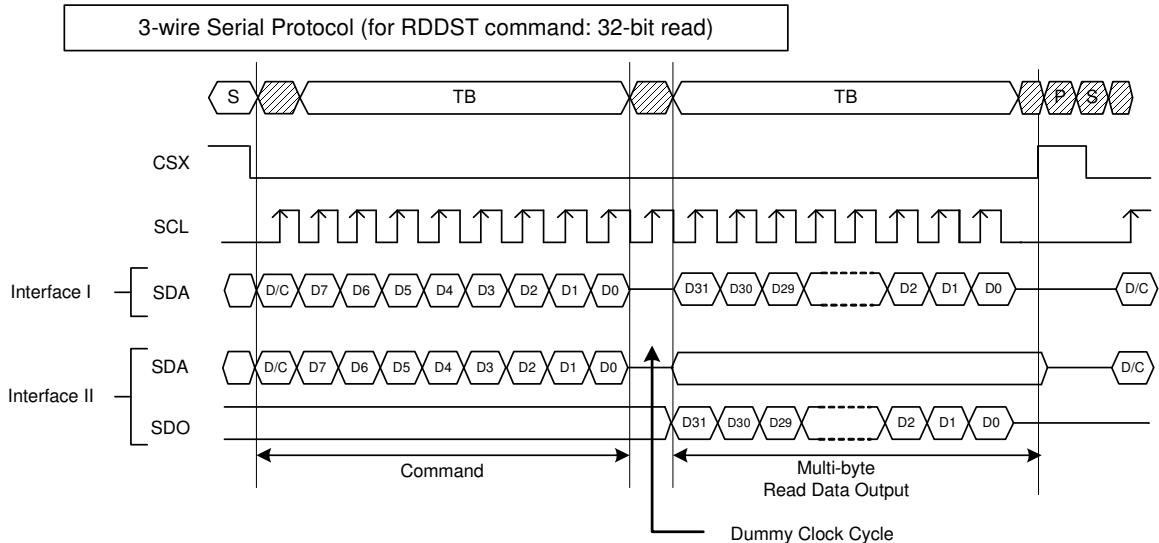


7.1.10. Read Cycle Sequence

The read mode of interface means that the host reads register's parameter or display data from ILI9341. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. ILI9341 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

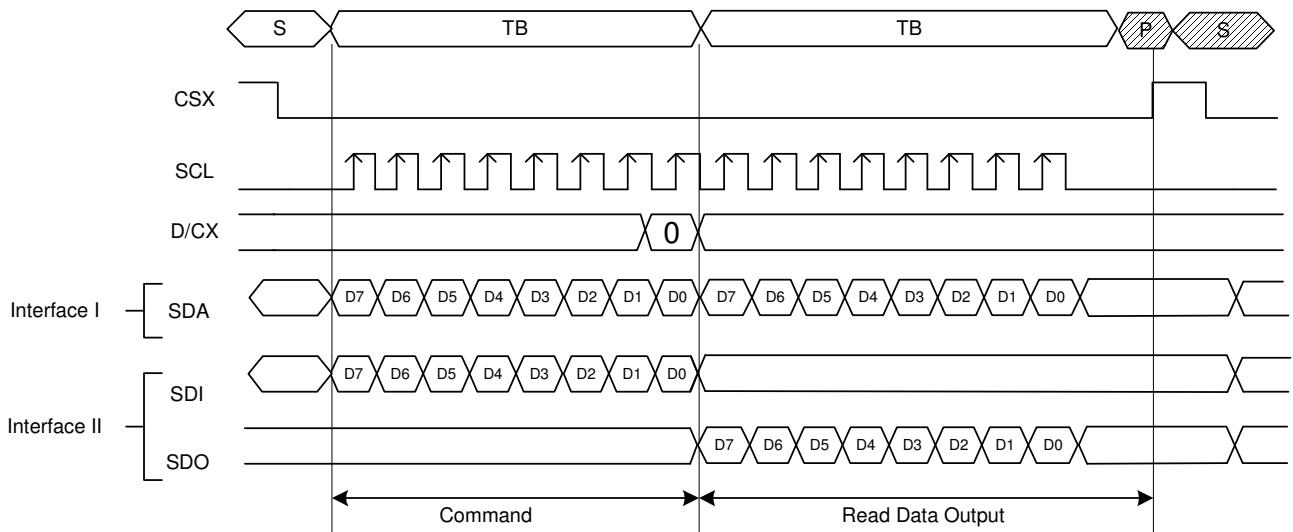
3-wire Serial Interface Protocol



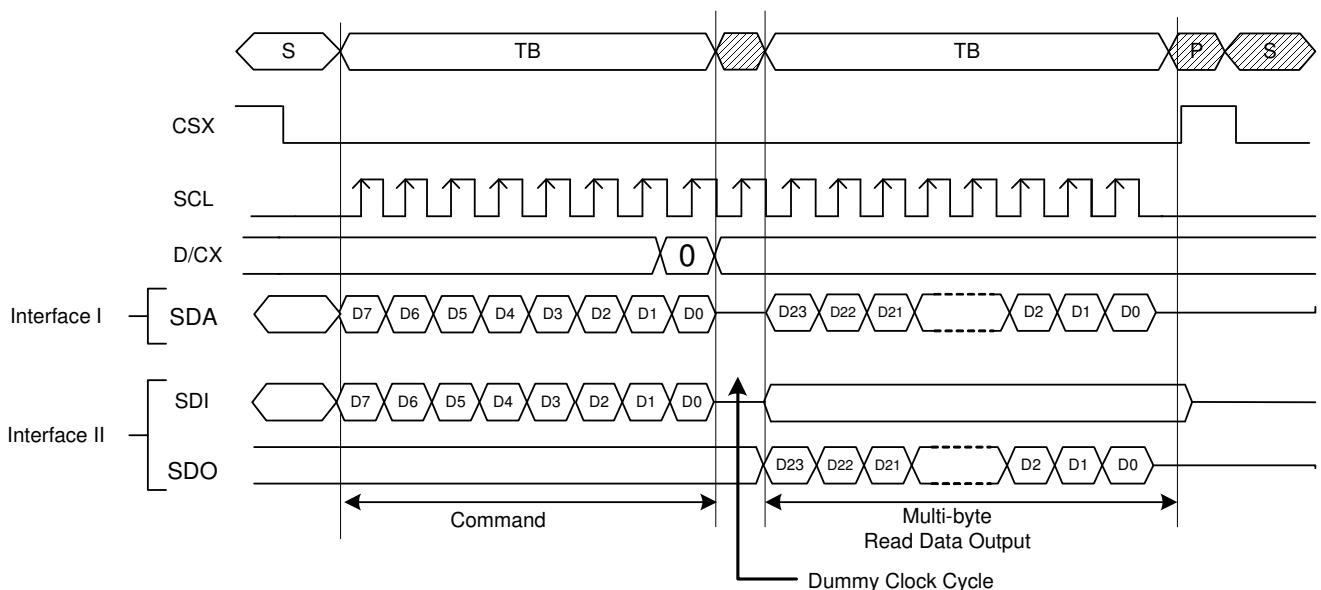


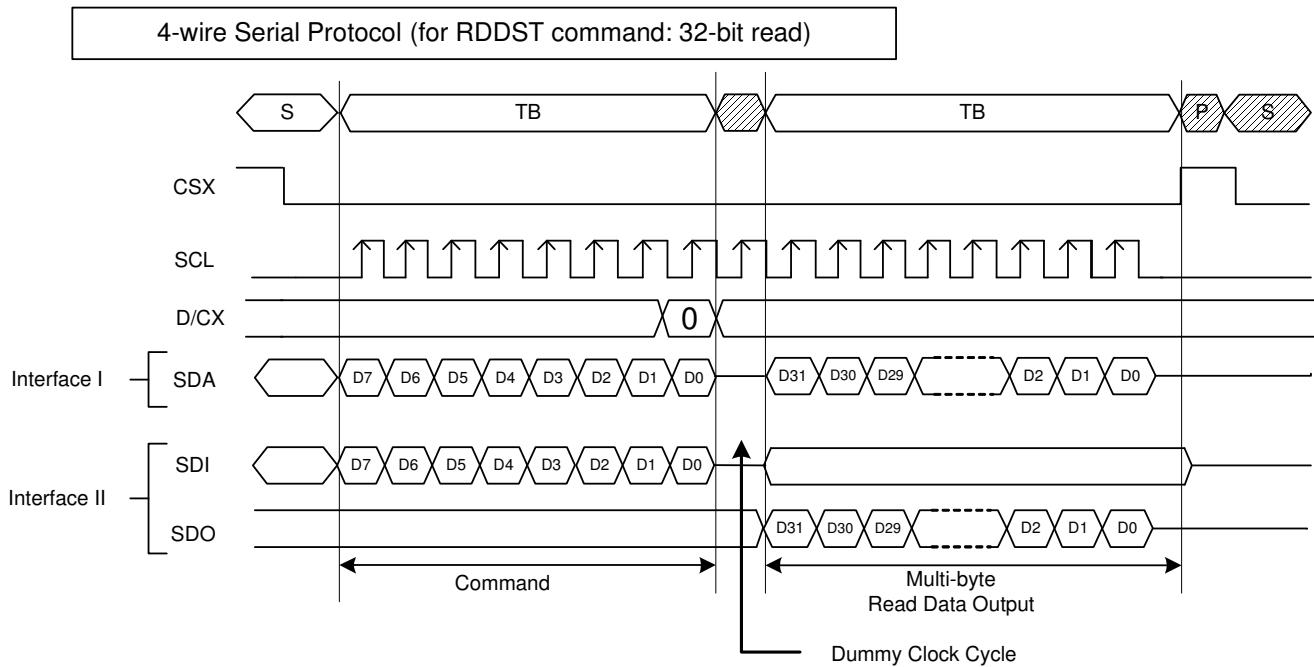
4-wire Serial Interface Protocol

4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command: 8-bit read)



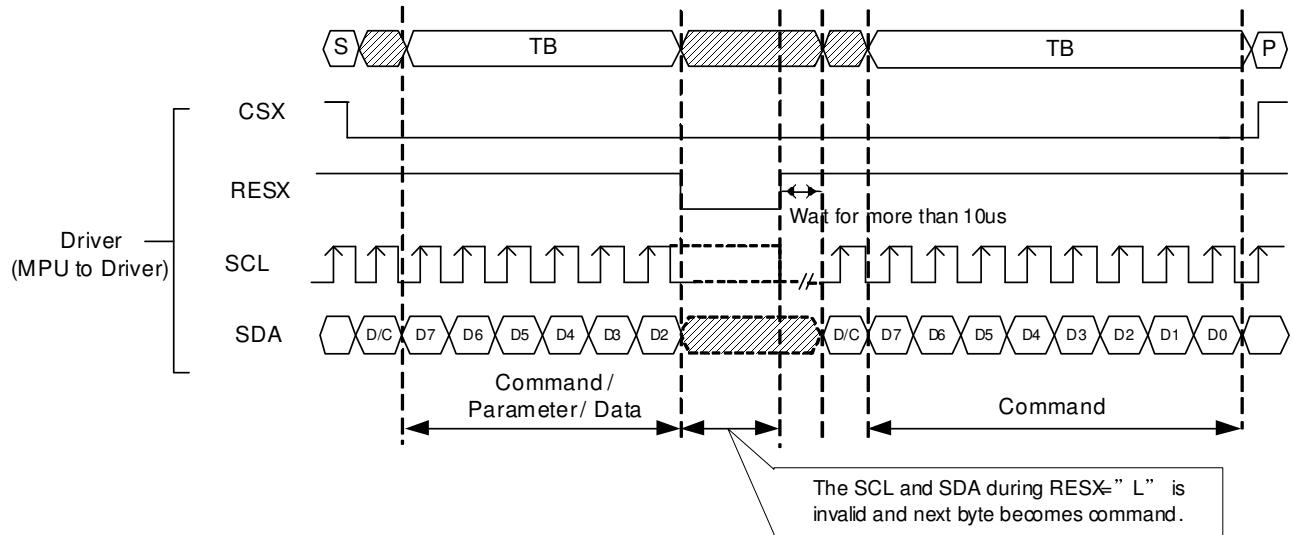
4-wire Serial Protocol (for RDDID command: 24-bit read)



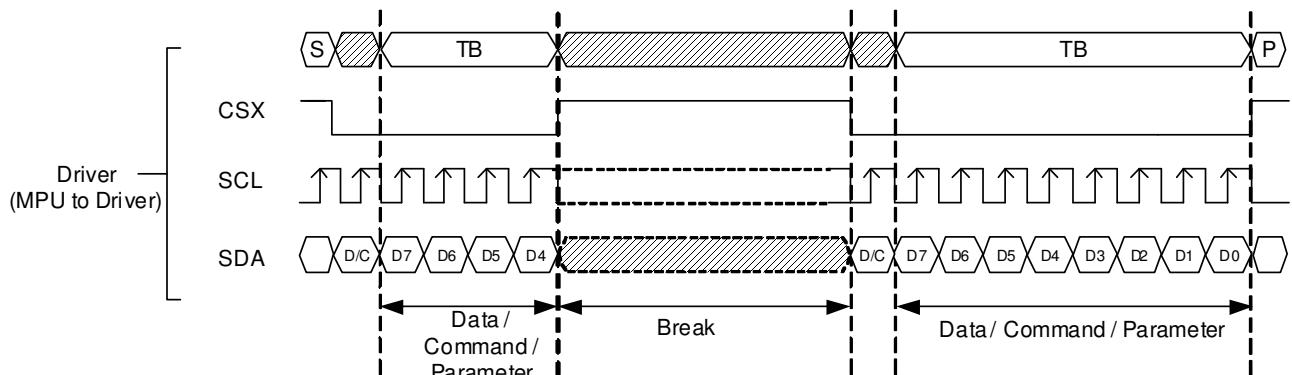


7.1.11. Data Transfer Break and Recovery

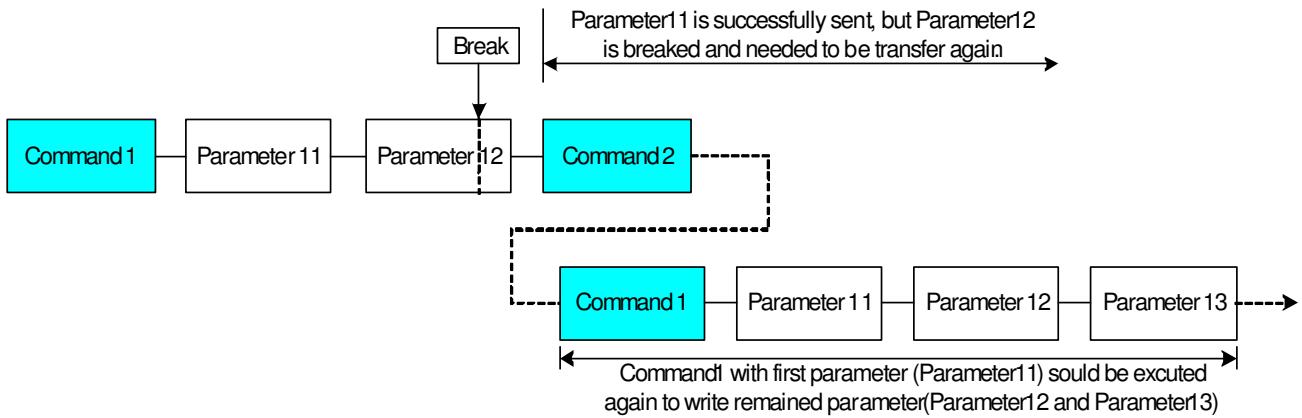
If there is a break in data transmission by RESX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



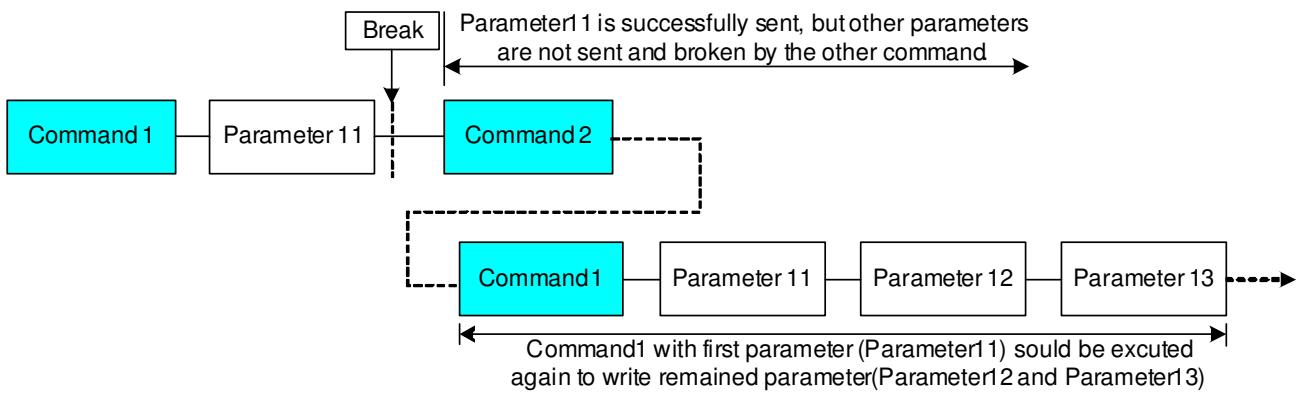
If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.



If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.

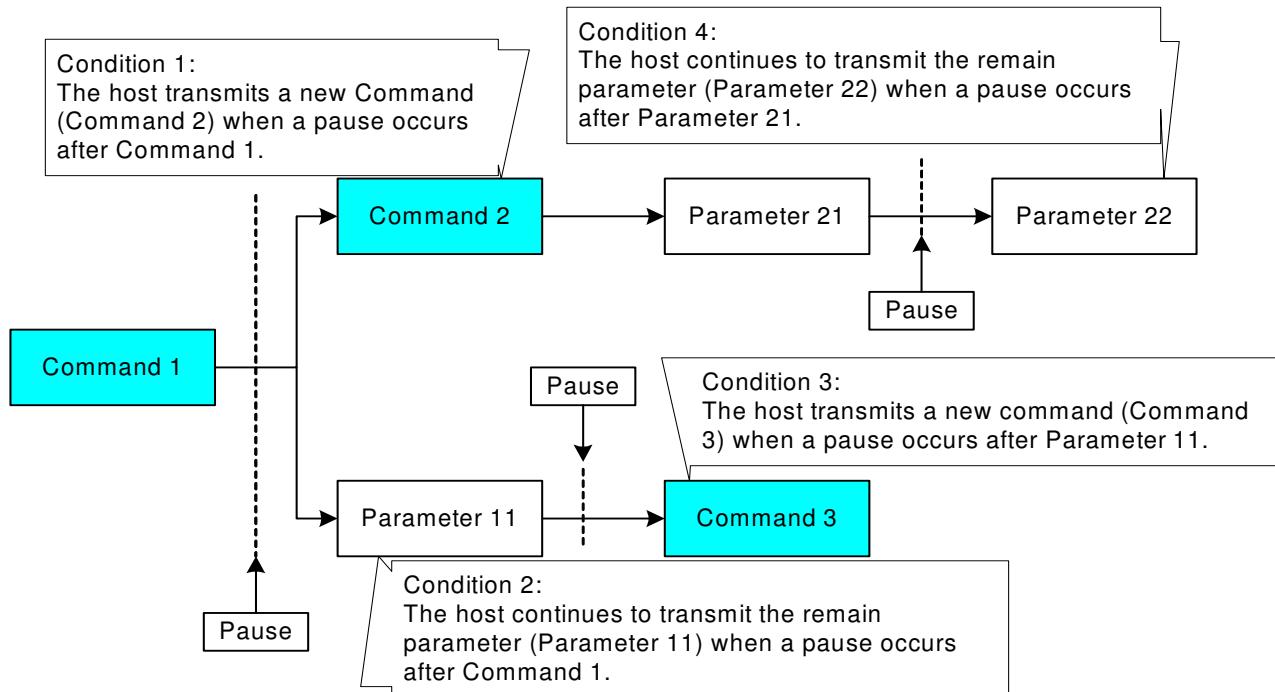


7.1.12. Data Transfer Pause

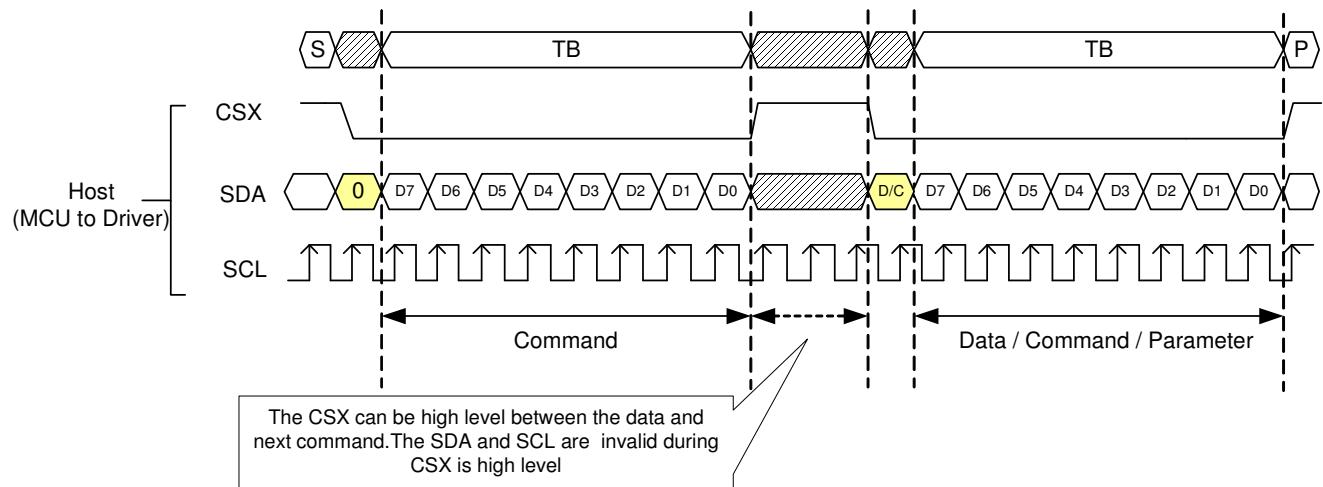
It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then ILI9341 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:

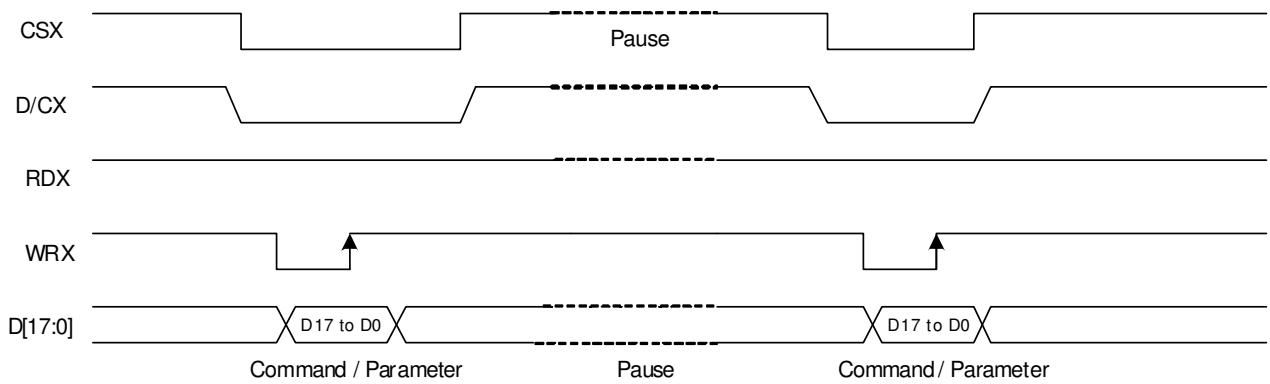
- 1) Command-Pause-Command
- 2) Command-Pause-Parameter
- 3) Parameter-Pause-Command
- 4) Parameter-Pause-Parameter



7.1.13. Serial Interface Pause (3_wire)



7.1.14. Parallel Interface Pause

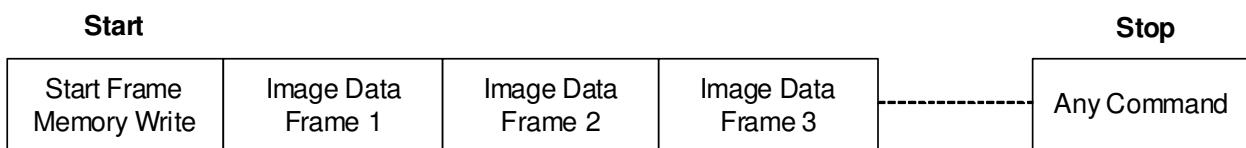


7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

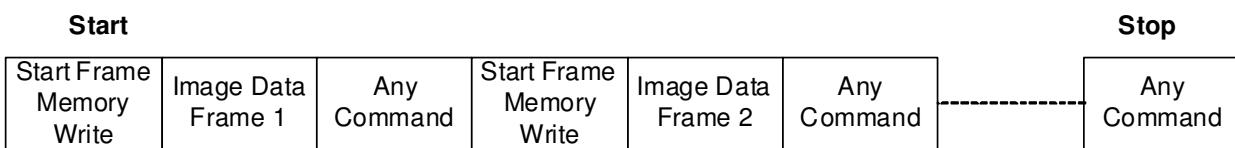
7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.

Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

7.2. RGB Interface

7.2.1. RGB Interface Selection

ILI9341 has two kinds of RGB interface and these interfaces can be selected by RCM [1:0] bits. When RCM [1:0] bits are set to “10”, the DE mode is selected which utilizes VSYNC, HSYNC, DOTCLK, DE, D [17:0] pins; when RCM [1:0] bits are set to “11”, the SYNC mode is selected which utilizes VSYNC, HSYNC, DOTCLK, D [17:0] pins. Using RGB interface must selection serial interface.

ILI9341 supports several pixel formats that can be selected by DPI [2:0] bits of “Pixel Format Set (3Ah)” and RIM bit of RF6h command. The selection of a given interfaces is done by setting RCM [1:0] and DPI [2:0] as show in the following table.

RCM[1:0]	RIM	DPI[2:0]		RGB Interface Mode		RGB Mode						Used Pins					
1	0	0	1	1	0	DE Mode Valid data is determined by the DE signal						VSYNC, HSYNC, DE, DOTCLK, D[17:0]					
1	0	0	1	0	1							VSYNC, HSYNC, DE, DOTCLK, D[17:13] & D[11:1]					
1	0	1	1	1	0							VSYNC, HSYNC, DE, DOTCLK, D[5:0]					
1	0	1	1	0	1							VSYNC, HSYNC, DE, DOTCLK, D[5:0]					
1	1	0	1	1	0							VSYNC, HSYNC, DOTCLK, D[17:0]					
1	1	0	1	0	1							VSYNC, HSYNC, DOTCLK, D[17:13] & D[11:1]					
1	1	1	1	1	0							VSYNC, HSYNC, DOTCLK, D[5:0]					
1	1	1	1	0	1							VSYNC, HSYNC, DOTCLK, D[5:0]					

18-bit data bus interface (D[17:0] is used) , DPI[2:0] = 110, and RIM=0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

16-bit data bus interface (D[17:13] & D[11:1] is used) , DPI[2:0] = 101, and RIM=0

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 110, and RIM=1

D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	
18bpp Frame Memory Write	R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

6-bit data bus interface (D[5:0] is used) , DPI[2:0] = 101, and RIM=1

D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0	D5	D4	D3	D2	D1	D0
16bpp Frame Memory Write	R[4]	R[3]	R[2]	R[1]	R[0]		G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]

The LSB data of red/blue color depends on the EPF[1:0] setting.

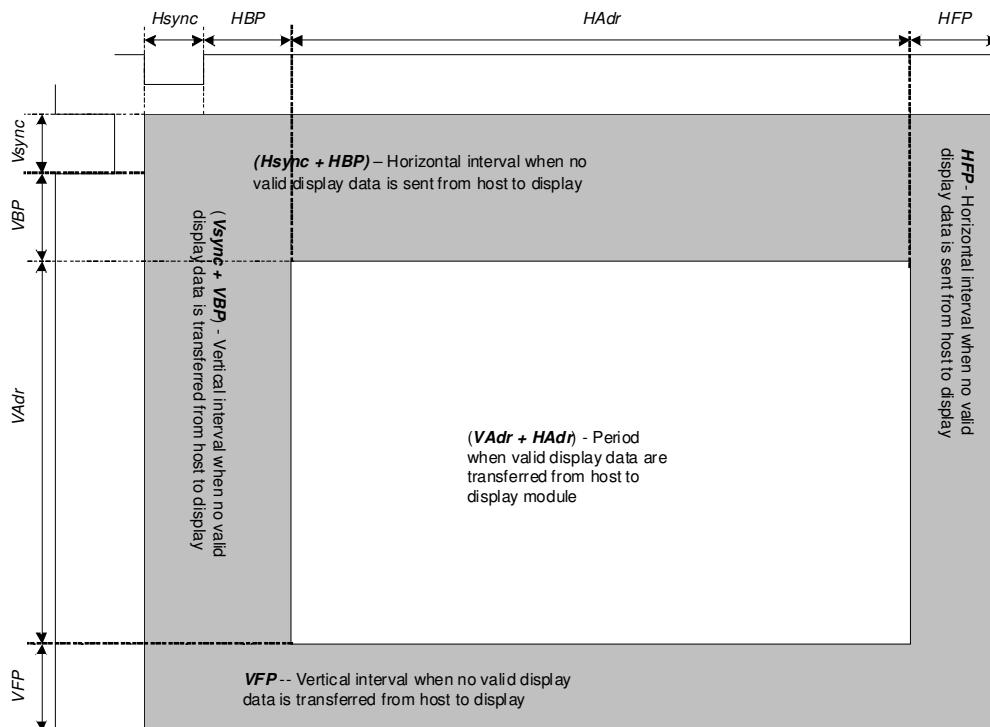
Pixel clock (DOTCLK) is running all the time without stopping and used to enter VSYNC, HSYNC, DE and D [17:0] states when there is a rising edge of the DOTCLK. Vertical synchronization (VSYNC) is used to tell when

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there is received a new frame of the display. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

Horizontal synchronization (Hsync) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the DOTCLK signal.

In DE mode, Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the DOTCLK signal. D [17:0] are used to tell what is the information of the image that is transferred on the display (When DE= '0' (low) and there is a rising edge of DOTCLK). D [17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the DOTCLK signal. In SYNC mode, the valid display data is inputted in pixel unit via D [17:0] according to HFP/HBP settings of HSYNC signal and VFP/VBP setting of VSYNC. In both RGB interface modes, the input display data is written to GRAM first then outputs corresponding source voltage according the gray data from GRAM.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Address	HAdr		-	240	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	320	-	Line
Vertical Front Porch	VFP		3	4	-	Line

Typical values are setting example when used with panel resolution 240 x 320 (QVGA), clock frequency 6.35MHz and frame

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frequency about 70Hz.

Notes:

1. Vertical period (one frame) shall be equal to the sum of **Vsync + VBP + VAdr + VFP**.
2. Horizontal period (one line) shall be equal to the sum of **Hsync + HBP + HAdr + HFP**.
3. Control signals PCLK and Hsync shall be transmitted as specified at all times while valid pixels are transferred between the host processor and the display module.

Also make sure that

(Number of PCLK per 1 line) \geq (Number of RTN clock) \times Division ratio (DIV) \times PCDIV

Setting Example for Display Control Clock in RGB Interface Operation

Register Display operation using DPI is in synchronization with internal clock PCLKD which is generated by dividing DOTCLK.

PCDIV [5:0]: Number of DOTCLK during internal clock PCLKD's high / low period. In units of 1 clock.

PCDIV specifying DOTCLK's division ratio, are determined so that difference between PCLKD's frequency and internal oscillation clock 615KHz is the smallest. Set PCDIV follow the restriction

(Number of PCLK in 1H) \geq (Number of RTN clock) \times Division ratio (DIV) \times PCDIV.

Setting Example: To set frame frequency to 70Hz:

Internal Clock

Internal Oscillation Clock: 615KHz

DIV[1:0] = 2'b0 (x 1/1)

RTN[4:0] = 5'h1b (27 clocks)

FP = 7'h2 (2 lines), BP = 7'h2 (2 lines), NL = 6'h27 (320 lines)

Frame Rate \rightarrow 70.30Hz

DOTCLK

HSYNC = 10 CLK

HBP = 20 CLK

HFP=10 CLK

70Hz \times (2 + 320 + 2) lines \times (10 + 20 + 240 + 10) clocks = 6.35MHz

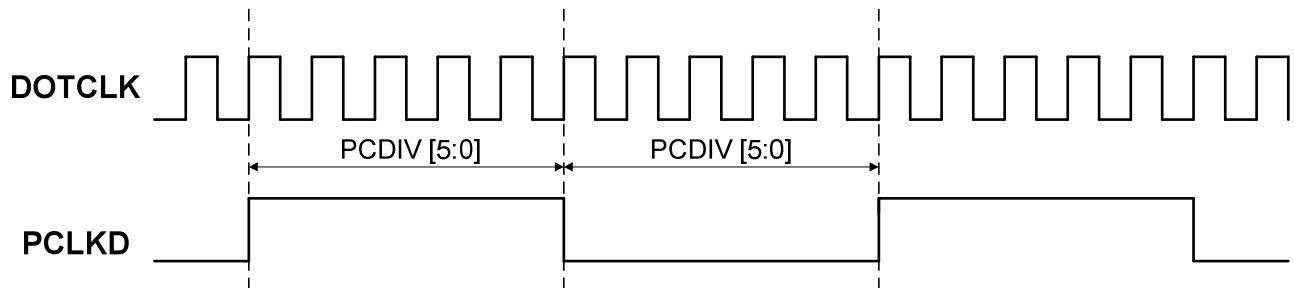
DOTCLK frequency = 6.35MHz

6.35 MHz / 615KHz = 10.32 \square Set PCDIV so that PCLK is divided by 10.

external fosc = 6.35 MHz / 10 = 635KHz

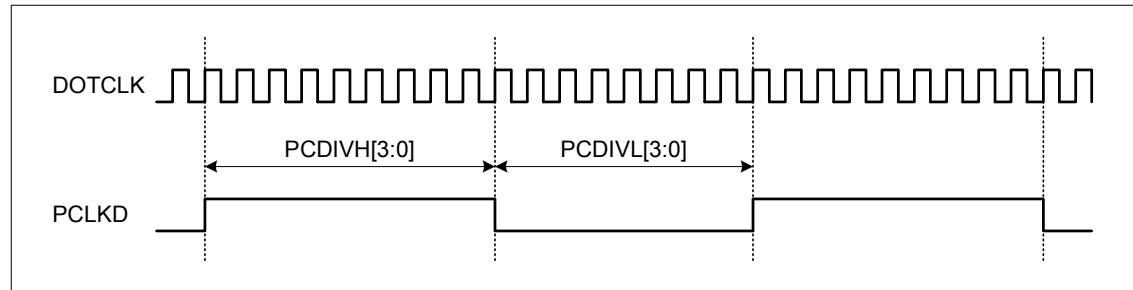
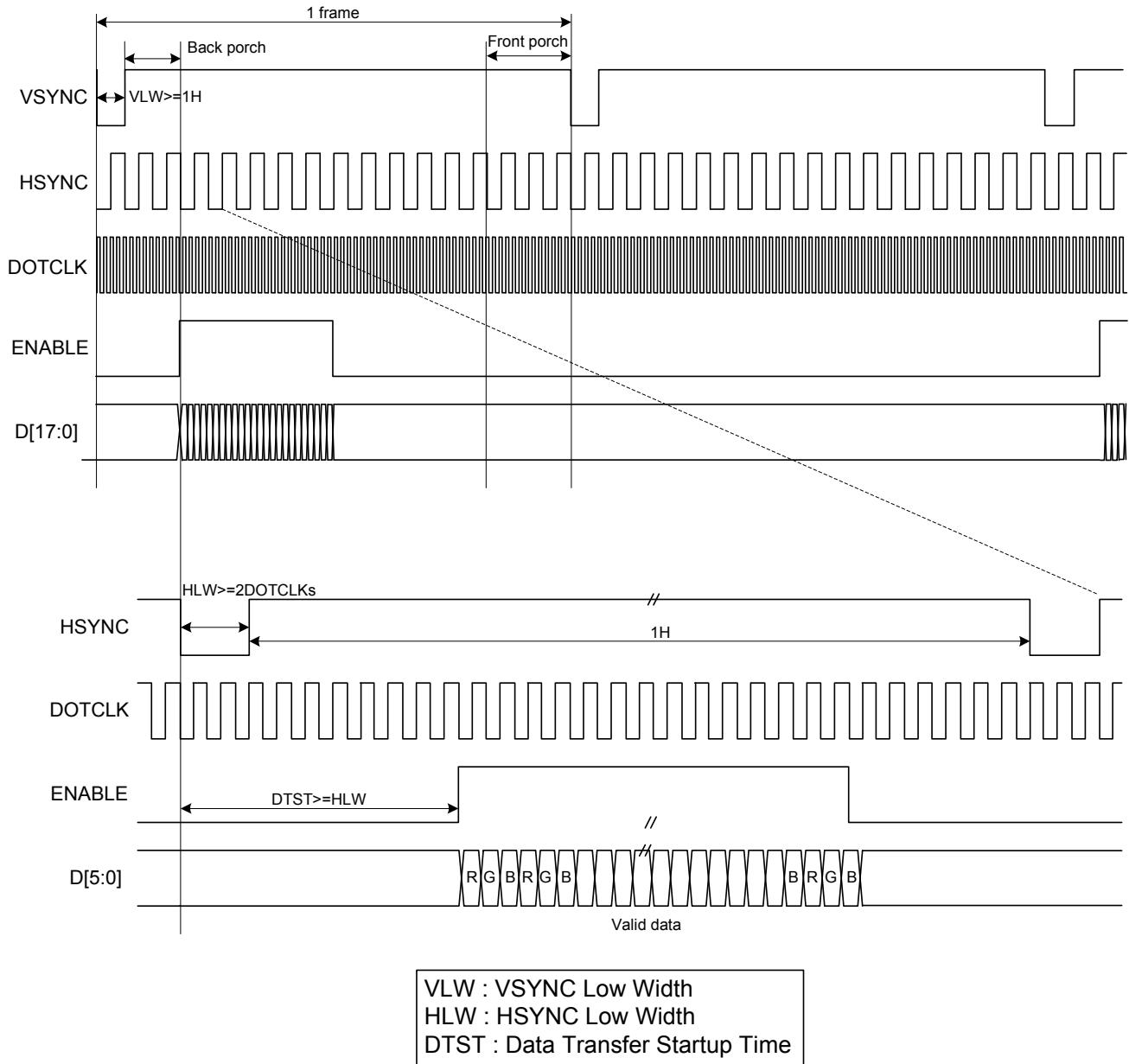
PCDIV = [6.35MHz / 635KHz] / 2] - 1 = 4

PCDIV[5:0] = 6'h04 (10 DOTCLK)



7.2.2. RGB Interface Timing

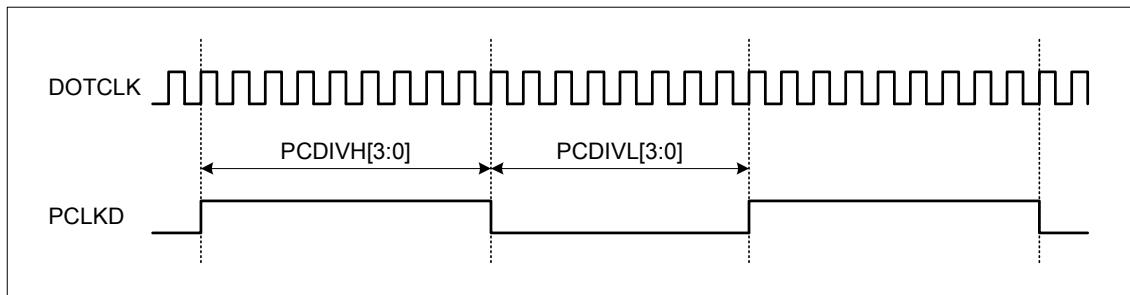
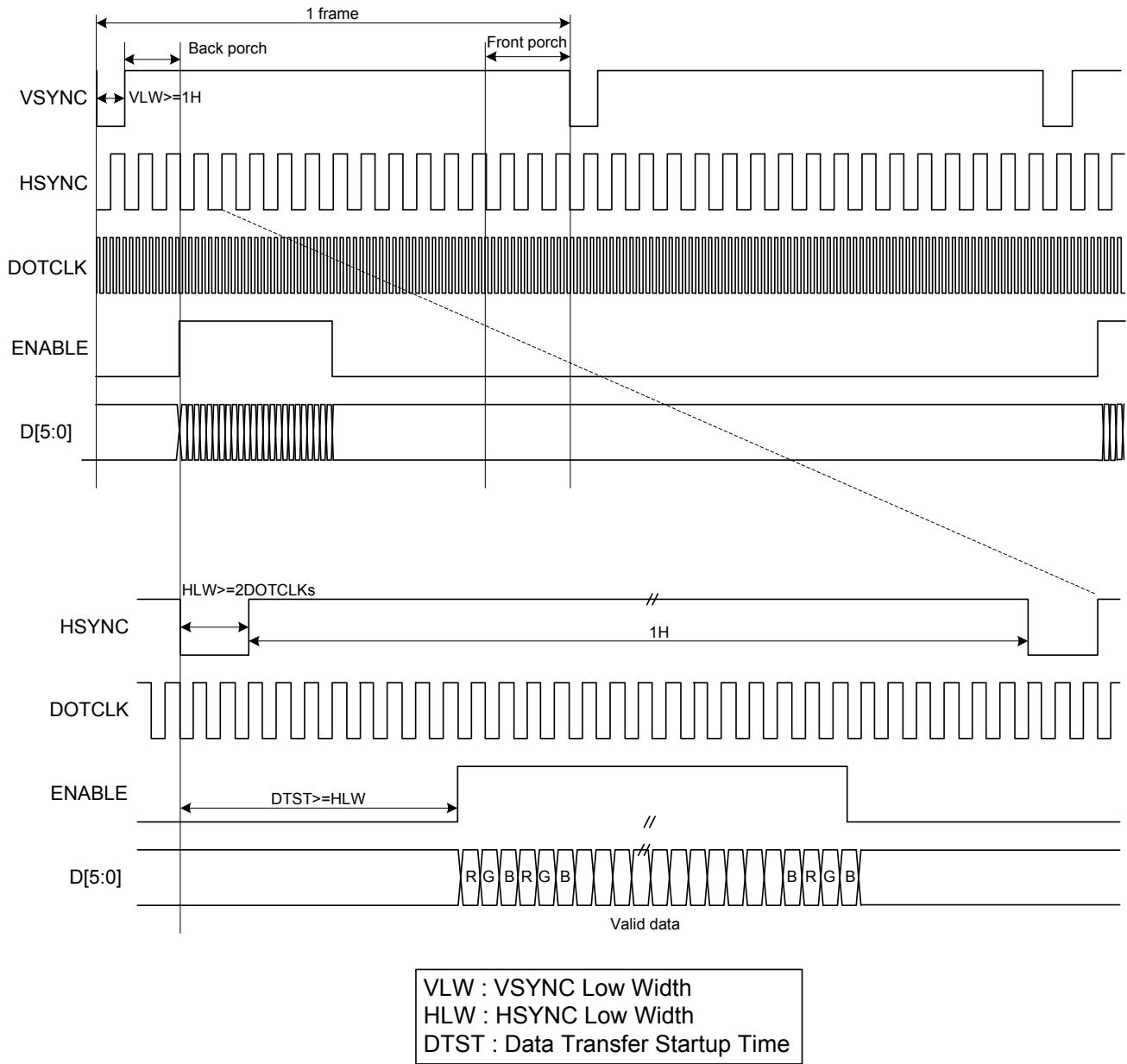
The timing chart of 18-/16-bit RGB interface mode is shown as below.



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

The timing chart of 6-bit RGB interface mode is shown as below:



Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

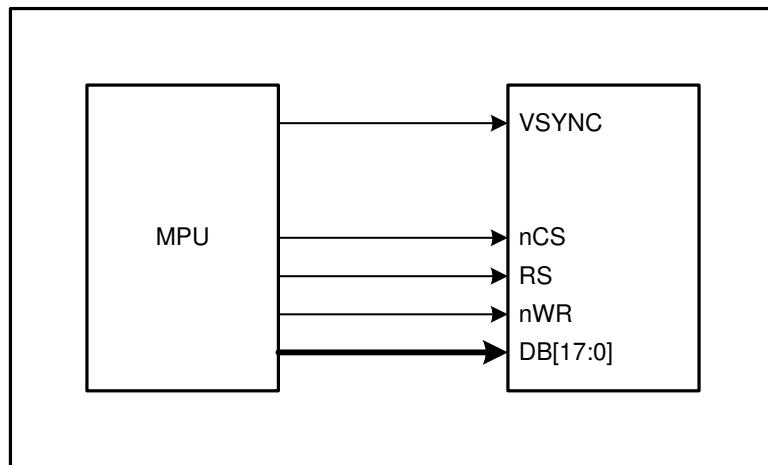
Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='0' of "Interface Mode Control (B0h)" command.

Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

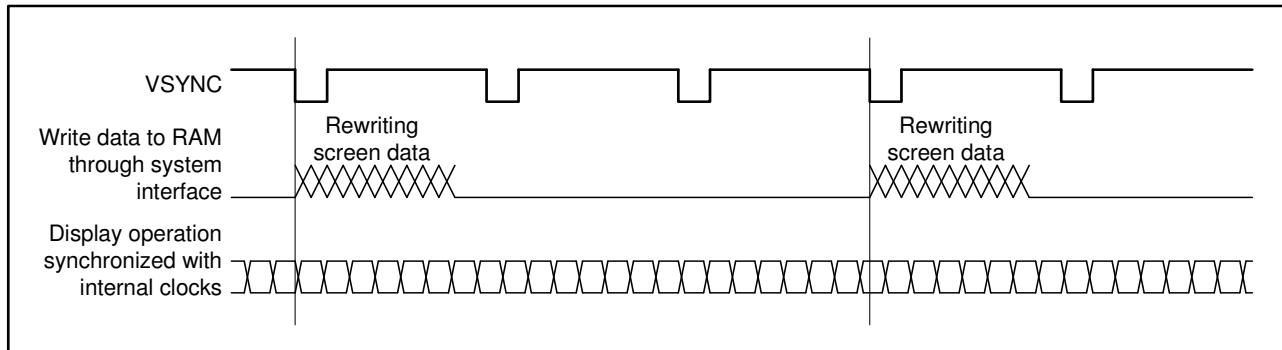
Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.

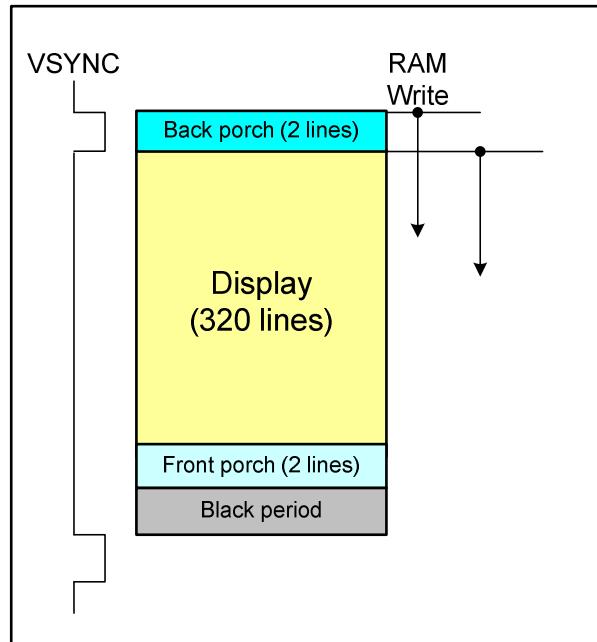
7.3. VSYNC Interface

ILI9341 supports the VSYNC interface in synchronization with the frame-synchronizing signal VSYNC to display the moving picture with the 8080-I /8080-II system interface. When the VSYNC interface is selected to display a moving picture, the minimum GRAM update speed is limited and the VSYNC interface is enabled by setting DM[1:0] = "10" and RM = "0".



In the VSYNC mode, the display operation is synchronized with the internal clock and VSYNC input and the frame rate is determined by the pulse rate of VSYNC signal. All display data are stored in GRAM to minimize total data transfer required for moving picture display.





The VSYNC interface has the minimum speed limitation of writing data to the internal GRAM via the system interface, which are calculated from the following formula.

Internal clock frequency (fosc.) [Hz] = FrameFrequency x (DisplayLine (NL) + FrontPorch (VFP) + BackPorch (VBP)) x ClockCyclePerLines (RTN) x FrequencyFluctuation.

$$\text{Minimum RAM write speed [Hz]} > \frac{240 \times \text{DisplayLines}(NL)}{[\text{BackPorch}(VBP) + \text{DisplayLines}(NL) - \text{margins}] \times \text{Clocks per line} \times (1/fosc)}$$

Note: When the RAM write operation does not start from the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum GRAM writing speed and internal clock frequency in VSYNC interface mode is as below.

[Example]

Display size: 240 RGB × 320 lines

Lines: 320 lines (NL = 100111)

Back porch: 2 lines (VBP = 0000010)

Front porch: 2 lines (VFP = 0000010)

Frame frequency: 70 Hz

Frequency fluctuation: 10%

$$\text{Internal oscillator clock (fosc.) [Hz]} = 70 \times [320 + 2 + 2] \times 27 \text{ clocks} \times (1.1/0.9) \doteq 748\text{KHz}$$

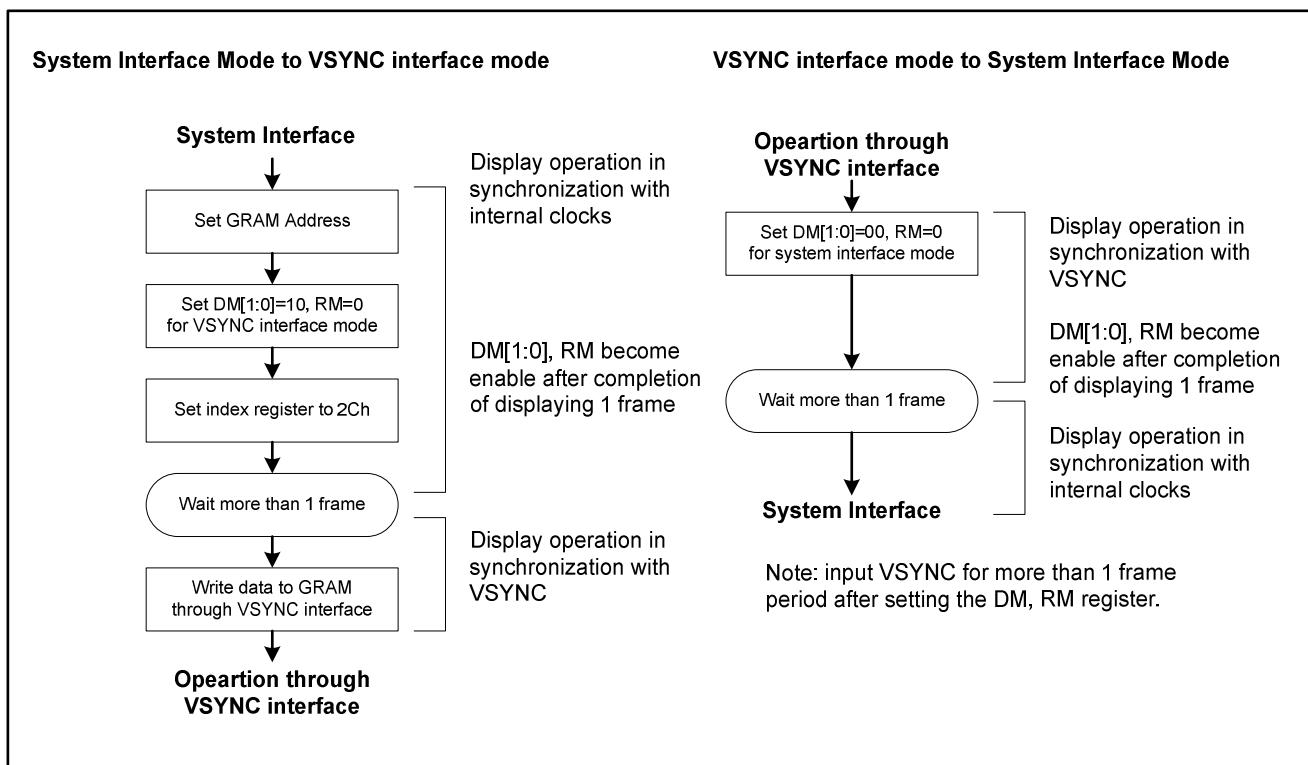
When calculate the internal clock frequency, the oscillator variation is needed to be taken into consideration. In the above example, the calculated internal clock frequency with $\pm 10\%$ margin variation is considered and ensures to complete the display operation within one VSYNC cycle. The causes of frequency variation come from fabrication process of LSI, room temperature, external resistors and VCI voltage variation.

$$\text{Minimum speed for RAM writing [Hz]} > 240 \times 320 \times 748K / [(2 + 320 - 2)\text{lines} \times 27\text{clocks}] \doteq 6.65 \text{ MHz}$$

The above theoretical value is calculated based on the premise that the ILI9341 starts to write data into the internal GRAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line and the GRAM line address where data writing operation is performed. The GRAM write speed of 6.65MHz or more will guarantee the completion of GRAM write operation before the ILI9341 starts to display the GRAM data on the screen and enable to rewrite the entire screen without flicker.

Notes in using the VSYNC interface

1. The minimum GRAM write speed must be satisfied and the frequency variation must be taken into consideration.
2. The display frame rate is determined by the VSYNC signal and the period of VSYNC must be longer than the scan period of an entire display.
3. When switching from the internal clock operation mode ($DM[1:0] = "00"$) to the VSYNC interface mode or inversely, the switching starts from the next VSYNC cycle, i.e. after completing the display of the frame.
4. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.



7.4. Color Depth Conversion Look Up Table

When ILI9341 operates in parallel 16-bit interface, the color depth conversion is done by look-up table and extend input data format to 18-bit. See the detailed for look-up table of color depth conversion.

R input (5-bit) 16-bit/pixel –mode 65,536 colors	R output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	R ₀₀₅ R ₀₀₄ R ₀₀₃ R ₀₀₂ R ₀₀₁ R ₀₀₀	1
00001	R ₀₁₅ R ₀₁₄ R ₀₁₃ R ₀₁₂ R ₀₁₁ R ₀₁₀	2
00010	R ₀₂₅ R ₀₂₄ R ₀₂₃ R ₀₂₂ R ₀₂₁ R ₀₂₀	3
00011	R ₀₃₅ R ₀₃₄ R ₀₃₃ R ₀₃₂ R ₀₃₁ R ₀₃₀	4
00100	R ₀₄₅ R ₀₄₄ R ₀₄₃ R ₀₄₂ R ₀₄₁ R ₀₄₀	5
00101	R ₀₅₅ R ₀₅₄ R ₀₅₃ R ₀₅₂ R ₀₅₁ R ₀₅₀	6
00110	R ₀₆₅ R ₀₆₄ R ₀₆₃ R ₀₆₂ R ₀₆₁ R ₀₆₀	7
00111	R ₀₇₅ R ₀₇₄ R ₀₇₃ R ₀₇₂ R ₀₇₁ R ₀₇₀	8
01000	R ₀₈₅ R ₀₈₄ R ₀₈₃ R ₀₈₂ R ₀₈₁ R ₀₈₀	9
01001	R ₀₉₅ R ₀₉₄ R ₀₉₃ R ₀₉₂ R ₀₉₁ R ₀₉₀	10
01010	R ₁₀₅ R ₁₀₄ R ₁₀₃ R ₁₀₂ R ₁₀₁ R ₁₀₀	11
01011	R ₁₁₅ R ₁₁₄ R ₁₁₃ R ₁₁₂ R ₁₁₁ R ₁₁₀	12
01100	R ₁₂₅ R ₁₂₄ R ₁₂₃ R ₁₂₂ R ₁₂₁ R ₁₂₀	13
01101	R ₁₃₅ R ₁₃₄ R ₁₃₃ R ₁₃₂ R ₁₃₁ R ₁₃₀	14
01110	R ₁₄₅ R ₁₄₄ R ₁₄₃ R ₁₄₂ R ₁₄₁ R ₁₄₀	15
01111	R ₁₅₅ R ₁₅₄ R ₁₅₃ R ₁₅₂ R ₁₅₁ R ₁₅₀	16
10000	R ₁₆₅ R ₁₆₄ R ₁₆₃ R ₁₆₂ R ₁₆₁ R ₁₆₀	17
10001	R ₁₇₅ R ₁₇₄ R ₁₇₃ R ₁₇₂ R ₁₇₁ R ₁₇₀	18
10010	R ₁₈₅ R ₁₈₄ R ₁₈₃ R ₁₈₂ R ₁₈₁ R ₁₈₀	19
10011	R ₁₉₅ R ₁₉₄ R ₁₉₃ R ₁₉₂ R ₁₉₁ R ₁₉₀	20
10100	R ₂₀₅ R ₂₀₄ R ₂₀₃ R ₂₀₂ R ₂₀₁ R ₂₀₀	21
10101	R ₂₁₅ R ₂₁₄ R ₂₁₃ R ₂₁₂ R ₂₁₁ R ₂₁₀	22
10110	R ₂₂₅ R ₂₂₄ R ₂₂₃ R ₂₂₂ R ₂₂₁ R ₂₂₀	23
10111	R ₂₃₅ R ₂₃₄ R ₂₃₃ R ₂₃₂ R ₂₃₁ R ₂₃₀	24
11000	R ₂₄₅ R ₂₄₄ R ₂₄₃ R ₂₄₂ R ₂₄₁ R ₂₄₀	25
11001	R ₂₅₅ R ₂₅₄ R ₂₅₃ R ₂₅₂ R ₂₅₁ R ₂₅₀	26
11010	R ₂₆₅ R ₂₆₄ R ₂₆₃ R ₂₆₂ R ₂₆₁ R ₂₆₀	27
11011	R ₂₇₅ R ₂₇₄ R ₂₇₃ R ₂₇₂ R ₂₇₁ R ₂₇₀	28
11100	R ₂₈₅ R ₂₈₄ R ₂₈₃ R ₂₈₂ R ₂₈₁ R ₂₈₀	29
11101	R ₂₉₅ R ₂₉₄ R ₂₉₃ R ₂₉₂ R ₂₉₁ R ₂₉₀	30
11110	R ₃₀₅ R ₃₀₄ R ₃₀₃ R ₃₀₂ R ₃₀₁ R ₃₀₀	31
11111	R ₃₁₅ R ₃₁₄ R ₃₁₃ R ₃₁₂ R ₃₁₁ R ₃₁₀	32

G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
000000	G ₀₀₅ G ₀₀₄ G ₀₀₃ G ₀₀₂ G ₀₀₁ G ₀₀₀	33
000001	G ₀₁₅ G ₀₁₄ G ₀₁₃ G ₀₁₂ G ₀₁₁ G ₀₁₀	34
000010	G ₀₂₅ G ₀₂₄ G ₀₂₃ G ₀₂₂ G ₀₂₁ G ₀₂₀	35
000011	G ₀₃₅ G ₀₃₄ G ₀₃₃ G ₀₃₂ G ₀₃₁ G ₀₃₀	36
000100	G ₀₄₅ G ₀₄₄ G ₀₄₃ G ₀₄₂ G ₀₄₁ G ₀₄₀	37
000101	G ₀₅₅ G ₀₅₄ G ₀₅₃ G ₀₅₂ G ₀₅₁ G ₀₅₀	38
000110	G ₀₆₅ G ₀₆₄ G ₀₆₃ G ₀₆₂ G ₀₆₁ G ₀₆₀	39
000111	G ₀₇₅ G ₀₇₄ G ₀₇₃ G ₀₇₂ G ₀₇₁ G ₀₇₀	40
001000	G ₀₈₅ G ₀₈₄ G ₀₈₃ G ₀₈₂ G ₀₈₁ G ₀₈₀	41
001001	G ₀₉₅ G ₀₉₄ G ₀₉₃ G ₀₉₂ G ₀₉₁ G ₀₉₀	42
001010	G ₁₀₅ G ₁₀₄ G ₁₀₃ G ₁₀₂ G ₁₀₁ G ₁₀₀	43
001011	G ₁₁₅ G ₁₁₄ G ₁₁₃ G ₁₁₂ G ₁₁₁ G ₁₁₀	44
001100	G ₁₂₅ G ₁₂₄ G ₁₂₃ G ₁₂₂ G ₁₂₁ G ₁₂₀	45
001101	G ₁₃₅ G ₁₃₄ G ₁₃₃ G ₁₃₂ G ₁₃₁ G ₁₃₀	46
001110	G ₁₄₅ G ₁₄₄ G ₁₄₃ G ₁₄₂ G ₁₄₁ G ₁₄₀	47
001111	G ₁₅₅ G ₁₅₄ G ₁₅₃ G ₁₅₂ G ₁₅₁ G ₁₅₀	48
010000	G ₁₆₅ G ₁₆₄ G ₁₆₃ G ₁₆₂ G ₁₆₁ G ₁₆₀	49
010001	G ₁₇₅ G ₁₇₄ G ₁₇₃ G ₁₇₂ G ₁₇₁ G ₁₇₀	50
010010	G ₁₈₅ G ₁₈₄ G ₁₈₃ G ₁₈₂ G ₁₈₁ G ₁₈₀	51
010011	G ₁₉₅ G ₁₉₄ G ₁₉₃ G ₁₉₂ G ₁₉₁ G ₁₉₀	52
010100	G ₂₀₅ G ₂₀₄ G ₂₀₃ G ₂₀₂ G ₂₀₁ G ₂₀₀	53
010101	G ₂₁₅ G ₂₁₄ G ₂₁₃ G ₂₁₂ G ₂₁₁ G ₂₁₀	54
010110	G ₂₂₅ G ₂₂₄ G ₂₂₃ G ₂₂₂ G ₂₂₁ G ₂₂₀	55
010111	G ₂₃₅ G ₂₃₄ G ₂₃₃ G ₂₃₂ G ₂₃₁ G ₂₃₀	56
011000	G ₂₄₅ G ₂₄₄ G ₂₄₃ G ₂₄₂ G ₂₄₁ G ₂₄₀	57
011001	G ₂₅₅ G ₂₅₄ G ₂₅₃ G ₂₅₂ G ₂₅₁ G ₂₅₀	58
011010	G ₂₆₅ G ₂₆₄ G ₂₆₃ G ₂₆₂ G ₂₆₁ G ₂₆₀	59
011011	G ₂₇₅ G ₂₇₄ G ₂₇₃ G ₂₇₂ G ₂₇₁ G ₂₇₀	60
011100	G ₂₈₅ G ₂₈₄ G ₂₈₃ G ₂₈₂ G ₂₈₁ G ₂₈₀	61
011101	G ₂₉₅ G ₂₉₄ G ₂₉₃ G ₂₉₂ G ₂₉₁ G ₂₉₀	62
011110	G ₃₀₅ G ₃₀₄ G ₃₀₃ G ₃₀₂ G ₃₀₁ G ₃₀₀	63
011111	G ₃₁₅ G ₃₁₄ G ₃₁₃ G ₃₁₂ G ₃₁₁ G ₃₁₀	64
100000	G ₃₂₅ G ₃₂₄ G ₃₂₃ G ₃₂₂ G ₃₂₁ G ₃₂₀	65
100001	G ₃₃₅ G ₃₃₄ G ₃₃₃ G ₃₃₂ G ₃₃₁ G ₃₃₀	66

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G input (6-bit) 16-bit/pixel –mode 65,536 colors	G output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
100010	G ₃₄₅ G ₃₄₄ G ₃₄₃ G ₃₄₂ G ₃₄₁ G ₃₄₀	67
100011	G ₃₅₅ G ₃₅₄ G ₃₅₃ G ₃₅₂ G ₃₅₁ G ₃₅₀	68
100100	G ₃₆₅ G ₃₆₄ G ₃₆₃ G ₃₆₂ G ₃₆₁ G ₃₆₀	69
100101	G ₃₇₅ G ₃₇₄ G ₃₇₃ G ₃₇₂ G ₃₇₁ G ₃₇₀	70
100110	G ₃₈₅ G ₃₈₄ G ₃₈₃ G ₃₈₂ G ₃₈₁ G ₃₈₀	71
100111	G ₃₉₅ G ₃₉₄ G ₃₉₃ G ₃₉₂ G ₃₉₁ G ₃₉₀	72
101000	G ₄₀₅ G ₄₀₄ G ₄₀₃ G ₄₀₂ G ₄₀₁ G ₄₀₀	73
101001	G ₄₁₅ G ₄₁₄ G ₄₁₃ G ₄₁₂ G ₄₁₁ G ₄₁₀	74
101010	G ₄₂₅ G ₄₂₄ G ₄₂₃ G ₄₂₂ G ₄₂₁ G ₄₂₀	75
101011	G ₄₃₅ G ₄₃₄ G ₄₃₃ G ₄₃₂ G ₄₃₁ G ₄₃₀	76
101100	G ₄₄₅ G ₄₄₄ G ₄₄₃ G ₄₄₂ G ₄₄₁ G ₄₄₀	77
101101	G ₄₅₅ G ₄₅₄ G ₄₅₃ G ₄₅₂ G ₄₅₁ G ₄₅₀	78
101110	G ₄₆₅ G ₄₆₄ G ₄₆₃ G ₄₆₂ G ₄₆₁ G ₄₆₀	79
101111	G ₄₇₅ G ₄₇₄ G ₄₇₃ G ₄₇₂ G ₄₇₁ G ₄₇₀	80
110000	G ₄₈₅ G ₄₈₄ G ₄₈₃ G ₄₈₂ G ₄₈₁ G ₄₈₀	81
110001	G ₄₉₅ G ₄₉₄ G ₄₉₃ G ₄₉₂ G ₄₉₁ G ₄₉₀	82
110010	G ₅₀₅ G ₅₀₄ G ₅₀₃ G ₅₀₂ G ₅₀₁ G ₅₀₀	83
110011	G ₅₁₅ G ₅₁₄ G ₅₁₃ G ₅₁₂ G ₅₁₁ G ₅₁₀	84
110100	G ₅₂₅ G ₅₂₄ G ₅₂₃ G ₅₂₂ G ₅₂₁ G ₅₂₀	85
110101	G ₅₃₅ G ₅₃₄ G ₅₃₃ G ₅₃₂ G ₅₃₁ G ₅₃₀	86
110110	G ₅₄₅ G ₅₄₄ G ₅₄₃ G ₅₄₂ G ₅₄₁ G ₅₄₀	87
110111	G ₅₅₅ G ₅₅₄ G ₅₅₃ G ₅₅₂ G ₅₅₁ G ₅₅₀	88
111000	G ₅₆₅ G ₅₆₄ G ₅₆₃ G ₅₆₂ G ₅₆₁ G ₅₆₀	89
111001	G ₅₇₅ G ₅₇₄ G ₅₇₃ G ₅₇₂ G ₅₇₁ G ₅₇₀	90
111010	G ₅₈₅ G ₅₈₄ G ₅₈₃ G ₅₈₂ G ₅₈₁ G ₅₈₀	91
111011	G ₅₉₅ G ₅₉₄ G ₅₉₃ G ₅₉₂ G ₅₉₁ G ₅₉₀	92
111100	G ₆₀₅ G ₆₀₄ G ₆₀₃ G ₆₀₂ G ₆₀₁ G ₆₀₀	93
111101	G ₆₁₅ G ₆₁₄ G ₆₁₃ G ₆₁₂ G ₆₁₁ G ₆₁₀	94
111110	G ₆₂₅ G ₆₂₄ G ₆₂₃ G ₆₂₂ G ₆₂₁ G ₆₂₀	95
111111	G ₆₃₅ G ₆₃₄ G ₆₃₃ G ₆₃₂ G ₆₃₁ G ₆₃₀	96

B input (5-bit) 16-bit/pixel –mode 65,536 colors	B output (6-bit) 18-bit/pixel –mode 262,144 colors	Command Code (0x2Dh) RGBSET Parameter
00000	B ₀₀₅ B ₀₀₄ B ₀₀₃ B ₀₀₂ B ₀₀₁ B ₀₀₀	97
00001	B ₀₁₅ B ₀₁₄ B ₀₁₃ B ₀₁₂ B ₀₁₁ B ₀₁₀	98
00010	B ₀₂₅ B ₀₂₄ B ₀₂₃ B ₀₂₂ B ₀₂₁ B ₀₂₀	99
00011	B ₀₃₅ B ₀₃₄ B ₀₃₃ B ₀₃₂ B ₀₃₁ B ₀₃₀	100
00100	B ₀₄₅ B ₀₄₄ B ₀₄₃ B ₀₄₂ B ₀₄₁ B ₀₄₀	101
00101	B ₀₅₅ B ₀₅₄ B ₀₅₃ B ₀₅₂ B ₀₅₁ B ₀₅₀	102
00110	B ₀₆₅ B ₀₆₄ B ₀₆₃ B ₀₆₂ B ₀₆₁ B ₀₆₀	103
00111	B ₀₇₅ B ₀₇₄ B ₀₇₃ B ₀₇₂ B ₀₇₁ B ₀₇₀	104
01000	B ₀₈₅ B ₀₈₄ B ₀₈₃ B ₀₈₂ B ₀₈₁ B ₀₈₀	105
01001	B ₀₉₅ B ₀₉₄ B ₀₉₃ B ₀₉₂ B ₀₉₁ B ₀₉₀	106
01010	B ₁₀₅ B ₁₀₄ B ₁₀₃ B ₁₀₂ B ₁₀₁ B ₁₀₀	107
01011	B ₁₁₅ B ₁₁₄ B ₁₁₃ B ₁₁₂ B ₁₁₁ B ₁₁₀	108
01100	B ₁₂₅ B ₁₂₄ B ₁₂₃ B ₁₂₂ B ₁₂₁ B ₁₂₀	109
01101	B ₁₃₅ B ₁₃₄ B ₁₃₃ B ₁₃₂ B ₁₃₁ B ₁₃₀	110
01110	B ₁₄₅ B ₁₄₄ B ₁₄₃ B ₁₄₂ B ₁₄₁ B ₁₄₀	111
01111	B ₁₅₅ B ₁₅₄ B ₁₅₃ B ₁₅₂ B ₁₅₁ B ₁₅₀	112
10000	B ₁₆₅ B ₁₆₄ B ₁₆₃ B ₁₆₂ B ₁₆₁ B ₁₆₀	113
10001	B ₁₇₅ B ₁₇₄ B ₁₇₃ B ₁₇₂ B ₁₇₁ B ₁₇₀	114
10010	B ₁₈₅ B ₁₈₄ B ₁₈₃ B ₁₈₂ B ₁₈₁ B ₁₈₀	115
10011	B ₁₉₅ B ₁₉₄ B ₁₉₃ B ₁₉₂ B ₁₉₁ B ₁₉₀	116
10100	B ₂₀₅ B ₂₀₄ B ₂₀₃ B ₂₀₂ B ₂₀₁ B ₂₀₀	117
10101	B ₂₁₅ B ₂₁₄ B ₂₁₃ B ₂₁₂ B ₂₁₁ B ₂₁₀	118
10110	B ₂₂₅ B ₂₂₄ B ₂₂₃ B ₂₂₂ B ₂₂₁ B ₂₂₀	119
10111	B ₂₃₅ B ₂₃₄ B ₂₃₃ B ₂₃₂ B ₂₃₁ B ₂₃₀	120
11000	B ₂₄₅ B ₂₄₄ B ₂₄₃ B ₂₄₂ B ₂₄₁ B ₂₄₀	121
11001	B ₂₅₅ B ₂₅₄ B ₂₅₃ B ₂₅₂ B ₂₅₁ B ₂₅₀	122
11010	B ₂₆₅ B ₂₆₄ B ₂₆₃ B ₂₆₂ B ₂₆₁ B ₂₆₀	123
11011	B ₂₇₅ B ₂₇₄ B ₂₇₃ B ₂₇₂ B ₂₇₁ B ₂₇₀	124
11100	B ₂₈₅ B ₂₈₄ B ₂₈₃ B ₂₈₂ B ₂₈₁ B ₂₈₀	125
11101	B ₂₉₅ B ₂₉₄ B ₂₉₃ B ₂₉₂ B ₂₉₁ B ₂₉₀	126
11110	B ₃₀₅ B ₃₀₄ B ₃₀₃ B ₃₀₂ B ₃₀₁ B ₃₀₀	127
11111	B ₃₁₅ B ₃₁₄ B ₃₁₃ B ₃₁₂ B ₃₁₁ B ₃₁₀	128

7.5. Display Data RAM (DDRAM)

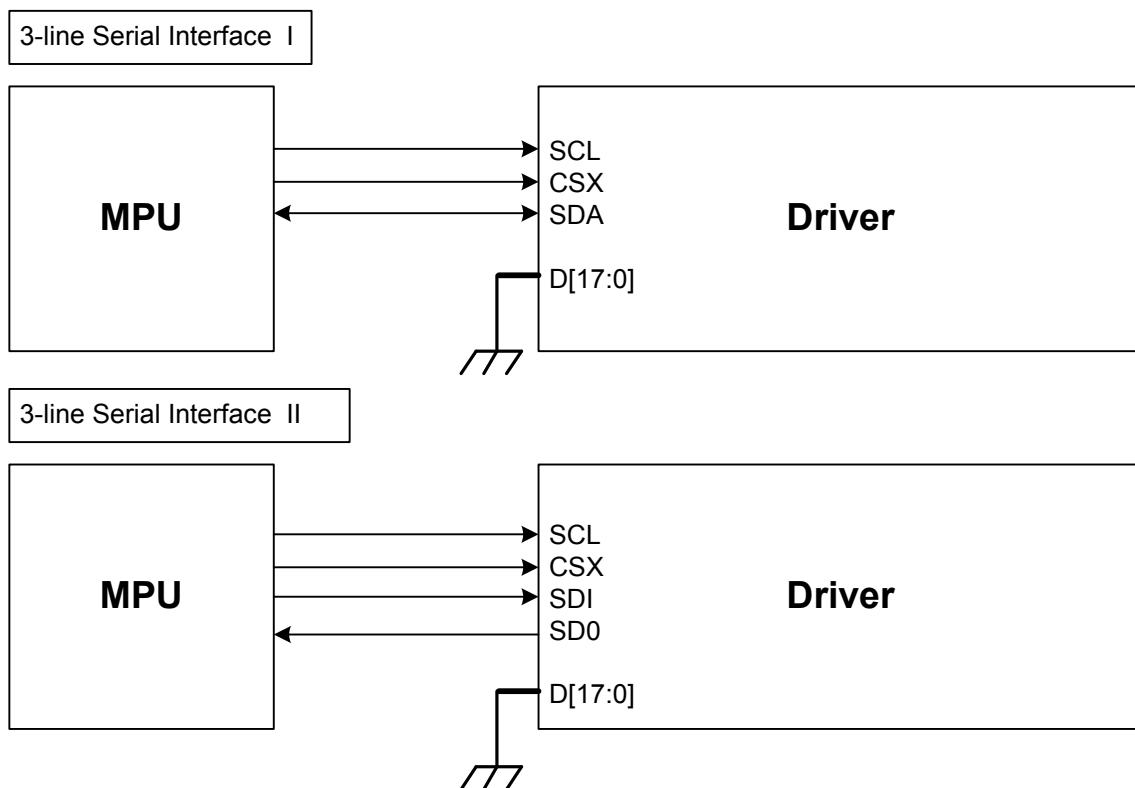
ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-I /8080-II series, 3-/4-line serial interface and 6-/16-/18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

7.6.1. 3-line Serial Interface

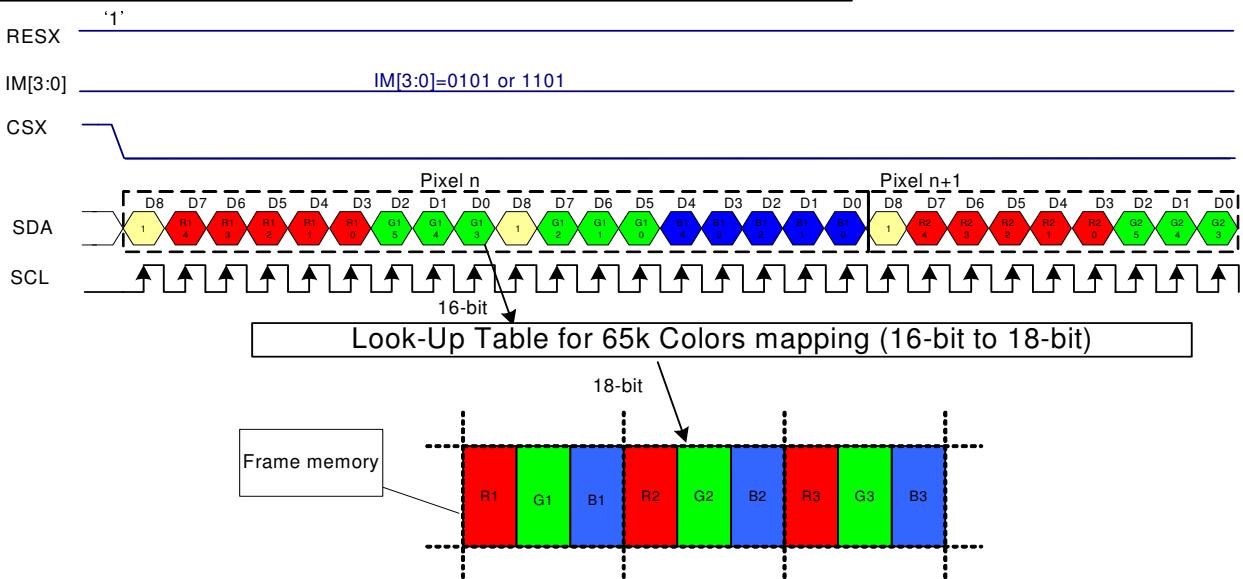
The 3-line/9-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-line SPI interface.



In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

- 65k colors, RGB 5, 6, 5 -bits input
- 262k colors, RGB 6, 6, 6 -bits input.

16 bit/pixel color order (R:5-bit, G:6-bit, B:5-bit), 65,536 colors



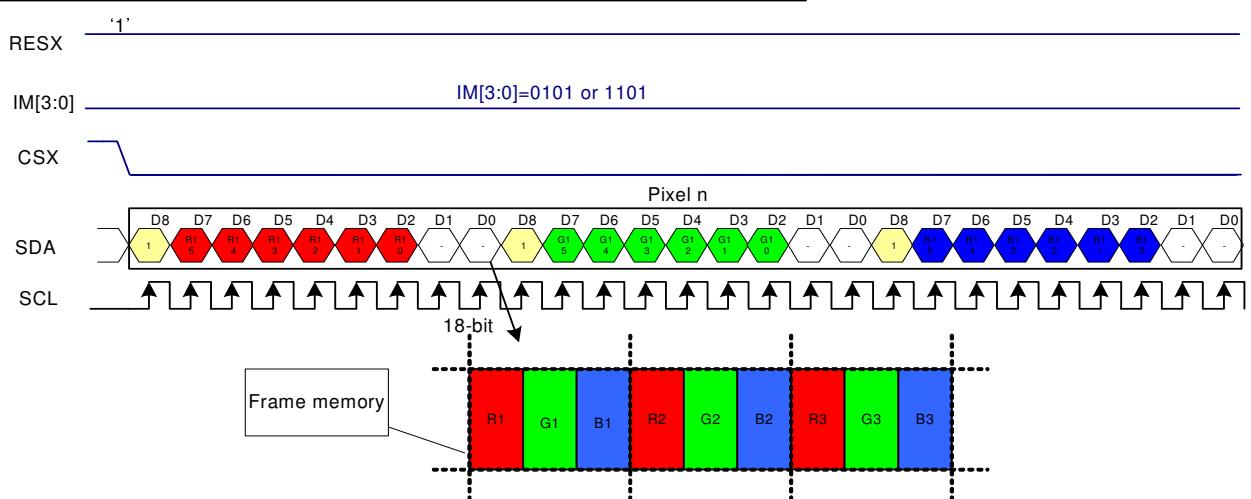
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-' = Don't care - Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



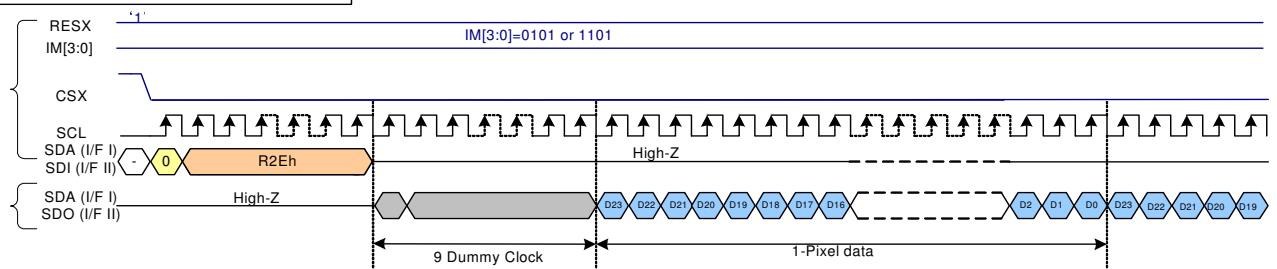
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are : Rx0, Gx0 and Bx0.

Note 4: '-' = Don't care - Can be set "0" or "1".

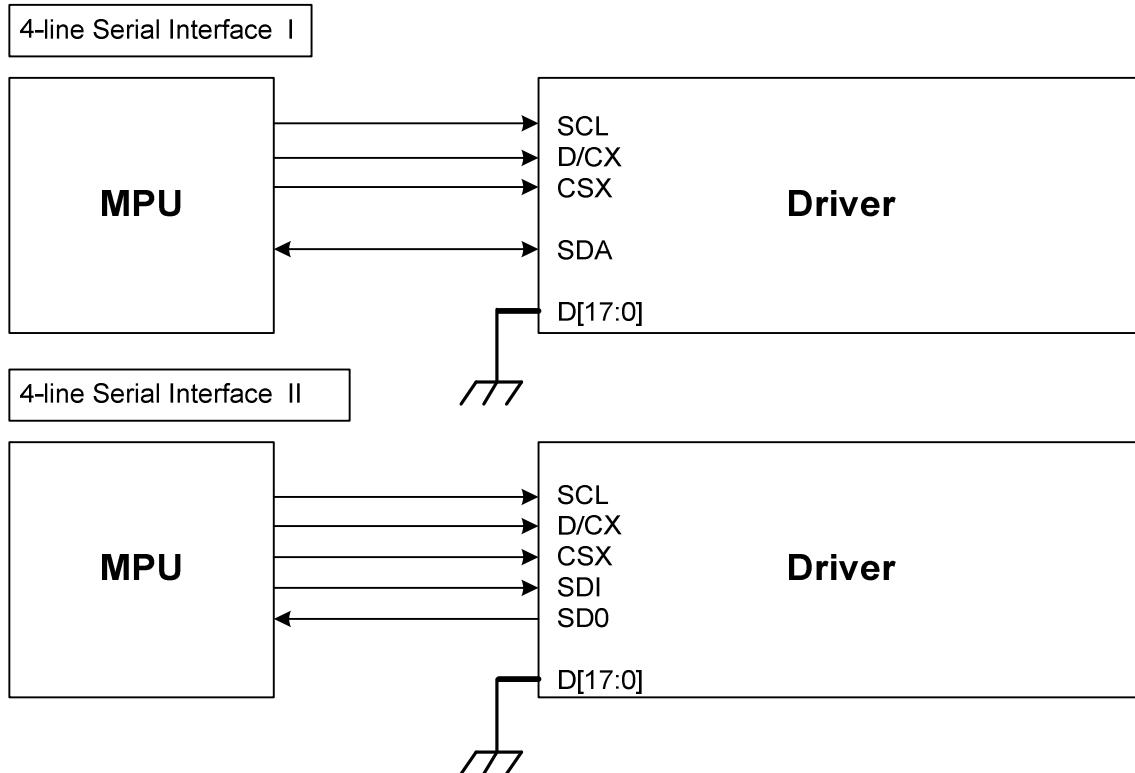
Read data through 3-line SPI mode



Note 1: '-'= Don't care –Can be set "0" or "1".

7.6.2. 4-line Serial Interface

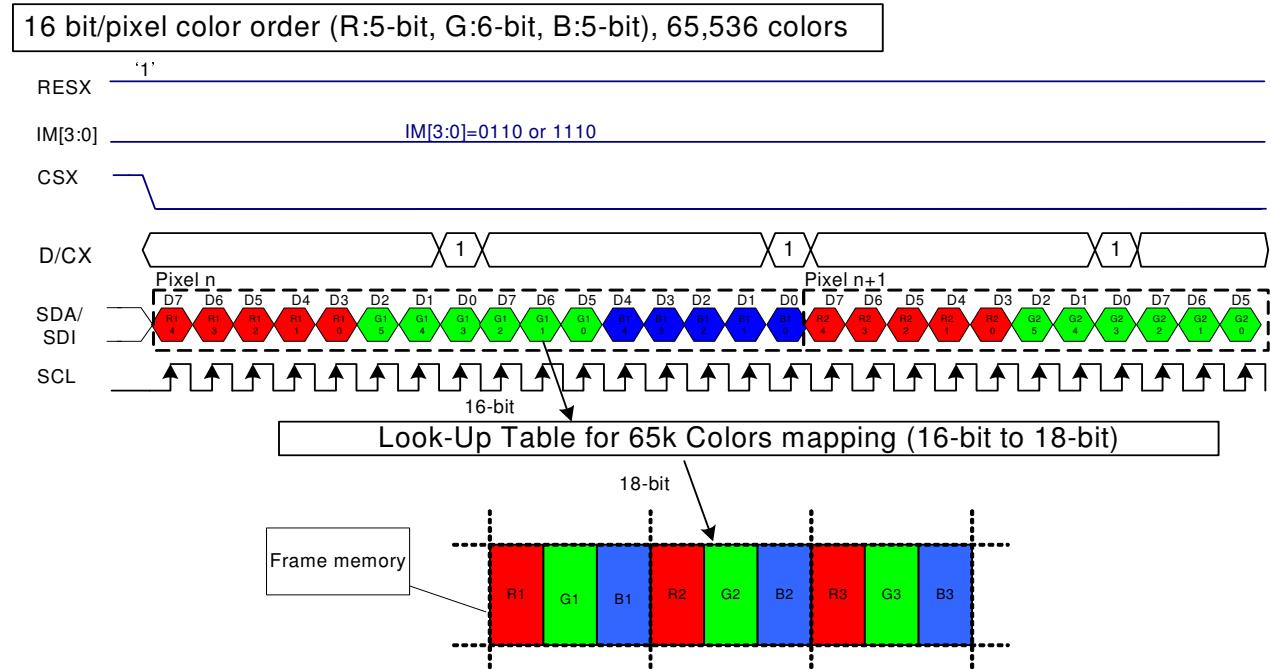
The 4-line/8-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0110" for serial interface I or IM [3:0] to "1110" for serial interface II. The shown figure is the example of 4-line SPI interface.



In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



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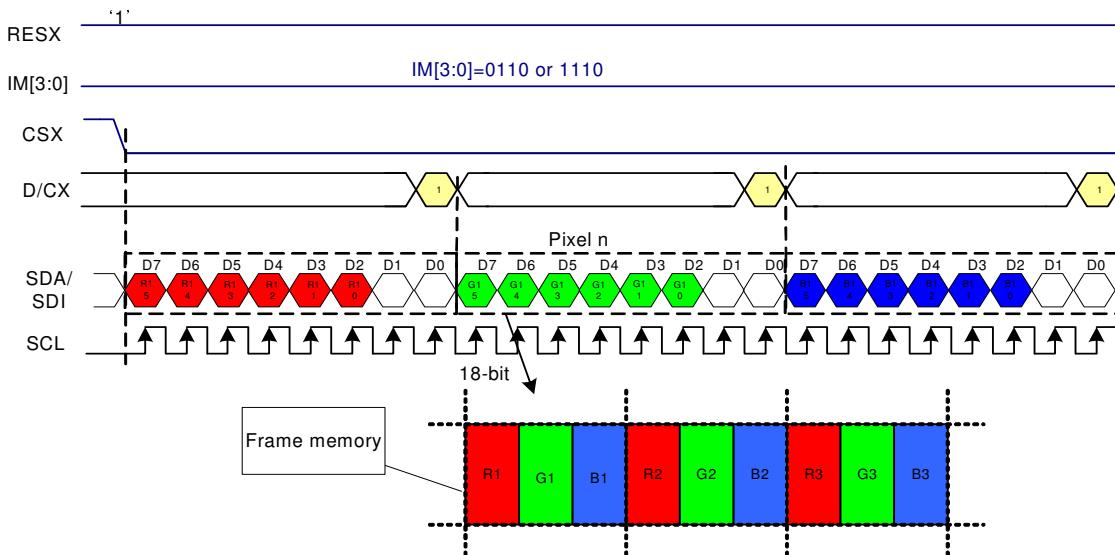
Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-' = Don't care –Can be set "0" or "1".

18 bit/pixel color order (R:6-bit, G:6-bit, B:6-bit), 262,144 colors



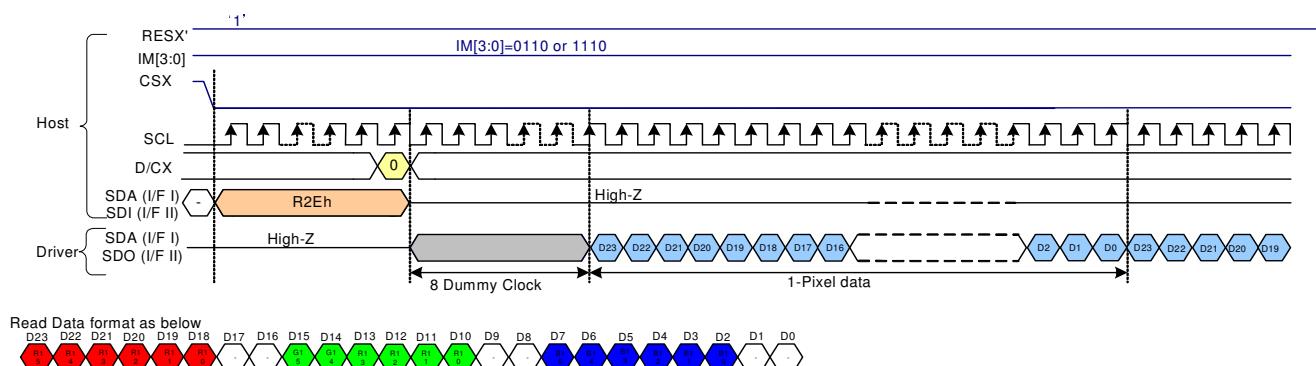
Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-' = Don't care –Can be set "0" or "1".

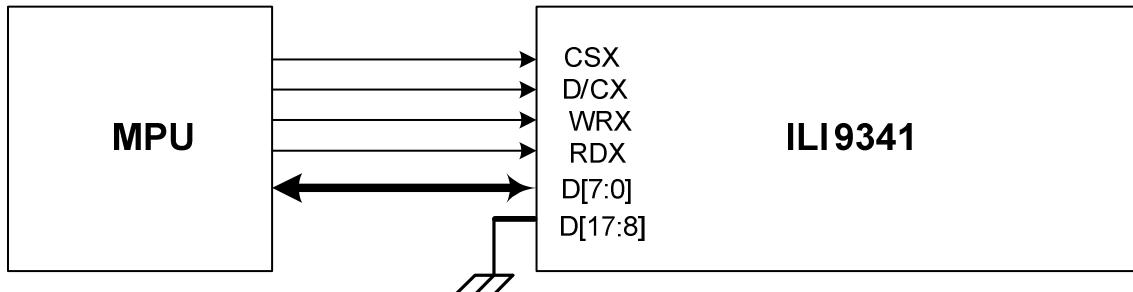
Read data through 4-line SPI mode



Note 1: '-' = Don't care – Can be set "0" or "1".

7.6.3. 8-bit Parallel MCU Interface

The 8080- I system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0000".The following shown figure is the example of interface with 8080- I MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

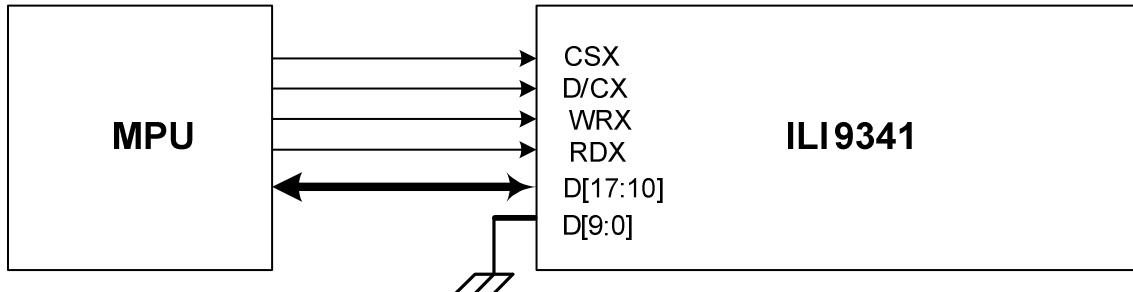
Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D7	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D7	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D1	C1				...			
D0	C0				...			

The 8080-II system 8-bit parallel bus interface of ILI9341 can be used by settings as IM [3:0] = "1001". The following shown figure is the example of interface with 8080-II MCU system interface.



Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D17	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D16	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D15	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D14	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D13	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D12	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D11	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D10	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

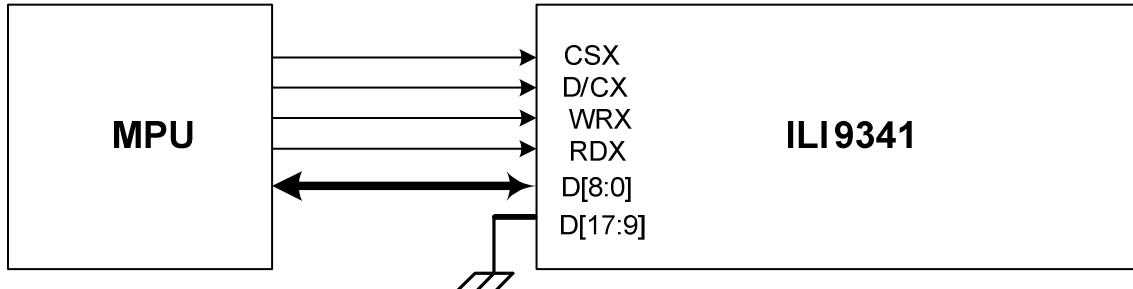
262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D17	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D16	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D15	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D14	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D13	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D12	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D11	C1				...			
D10	C0				...			

7.6.4. 9-bit Parallel MCU Interface

The 8080- I system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "0010". The following shown figure is the example of interface with 8080- I MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D8										
D7	C7	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D6	C6	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D5	C5	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D4	C4	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D3	C3	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D2	C2	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D1	C1	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D0	C0	0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

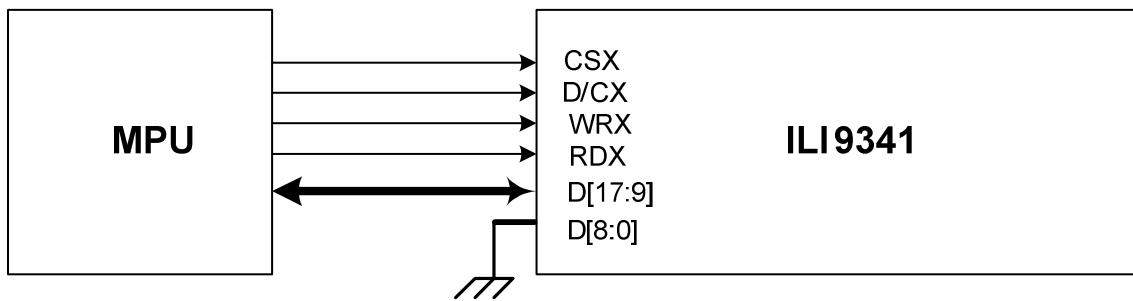
MDT[1:0] = "00"

Count	0	1	2	3	4	...	478	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D8										
D7	C7	0R5	0G2	1R5	1G2	...	238R5	238G2	239R5	239G2
D6	C6	0R4	0G1	1R4	1G1	...	238R4	238G1	239R4	239G1
D5	C5	0R3	0G0	1R3	1G0	...	238R3	238G0	239R3	239G0
D4	C4	0R2	0B5	1R2	1B5	...	238R2	238B5	239R2	239B5
D3	C3	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D2	C2	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D1	C1	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D0	C0	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1

MDT[1:0] = "01"

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D8								
D7	C7	0R5	0G5	0B5	...	239R5	239G5	239B5
D6	C6	0R4	0G4	0B4	...	239R4	239G4	239B4
D5	C5	0R3	0G3	0B3	...	239R3	239G3	239B3
D4	C4	0R2	0G2	0B2	...	239R2	239G2	239B2
D3	C3	0R1	0G1	0B1	...	239R1	239G1	239B1
D2	C2	0R0	0G0	0B0	...	239R0	239G0	239B0
D1	C1				...			
D0	C0				...			

The 8080-II system 9-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM [3:0] to "1011". The following shown figure is the example of interface with 8080-II MCU system interface.



65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	4	...	477	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D17	C7									
D16	C6	0R4	0G2	1R4	1G2	...	238R4	238G2	239R4	239G2
D15	C5	0R3	0G1	1R3	1G1	...	238R3	238G1	239R3	239G1
D14	C4	0R2	0G0	1R2	1G0	...	238R2	238G0	239R2	239G0
D13	C3	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

There are 2 pixels (6 sub-pixels) display data is sent by 4 transfers, when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0] = "00"

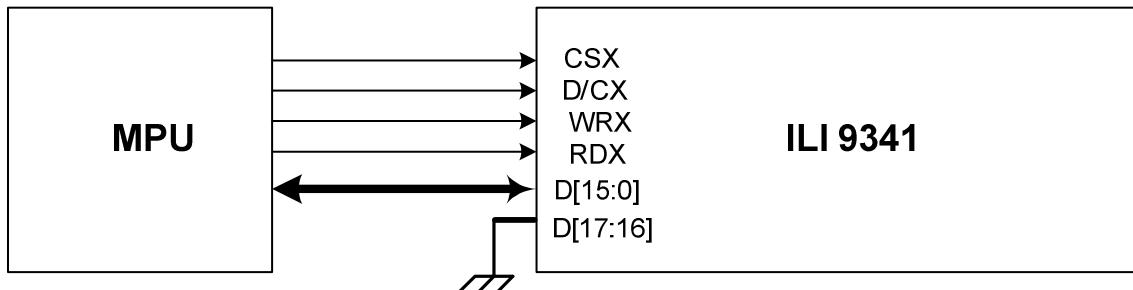
Count	0	1	2	3	4	...	478	478	479	480
D/CX	0	1	1	1	1	...	1	1	1	1
D17	C7	0R5	0G2	1R5	1G2	...	238R5	238G2	239R5	239G2
D16	C6	0R4	0G1	1R4	1G1	...	238R4	238G1	239R4	239G1
D15	C5	0R3	0G0	1R3	1G0	...	238R3	238G0	239R3	239G0
D14	C4	0R2	0B5	1R2	1B5	...	238R2	238B5	239R2	239B5
D13	C3	0R1	0B4	1R1	1B4	...	238R1	238B4	239R1	239B4
D12	C2	0R0	0B3	1R0	1B3	...	238R0	238B3	239R0	239B3
D11	C1	0G5	0B2	1G5	1B2	...	238G5	238B2	239G5	239B2
D10	C0	0G4	0B1	1G4	1B1	...	238G4	238B1	239G4	239B1
D9		0G3	0B0	1G3	1B0	...	238G3	238B0	239G3	239B0

MDT[1:0] = "01"

Count	0	1	2	3	...	718	719	720
D/CX	0	1	1	1	...	1	1	1
D17	C7							
D16	C6	0R5	0G5	0B5	...	239R5	239G5	239B5
D15	C5	0R4	0G4	0B4	...	239R4	239G4	239B4
D14	C4	0R3	0G3	0B3	...	239R3	239G3	239B3
D13	C3	0R2	0G2	0B2	...	239R2	239G2	239B2
D12	C2	0R1	0G1	0B1	...	239R1	239G1	239B1
D11	C1	0R0	0G0	0B0	...	239R0	239G0	239B0
D10	C0				...			
D9					...			

7.6.5. 16-bit Parallel MCU Interface

The 8080-I system 16-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM[3:0] to "0001". The following shown figure is the example of interface with 8080-I MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D15		0R4	1R4	2R4	...	237R4	238R4	239R4
D14		0R3	1R3	2R3	...	237R3	238R3	239R3
D13		0R2	1R2	2R2	...	237R2	238R2	239R2
D12		0R1	1R1	2R1	...	237R1	238R1	239R1
D11		0R0	1R0	2R0	...	237R0	238R0	239R0
D10		0G5	1G5	2G5	...	237G5	238G5	239G5
D9		0G4	1G4	2G4	...	237G4	238G4	239G4
D8		0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0] = "00"

Count	0	1	2	3	...	358	359	360
D/CX	0	1	1	1	...	1	1	1
D15		0R5	0B5	1G5	...	238R5	238B5	239G5
D14		0R4	0B4	1G4	...	238R4	238B4	239G4
D13		0R3	0B3	1G3	...	238R3	238B3	239G3
D12		0R2	0B2	1G2	...	238R2	238B2	239G2
D11		0R1	0B1	1G1	...	238R1	238B1	239G1
D10		0R0	0B0	1G0	...	238R0	238B0	239G0
D9					...			
D8					...			
D7	C7	0G5	1R5	1B5	...	238G5	239R5	239B5
D6	C6	0G4	1R4	1B4	...	238G4	239R4	239B4
D5	C5	0G3	1R3	1B3	...	238G3	239R3	239B3
D4	C4	0G2	1R2	1B2	...	238G2	239R2	239B2
D3	C3	0G1	1R1	1B1	...	238G1	239R1	239B1
D2	C2	0G0	1R0	1B0	...	238G0	239R0	239B0
D1	C1				...			
D0	C0				...			

MDT[1:0] = "01"

Count	0	1	2	3	...	357	358	479	480
D/CX	0	1	1	1	...		1	1	1
D15		0R5	0B5	1R5	1B5	...	238R5	238B5	239R5
D14		0R4	0B4	1R4	1B4	...	238R4	238B4	239R4
D13		0R3	0B3	1R3	1B3	...	238R3	238B3	239R3
D12		0R2	0B2	1R2	1B2	...	238R2	238B2	239R2
D11		0R1	0B1	1R1	1B1	...	238R1	238B1	239R1
D10		0R0	0B0	1R0	1B0	...	238R0	238B0	239R0
D9					...				
D8					...				
D7	C7	0G5		1G5		...	238G5		239G5
D6	C6	0G4		1G4		...	238G4		239G4
D5	C5	0G3		1G3		...	238G3		239G3
D4	C4	0G2		1G2		...	238G2		239G2
D3	C3	0G1		1G1		...	238G1		239G1
D2	C2	0G0		1G0		...	238G0		239G0
D1	C1				...				
D0	C0				...				

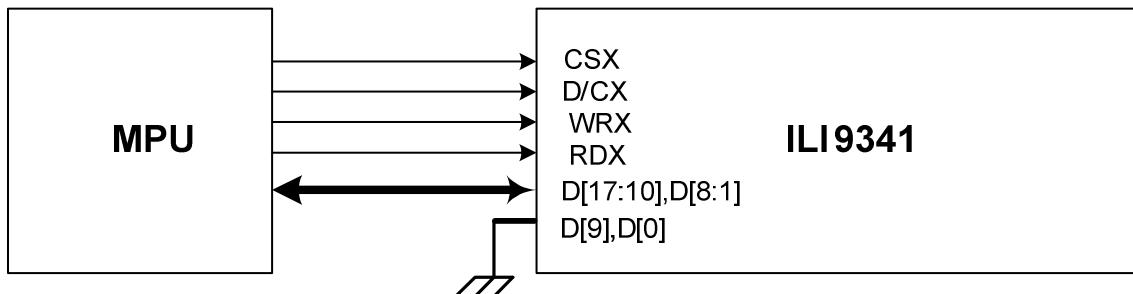
MDT[1:0] = "10"

Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D15		0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D14		0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0
D13		0R3		1R3		...	238R3		239R3	
D12		0R2		1R2		...	238R2		239R2	
D11		0R1		1R1		...	238R1		239R1	
D10		0R0		1R0		...	238R0		239R0	
D9		0G5		1G5		...	238G5		239G5	
D8		0G4		1G4		...	238G4		239G4	
D7	C7	0G3		1G3		...	238G3		239G3	
D6	C6	0G2		1G2		...	238G2		239G2	
D5	C5	0G1		1G1		...	238G1		239G1	
D4	C4	0G0		1G0		...	238G0		239G0	
D3	C3	0B5		1B5		...	238B5		239B5	
D2	C2	0B4		1B4		...	238B4		239B4	
D1	C1	0B3		1B3		...	238B3		239B3	
D0	C0	0B2		1B2		...	238B2		239B2	

MDT[1:0] = "11"

Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D15			0R3		1R3	...		238R3		239R3
D14			0R2		1R2	...		238R2		239R2
D13			0R1		1R1	...		238R1		239R1
D12			0R0		1R0	...		238R0		239R0
D11			0G5		1G5	...		238G5		239G5
D10			0G4		1G4	...		238G4		239G4
D9			0G3		1G3	...		238G3		239G3
D8			0G2		1G2	...		238G2		239G2
D7	C7		0G1		1G1	...		238G1		239G1
D6	C6		0G0		1G0	...		238G0		239G0
D5	C5		0B5		1B5	...		238B5		239B5
D4	C4		0B4		1B4	...		238B4		239B4
D3	C3		0B3		1B3	...		238B3		239B3
D2	C2		0B2		1B2	...		238B2		239B2
D1	C1	0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D0	C0	0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0

The 8080-II system 16-bit parallel bus interface of ILI9341 can be selected by settings IM [3:0] = "1000". The following shown figure is the example of interface with 8080-II MCU system interface.



Different display data format is available for two colors depth supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17		0R4	1R4	2R4	...	237R4	238R4	239R4
D16		0R3	1R3	2R3	...	237R3	238R3	239R3
D15		0R2	1R2	2R2	...	237R2	238R2	239R2
D14		0R1	1R1	2R1	...	237R1	238R1	239R1
D13		0R0	1R0	2R0	...	237R0	238R0	239R0
D12		0G5	1G5	2G5	...	237G5	238G5	239G5
D11		0G4	1G4	2G4	...	237G4	238G4	239G4
D10		0G3	1G3	2G3	...	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D5	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D4	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D3	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D2	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D1	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 2 transfers when DBI [2:0] bits of 3Ah register are set to "110".

MDT[1:0] = "00"

Count	0	1	2	3	...	358	359	360
D/CX	0	1	1	1	...	1	1	1
D17		0R5	0B5	1G5	...	238R5	238B5	239G5
D16		0R4	0B4	1G4	...	238R4	238B4	239G4
D15		0R3	0B3	1G3	...	238R3	238B3	239G3
D14		0R2	0B2	1G2	...	238R2	238B2	239G2
D13		0R1	0B1	1G1	...	238R1	238B1	239G1
D12		0R0	0B0	1G0	...	238R0	238B0	239G0
D11					...			
D10					...			
D8	C7	0G5	1R5	1B5	...	238G5	239R5	239B5
D7	C6	0G4	1R4	1B4	...	238G4	239R4	239B4
D6	C5	0G3	1R3	1B3	...	238G3	239R3	239B3
D5	C4	0G2	1R2	1B2	...	238G2	239R2	239B2
D4	C3	0G1	1R1	1B1	...	238G1	239R1	239B1
D3	C2	0G0	1R0	1B0	...	238G0	239R0	239B0
D2	C1				...			
D1	C0				...			

MDT[1:0] = "01"

Count	0	1	2	3	...	357	358	479	480
D/CX	0	1	1	1	...		1	1	1
D17		0R5	0B5	1R5	1B5	...	238R5	238B5	239R5
D16		0R4	0B4	1R4	1B4	...	238R4	238B4	239R4
D15		0R3	0B3	1R3	1B3	...	238R3	238B3	239R3
D14		0R2	0B2	1R2	1B2	...	238R2	238B2	239R2
D13		0R1	0B1	1R1	1B1	...	238R1	238B1	239R1
D12		0R0	0B0	1R0	1B0	...	238R0	238B0	239R0
D11					...				
D10					...				
D8	C7	0G5		1G5		...	238G5		239G5
D7	C6	0G4		1G4		...	238G4		239G4
D6	C5	0G3		1G3		...	238G3		239G3
D5	C4	0G2		1G2		...	238G2		239G2
D4	C3	0G1		1G1		...	238G1		239G1
D3	C2	0G0		1G0		...	238G0		239G0
D2	C1				...				
D1	C0				...				

MDT[1:0] = "10"

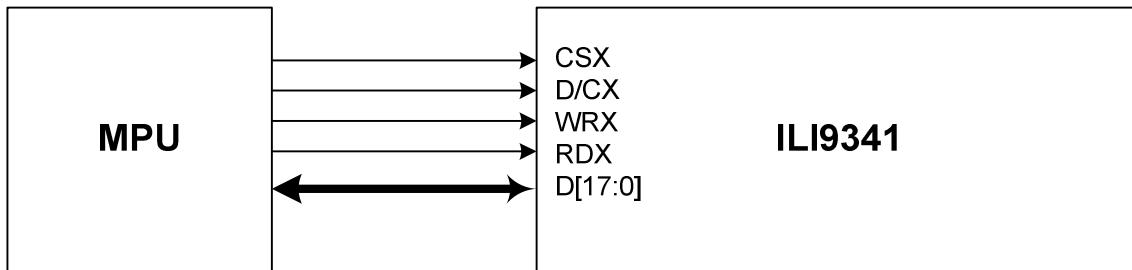
Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D17		0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D16		0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0
D15		0R3		1R3		...	238R3		239R3	
D14		0R2		1R2		...	238R2		239R2	
D13		0R1		1R1		...	238R1		239R1	
D12		0R0		1R0		...	238R0		239R0	
D11		0G5		1G5		...	238G5		239G5	
D10		0G4		1G4		...	238G4		239G4	
D8	C7	0G3		1G3		...	238G3		239G3	
D7	C6	0G2		1G2		...	238G2		239G2	
D6	C5	0G1		1G1		...	238G1		239G1	
D5	C4	0G0		1G0		...	238G0		239G0	
D4	C3	0B5		1B5		...	238B5		239B5	
D3	C2	0B4		1B4		...	238B4		239B4	
D2	C1	0B3		1B3		...	238B3		239B3	
D1	C0	0B2		1B2		...	238B2		239B2	

MDT[1:0] = "11"

Count	0	1	2	3		...	357	358	479	480
D/CX	0	1	1	1		...		1	1	1
D17			0R3		1R3	...	238R3		239R3	
D16			0R2		1R2	...	238R2		239R2	
D15			0R1		1R1	...	238R1		239R1	
D14			0R0		1R0	...	238R0		239R0	
D13			0G5		1G5	...	238G5		239G5	
D12			0G4		1G4	...	238G4		239G4	
D11			0G3		1G3	...	238G3		239G3	
D10			0G2		1G2	...	238G2		239G2	
D8	C7		0G1		1G1	...	238G1		239G1	
D7	C6		0G0		1G0	...	238G0		239G0	
D6	C5		0B5		1B5	...	238B5		239B5	
D5	C4		0B4		1B4	...	238B4		239B4	
D4	C3		0B3		1B3	...	238B3		239B3	
D3	C2		0B2		1B2	...	238B2		239B2	
D2	C1	0R5	0B1	1R5	1B1	...	238R5	238B1	239R5	239B1
D1	C0	0R4	0B0	1R4	1B0	...	238R4	238B0	239R4	239B0

7.6.6. 18-bit Parallel MCU Interface

The 8080-I system 18-bit parallel bus interface of ILI9341 can be selected by setting hardware pin IM[3:0] to "0011". The following shown figure is the example of interface with 8080-I MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

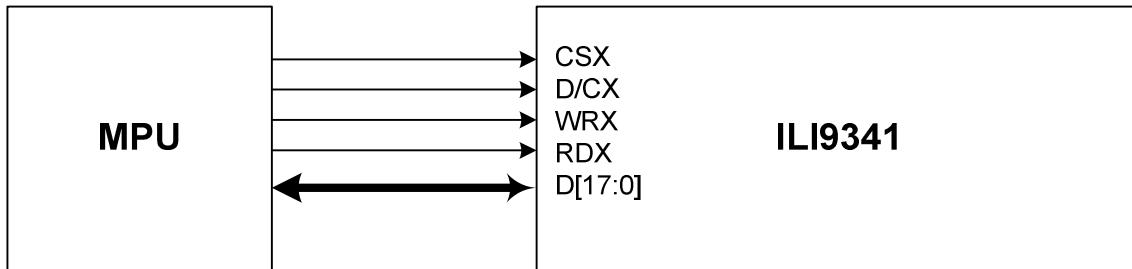
Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	...	237R4	238R4	239R4
D14		0R3	1R3	2R3	...	237R3	238R3	239R3
D13		0R2	1R2	2R2	...	237R2	238R2	239R2
D12		0R1	1R1	2R1	...	237R1	238R1	239R1
D11		0R0	1R0	2R0	...	237R0	238R0	239R0
D10		0G5	1G5	2G5	...	237G5	238G5	239G5
D9		0G4	1G4	2G4	...	237G4	238G4	239G4
D8		0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17		0R5	1R5	2R5	...	237R5	238R5	239R5
D16		0R4	1R4	2R4	...	237R4	238R4	239R4
D15		0R3	1R3	2R3	...	237R3	238R3	239R3
D14		0R2	1R2	2R2	...	237R2	238R2	239R2
D13		0R1	1R1	2R1	...	237R1	238R1	239R1
D12		0R0	1R0	2R0	...	237R0	238R0	239R0
D11		0G5	1G5	2G5	...	237G5	238G5	239G5
D10		0G4	1G4	2G4	...	237G4	238G4	239G4
D9		0G3	1G3	2G3	...	237G3	238G3	239G3
D8		0G2	1G2	2G2	...	237G2	238G2	239G2
D7	C7	0G1	1G1	2G1	...	237G1	238G1	239G1
D6	C6	0G0	1G0	2G0	...	237G0	238G0	239G0
D5	C5	0B5	1B5	2B5	...	237B5	238B5	239B5
D4	C4	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C3	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C2	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C1	0B1	1B1	2B1	...	237B1	238B1	239B1
D0	C0	0B0	1B0	2B0	...	237B0	238B0	239B0

The 8080-II system 18-bit parallel bus interface mode can be selected by settings IM [3:0] = "1010". The following shown figure is the example of interface with 8080-II MCU system interface.



Different display data format is available for one color depth only supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "101".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17								
D16								
D15		0R4	1R4	2R4	...	237R4	238R4	239R4
D14		0R3	1R3	2R3	...	237R3	238R3	239R3
D13		0R2	1R2	2R2	...	237R2	238R2	239R2
D12		0R1	1R1	2R1	...	237R1	238R1	239R1
D11		0R0	1R0	2R0	...	237R0	238R0	239R0
D10		0G5	1G5	2G5	...	237G5	238G5	239G5
D9		0G4	1G4	2G4	...	237G4	238G4	239G4
D8	C7	0G3	1G3	2G3	...	237G3	238G3	239G3
D7	C6	0G2	1G2	2G2	...	237G2	238G2	239G2
D6	C5	0G1	1G1	2G1	...	237G1	238G1	239G1
D5	C4	0G0	1G0	2G0	...	237G0	238G0	239G0
D4	C3	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	...	237B1	238B1	239B1
D0		0B0	1B0	2B0	...	237B0	238B0	239B0

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

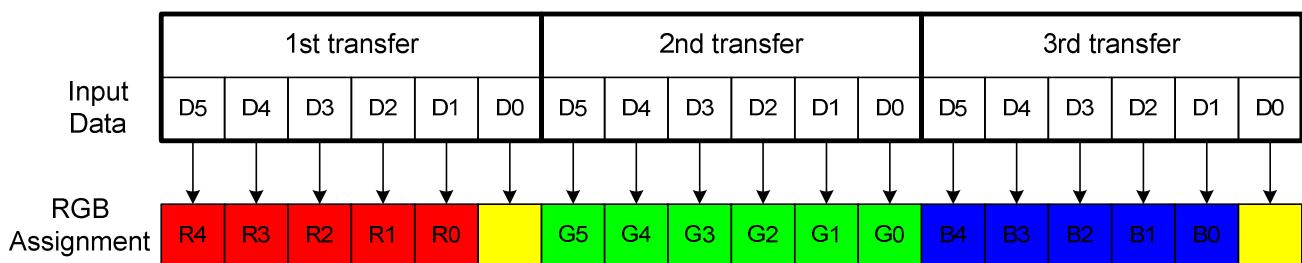
One pixel (3 sub-pixels) display data is sent by 1 transfer when DBI [2:0] bits of 3Ah register are set to "110".

Count	0	1	2	3	...	238	239	240
D/CX	0	1	1	1	...	1	1	1
D17		0R5	1R5	2R5	...	237R5	238R5	239R5
D16		0R4	1R4	2R4	...	237R4	238R4	239R4
D15		0R3	1R3	2R3	...	237R3	238R3	239R3
D14		0R2	1R2	2R2	...	237R2	238R2	239R2
D13		0R1	1R1	2R1	...	237R1	238R1	239R1
D12		0R0	1R0	2R0	...	237R0	238R0	239R0
D11		0G5	1G5	2G5	...	237G5	238G5	239G5
D10		0G4	1G4	2G4	...	237G4	238G4	239G4
D9		0G3	1G3	2G3	...	237G3	238G3	239G3
D8	C7	0G2	1G2	2G2	...	237G2	238G2	239G2
D7	C6	0G1	1G1	2G1	...	237G1	238G1	239G1
D6	C5	0G0	1G0	2G0	...	237G0	238G0	239G0
D5	C4	0B5	1B5	2B5	...	237B5	238B5	239B5
D4	C3	0B4	1B4	2B4	...	237B4	238B4	239B4
D3	C2	0B3	1B3	2B3	...	237B3	238B3	239B3
D2	C1	0B2	1B2	2B2	...	237B2	238B2	239B2
D1	C0	0B1	1B1	2B1	...	237B1	238B1	239B1
D0		0B0	1B0	2B0	...	237B0	238B0	239B0

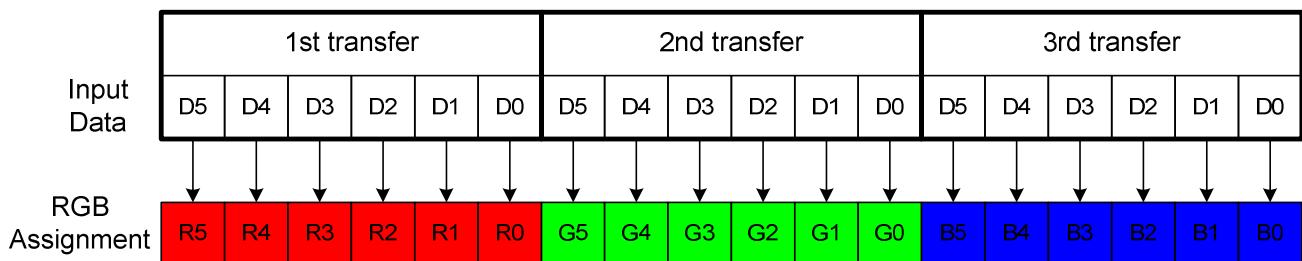
7.6.7. 6-bit Parallel RGB Interface

The 6-bit RGB interface is selected by setting the DPI [2:0] bit to "110". When RCM [1:0] are set to "10" and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 6-bit RGB data bus (D [5:0]) according to the data enable signal (DE) when RCM [1:0] are set to "10". The RGB interface SYNC mode is selected by setting the RCM [1:0] to "11", the valid display data is inputted in pixel unit via D [5:0] according to the VFP/VBP and HFP/HBP settings. Unused pins must be connected to GND to ensure normally operation. Registers can be set by the SPI system interface.

65K color: 16-bit/pixel (RGB 5-6-5 bits input)



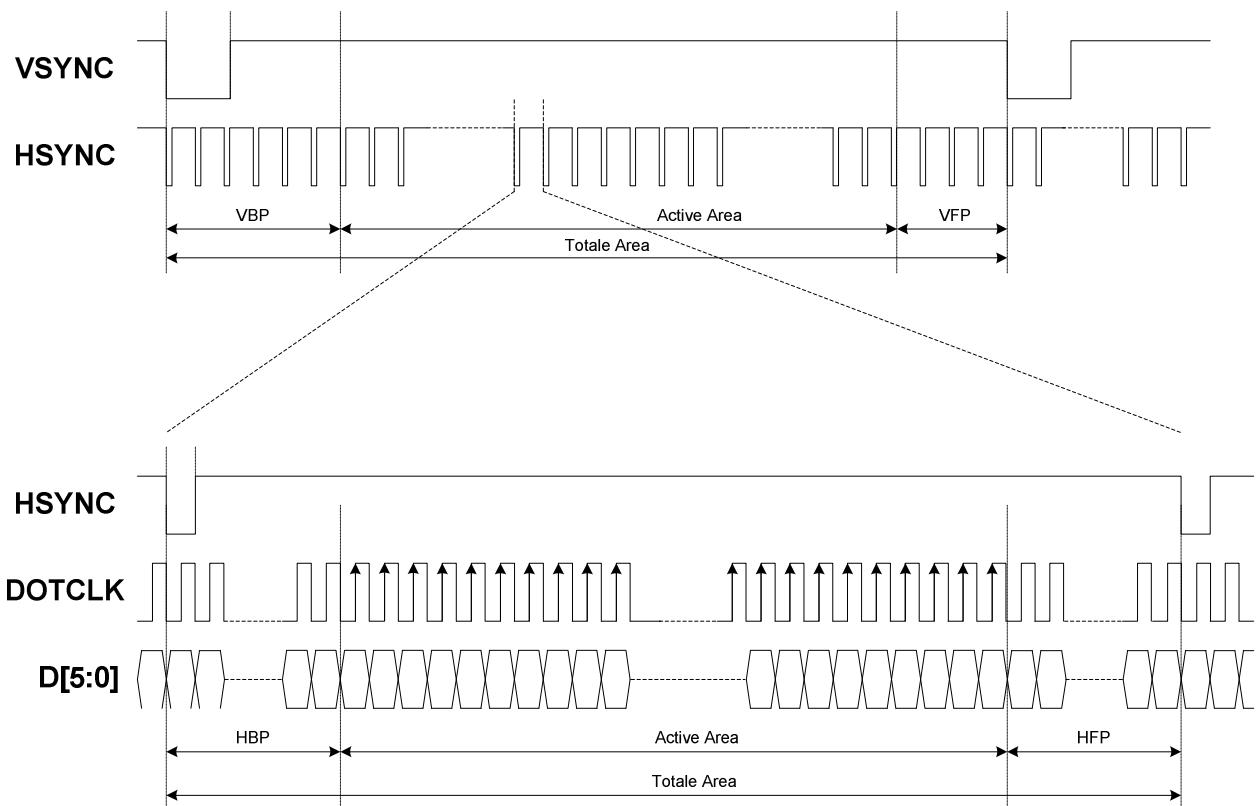
262K color: 18-bit/pixel (RGB 6-6-6 bits input)



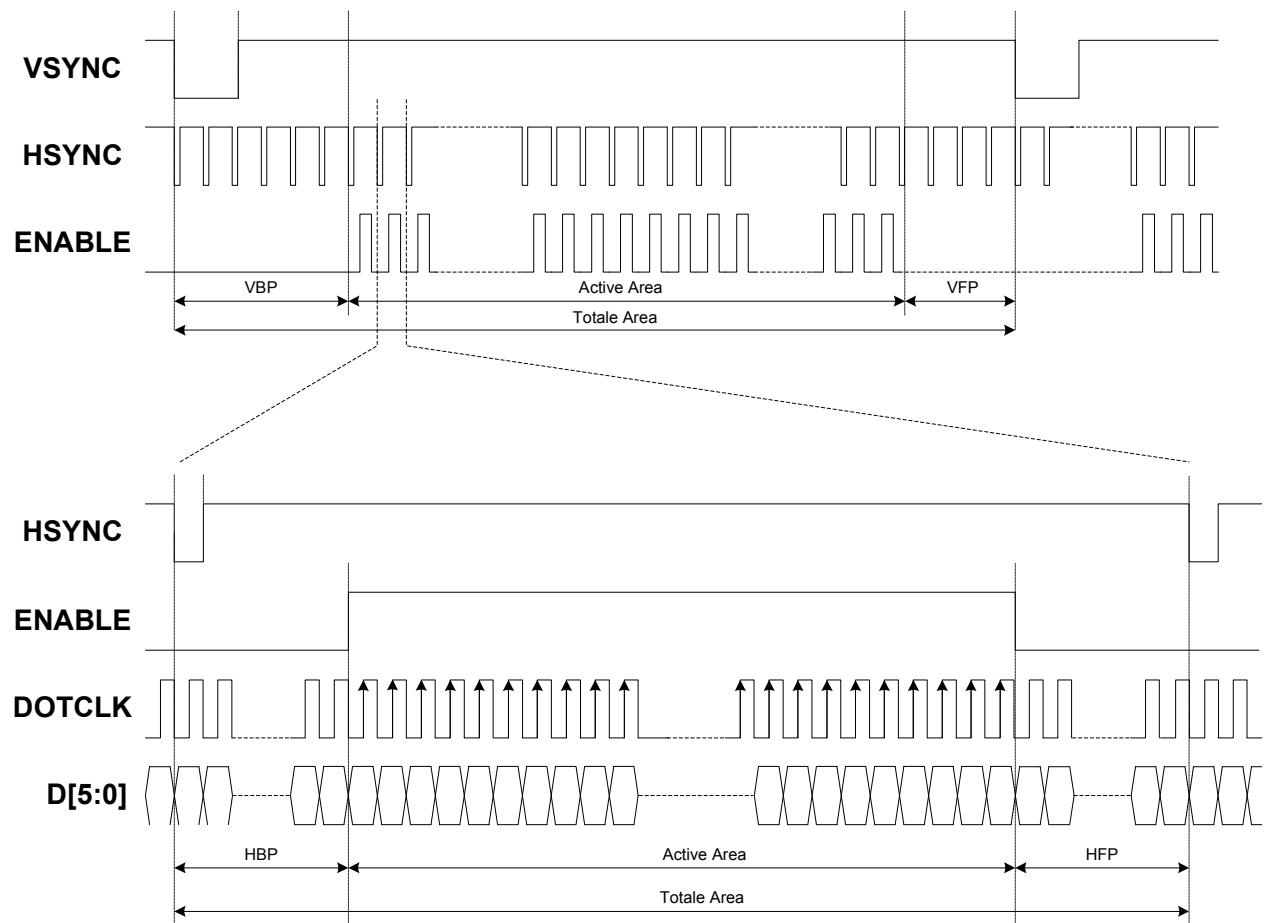
ILI9341 has data transfer counters to count the first, second, third data transfer in 6-bit RGB interface mode. The transfer counter is always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counter is reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

SYNC Mode, RCM[1:0] = "11"

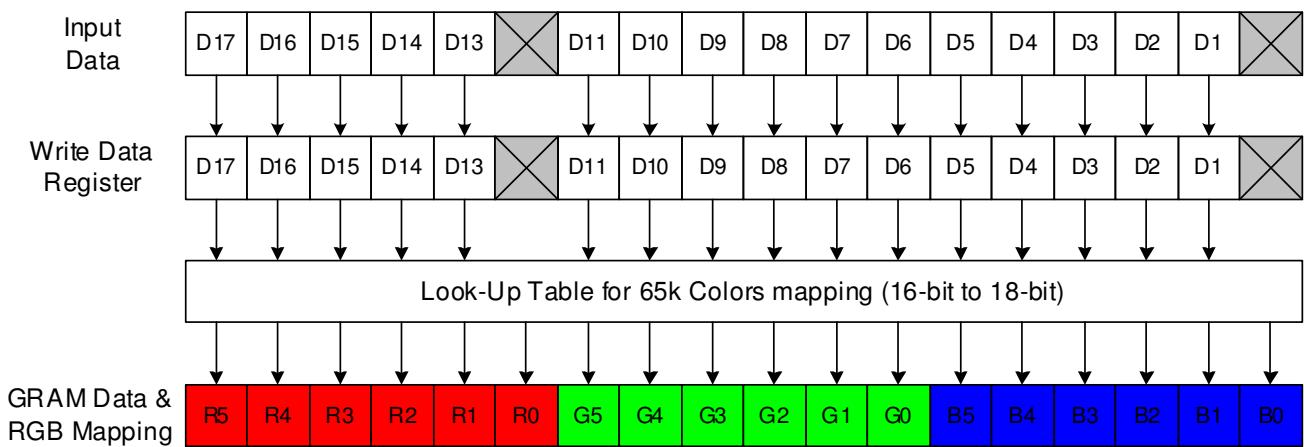


DE Mode, RCM[1:0] = "10"



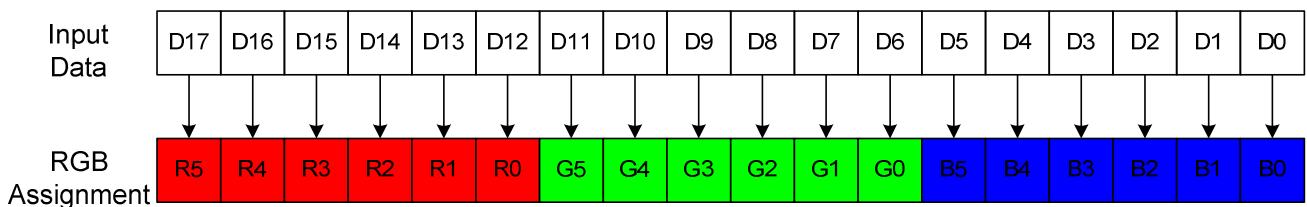
7.6.8. 16-bit Parallel RGB Interface

The 16-bit RGB interface is selected by setting the DPI [2:0] bits to “101”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data is transferred to the internal GRAM in synchronization with the display operation via 16-bit RGB data bus (D [17:13] & D [11:1]) according to the data enable signal (DE). The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:13] and D [11:1] according to the VFP/VBP and HFP/HBP settings. The unused D12 and D0 pins must be connected to GND for ensure normally operation. Registers can be set by the SPI system interface.



7.6.9. 18-bit Parallel RGB Interface

The 18-bit RGB interface is selected by setting the DPI [2:0] bits to “110”. When RCM [1:0] are set to “10” and DE mode is selected, the display operation is synchronized with VSYNC, HSYNC and DOTCLK signals. The display data are transferred to the internal GRAM in synchronization with the display operation via 18-bit RGB data bus (D [17:0]) according to the data enable signal (DE) when RCM [1:0] are set to “10”. The RGB interface SYNC mode is selected by setting the RCM [1:0] to “11”, the valid display data is inputted in pixel unit via D [17:0] according to the VFP/VBP and HFP/HBP settings. Registers can be set by the SPI system interface.



8. Command

8.1. Command List

Regulative Command Set														
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
No Operation	0	1	↑	XX	0	0	0	0	0	0	0	0	00h	
Software Reset	0	1	↑	XX	0	0	0	0	0	0	0	1	01h	
Read Display Identification Information	0	1	↑	XX	0	0	0	0	0	1	0	0	04h	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	ID1 [7:0]								XX	
	1	↑	1	XX	ID2 [7:0]								XX	
	1	↑	1	XX	ID3 [7:0]								XX	
Read Display Status	0	1	↑	XX	0	0	0	0	1	0	0	1	09h	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	D [31:25]								X 00	
	1	↑	1	XX	X	D [22:20]				D [19:16]				61
	1	↑	1	XX	X	X	X	X	X	D [10:8]			00	
	1	↑	1	XX	D [7:5]			X	X	X	X	X	00	
Read Display Power Mode	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	D [7:2]								0 08	
Read Display MADCTL	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	D [7:2]								0 00	
Read Display Pixel Format	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
Read Display Image Format	1	↑	1	XX	RIM	DPI [2:0]				X	DBI [2:0]			06
	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
Read Display Signal Mode	1	↑	1	XX	X	X	X	X	X	D [2:0]				00
	0	1	↑	XX	0	0	0	0	1	1	1	0	0Eh	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
Read Display Self-Diagnostic Result	1	↑	1	XX	D [7:2]								0 00	
	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh	
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX	
Enter Sleep Mode	1	↑	1	XX	D [7:6]								00	
	0	1	↑	XX	0	0	0	0	1	0	0	0	10h	
	0	1	↑	XX	0	0	0	0	1	0	0	0	11h	
Sleep OUT	0	1	↑	XX	0	0	0	0	1	0	0	0	1	12h
	0	1	↑	XX	0	0	0	0	1	0	0	0	1	13h
Partial Mode ON	0	1	↑	XX	0	0	0	0	1	0	0	0	1	20h
	0	1	↑	XX	0	0	0	0	1	0	0	0	1	21h
Normal Display Mode ON	0	1	↑	XX	0	0	0	0	1	0	0	0	1	26h
	0	1	↑	XX	0	0	0	0	1	0	0	0	1	27h
Display Inversion OFF	0	1	↑	XX	0	0	0	0	1	0	0	0	0	28h
	0	1	↑	XX	0	0	0	0	1	0	0	0	0	29h
Display Inversion ON	0	1	↑	XX	0	0	0	0	1	0	0	0	0	2Ah
	0	1	↑	XX	0	0	0	0	1	0	0	1	0	2Bh
Gamma Set	1	1	↑	XX	GC [7:0]								01	
	0	1	↑	XX	0	0	1	0	1	0	0	0	0	28h
Display OFF	0	1	↑	XX	0	0	1	0	1	0	0	0	1	29h
	0	1	↑	XX	0	0	1	0	1	0	0	0	1	2Ah
Column Address Set	0	1	↑	XX	0	0	1	0	1	0	0	1	0	2Ah
	1	1	↑	XX	SC [15:8]								XX	
	1	1	↑	XX	SC [7:0]								XX	
	1	1	↑	XX	EC [15:8]								XX	
Page Address Set	1	1	↑	XX	EC [7:0]								XX	
	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh	
	1	1	↑	XX	SP [15:8]								XX	
	1	1	↑	XX	SP [7:0]								XX	
	1	1	↑	XX	EP [15:8]								XX	
	1	1	↑	XX	EP [7:0]								XX	

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Memory Write	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch			
	1	1	↑		D [17:0]											
Color SET	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh			
	1	↑	1	XX				R00 [5:0]					XX			
	1	↑	1	XX				Rnn [5:0]					XX			
	1	↑	1	XX				R31 [5:0]					XX			
	1	↑	1	XX				G00 [5:0]					XX			
	1	↑	1	XX				Gnn [5:0]					XX			
	1	↑	1	XX				G64 [5:0]					XX			
	1	↑	1	XX				B00 [5:0]					XX			
	1	↑	1	XX				Bnn [5:0]					XX			
	1	↑	1	XX				B31 [5:0]					XX			
Memory Read	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh			
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX			
	1	↑	1		D [17:0]										XX	
Partial Area	0	1	↑	XX	0	0	1	1	0	0	0	0	30h			
	1	1	↑	XX		SR [15:8]										00
	1	1	↑	XX		SR [7:0]										00
	1	1	↑	XX		ER [15:8]										01
	1	1	↑	XX		ER [7:0]										3F
Vertical Scrolling Definition	0	1	↑	XX	0	0	1	1	0	0	1	1	33h			
	1	1	↑	XX	TFA [15:8]										00	
	1	1	↑	XX	TFA [7:0]										00	
	1	1	↑	XX	VSA [15:8]										01	
	1	1	↑	XX	VSA [7:0]										40	
	1	1	↑	XX	BFA [15:8]										00	
	1	1	↑	XX	BFA [7:0]										00	
Tearing Effect Line OFF	0	1	↑	XX	0	0	1	1	0	1	0	0	34h			
Tearing Effect Line ON	0	1	↑	XX	0	0	1	1	0	1	0	1	35h			
	1	1	↑	XX	X	X	X	X	X	X	X	M	00			
Memory Access Control	0	1	↑	XX	0	0	1	1	0	1	1	0	36h			
	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	X	X	00			
Vertical Scrolling Start Address	0	1	↑	XX	0	0	1	1	0	1	1	1	37h			
	1	1	↑	XX	VSP [15:8]										00	
	1	1	↑	XX	VSP [7:0]										00	
Idle Mode OFF	0	1	↑	XX	0	0	1	1	1	0	0	0	38h			
Idle Mode ON	0	1	↑	XX	0	0	1	1	1	0	0	1	39h			
Pixel Format Set	0	1	↑	XX	0	0	1	1	1	0	1	0	3Ah			
	1	1	↑	XX	X	DPI [2:0]				X	DBI [2:0]			66		
Write Memory Continue	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch			
	1	1	↑		D [17:0]										XX	
Read Memory Continue	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh			
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX			
	1	↑	1		D [17:0]										XX	
Set Tear Scanline	0	1	↑	XX	0	1	0	0	0	1	0	0	44h			
	1	1	↑	XX	X	X	X	X	X	X	X	STS [8]	00			
	1	1	↑	XX	STS [7:0]										00	
Get Scanline	0	1	↑	XX	0	1	0	0	0	1	0	1	45h			
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX			
	1	↑	1	XX	X	X	X	X	X	X	X	GTS [9:8]	00			
	1	↑	1	XX	GTS [7:0]										00	
Write Display Brightness	0	1	↑	XX	0	1	0	1	0	0	0	1	51h			
	1	1	↑	XX	DBV [7:0]										00	

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Read Display Brightness	0	1	↑	XX	0	1	0	1	0	0	1	0	52h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	DBV [7:0]								
Write CTRL Display	0	1	↑	XX	0	1	0	1	0	0	1	1	53h
	1	1	↑	XX	X	X	BCTRL	X	DD	BL	X	X	00
Read CTRL Display	0	1	↑	XX	0	1	0	1	0	1	0	0	54h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X	X	BCTRL	X	DD	BL	X	X	00
Write Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	0	1	55h
	1	1	↑	XX	X	X	X	X	X	X	C [1:0]	00	
Read Content Adaptive Brightness Control	0	1	↑	XX	0	1	0	1	0	1	1	0	56h
	1	↑	1	XX	X	X	X	X	X	X	X	XX	
	1	↑	1	XX	X	X	X	X	X	X	C [1:0]	00	
Write CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
	1	1	↑	XX	CMB [7:0]								
Read CABC Minimum Brightness	0	1	↑	XX	0	1	0	1	0	1	1	1	5Fh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	CMB [7:0]								
Read ID1	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	Module's Manufacture [7:0]								
Read ID2	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver Version [7:0]								
Read ID3	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	LCD Module / Driver ID [7:0]								

Extended Command Set														
Command Function	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
RGB Interface Signal Control	0	1	↑	XX	1	0	1	1	0	0	0	0	B0h	
	1	1	↑	XX	ByPass_MODE	RCM [1:0]		X	VSPL	HSPL	DPL	EPL	40	
Frame Control (In Normal Mode)	0	1	↑	XX	1	0	1	1	0	0	0	1	B1h	
	1	1	↑	XX	X	X	X	X	X	X	DIVA [1:0]	00		
Frame Control (In Idle Mode)	1	1	↑	XX	X	X	X	RTNA [4:0]					1B	
	0	1	↑	XX	1	0	1	1	0	0	1	0	B2h	
	1	1	↑	XX	X	X	X	X	X	X	DIVB [1:0]	00		
Frame Control (In Partial Mode)	1	1	↑	XX	X	X	X	RTNB [4:0]					1B	
	0	1	↑	XX	1	0	1	1	0	0	1	1	B3h	
	1	1	↑	XX	X	X	X	X	X	X	DIVC [1:0]	00		
Display Inversion Control	1	1	↑	XX	X	X	X	RTNC [4:0]					1B	
	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h	
Blanking Porch Control	1	1	↑	XX	X	X	X	X	NLA	NLB	NLC	02		
	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h	
	1	1	↑	XX	0	VFP [6:0]								
	1	1	↑	XX	0	VBP [6:0]								
	1	1	↑	XX	0	0	0	HFP [4:0]					0A	
	1	1	↑	XX	0	0	0	HBP [4:0]					14	

	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h
	1	1	↑	XX	X	X	X	X	PTG [1:0]	PT [1:0]			0A
	1	1	↑	XX	REV	GS	SS	SM		ISC [3:0]			82
	1	1	↑	XX	X	X			NL [5:0]				27
	1	1	↑	XX	X	X			PCDIV [5:0]				XX
Display Function Control	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h
	1	1	↑	XX	X	X	X	X	0	GON	DTE	GAS	07
Entry Mode Set	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
Backlight Control 1	0	1	↑	XX	X	X	X	X		TH UI [3:0]			04
	1	1	↑	XX	X	X	X	X					XX
Backlight Control 2	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX		TH MV [3:0]			TH ST [3:0]				B8
Backlight Control 3	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX	X	X	X	X		DTH UI [3:0]			04
Backlight Control 4	0	1	↑	XX	1	0	1	1	1	0	1	1	BBh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX		DTH MV [3:0]			DTH ST [3:0]				C9
Backlight Control 5	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh
	1	1	↑	XX	X	X	X	X	X	X	X	X	XX
	1	1	↑	XX		DIM2 [3:0]			X		DIM1 [2:0]		44
Backlight Control 7	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh
	1	1	↑	XX			PWM DIV [7:0]						OF
Backlight Control 8	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh
	1	1	↑	XX	X	X	X	X	X	LEDONR	LEDONPOL	LEDPWMOPL	00
Power Control 1	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h
	1	1	↑	XX	X	X			VRH [5:0]				26
Power Control 2	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h
	1	1	↑	XX	X	X	X	X	X		BT [2:0]		00
VCOM Control 1	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h
	1	1	↑	XX	X		VMH [6:0]						31
VCOM Control 2	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
	1	1	↑	XX	nVM		VMF [6:0]						C0
NV Memory Write	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h
	1	1	↑	XX	X	X	X	X	X		PGM ADR [2:0]		00
	1	1	↑	XX			PGM DATA [7:0]						XX
NV Memory Protection Key	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h
	1	1	↑	XX			KEY [23:16]						55
	1	1	↑	XX			KEY [15:8]						AA
	1	1	↑	XX			KEY [7:0]						66
NV Memory Status Read	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	X		ID2_CNT [2:0]		X		ID1_CNT [2:0]		XX
	1	↑	1	XX	BUSY		VMF_CNT [2:0]		X		ID3_CNT [2:0]		XX

Read ID4	0	↑	1	XX	1	1	0	1	0	0	1	1	D3h
	1	↑	1	XX	X	X	X	X	X	X	X	X	XX
	1	↑	1	XX	0	0	0	0	0	0	0	0	00
	1	↑	1	XX	1	0	0	1	0	0	1	1	93
	1	↑	1	XX	0	1	0	0	0	0	0	1	41
Positive Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h
	1	1	↑	XX	X	X	X	X	VP0 [3:0]				08
	1	1	↑	XX	X	X			VP1 [5:0]				0E
	1	1	↑	XX	X	X			VP2 [5:0]				12
	1	1	↑	XX	X	X	X	X	VP4 [3:0]				05
	1	1	↑	XX	X	X	X	X	VP6 [4:0]				03
	1	1	↑	XX	X	X	X	X	VP13 [3:0]				09
	1	1	↑	XX	X				VP20 [6:0]				47
	1	1	↑	XX		VP36 [3:0]			VP27 [3:0]				86
	1	1	↑	XX	X				VP43 [6:0]				2B
	1	1	↑	XX	X	X	X	X	VP50 [3:0]				0B
	1	1	↑	XX	X	X	X	X	VP57 [4:0]				04
	1	1	↑	XX	X	X	X	X	VP59 [3:0]				00
	1	1	↑	XX	X	X			VP61 [5:0]				00
	1	1	↑	XX	X	X			VP62 [5:0]				00
	1	1	↑	XX	X	X	X	X	VP63 [3:0]				00
Negative Gamma Correction	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h
	1	1	↑	XX	X	X	X	X	VN0 [3:0]				08
	1	1	↑	XX	X	X			VN1 [5:0]				1A
	1	1	↑	XX	X	X			VN2 [5:0]				20
	1	1	↑	XX	X	X	X	X	VN4 [3:0]				07
	1	1	↑	XX	X	X	X	X	VN6 [4:0]				0E
	1	1	↑	XX	X	X	X	X	VN13 [3:0]				05
	1	1	↑	XX	X				VN20 [6:0]				3A
	1	1	↑	XX		VN36 [3:0]			VN27 [3:0]				8A
	1	1	↑	XX	X				VN43 [6:0]				40
	1	1	↑	XX	X	X	X	X	VN50 [3:0]				04
	1	1	↑	XX	X	X	X	X	VN57 [4:0]				18
	1	1	↑	XX	X	X	X	X	VN59 [3:0]				0F
	1	1	↑	XX	X	X			VN61 [5:0]				3F
	1	1	↑	XX	X	X			VN62 [5:0]				3F
	1	1	↑	XX	X	X	X	X	VN63 [3:0]				0F
Digital Gamma Control 1	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h
1 st Parameter	1	1	↑	XX		RCA0 [3:0]			BCA0 [3:0]				XX
:	1	1	↑	XX		RCAx [3:0]			BCAx [3:0]				XX
16 th Parameter	1	1	↑	XX		RCA15 [3:0]			BCA15 [3:0]				XX
Digital Gamma Control 2	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h
1 st Parameter	1	1	↑	XX		RFA0 [3:0]			BFA0 [3:0]				XX
:	1	1	↑	XX		RFAx [3:0]			BFAX [3:0]				XX
64 th Parameter	1	1	↑	XX		RFA63 [3:0]			BFA63 [3:0]				XX
Interface Control	0	1	↑	XX	1	1	1	1	0	1	1	1	F6h
	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	X	BGR_EOR	X	X	WEMODE	01
	1	1	↑	XX	X	X			X	X	MDT [1:0]		00
	1	1	↑	XX	X	X	ENDIAN	X	DM [1:0]	RM	RIM		00

Note 1: Undefined commands are treated as NOP (00h) command.

Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP

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(00h).

Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.

8.2. Description of Level 1 Command

8.2.1. NOP (00h)

NOP (No Operation)																										
00h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	0	0	0	0	0	0	0	00h													
Parameter	No Parameter.																									
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X = Don't care.																									
Restriction	None																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																									
Power On Sequence	N/A																									
SW Reset	N/A																									
HW Reset	N/A																									
Flow Chart	None																									

8.2.2. Software Reset (01h)

01h		SWRESET																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	0	0	0	1	01h												
Parameter	No Parameter.																								
Description	<p>When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)</p> <p>Note: The Frame Memory contents are unaffected by this command</p> <p>X = Don't care.</p>																								
Restriction	<p>It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
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Status	Default Value																								
Power On Sequence	N/A																								
SW Reset	N/A																								
HW Reset	N/A																								
Flow Chart	<pre> graph TD A[SWRESET(01h)] --> B([Display whole blank screen]) B --> C{Set Commands to S/W Default Values} C --> D([Sleep In Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.3. Read display identification information (04h)

04h		RDDIDIF (Read Display Identification Information)																								
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑		XX	0	0	0	0	0	1	0	0	04h												
1 st Parameter	1	↑	1		XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1		XX	ID1 [7:0]						XX														
3 rd Parameter	1	↑	1		XX	ID2 [7:0]						XX														
4 th Parameter	1	↑	1		XX	ID3 [7:0]						XX														
Description	<p>This read byte returns 24 bits display identification information.</p> <p>The 1st parameter is dummy data.</p> <p>The 2nd parameter (ID1 [7:0]): LCD module's manufacturer ID.</p> <p>The 3rd parameter (ID2 [7:0]): LCD module/driver version ID.</p> <p>The 4th parameter (ID3 [7:0]): LCD module/driver ID.</p>																									
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
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Status	Default Value																									
Power On Sequence	See description																									
SW Reset	See description																									
HW Reset	See description																									
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

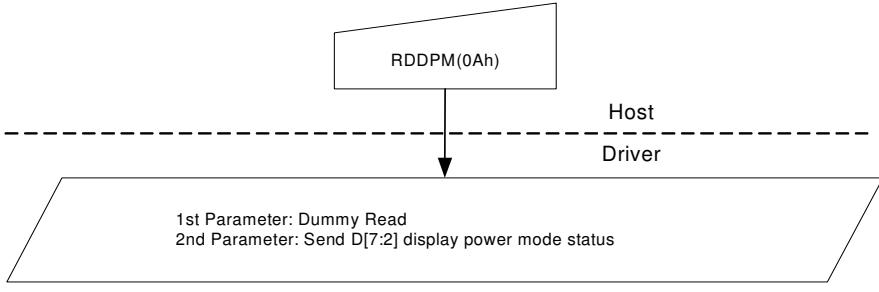
8.2.4. Read Display Status (09h)

09h		RDDST (Read Display Status)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	0	0	1	0	0	1	09h	
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X	
2 nd Parameter	1	↑	1	XX	D [31:25]						0	00		
3 rd Parameter	1	↑	1	XX	0	D [22:20]			D [19:16]				61	
4 th Parameter	1	↑	1	XX	0	0	0	0	0	0	D [10:8]			00
5 th Parameter	1	↑	1	XX	D [7:5]			0	0	0	0	0	00	
Description	This command indicates the current status of the display as described in the table below:													
	Bit	Description			Value	Status								
	D31	Booster voltage status			0	Booster OFF								
					1	Booster ON								
	D30	Row address order			0	Top to Bottom (When MADCTL B7='0')								
					1	Bottom to Top (When MADCTL B7='1')								
	D29	Column address order			0	Left to Right (When MADCTL B6='0').								
					1	Right to Left (When MADCTL B6='1').								
	D28	Row/column exchange			0	Normal Mode (When MADCTL B5='0').								
					1	Reverse Mode (When MADCTL B5='1').								
	D27	Vertical refresh			0	LCD Refresh Top to Bottom (When MADCTL B4='0')								
					1	LCD Refresh Bottom to Top (When MADCTL B4='1').								
	D26	RGB/BGR order			0	RGB (When MADCTL B3='0')								
					1	BGR (When MADCTL B3='1')								
	D25	Horizontal refresh order			0	LCD Refresh Left to Right (When MADCTL B2='0')								
					1	LCD Refresh Right to Left (When MADCTL B2='1')								
	D24	Not used			0	---								
	D23	Not used			0	---								
	D22	Interface color pixel format definition			101	16-bit/pixel								
	D21				110	18-bit/pixel								
	D20	Idle mode ON/OFF			0	Idle Mode OFF								
	D19				1	Idle Mode ON								
	D18	Partial mode ON/OFF			0	Partial Mode OFF								
					1	Partial Mode ON.								
	D17	Sleep IN/OUT			0	Sleep IN Mode								
					1	Sleep OUT Mode.								
	D16	Display normal mode ON/OFF			0	Display Normal Mode OFF.								
					1	Display Normal Mode ON.								
	D15	Vertical scrolling status			0	Scroll OFF								
	D14	Not used			0	---								
	D13	Inversion status			0	Not defined								
	D12	All pixel ON			0	Not defined								
	D11	All pixel OFF			0	Not defined								
	D10	Display ON/OFF			0	Display is OFF								
					1	Display is ON								
	D9	Tearing effect line ON/OFF			0	Tearing Effect Line OFF								
					1	Tearing Effect ON								
	D[8:6]	Gamma curve selection			000	GC0								
					001	---								
					010	---								
					011	---								
					other	Not defined								

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		D5	Tearing effect line mode	0	Mode 1, V-Blanking only												
				1	Mode 2, both H-Blanking and V-Blanking.												
		D4	Not used	0	---												
		D3	Not used	0	---												
		D2	Not used	0	---												
		D1	Not used	0	---												
		D0	Not used	0	---												
X = Don't care																	
Restriction																	
Register Availability					<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																
Normal Mode On, Idle Mode Off, Sleep Out	Yes																
Normal Mode On, Idle Mode On, Sleep Out	Yes																
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Sleep In	Yes																
Default					<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>32'h00610000h</td> </tr> <tr> <td>SW Reset</td> <td>32'h00610000h</td> </tr> <tr> <td>HW Reset</td> <td>32'h00610000h</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	32'h00610000h	SW Reset	32'h00610000h	HW Reset	32'h00610000h				
Status	Default Value																
Power On Sequence	32'h00610000h																
SW Reset	32'h00610000h																
HW Reset	32'h00610000h																
Flow Chart				<pre> graph TD RDDST[RDDST(09h)] --> Host[Host] Host -.-> Driver[Driver] subgraph Parameters [Parameters] direction TB P1[1st Parameter: Dummy Read] P2[2nd Parameter: Send D[31:25] display status] P3[3rd Parameter: Send D[19:16] display status] P4[4th Parameter: Send D[10:8] display status] P5[5th Parameter: Send D[7:5] display status] end Driver --> Parameters </pre>	Legend <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

8.2.5. Read Display Power Mode (0Ah)

0Ah		RDDPM (Read Display Power Mode)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	0	0	0	1	0	1	0	0Ah													
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X													
2 nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	08													
Description	This command indicates the current status of the display as described in the table below::																									
	Bit	Value	Description			Comment																				
	D7	0	Booster Off or has a fault.			---																				
		1	Booster On and working OK			---																				
	D6	0	Idle Mode Off.			---																				
		1	Idle Mode On.			---																				
	D5	0	Partial Mode Off.			---																				
		1	Partial Mode On.			---																				
	D4	0	Sleep In Mode			---																				
		1	Sleep Out Mode			---																				
	D3	0	Display Normal Mode Off.			---																				
		1	Display Normal Mode On			---																				
	D2	0	Display is Off.			---																				
		1	Display is On			---																				
	D1	--	Not Defined			Set to '0'																				
	D0	--	Not Defined			Set to '0'																				
X = Don't care																										
Restriction																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h08h</td></tr> <tr> <td>SW Reset</td><td>8'h08h</td></tr> <tr> <td>HW Reset</td><td>8'h08h</td></tr> </tbody> </table>														Status	Default Value	Power On Sequence	8'h08h	SW Reset	8'h08h	HW Reset	8'h08h				
Status	Default Value																									
Power On Sequence	8'h08h																									
SW Reset	8'h08h																									
HW Reset	8'h08h																									
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

8.2.6. Read Display MADCTL (0Bh)

RDDMADCTL (Read Display MADCTL)																																																																									
0Bh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																												
Command	0	1	↑	XX	0	0	0	0	1	0	1	1	0Bh																																																												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X																																																												
2 nd Parameter	1	↑	1	XX	D7	D6	D5	D4	D3	D2	D1	D0	00																																																												
Description	This command indicates the current status of the display as described in the table below:																																																																								
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Value</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>0</td> <td>Top to Bottom (When MADCTL B7='0').</td> <td>---</td> </tr> <tr> <td></td> <td>1</td> <td>Bottom to Top (When MADCTL B7='1').</td> <td>---</td> </tr> <tr> <td>D6</td> <td>0</td> <td>Left to Right (When MADCTL B6='0')</td> <td>---</td> </tr> <tr> <td></td> <td>1</td> <td>Right to Left (When MADCTL B6='1')</td> <td>---</td> </tr> <tr> <td>D5</td> <td>0</td> <td>Normal Mode (When MADCTL B5='0').</td> <td>---</td> </tr> <tr> <td></td> <td>1</td> <td>Reverse Mode (When MADCTL B5='1')</td> <td>---</td> </tr> <tr> <td>D4</td> <td>0</td> <td>LCD Refresh Top to Bottom (When MADCTL B4='0')</td> <td>---</td> </tr> <tr> <td></td> <td>1</td> <td>LCD Refresh Bottom to Top (When MADCTL B4='1')</td> <td>---</td> </tr> <tr> <td>D3</td> <td>0</td> <td>RGB (When MADCTL B3='0')</td> <td>---</td> </tr> <tr> <td></td> <td>1</td> <td>BGR (When MADCTL B3='1').</td> <td>---</td> </tr> <tr> <td>D2</td> <td>0</td> <td>LCD Refresh Left to Right (When MADCTL B2='0').</td> <td>---</td> </tr> <tr> <td></td> <td>1</td> <td>LCD Refresh Right to Left (When MADCTL B2='1').</td> <td>---</td> </tr> <tr> <td>D1</td> <td>--</td> <td>Switching between Segment outputs and RAM</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>--</td> <td>Switching between Segment outputs and RAM</td> <td>Set to '0'</td> </tr> </tbody> </table>													Bit	Value	Description	Comment	D7	0	Top to Bottom (When MADCTL B7='0').	---		1	Bottom to Top (When MADCTL B7='1').	---	D6	0	Left to Right (When MADCTL B6='0')	---		1	Right to Left (When MADCTL B6='1')	---	D5	0	Normal Mode (When MADCTL B5='0').	---		1	Reverse Mode (When MADCTL B5='1')	---	D4	0	LCD Refresh Top to Bottom (When MADCTL B4='0')	---		1	LCD Refresh Bottom to Top (When MADCTL B4='1')	---	D3	0	RGB (When MADCTL B3='0')	---		1	BGR (When MADCTL B3='1').	---	D2	0	LCD Refresh Left to Right (When MADCTL B2='0').	---		1	LCD Refresh Right to Left (When MADCTL B2='1').	---	D1	--	Switching between Segment outputs and RAM	Set to '0'	D0	--	Switching between Segment outputs and RAM	Set to '0'
Bit	Value	Description	Comment																																																																						
D7	0	Top to Bottom (When MADCTL B7='0').	---																																																																						
	1	Bottom to Top (When MADCTL B7='1').	---																																																																						
D6	0	Left to Right (When MADCTL B6='0')	---																																																																						
	1	Right to Left (When MADCTL B6='1')	---																																																																						
D5	0	Normal Mode (When MADCTL B5='0').	---																																																																						
	1	Reverse Mode (When MADCTL B5='1')	---																																																																						
D4	0	LCD Refresh Top to Bottom (When MADCTL B4='0')	---																																																																						
	1	LCD Refresh Bottom to Top (When MADCTL B4='1')	---																																																																						
D3	0	RGB (When MADCTL B3='0')	---																																																																						
	1	BGR (When MADCTL B3='1').	---																																																																						
D2	0	LCD Refresh Left to Right (When MADCTL B2='0').	---																																																																						
	1	LCD Refresh Right to Left (When MADCTL B2='1').	---																																																																						
D1	--	Switching between Segment outputs and RAM	Set to '0'																																																																						
D0	--	Switching between Segment outputs and RAM	Set to '0'																																																																						
	X = Don't care																																																																								
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HW Reset	8'h00h																																																																								
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																																								

8.2.7. Read Display Pixel Format (0Ch)

RDDCOLMOD (Read Display Pixel Format)																																														
0Ch	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																	
Command	0	1	↑	XX	0	0	0	0	1	1	0	0	0Ch																																	
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X																																	
2 nd Parameter	1	↑	1	XX	RIM	DPI [2:0]			0	DBI [2:0]			06																																	
Description	<p>This command indicates the current status of the display as described in the table below:</p> <table border="1"> <thead> <tr> <th>RIM</th> <th>DPI [2:0]</th> <th>RGB Interface Format</th> </tr> </thead> <tbody> <tr><td>0</td><td>0 0 0 0</td><td>Reserved</td></tr> <tr><td>0</td><td>0 0 0 1</td><td>Reserved</td></tr> <tr><td>0</td><td>0 0 1 0</td><td>Reserved</td></tr> <tr><td>0</td><td>0 0 1 1</td><td>Reserved</td></tr> <tr><td>0</td><td>1 0 0 0</td><td>Reserved</td></tr> <tr><td>0</td><td>1 0 0 1</td><td>16 bits / pixel</td></tr> <tr><td>0</td><td>1 1 0 0</td><td>18 bits / pixel</td></tr> <tr><td>0</td><td>1 1 1 0</td><td>Reserved</td></tr> <tr><td>1</td><td>1 0 0 1</td><td>16 bits / pixel (6-bit 3 times data transfer)</td></tr> <tr><td>1</td><td>1 1 0 0</td><td>18 bits / pixel (6-bit 3 times data transfer)</td></tr> </tbody> </table> <p>X = Don't care</p>													RIM	DPI [2:0]	RGB Interface Format	0	0 0 0 0	Reserved	0	0 0 0 1	Reserved	0	0 0 1 0	Reserved	0	0 0 1 1	Reserved	0	1 0 0 0	Reserved	0	1 0 0 1	16 bits / pixel	0	1 1 0 0	18 bits / pixel	0	1 1 1 0	Reserved	1	1 0 0 1	16 bits / pixel (6-bit 3 times data transfer)	1	1 1 0 0	18 bits / pixel (6-bit 3 times data transfer)
RIM	DPI [2:0]	RGB Interface Format																																												
0	0 0 0 0	Reserved																																												
0	0 0 0 1	Reserved																																												
0	0 0 1 0	Reserved																																												
0	0 0 1 1	Reserved																																												
0	1 0 0 0	Reserved																																												
0	1 0 0 1	16 bits / pixel																																												
0	1 1 0 0	18 bits / pixel																																												
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1	1 0 0 1	16 bits / pixel (6-bit 3 times data transfer)																																												
1	1 1 0 0	18 bits / pixel (6-bit 3 times data transfer)																																												
Restriction																																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																					
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Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>RIM</th> <th>DPI [2:0]</th> <th>DBI [2:0]</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>1'b0</td><td>3'b000</td><td>3'b110</td></tr> <tr><td>SW Reset</td><td>No Chang</td><td>No Chang</td><td>No Chang</td></tr> <tr><td>HW Reset</td><td>1'b0</td><td>3'b000</td><td>3'b110</td></tr> </tbody> </table>													Status	Default Value			RIM	DPI [2:0]	DBI [2:0]	Power On Sequence	1'b0	3'b000	3'b110	SW Reset	No Chang	No Chang	No Chang	HW Reset	1'b0	3'b000	3'b110														
Status	Default Value																																													
	RIM	DPI [2:0]	DBI [2:0]																																											
Power On Sequence	1'b0	3'b000	3'b110																																											
SW Reset	No Chang	No Chang	No Chang																																											
HW Reset	1'b0	3'b000	3'b110																																											
Flow Chart	<p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																													

8.2.8. Read Display Image Format (0Dh)

RDDIM (Read Display Image Mode)																									
0Dh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	0	1	1	0	1	0Dh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	0	0	0	0	0	0	D [2:0]		00												
Description	This command indicates the current status of the display as described in the table below:																								
	<table border="1"> <tr> <th>D [2:0]</th> <th>Description</th> </tr> <tr> <td>000</td> <td>Gamma curve 1 (G2.2)</td> </tr> <tr> <td>001</td> <td>---</td> </tr> <tr> <td>010</td> <td>---</td> </tr> <tr> <td>011</td> <td>---</td> </tr> <tr> <td>Other</td> <td>Not defined</td> </tr> </table>													D [2:0]	Description	000	Gamma curve 1 (G2.2)	001	---	010	---	011	---	Other	Not defined
D [2:0]	Description																								
000	Gamma curve 1 (G2.2)																								
001	---																								
010	---																								
011	---																								
Other	Not defined																								
	X = Don't care																								
Restriction																									
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Status	Default Value																								
Power On Sequence	3'b000																								
SW Reset	3'b000																								
HW Reset	3'b000																								
Flow Chart	<pre> graph TD RDDIM[RDDIM(0Dh)] --> Host[Host] Host --> Driver[Driver] RDDIM -.-> 1st[1st Parameter: Dummy Read] RDDIM -.-> 2nd[2nd Parameter: Send D[7:0] display image mode status] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.9. Read Display Signal Mode (0Eh)

0Eh	RDDSM (Read Display Signal Mode)																																																									
	D/CX	RDX	WRX	D17-8		D7	D6	D5	D4	D3	D2	D1	D0	HEX																																												
Command	0	1	↑	XX		0	0	0	0	1	1	1	0	0Eh																																												
1 st Parameter	1	↑	1	XX		X	X	X	X	X	X	X	X	X																																												
2 nd Parameter	1	↑	1	XX		D7	D6	D5	D4	D3	D2	D1	D0	00																																												
Description	This command indicates the current status of the display as described in the table below:																																																									
	<table border="1"> <thead> <tr> <th>Bit</th> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>0</td> <td>Tearing effect line OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Tearing effect line ON</td> </tr> <tr> <td>D6</td> <td>0</td> <td>Tearing effect line mode 1</td> </tr> <tr> <td></td> <td>1</td> <td>Tearing effect line mode 2</td> </tr> <tr> <td>D5</td> <td>0</td> <td>Horizontal sync. (RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Horizontal sync. (RGB interface) ON</td> </tr> <tr> <td>D4</td> <td>0</td> <td>Vertical sync. (RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Vertical sync. (RGB interface) ON</td> </tr> <tr> <td>D3</td> <td>0</td> <td>Pixel clock (DOTCLK, RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Pixel clock (DOTCLK, RGB interface) ON</td> </tr> <tr> <td>D2</td> <td>0</td> <td>Data enable (DE, RGB interface) OFF</td> </tr> <tr> <td></td> <td>1</td> <td>Data enable (DE, RGB interface) ON</td> </tr> <tr> <td>D1</td> <td>0</td> <td>Reserved</td> </tr> <tr> <td>D0</td> <td>0</td> <td>Reserved</td> </tr> </tbody> </table>													Bit	Value	Description	D7	0	Tearing effect line OFF		1	Tearing effect line ON	D6	0	Tearing effect line mode 1		1	Tearing effect line mode 2	D5	0	Horizontal sync. (RGB interface) OFF		1	Horizontal sync. (RGB interface) ON	D4	0	Vertical sync. (RGB interface) OFF		1	Vertical sync. (RGB interface) ON	D3	0	Pixel clock (DOTCLK, RGB interface) OFF		1	Pixel clock (DOTCLK, RGB interface) ON	D2	0	Data enable (DE, RGB interface) OFF		1	Data enable (DE, RGB interface) ON	D1	0	Reserved	D0	0	Reserved
Bit	Value	Description																																																								
D7	0	Tearing effect line OFF																																																								
	1	Tearing effect line ON																																																								
D6	0	Tearing effect line mode 1																																																								
	1	Tearing effect line mode 2																																																								
D5	0	Horizontal sync. (RGB interface) OFF																																																								
	1	Horizontal sync. (RGB interface) ON																																																								
D4	0	Vertical sync. (RGB interface) OFF																																																								
	1	Vertical sync. (RGB interface) ON																																																								
D3	0	Pixel clock (DOTCLK, RGB interface) OFF																																																								
	1	Pixel clock (DOTCLK, RGB interface) ON																																																								
D2	0	Data enable (DE, RGB interface) OFF																																																								
	1	Data enable (DE, RGB interface) ON																																																								
D1	0	Reserved																																																								
D0	0	Reserved																																																								
	X = Don't care																																																									
Restriction																																																										
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SW Reset	8'h00h																																																									
HW Reset	8'h00h																																																									
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																									

8.2.10. Read Display Self-Diagnostic Result (0Fh)

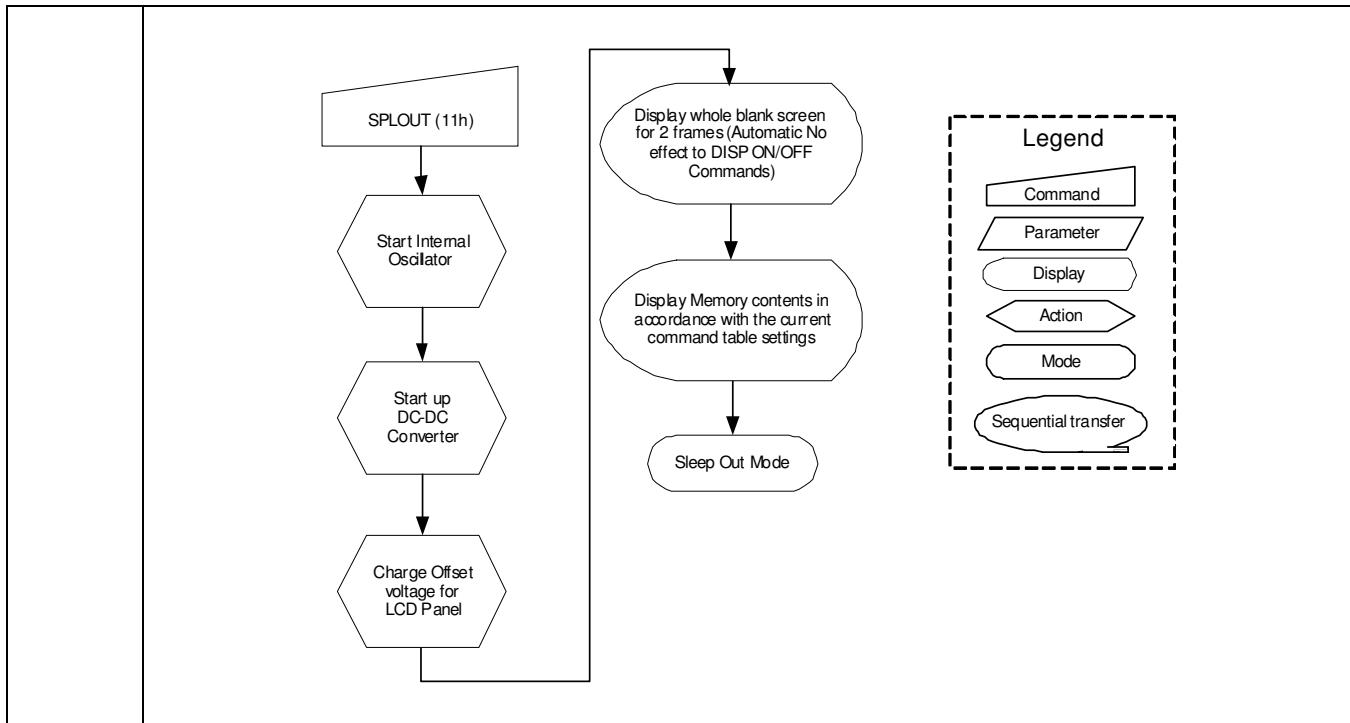
0Fh		RDDSDR (Read Display Self-Diagnostic Result)																									
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	0	0	0	0	1	1	1	1	0Fh														
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X														
2 nd Parameter	1	↑	1	XX	D7	D6	0	0	0	0	0	0	00														
Description	Bit	Description		Action																							
	D7	Register Loading Detection		Invert the D7 bit if register values loading work properly.																							
	D6	Functionality Detection		Invert the D6 bit if the display is functionality																							
	D5	Not Used		'0'																							
	D4	Not Used		'0'																							
	D3	Not Used		'0'																							
	D2	Not Used		'0'																							
	D1	Not Used		'0'																							
	D0	Not Used		'0'																							
Restriction																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes	
Status	Availability																										
Normal Mode On, Idle Mode Off, Sleep Out	Yes																										
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																										
Partial Mode On, Idle Mode On, Sleep Out	Yes																										
Sleep In	Yes																										
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Status	Default Value																										
Power On Sequence	8'h00h																										
SW Reset	8'h00h																										
HW Reset	8'h00h																										
Flow Chart	<pre> graph TD RDDSDR[RDDSDR(0Fh)] --> Host[Host] Host --> Driver[Driver] Driver -- "1st Parameter: Dummy Read
2nd Parameter: Send D[7:6] display self-diagnostic status" --> RDDSDR </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																										

8.2.11. Enter Sleep Mode (10h)

SPLIN (Enter Sleep Mode)																									
10h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	0	0	10h												
Parameter	No Parameter																								
Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p> <p>MCU interface and memory are still working and the memory keeps its contents.</p> <p>X = Don't care</p>																								
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Status	Default Value																								
Power On Sequence	Sleep IN Mode																								
SW Reset	Sleep IN Mode																								
HW Reset	Sleep IN Mode																								
Flow Chart	<p>It takes 120msec to get into Sleep In mode after SLPIN command issued.</p> <pre> graph TD A[SPLIN (10h)] --> B([Display whole blank screen Automatic No effect to DISP ON/OFF commands]) B --> C([Drain charge from LCD panel]) C --> D([Stop DC/DC Converter]) D --> E([Stop Internal Oscillator]) E --> F([Sleep In Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.12. Sleep Out (11h)

SLPOUT (Sleep Out)																									
11h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	0	1	11h												
Parameter	No Parameter																								
Description	<p>This command turns off sleep mode.</p> <p>In this mode e.g. the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> <p>X = Don't care</p>																								
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Sleep IN Mode</td> </tr> <tr> <td>SW Reset</td> <td>Sleep IN Mode</td> </tr> <tr> <td>HW Reset</td> <td>Sleep IN Mode</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Sleep IN Mode	SW Reset	Sleep IN Mode	HW Reset	Sleep IN Mode				
Status	Default Value																								
Power On Sequence	Sleep IN Mode																								
SW Reset	Sleep IN Mode																								
HW Reset	Sleep IN Mode																								
Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued.																								



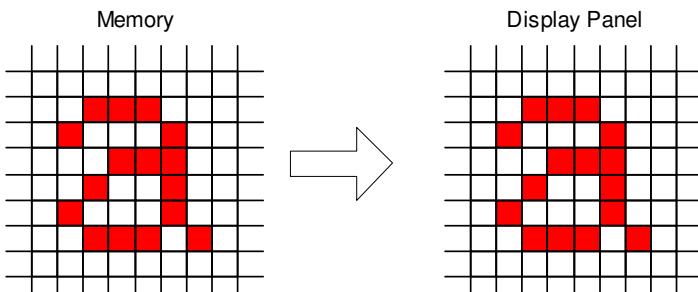
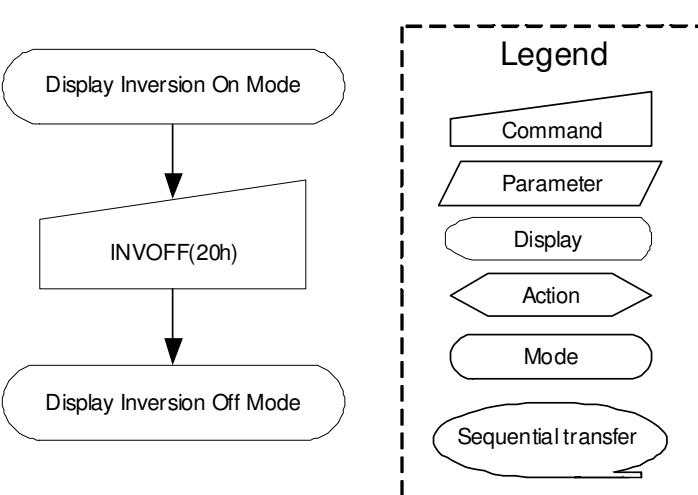
8.2.13. Partial Mode ON (12h)

PTLON (Partial Mode On)																									
12h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	1	0	12h												
Parameter	No Parameter																								
Description	This command turns on partial mode. The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written. X = Don't care																								
Restriction	This command has no effect when Partial mode is active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	Normal Display Mode ON																								
SW Reset	Normal Display Mode ON																								
HW Reset	Normal Display Mode ON																								
Flow Chart	See Partial Area (30h)																								

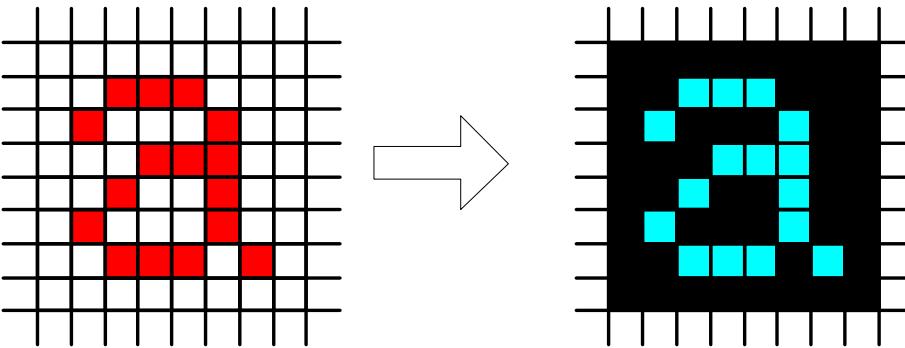
8.2.14. Normal Display Mode ON (13h)

NORON (Normal Display Mode On)																									
13h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	0	1	0	0	1	1	13h												
Parameter	No Parameter																								
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off. Exit from NORON by the Partial mode On command (12h) X = Don't care																								
Restriction	This command has no effect when Normal Display mode is active.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
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Status	Default Value																								
Power On Sequence	Normal Display Mode ON																								
SW Reset	Normal Display Mode ON																								
HW Reset	Normal Display Mode ON																								
Flow Chart	See Partial Area (30h)																								

8.2.15. Display Inversion OFF (20h)

20h		DINVOFF (Display Inversion OFF)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	0	1	0	0	0	0	0	20h													
Parameter	No Parameter																									
Description	<p>This command is used to recover from display inversion mode.</p> <p>This command makes no change of the content of frame memory.</p> <p>This command doesn't change any other status.</p>  <p>X = Don't care</p>																									
Restriction	This command has no effect when module already is inversion OFF mode.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
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Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion OFF</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Display Inversion OFF	SW Reset	Display Inversion OFF	HW Reset	Display Inversion OFF				
Status	Default Value																									
Power On Sequence	Display Inversion OFF																									
SW Reset	Display Inversion OFF																									
HW Reset	Display Inversion OFF																									
Flow Chart	 <pre> graph TD A([Display Inversion On Mode]) --> B[INVOFF(20h)] B --> C([Display Inversion Off Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

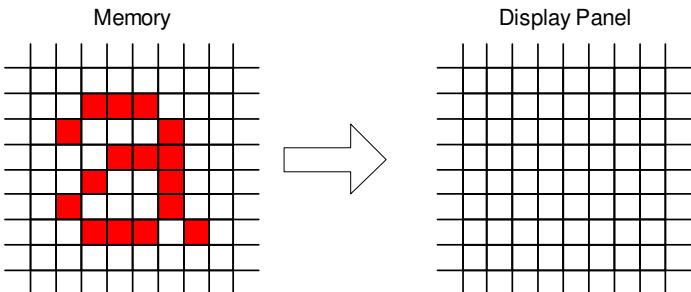
8.2.16. Display Inversion ON (21h)

21h		DINVON (Display Inversion ON)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	0	0	1	21h												
Parameter	No Parameter																								
Description	<p>This command is used to enter into display inversion mode.</p> <p>This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.</p> <p>This command doesn't change any other status.</p> <p>To exit Display inversion mode, the Display inversion OFF command (20h) should be written.</p>  <p>X = Don't care</p>																								
Restriction	This command has no effect when module already is inversion ON mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Inversion OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display Inversion OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display Inversion OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display Inversion OFF	SW Reset	Display Inversion OFF	HW Reset	Display Inversion OFF				
Status	Default Value																								
Power On Sequence	Display Inversion OFF																								
SW Reset	Display Inversion OFF																								
HW Reset	Display Inversion OFF																								
Flow Chart	<pre> graph TD A([Display Inversion On Mode]) --> B[INVON(21h)] B --> C([Display Inversion Off Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

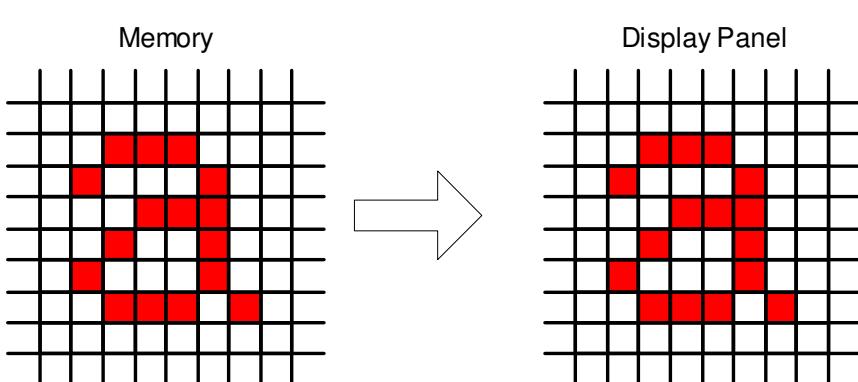
8.2.17. Gamma Set (26h)

26h		GAMSET (Gamma Set)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	0	1	1	0	26h												
Parameter	1	1	↑	XX	GC [7:0]								01												
Description	<p>This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table:</p> <table border="1"> <tr> <th>GC [7:0]</th><th>Curve Selected</th></tr> <tr> <td>01h</td><td>Gamma curve 1 (G2.2)</td></tr> <tr> <td>02h</td><td>---</td></tr> <tr> <td>04h</td><td>---</td></tr> <tr> <td>08h</td><td>---</td></tr> </table> <p>Note: All other values are undefined.</p> <p>X = Don't care</p>													GC [7:0]	Curve Selected	01h	Gamma curve 1 (G2.2)	02h	---	04h	---	08h	---		
GC [7:0]	Curve Selected																								
01h	Gamma curve 1 (G2.2)																								
02h	---																								
04h	---																								
08h	---																								
Restriction	<p>Values of GC [7:0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.</p>																								
Register Availability	<table border="1"> <tr> <th>Status</th><th>Availability</th></tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <tr> <th>Status</th><th>Default Value</th></tr> <tr> <td>Power On Sequence</td><td>8'h01h</td></tr> <tr> <td>SW Reset</td><td>8'h01h</td></tr> <tr> <td>HW Reset</td><td>8'h01h</td></tr> </table>													Status	Default Value	Power On Sequence	8'h01h	SW Reset	8'h01h	HW Reset	8'h01h				
Status	Default Value																								
Power On Sequence	8'h01h																								
SW Reset	8'h01h																								
HW Reset	8'h01h																								
Flow Chart	<pre> graph TD A[GAMSET (26h)] --> B{1st Parameter: GC[7:0]} B --> C{New Gamma Curve Loaded} style C fill:none,stroke:none style B fill:none,stroke:none style A fill:none,stroke:none </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

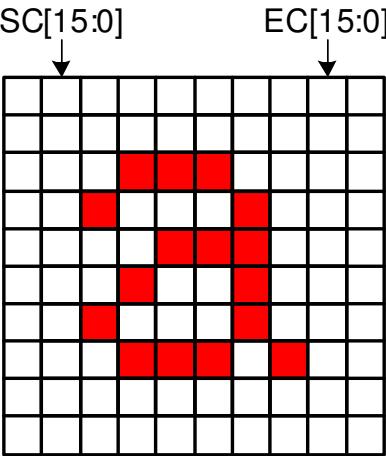
8.2.18. Display OFF (28h)

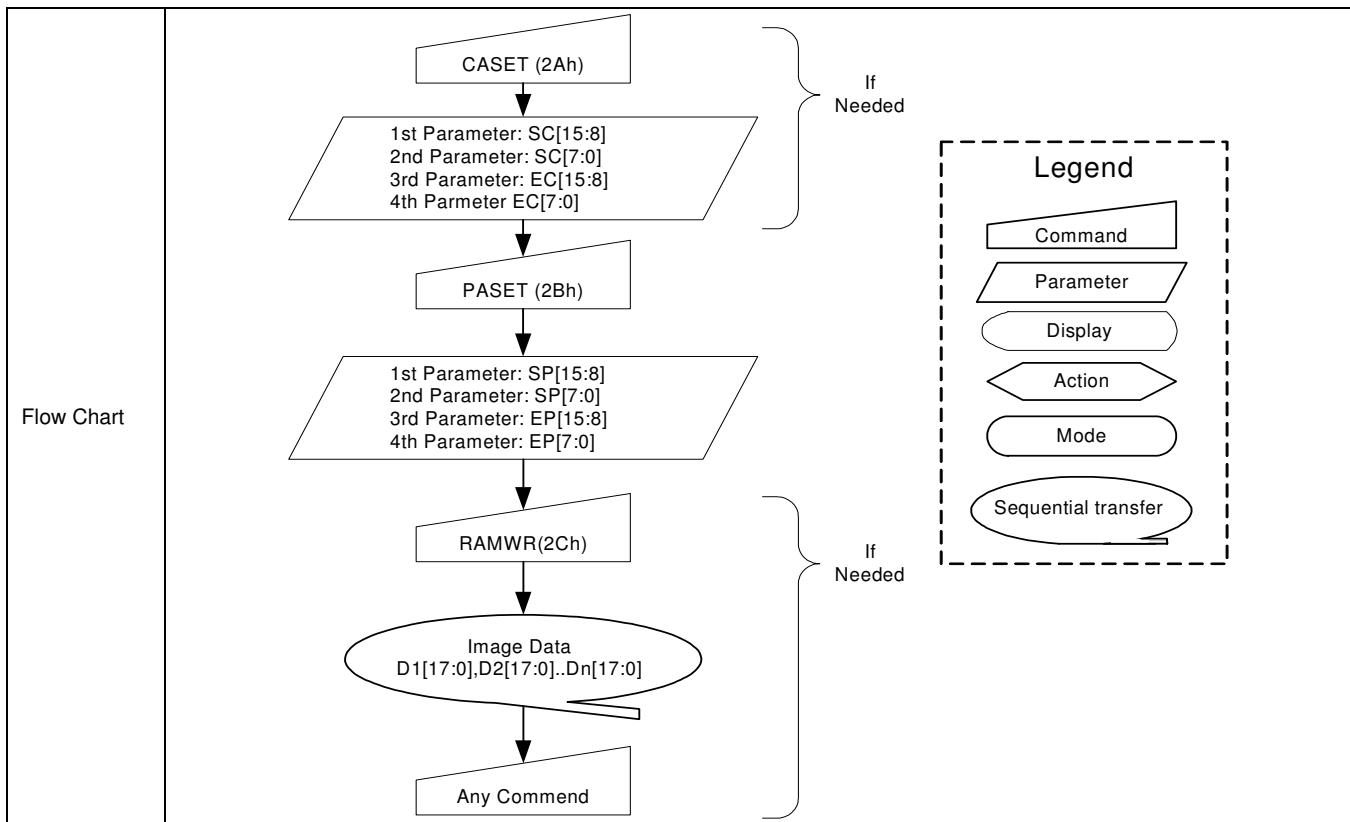
28h		DISPOFF (Display OFF)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	0	0	28h												
Parameter	No Parameter																								
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p>  <p>X = Don't care.</p>																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display OFF	SW Reset	Display OFF	HW Reset	Display OFF				
Status	Default Value																								
Power On Sequence	Display OFF																								
SW Reset	Display OFF																								
HW Reset	Display OFF																								
Flow Chart	<pre> graph TD A([Display On Mode]) --> B[DISPOFF(28h)] B --> C([Display Off Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.19. Display ON (29h)

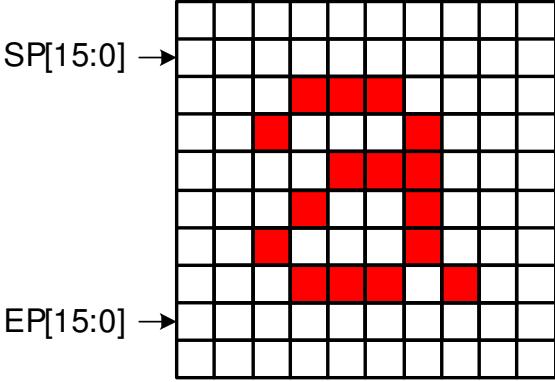
DISPON (Display ON)																									
29h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	0	0	1	29h												
Parameter	No Parameter																								
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status</p>  <p>X = Don't care.</p>																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display OFF</td> </tr> <tr> <td>SW Reset</td> <td>Display OFF</td> </tr> <tr> <td>HW Reset</td> <td>Display OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Display OFF	SW Reset	Display OFF	HW Reset	Display OFF				
Status	Default Value																								
Power On Sequence	Display OFF																								
SW Reset	Display OFF																								
HW Reset	Display OFF																								
Flow Chart	<pre> graph TD A([Display Off Mode]) --> B[DISPON(29h)] B --> C([Display On Mode]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

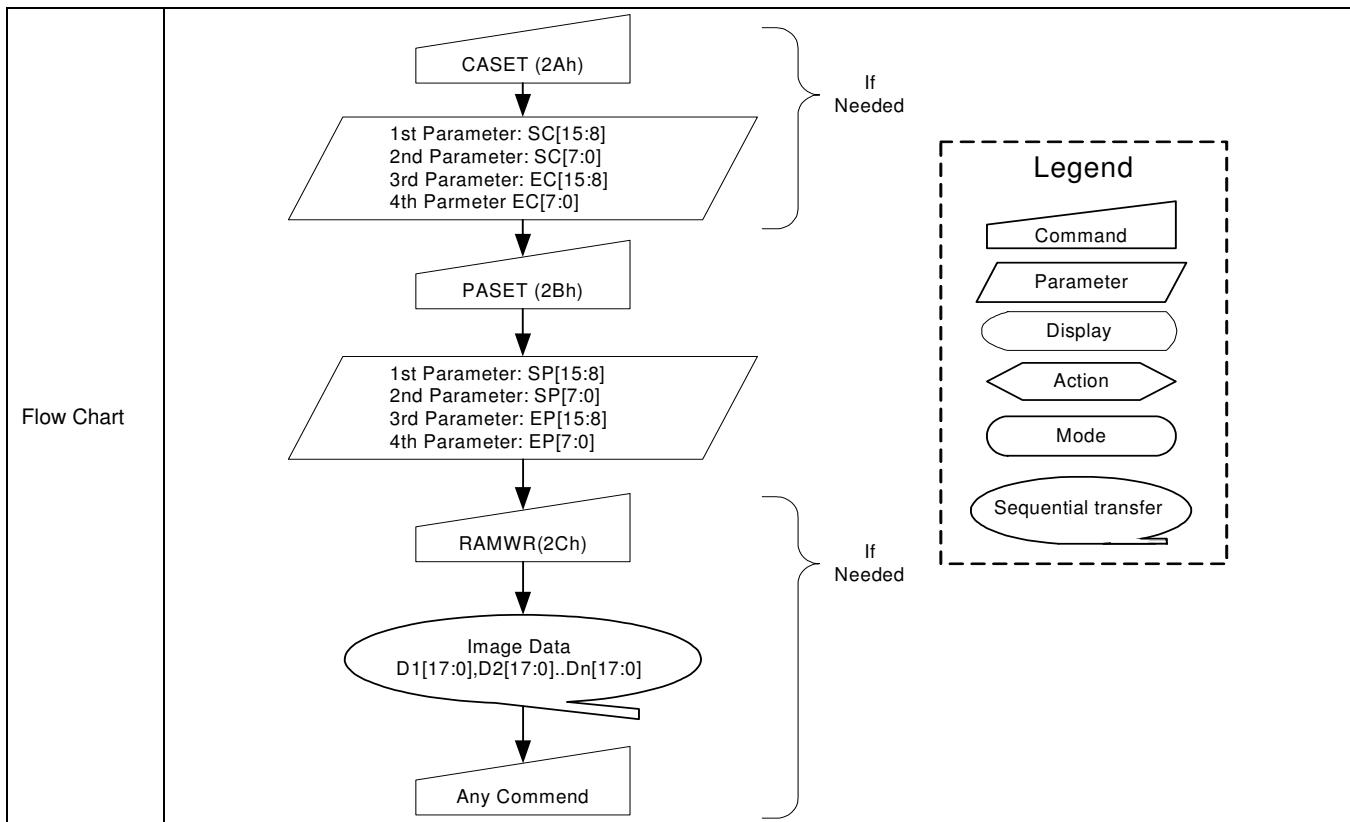
8.2.20. Column Address Set (2Ah)

2Ah		CASET (Column Address Set)												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑		XX	0	0	1	0	1	0	1	0	2Ah
1 st Parameter	1	1	↑		XX	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2 nd Parameter	1	1	↑		XX	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	
3 rd Parameter	1	1	↑		XX	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	
4 th Parameter	1	1	↑		XX	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.</p>  <p>X = Don't care</p>													
Restriction	<p>SC [15:0] always must be equal to or less than EC [15:0].</p> <p>Note 1: When SC [15:0] or EC [15:0] is greater than 00EFh (When MADCTL's B5 = 0) or 013Fh (When MADCTL's B5 = 1), data of out of range will be ignored</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th colspan="2">Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>SC [15:0]=0000h</td><td>EC [15:0]=00EFh</td></tr> <tr> <td>SW Reset</td><td>SC [15:0]=0000h</td><td>If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh</td></tr> <tr> <td>HW Reset</td><td>SC [15:0]=0000h</td><td>EC [15:0]=00EFh</td></tr> </tbody> </table>		Status	Default Value		Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh	SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh	HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh
Status	Default Value													
Power On Sequence	SC [15:0]=0000h	EC [15:0]=00EFh												
SW Reset	SC [15:0]=0000h	If MADCTL's B5 = 0: EC [15:0]=00EFh If MADCTL's B5 = 1: EC [15:0]=013Fh												
HW Reset	SC [15:0]=0000h	EC [15:0]=00EFh												



8.2.21. Page Address Set (2Bh)

2Bh		PASET (Page Address Set)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2Bh	
1 st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note1	
2 nd Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0		
3 rd Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note1	
4 th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0		
Description	<p>This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.</p>  <p>X = Don't care</p>													
Restriction	<p>SP [15:0] always must be equal to or less than EP [15:0]</p> <p>Note 1: When SP [15:0] or EP [15:0] is greater than 013Fh (When MADCTL's B5 = 0) or 00EFh (When MADCTL's B5 = 1), data of out of range will be ignored.</p>													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
Partial Mode On, Idle Mode On, Sleep Out	Yes													
Sleep In	Yes													
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Status	Default Value													
Power On Sequence	SP [15:0]=0000h	EP [15:0]=013Fh												
SW Reset	SP [15:0]=0000h	If MADCTL's B5 = 0: EP [15:0]=013Fh If MADCTL's B5 = 1: EP [15:0]=00EFh												
HW Reset	SP [15:0]=0000h	EP [15:0]=013Fh												



8.2.22. Memory Write (2Ch)

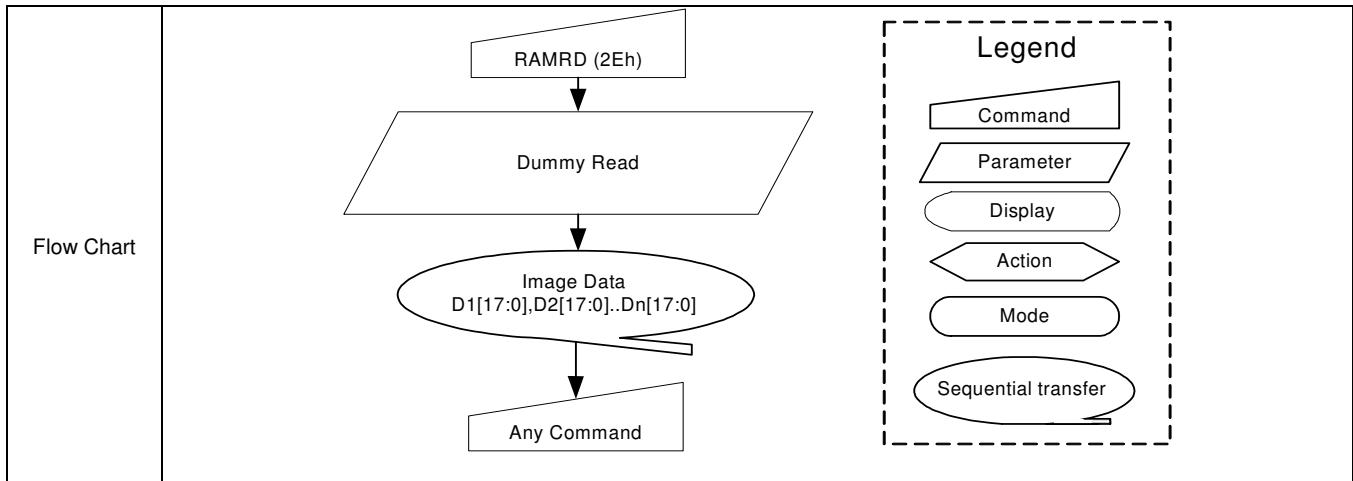
2Ch		RAMWR (Memory Write)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	0	1	0	1	1	0	0	2Ch													
1 st Parameter	1	1	↑	D1 [17:0]					XX																	
:	1	1	↑	Dx [17:0]					XX																	
N th Parameter	1	1	↑	Dn [17:0]					XX																	
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don't care.																									
Restriction	In all color modes, there is no restriction on length of parameters.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is not cleared</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is not cleared</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is not cleared	HW Reset	Contents of memory is not cleared				
Status	Default Value																									
Power On Sequence	Contents of memory is set randomly																									
SW Reset	Contents of memory is not cleared																									
HW Reset	Contents of memory is not cleared																									
Flow Chart	<pre> graph TD CASET[CASET (2Ah)] --> PASET[PASET (2Bh)] PASET --> RAMWR[RAMWR (2Ch)] RAMWR --> ImageData([Image Data D1[17:0], D2[17:0]..Dn[17:0]]) ImageData --> AnyCommand[Any Command] </pre> <p>The flowchart illustrates the sequence of commands for memory write:</p> <ul style="list-style-type: none"> CASET (2Ah): Initial command. PASET (2Bh): Second command. RAMWR (2Ch): Third command. Image Data (D1[17:0], D2[17:0]..Dn[17:0]): Sequential transfer of data. Any Command: Final command. <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

8.2.23. Color Set (2Dh)

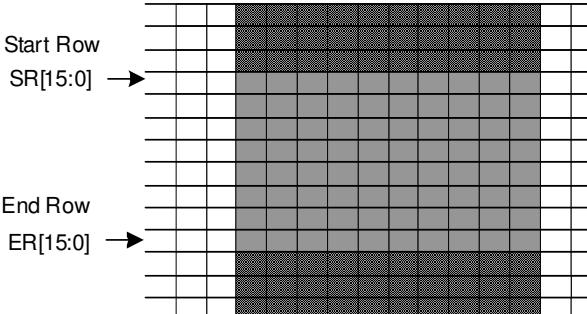
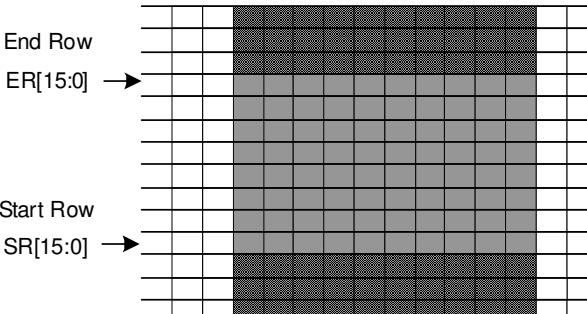
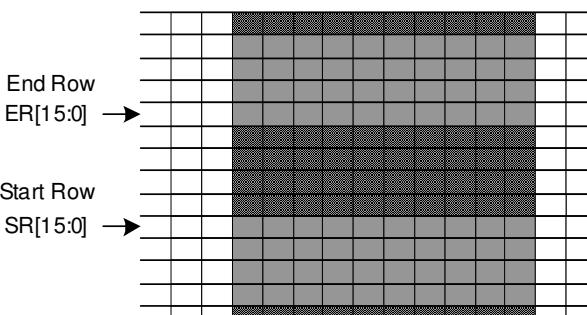
2Dh		RGBSET (Color Set)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	1	0	1	2Dh												
1 st Parameter	1	1	↑	XX	0	0							XX												
n th Parameter	1	1	↑	XX	0	0							XX												
32 nd Parameter	1	1	↑	XX	0	0							XX												
33 rd Parameter	1	1	↑	XX	0	0							XX												
n th Parameter	1	1	↑	XX	0	0							XX												
96 th Parameter	1	1	↑	XX	0	0							XX												
97 th Parameter	1	1	↑	XX	0	0							XX												
n th Parameter	1	1	↑	XX	0	0							XX												
128 th Parameter	1	1	↑	XX	0	0							XX												
Description	<p>This command is used to define the LUT for 16-bit to 18-bit color depth conversion.</p> <p>128 bytes must be written to the LUT regardless of the color mode. Only the values in Section 7.4 are referred.</p> <p>This command has no effect on other commands, parameter and contents of frame memory. Visible change takes effect next time the frame memory is written to.</p>																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
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Status	Default Value																								
Power On Sequence	Random values																								
SW Reset	Contents of LUT protected																								
HW Reset	Random values																								
Flow Chart																									

8.2.24. Memory Read (2Eh)

RAMRD (Memory Read)																									
2Eh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	0	1	1	1	0	2Eh												
1 st Parameter	1	1	↑	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	1	↑					D1 [17:0]					XX												
:	1	1	↑					Dx [17:0]					XX												
(N+1) th Parameter	1	1	↑					Dn [17:0]					XX												
Description	This command transfers image data from ILI9341's frame memory to the host processor starting at the pixel location specified by preceding set_column_address and set_page_address commands.																								
	<p>If Memory Access control B5 = 0:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The column register is then incremented and pixels read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value or the host processor sends another command.</p> <p>If Memory Access Control B5 = 1:</p> <p>The column and page registers are reset to the Start Column (SC) and Start Page (SP), respectively. Pixels are read from frame memory at (SC, SP). The page register is then incremented and pixels read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value or the host processor sends another command.</p>																								
Restriction	There is no restriction on length of parameters.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>SW Reset</td> <td>Contents of memory is set randomly</td> </tr> <tr> <td>HW Reset</td> <td>Contents of memory is set randomly</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	Contents of memory is set randomly	SW Reset	Contents of memory is set randomly	HW Reset	Contents of memory is set randomly				
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Power On Sequence	Contents of memory is set randomly																								
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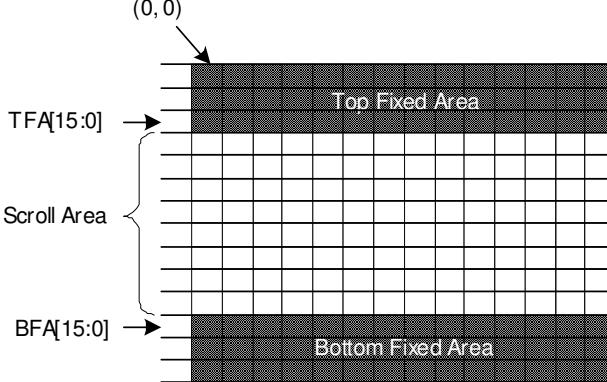


8.2.25. Partial Area (30h)

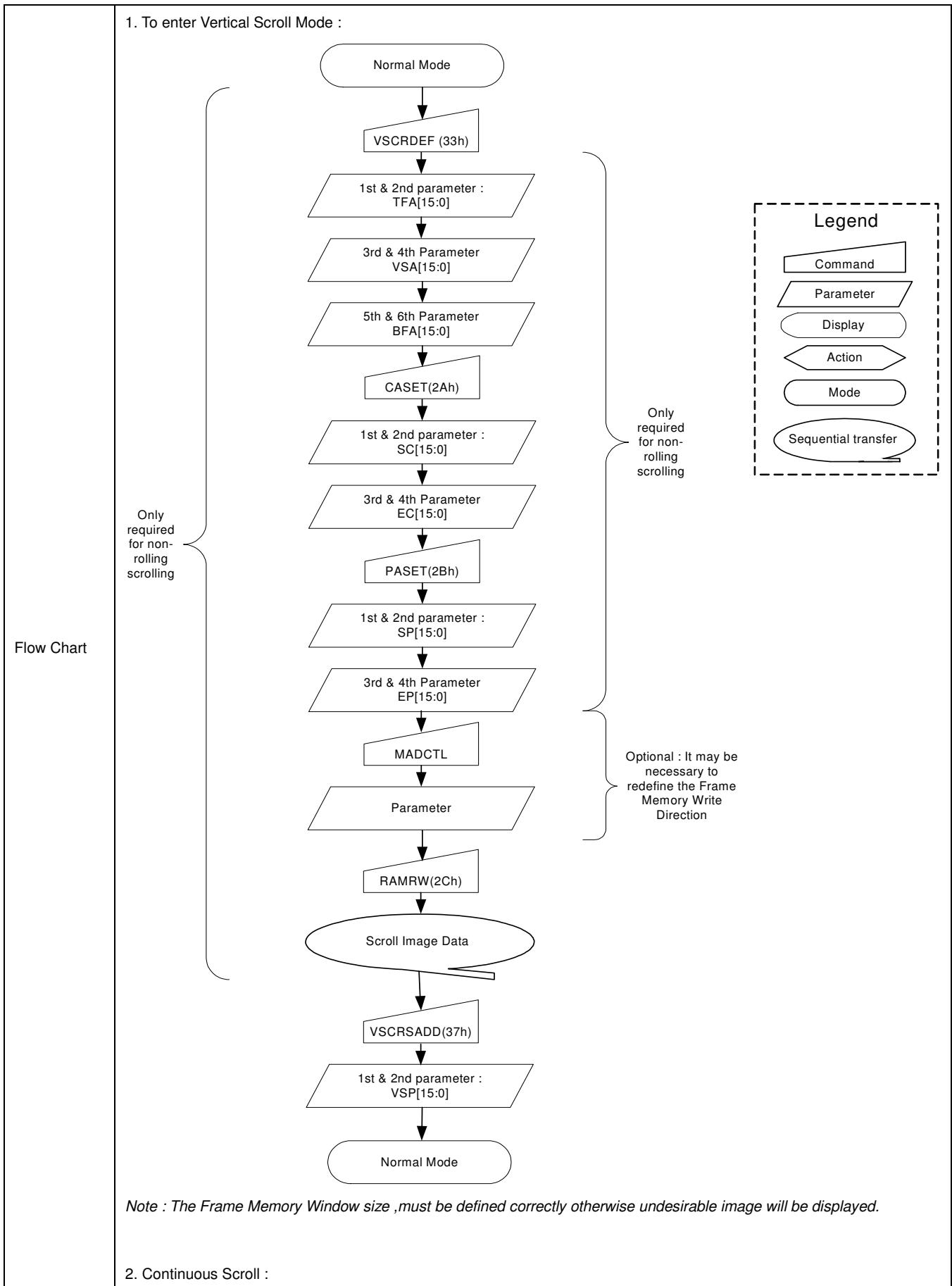
PLTAR (Partial Area)													
30h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	0	0	30h
1 st Parameter	1	1	↑	XX	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2 nd Parameter	1	1	↑	XX	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3 rd Parameter	1	1	↑	XX	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	01
4 th Parameter	1	1	↑	XX	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	3F
Description	<p>This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer.</p> <p>If End Row>Start Row when MADCTL B4=0:-</p>  <p>If End Row>Start Row when MADCTL B4=1:-</p>  <p>If End Row<Start Row when MADCTL B4=0:-</p>  <p>If End Row = Start Row then the Partial Area will be one row deep.</p> <p>X = Don't care.</p>												
Restriction	SR [15...0] and ER [15...0] cannot be 0000h nor exceed 013Fh.												

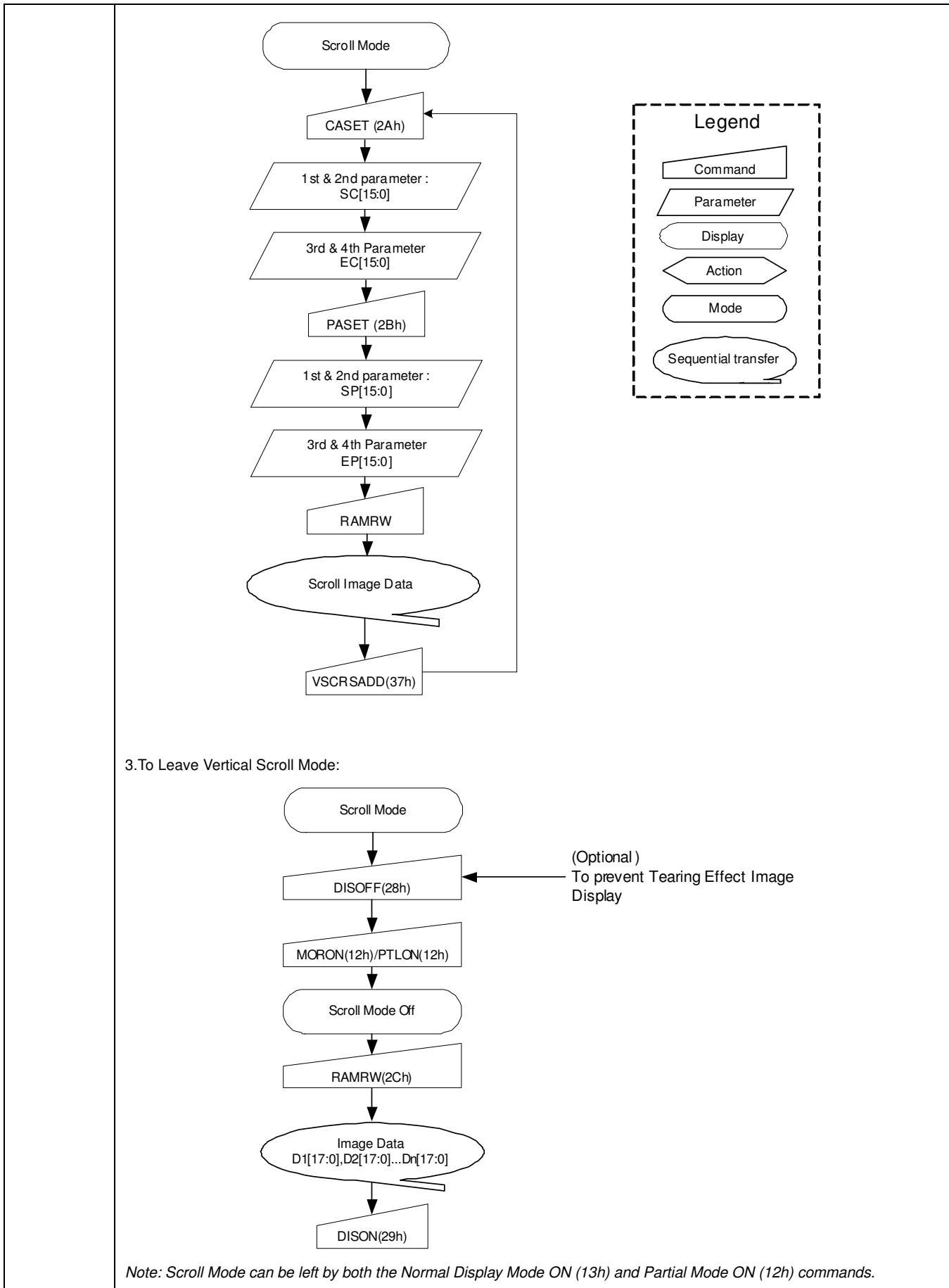
Register Availability		<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability														
Normal Mode On, Idle Mode Off, Sleep Out	Yes														
Normal Mode On, Idle Mode On, Sleep Out	Yes														
Partial Mode On, Idle Mode Off, Sleep Out	Yes														
Partial Mode On, Idle Mode On, Sleep Out	Yes														
Sleep In	Yes														
<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>SR [15:0]</th><th>ER [15:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>16'h0000h</td><td>16'h013Fh</td></tr> <tr> <td>SW Reset</td><td>16'h 0000h</td><td>16'h 013Fh</td></tr> <tr> <td>HW Reset</td><td>16'h 0000h</td><td>16'h 013Fh</td></tr> </tbody> </table>		Status	Default Value		SR [15:0]	ER [15:0]	Power On Sequence	16'h0000h	16'h013Fh	SW Reset	16'h 0000h	16'h 013Fh	HW Reset	16'h 0000h	16'h 013Fh
Status	Default Value														
	SR [15:0]	ER [15:0]													
Power On Sequence	16'h0000h	16'h013Fh													
SW Reset	16'h 0000h	16'h 013Fh													
HW Reset	16'h 0000h	16'h 013Fh													
Flow Chart	<p>1. To Enter Partial Mode</p> <pre> graph TD PLTAR[PLTAR(30h)] --> P1[1st Parameter: SR[15:8] 2nd Parameter: SR[7:0]] P1 --> P2[3rd Parameter: ER[15:8] 4th Parameter: ER[7:0]] P2 --> PTLON[PTLON(12h)] PTLON --> PM[Partial Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 														
	<p>2. To Leave Partial Mode</p> <pre> graph TD PM[Partial Mode] --> DISPOFF[DISPOFF(28h)] DISPOFF --> NORON[NORON(13h)] NORON --> RAMRW[RAMRW(2Ch)] RAMRW --> ID{Image Data D1[17:0], D2[17:0]..Dn[17:0]} ID --> DISPON[DISPON(29h)] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 														

8.2.26. Vertical Scrolling Definition (33h)

VSCRDEF (Vertical Scrolling Definition)													
33h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	0	0	1	1	33h
1 st Parameter	1	↑	1	XX					TFA [15:8]				00
2 nd Parameter	1	↑	1	XX					TFA [7:0]				00
3 rd Parameter	1	↑	1	XX					VSA [15:8]				01
4 th Parameter	1	↑	1	XX					VSA [7:0]				40
5 th Parameter	1	↑	1	XX					BFA [15:8]				00
6 th Parameter	1	↑	1	XX					BFA [7:0]				00
Description	<p>This command defines the Vertical Scrolling Area of the display.</p> <p>When MADCTL B4=0</p> <p>The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p> <p>The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.</p> <p>The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.</p>  <p>When MADCTL B4=1</p> <p>The 1st & 2nd parameter TFA [15...0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).</p> <p>The 3rd & 4th parameter VSA [15...0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.</p> <p>The 5th & 6th parameter BFA [15...0] describes the Bottom Fixed Area (in No. of lines from Top of the Frame Memory and Display).</p>												

	<p>The diagram illustrates the LCD panel structure. It features a central 'Scroll Area' bounded by 'BFA[15:0]' (Bottom Fixed Area) at the top and 'TFA[15:0]' (Top Fixed Area) at the bottom. The origin (0,0) is marked at the top-left corner of the scroll area. An arrow points from the text 'First line read from memory' to the bottom edge of the scroll area.</p> <p>X = Don't care</p>																			
Restriction																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																			
Normal Mode On, Idle Mode Off, Sleep Out	Yes																			
Normal Mode On, Idle Mode On, Sleep Out	Yes																			
Partial Mode On, Idle Mode Off, Sleep Out	Yes																			
Partial Mode On, Idle Mode On, Sleep Out	Yes																			
Sleep In	Yes																			
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="3">Default Value</th></tr> <tr> <th>TFA [15:0]</th><th>VSA [15:0]</th><th>BFA [15:0]</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>16'h0000h</td><td>16'h0140h</td><td>16'h0000h</td></tr> <tr> <td>SW Reset</td><td>16'h0000h</td><td>16'h0140h</td><td>16'h0000h</td></tr> <tr> <td>HW Reset</td><td>16'h0000h</td><td>16'h0140h</td><td>16'h0000h</td></tr> </tbody> </table>	Status	Default Value			TFA [15:0]	VSA [15:0]	BFA [15:0]	Power On Sequence	16'h0000h	16'h0140h	16'h0000h	SW Reset	16'h0000h	16'h0140h	16'h0000h	HW Reset	16'h0000h	16'h0140h	16'h0000h
Status	Default Value																			
	TFA [15:0]	VSA [15:0]	BFA [15:0]																	
Power On Sequence	16'h0000h	16'h0140h	16'h0000h																	
SW Reset	16'h0000h	16'h0140h	16'h0000h																	
HW Reset	16'h0000h	16'h0140h	16'h0000h																	

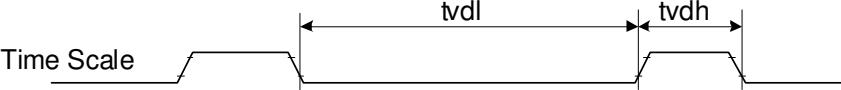
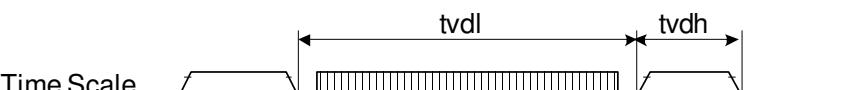


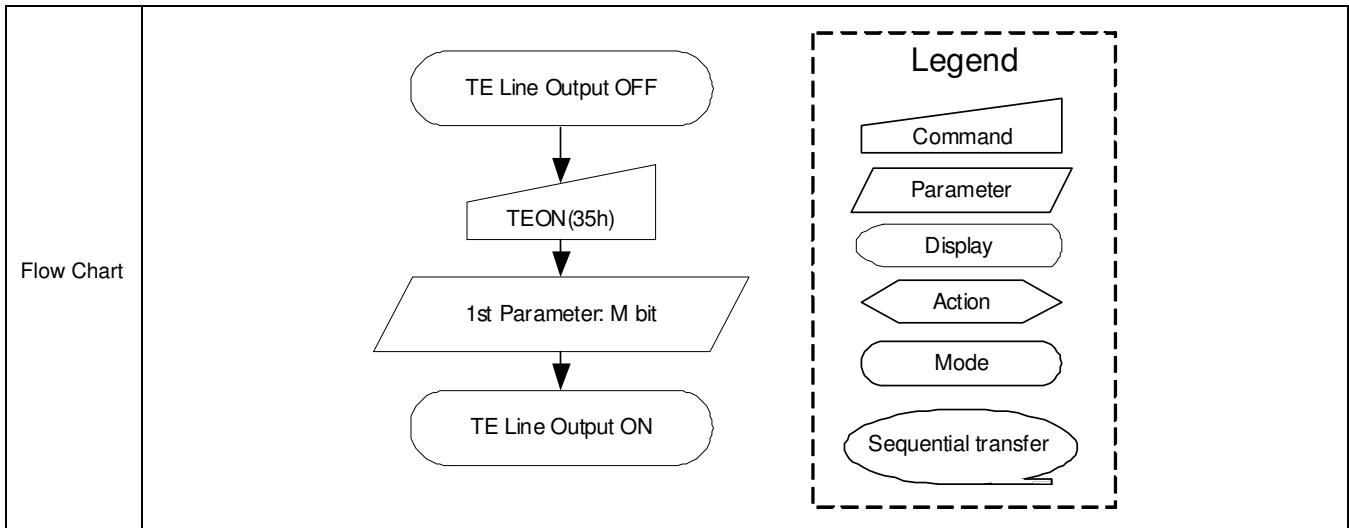


8.2.27. Tearing Effect Line OFF (34h)

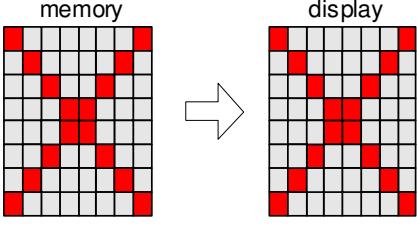
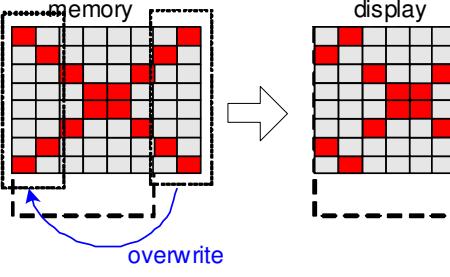
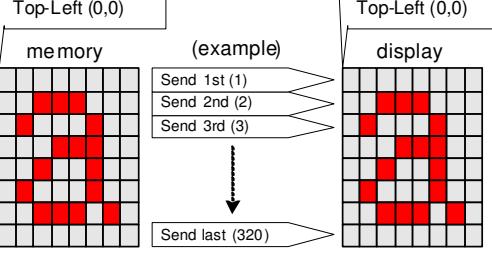
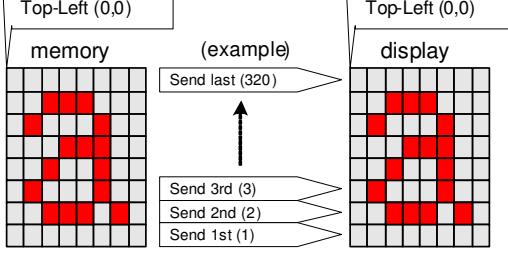
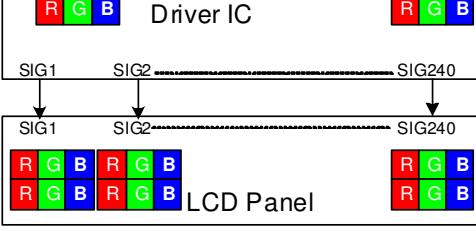
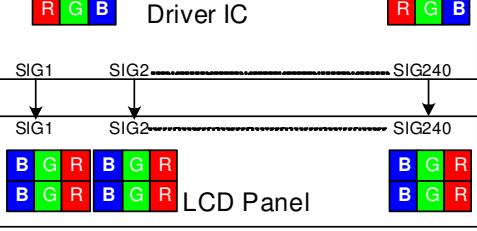
34h		TEOFF (Tearing Effect Line OFF)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	0	1	0	0	34h												
Parameter	No Parameter																								
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line. X = Don't care.																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								
Flow Chart	<pre> graph TD A([TE Line Output ON]) --> B[TEOFF(34h)] B --> C([TE Line Output OFF]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

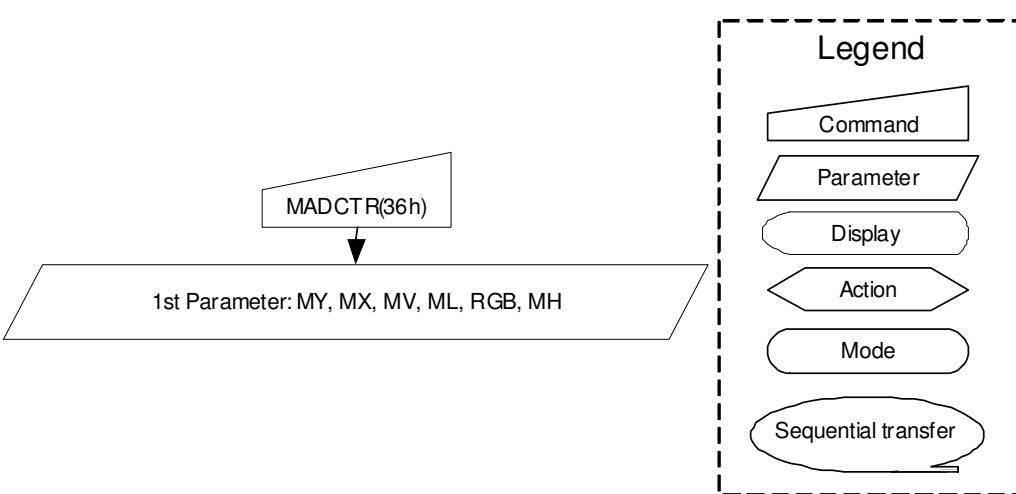
8.2.28. Tearing Effect Line ON (35h)

TEON (Tearing Effect Line ON)																									
35h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	0	1	0	1	35h												
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	M	00												
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. When M=0 : The Tearing Effect Output line consists of V-Blanking information only:  When M=1 : The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:  Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low. X = Don't care.																								
Restriction	This command has no effect when Tearing Effect output is already ON																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>													Status	Default Value	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value																								
Power On Sequence	OFF																								
SW Reset	OFF																								
HW Reset	OFF																								

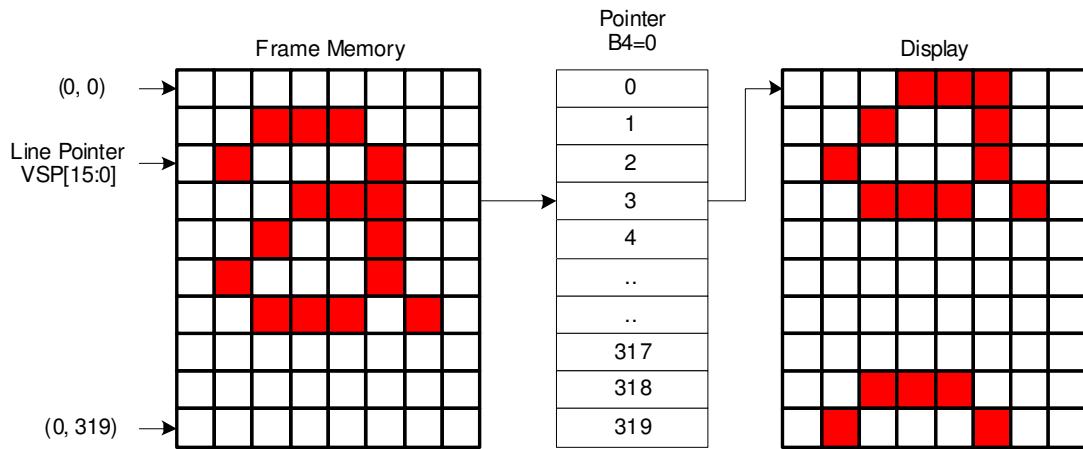
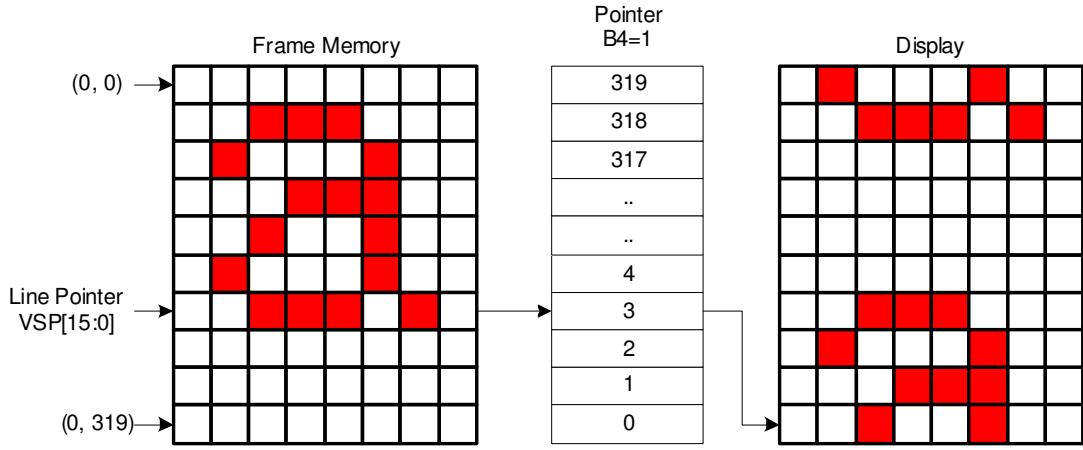


8.2.29. Memory Access Control (36h)

36h		MADCTL (Memory Access Control)																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	↑	XX	0	0	1	1	0	1	1	0	36h																					
Parameter	1	1	↑	XX	MY	MX	MV	ML	BGR	MH	0	0	00																					
This command defines read/write scanning direction of frame memory.																																		
This command makes no change on the other driver status.																																		
<table border="1"> <thead> <tr> <th>Bit</th> <th>Name</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>MY</td> <td>Row Address Order</td> <td>These 3 bits control MCU to memory write/read direction.</td> </tr> <tr> <td>MX</td> <td>Column Address Order</td> <td></td> </tr> <tr> <td>MV</td> <td>Row / Column Exchange</td> <td>LCD vertical refresh direction control.</td> </tr> <tr> <td>ML</td> <td>Vertical Refresh Order</td> <td>Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)</td> </tr> <tr> <td>BGR</td> <td>RGB-BGR Order</td> <td>LCD horizontal refreshing direction control.</td> </tr> <tr> <td>MH</td> <td>Horizontal Refresh ORDER</td> <td></td> </tr> </tbody> </table>														Bit	Name	Description	MY	Row Address Order	These 3 bits control MCU to memory write/read direction.	MX	Column Address Order		MV	Row / Column Exchange	LCD vertical refresh direction control.	ML	Vertical Refresh Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)	BGR	RGB-BGR Order	LCD horizontal refreshing direction control.	MH	Horizontal Refresh ORDER	
Bit	Name	Description																																
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MX	Column Address Order																																	
MV	Row / Column Exchange	LCD vertical refresh direction control.																																
ML	Vertical Refresh Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)																																
BGR	RGB-BGR Order	LCD horizontal refreshing direction control.																																
MH	Horizontal Refresh ORDER																																	
Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.																																		
X = Don't care.																																		
Description	<p>MV(Vertical refresh order bit)="0"</p> 							<p>MV(Vertical refresh order bit)="1"</p> 																										
	<p>ML(Vertical refresh order bit)="0"</p> 							<p>ML(Vertical refresh order bit)="1"</p> 																										
	<p>BGR(RGB-BGR Order control bit)="0"</p> 							<p>BGR(RGB-BGR Order control bit)="1"</p> 																										

	MH(Horizontal refresh order control bit)="0"	MH(Horizontal refresh order control bit)="1"												
Note: Top-Left (0,0) means a physical memory location.														
Restriction														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability													
Normal Mode On, Idle Mode Off, Sleep Out	Yes													
Normal Mode On, Idle Mode On, Sleep Out	Yes													
Partial Mode On, Idle Mode Off, Sleep Out	Yes													
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Sleep In	Yes													
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h00h</td></tr> <tr> <td>SW Reset</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>8'h00h</td></tr> </tbody> </table>		Status	Default Value	Power On Sequence	8'h00h	SW Reset	No change	HW Reset	8'h00h				
Status	Default Value													
Power On Sequence	8'h00h													
SW Reset	No change													
HW Reset	8'h00h													
Flow Chart	 <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 													

8.2.30. Vertical Scrolling Start Address (37h)

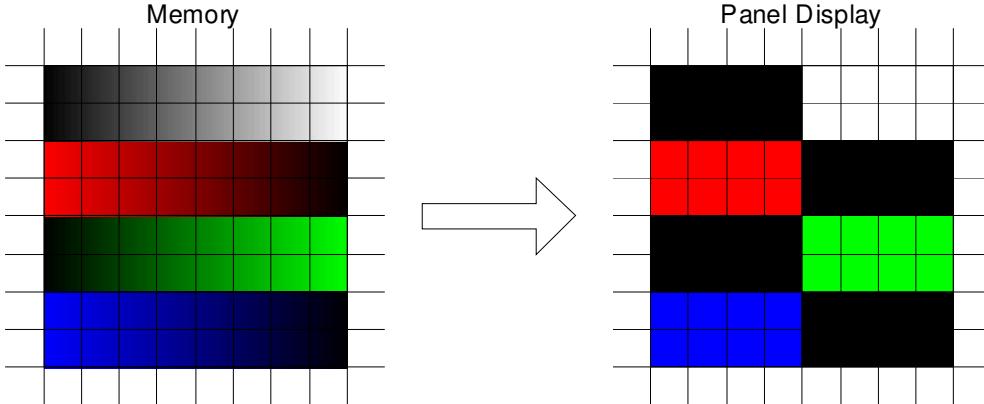
37h		VSCRSADD (Vertical Scrolling Start Address)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	0	0	1	1	0	1	1	1	37h	
1 st Parameter	1	↑	1	XX	VSP [15:8]									00
2 nd Parameter	1	↑	1	XX	VSP [7:0]									00
Description	<p>This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below:-</p> <p>When MADCTL B4=0</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.</p>  <p>When MADCTL B4=1</p> <p>Example:</p> <p>When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 320 and VSP='3'.</p>  <p>Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. VSP refers to the Frame Memory line Pointer. (2) This command is ignored when the ILI9341 enters Partial mode.</p> <p>X = Don't care</p>													

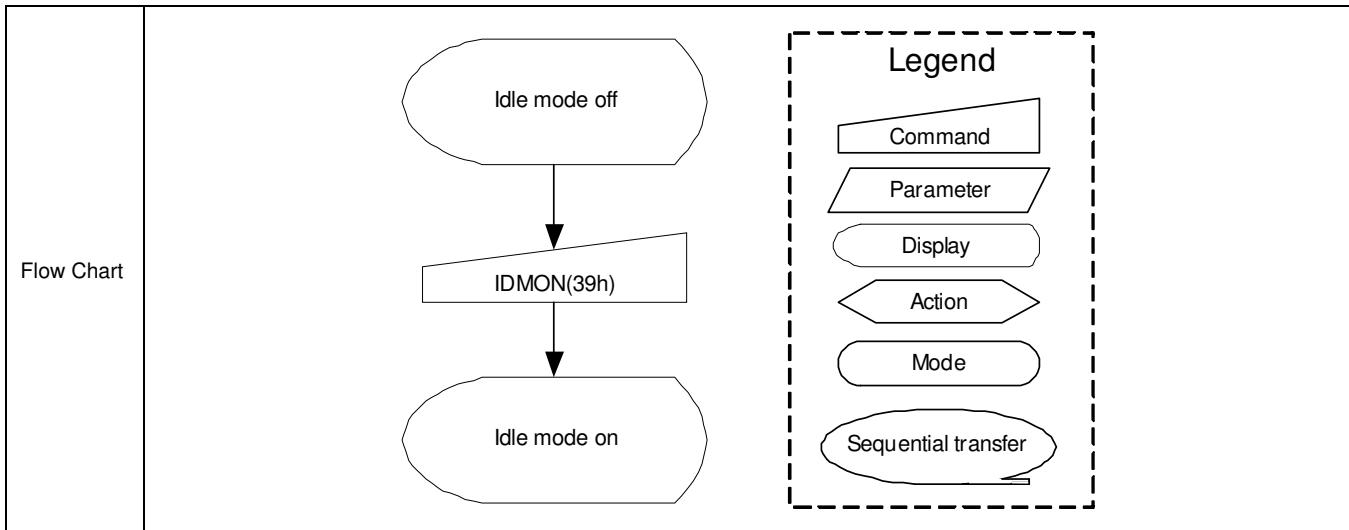
Restriction													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>No</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>No</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	No	Partial Mode On, Idle Mode On, Sleep Out	No	Sleep In	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
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Sleep In	Yes												
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Status	Default Value												
VSP [15:0]													
Power On Sequence	16'h0000h												
SW Reset	16'h0000h												
HW Reset	16'h0000h												
Flow Chart	See Vertical Scrolling Definition (33h) description.												

8.2.31. Idle Mode OFF (38h)

38h		IDMOFF (Idle Mode OFF)																							
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command		0	1	↑	XX	0	0	1	1	1	0	0	0	38h											
Parameter	No Parameter																								
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 262,144 colors. X = Don't care.																								
Restriction	This command has no effect when module is already in idle off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Status	Default Value																								
Power On Sequence	Idle mode OFF																								
SW Reset	Idle mode OFF																								
HW Reset	Idle mode OFF																								
Flow Chart	<pre> graph TD A([Idle mode on]) --> B[IDMOFF(38h)] B --> C([Idle mode off]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.32. Idle Mode ON (39h)

39h		IDMON (Idle Mode ON)																																																																																																																																																																																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																											
Command	0	1	↑	XX	0	0	1	1	1	0	0	1	39h																																																																																																																																																																																											
Parameter	No Parameter																																																																																																																																																																																																							
Description	<p>This command is used to enter into Idle mode on.</p> <p>In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.</p>  <table border="1"> <thead> <tr> <th colspan="15">Memory Contents vs. Display Color</th> </tr> <tr> <th></th> <th>R₅</th> <th>R₄</th> <th>R₃</th> <th>R₂</th> <th>R₁</th> <th>R₀</th> <th>G₅</th> <th>G₄</th> <th>G₃</th> <th>G₂</th> <th>G₁</th> <th>G₀</th> <th>B₅</th> <th>B₄</th> <th>B₃</th> <th>B₂</th> <th>B₁</th> <th>B₀</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Blue</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Red</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Magenta</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Green</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Cyan</td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>Yellow</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>0XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>White</td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>1XXXXX</td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> <p>X = Don't care.</p>														Memory Contents vs. Display Color																R ₅	R ₄	R ₃	R ₂	R ₁	R ₀	G ₅	G ₄	G ₃	G ₂	G ₁	G ₀	B ₅	B ₄	B ₃	B ₂	B ₁	B ₀	Black	0XXXXX						0XXXXX						0XXXXX						Blue	0XXXXX						0XXXXX						1XXXXX						Red	1XXXXX						0XXXXX						0XXXXX						Magenta	1XXXXX						0XXXXX						1XXXXX						Green	0XXXXX						1XXXXX						0XXXXX						Cyan	0XXXXX						1XXXXX						1XXXXX						Yellow	1XXXXX						1XXXXX						0XXXXX						White	1XXXXX						1XXXXX						1XXXXX					
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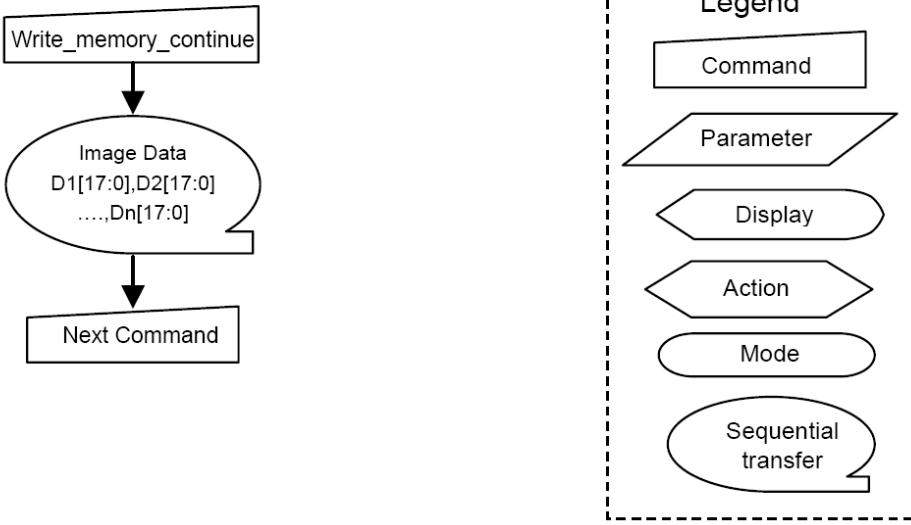


8.2.33. COLMOD: Pixel Format Set (3Ah)

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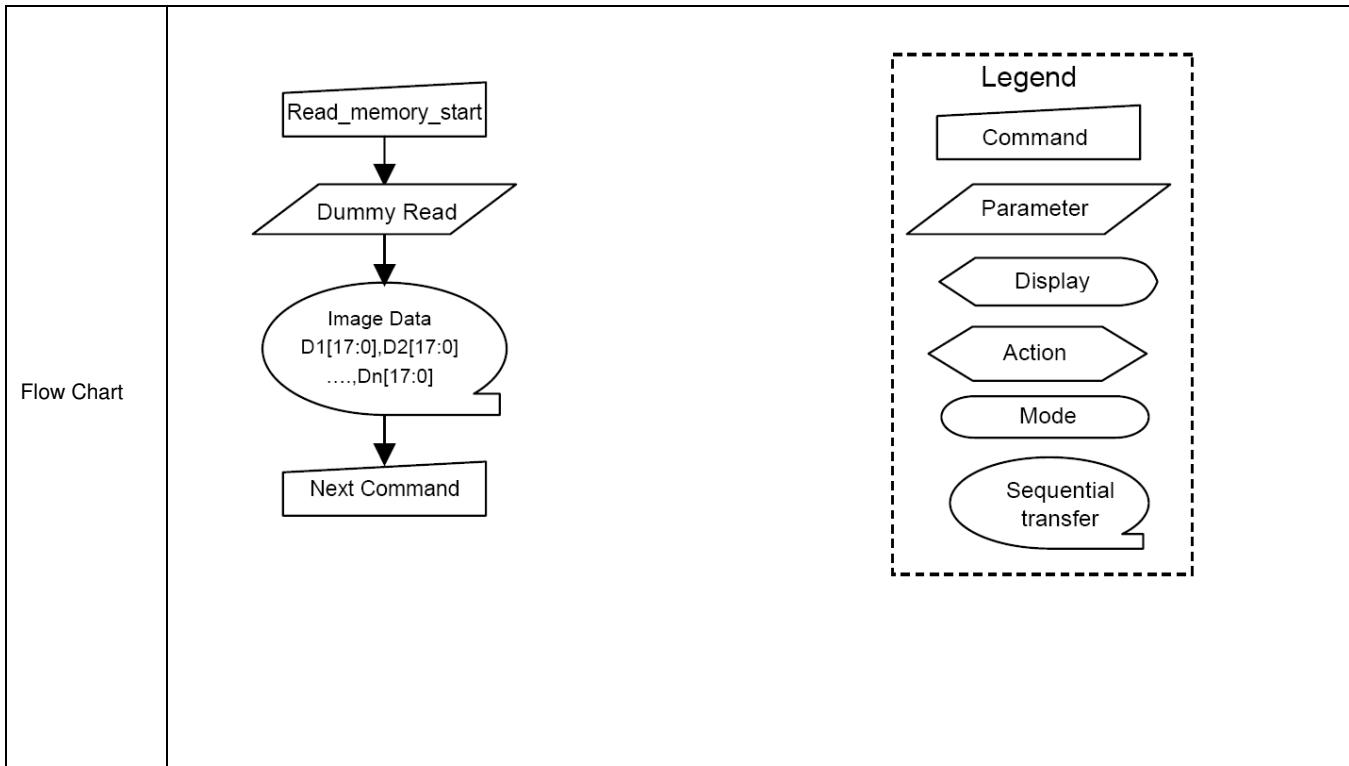
8.2.34. Write_Memory_Continue (3Ch)

Write_Memory_Continue													
3Ch	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	1	1	1	0	0	3Ch
1 st Parameter	1	1	↑	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF
X th Parameter	1	1	↑	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF
N th Parameter	1	1	↑	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF
Description	<p>This command transfers image data from the host processor to the display module's frame memory continuing from the pixel location following the previous write_memory_continue or write_memory_start command.</p> <p>If set_address_mode B5 = 0:</p> <p>Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The column register is then incremented and pixels are written to the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are written to the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p> <p>If set_address_mode B5 = 1:</p> <p>Data is written continuing from the pixel location after the write range of the previous write_memory_start or write_memory_continue. The page register is then incremented and pixels are written to the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are written to the frame memory until the column register equals the End column (EC) value and the page register equals the EP value, or the host processor sends another command. If the number of pixels exceeds (EC – SC + 1) * (EP – SP + 1) the extra pixels are ignored.</p> <p>Sending any other command can stop frame Write.</p> <p>Frame Memory Access and Interface setting (B3h), WEMODE=0 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored.</p> <p>Frame Memory Access and Interface setting (B3h), WEMODE=1 When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.</p>												
Restriction	<p>A write_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the write address. Otherwise, data written with write_memory_continue is written to undefined addresses.</p>												

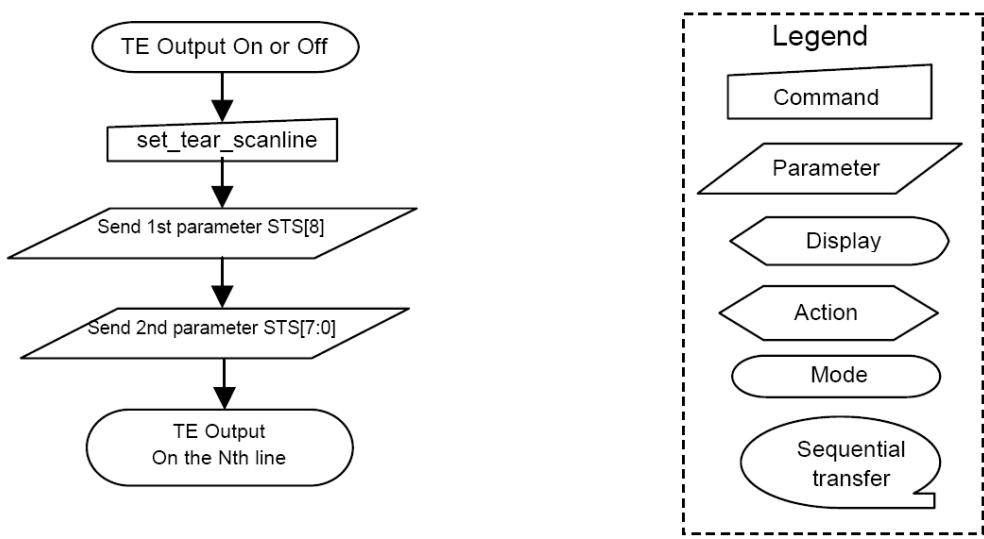
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>No</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	No
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Status	Default Value												
Power On Sequence	Random value												
SW Reset	No change												
HW Reset	No change												
Flow Chart	 <pre> graph TD A[Write_memory_continue] --> B((Image Data D1[17:0], D2[17:0] ..., Dn[17:0])) B --> C[Next Command] </pre> <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </div>												

8.2.35. Read_Memory_Continue (3Eh)

3Eh		Read_Memory_Continue																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	0	1	1	1	1	1	0	3Eh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	D1 [17..8]	D1 [7]	D1 [6]	D1 [5]	D1 [4]	D1 [3]	D1 [2]	D1 [1]	D1 [0]	000 3FF												
x st Parameter	1	↑	1	Dx [17..8]	Dx [7]	Dx [6]	Dx [5]	Dx [4]	Dx [3]	Dx [2]	Dx [1]	Dx [0]	000 3FF												
N st Parameter	1	↑	1	Dn [17..8]	Dn [7]	Dn [6]	Dn [5]	Dn [4]	Dn [3]	Dn [2]	Dn [1]	Dn [0]	000 3FF												
Description	<p>This command transfers image data from the display module's frame memory to the host processor continuing from the location following the previous read_memory_continue (3Eh) or read_memory_start (2Eh) command.</p> <p>If set_address_mode B5 = 0:</p> <p>Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The column register is then incremented and pixels are read from the frame memory until the column register equals the End Column (EC) value. The column register is then reset to SC and the page register is incremented. Pixels are read from the frame memory until the page register equals the End Page (EP) value and the column register equals the EC value, or the host processor sends another command.</p> <p>If set_address_mode B5 = 1:</p> <p>Pixels are read continuing from the pixel location after the read range of the previous read_memory_start or read_memory_continue. The page register is then incremented and pixels are read from the frame memory until the page register equals the End Page (EP) value. The page register is then reset to SP and the column register is incremented. Pixels are read from the frame memory until the column register equals the End Column (EC) value and the page register equals the EP value, or the host processor sends another command.</p> <p>This command makes no change to the other driver status.</p>																								
Restriction	<p>A read_memory_start should follow a set_column_address, set_page_address or set_address_mode to define the read location. Otherwise, data read with read_memory_continue is undefined.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
Power On Sequence	Random data																								
SW Reset	No change																								
HW Reset	No change																								



8.2.36. Set_Tear_Scanline (44h)

44h		Set_Tear_Scanline																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	0	0	1	0	0	44h												
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	STS [8]	00												
2 nd Parameter	1	1	↑	XX	STS [7]	STS [6]	STS [5]	STS [4]	STS [3]	STS [2]	STS [1]	STS [0]	00												
Description	<p>This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line STS.</p> <p>The TE signal is not affected by changing set_address_mode bit B4. The Tearing Effect Line On has one parameter that describes the Tearing Effect Output Line mode.</p>  <p>Note that set_tear_scanline with STS=0 is equivalent to set_tear_on with M=0.</p> <p>The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</p>																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>STS [8:0]=0000h</td></tr> <tr> <td>SW Reset</td><td>STS [8:0]=0000h</td></tr> <tr> <td>HW Reset</td><td>STS [8:0]=0000h</td></tr> </tbody> </table>													Status	Default Value	Power On Sequence	STS [8:0]=0000h	SW Reset	STS [8:0]=0000h	HW Reset	STS [8:0]=0000h				
Status	Default Value																								
Power On Sequence	STS [8:0]=0000h																								
SW Reset	STS [8:0]=0000h																								
HW Reset	STS [8:0]=0000h																								
Flow Chart	 <pre> graph TD A([TE Output On or Off]) --> B[/set_tear_scanline/] B --> C[/Send 1st parameter STS[8]/] C --> D[/Send 2nd parameter STS[7:0]/] D --> E([TE Output On the Nth line]) </pre>																								

8.2.37. Get_Scanline (45h)

45h		Get_Scanline																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	1	0	0	0	1	0	1	45h													
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X													
2 nd Parameter	1	↑	1	XX	0	0	0	0	0	0	GTS [9]	GTS [8]	00													
3 rd Parameter	1	↑	1	XX	GTS [7]	GTS [6]	GTS [5]	GTS [4]	GTS [3]	GTS [2]	GTS [1]	GTS [0]	00													
Description	<p>The display returns the current scan line, GTS, used to update the display device. The total number of scan lines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scan line is defined as the first line of V-Sync and is denoted as Line 0.</p> <p>When in Sleep Mode, the value returned by get_scanline is undefined.</p>																									
Restriction	None																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
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Sleep In	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value</th></tr> </thead> <tbody> <tr> <td>GTS [9:0]</td><td></td></tr> <tr> <td>Power On Sequence</td><td>GTS [9:0]=0000h</td></tr> <tr> <td>SW Reset</td><td>GTS [9:0]=0000h</td></tr> <tr> <td>HW Reset</td><td>GTS [9:0]=0000h</td></tr> </tbody> </table>														Status	Default Value	GTS [9:0]		Power On Sequence	GTS [9:0]=0000h	SW Reset	GTS [9:0]=0000h	HW Reset	GTS [9:0]=0000h		
Status	Default Value																									
GTS [9:0]																										
Power On Sequence	GTS [9:0]=0000h																									
SW Reset	GTS [9:0]=0000h																									
HW Reset	GTS [9:0]=0000h																									
Flow Chart	<pre> graph TD A[get_scanline] --> B{Wait 3us} B --> C{Dummy Read} C --> D[Send 1st parameter GTS[9:8]] D --> E[Send 2nd parameter GTS[7:0]] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

8.2.38. Write Display Brightness (51h)

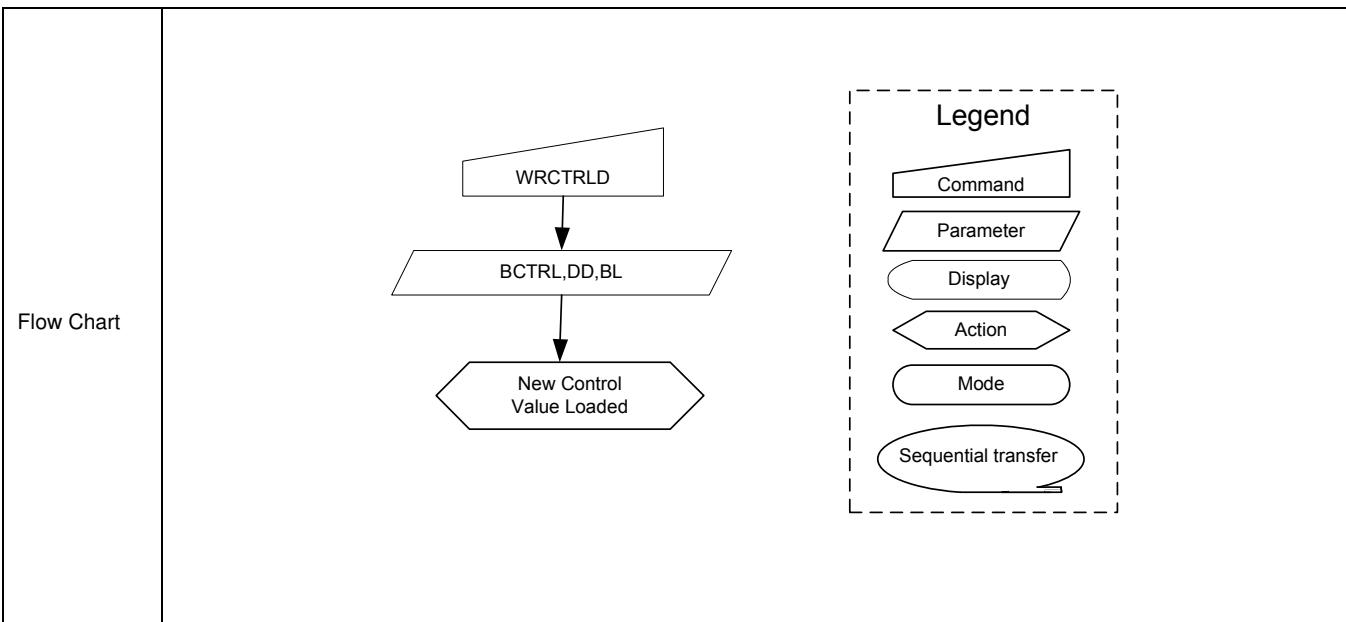
WRDISBV (Write Display Brightness)																									
51h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	0	0	1	51h												
Parameter	1	1	↑	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00												
Description	<p>This command is used to adjust the brightness value of the display.</p> <p>It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>DBV [7:0]</td> <td></td> </tr> <tr> <td>Power On Sequence</td> <td>8'h00h</td> </tr> <tr> <td>SW Reset</td> <td>8'h00h</td> </tr> <tr> <td>HW Reset</td> <td>8'h00h</td> </tr> </tbody> </table>													Status	Default Value	DBV [7:0]		Power On Sequence	8'h00h	SW Reset	8'h00h	HW Reset	8'h00h		
Status	Default Value																								
DBV [7:0]																									
Power On Sequence	8'h00h																								
SW Reset	8'h00h																								
HW Reset	8'h00h																								
Flow Chart	<pre> graph TD WRDISBV[WRDISBV] --> DBV[7..0] DBV[7..0] --> NewDisplayBrightnessValueLoaded{New Display Brightness Value Loaded} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.39. Read Display Brightness (52h)

RDDISBV (Read Display Brightness Value)																									
52h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	0	1	0	52h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	DBV[7]	DBV[6]	DBV[5]	DBV[4]	DBV[3]	DBV[2]	DBV[1]	DBV[0]	00												
Description	<p>This command returns the brightness value of the display.</p> <p>It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p>																								
Restriction	<p>The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI Mode.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>DBV [7:0]</td> <td></td> </tr> <tr> <td>Power On Sequence</td> <td>8'h00h</td> </tr> <tr> <td>SW Reset</td> <td>8'h00h</td> </tr> <tr> <td>HW Reset</td> <td>8'h00h</td> </tr> </tbody> </table>													Status	Default Value	DBV [7:0]		Power On Sequence	8'h00h	SW Reset	8'h00h	HW Reset	8'h00h		
Status	Default Value																								
DBV [7:0]																									
Power On Sequence	8'h00h																								
SW Reset	8'h00h																								
HW Reset	8'h00h																								
Flow Chart	<pre> graph TD Start[Read RDDISBV] --> Send1[Send 1st Parameter] Send1 --> Send2[Send 2nd Parameter] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

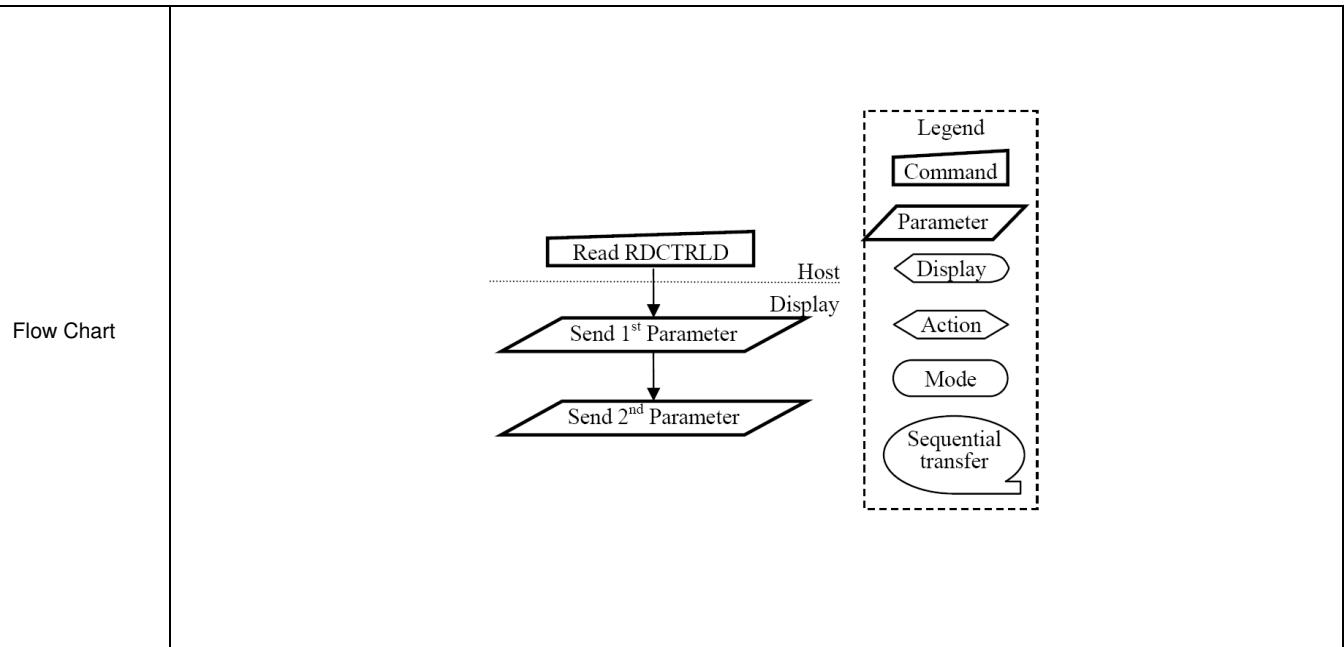
8.2.40. Write CTRL Display (53h)

WRCTRLD (Write Control Display)																																
53h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	0	1	0	1	0	0	1	1	53h																			
Parameter	1	1	↑	XX	0	0	BCTRL	0	DD	BL	0	0	00																			
Description	<p>This command is used to control display brightness.</p> <p>BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display.</p> <p>0 = Off (Brightness registers are 00h, DBV[7..0])</p> <p>1 = On (Brightness registers are active, according to the other parameters.)</p> <p>DD: Display Dimming, only for manual brightness setting</p> <p>DD = 0: Display Dimming is off</p> <p>DD = 1: Display Dimming is on</p> <p>BL: Backlight Control On/Off</p> <p>0 = Off (Completely turn off backlight circuit. Control lines must be low.)</p> <p>1 = On</p> <p>Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 → 1 or 1 → 0.</p> <p>When BL bit change from “On” to “Off”, backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected.</p>																															
Restriction	None																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																															
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Sleep In	Yes																															
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Status	Default Value																															
	BCTRL	DD	BL																													
Power On Sequence	1'b0	1'b0	1'b0																													
SW Reset	1'b0	1'b0	1'b0																													
HW Reset	1'b0	1'b0	1'b0																													

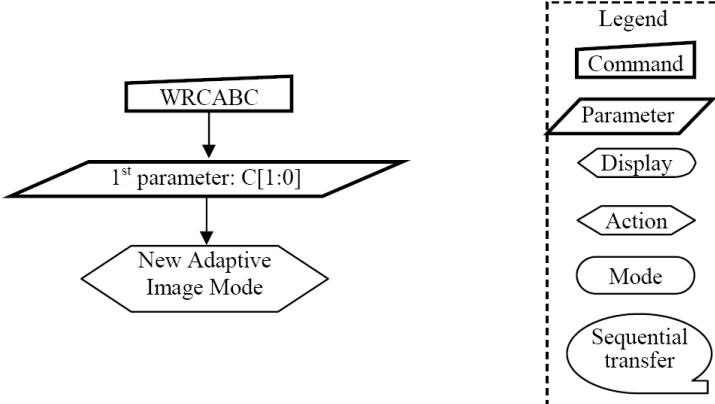


8.2.41. Read CTRL Display (54h)

RDCTRLD (Read Control Display)																																	
54h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	XX	0	1	0	1	0	1	0	0	54h																				
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX																				
2 nd Parameter	1	↑	1	XX	0	0	BCTRL	0	DD	BL	0	0	00																				
Description	<p>This command is used to return brightness setting.</p> <p>BCTRL: Brightness Control Block On/Off, '0' = Off (Brightness registers are 00h) '1' = On (Brightness registers are active, according to the DBV[7..0] parameters.)</p> <p>DD: Display Dimming '0' = Display Dimming is off '1' = Display Dimming is on</p> <p>BL: Backlight On/Off '0' = Off (Completely turn off backlight circuit. Control lines must be low.) '1' = On</p>																																
Restriction	<p>The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes							
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Normal Mode On, Idle Mode Off, Sleep Out	Yes																																
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Status	Default Value																																
	BCTRL	DD	BL																														
Power On Sequence	1'b0	1'b0	1'b0																														
SW Reset	1'b0	1'b0	1'b0																														
HW Reset	1'b0	1'b0	1'b0																														



8.2.42. Write Content Adaptive Brightness Control (55h)

55h		WRCABC (Write Content Adaptive Brightness Control)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	1	0	1	55h												
Parameter	1	1	↑	XX	0	0	0	0	0	0	C [1]	C [0]	00												
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1"> <tr> <th>C [1:0]</th><th>Default Value</th></tr> <tr> <td>2'b00</td><td>Off</td></tr> <tr> <td>2'b01</td><td>User Interface Image</td></tr> <tr> <td>2'b10</td><td>Still Picture</td></tr> <tr> <td>2'b11</td><td>Moving Image</td></tr> </table>													C [1:0]	Default Value	2'b00	Off	2'b01	User Interface Image	2'b10	Still Picture	2'b11	Moving Image		
C [1:0]	Default Value																								
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2'b10	Still Picture																								
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Restriction	None																								
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Status	Default Value																								
Power On Sequence	C [1:0]=00h																								
SW Reset	C [1:0]=00h																								
HW Reset	C [1:0]=00h																								
Flow Chart	 <pre> graph TD WRCABC[WRCABC] --> Param1[1st parameter: C[1:0]] Param1 --> ModeMode{New Adaptive Image Mode} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.43. Read Content Adaptive Brightness Control (56h)

RDCABC (Read Content Adaptive Brightness Control)																									
56h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	0	1	0	1	0	1	1	0	56h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	XX												
2 nd Parameter	1	↑	1	XX	0	0	0	0	0	0	C [1]	C [0]	00												
Description	<p>This command is used to read the settings for image content based adaptive brightness control functionality.</p> <p>It is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.</p> <table border="1"> <tr> <td>C [1:0]</td><td>Default Value</td></tr> <tr> <td>2'b00</td><td>Off</td></tr> <tr> <td>2'b01</td><td>User Interface Image</td></tr> <tr> <td>2'b10</td><td>Still Picture</td></tr> <tr> <td>2'b11</td><td>Moving Image</td></tr> </table>													C [1:0]	Default Value	2'b00	Off	2'b01	User Interface Image	2'b10	Still Picture	2'b11	Moving Image		
C [1:0]	Default Value																								
2'b00	Off																								
2'b01	User Interface Image																								
2'b10	Still Picture																								
2'b11	Moving Image																								
Restriction	<p>The display module is sending 2nd parameter value on the data lines if the MCU wants to read more than one parameter (= more than 2 RDX cycle) on DBI.</p> <p>Only 2nd parameter is sent on DSI (The 1st parameter is not sent).</p>																								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <tr> <th>Status</th><th>Default Value</th></tr> <tr> <td>Power On Sequence</td><td>C [1:0]=00h</td></tr> <tr> <td>SW Reset</td><td>C [1:0]=00h</td></tr> <tr> <td>HW Reset</td><td>C [1:0]=00h</td></tr> </table>													Status	Default Value	Power On Sequence	C [1:0]=00h	SW Reset	C [1:0]=00h	HW Reset	C [1:0]=00h				
Status	Default Value																								
Power On Sequence	C [1:0]=00h																								
SW Reset	C [1:0]=00h																								
HW Reset	C [1:0]=00h																								
Flow Chart	<pre> graph TD Host[Host] -- "Read RDCABC" --> Display[Display] Display -- "Send 1st Parameter" --> Host Display -- "Send 2nd Parameter" --> Host </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

8.2.44. Write CABC Minimum Brightness (5Eh)

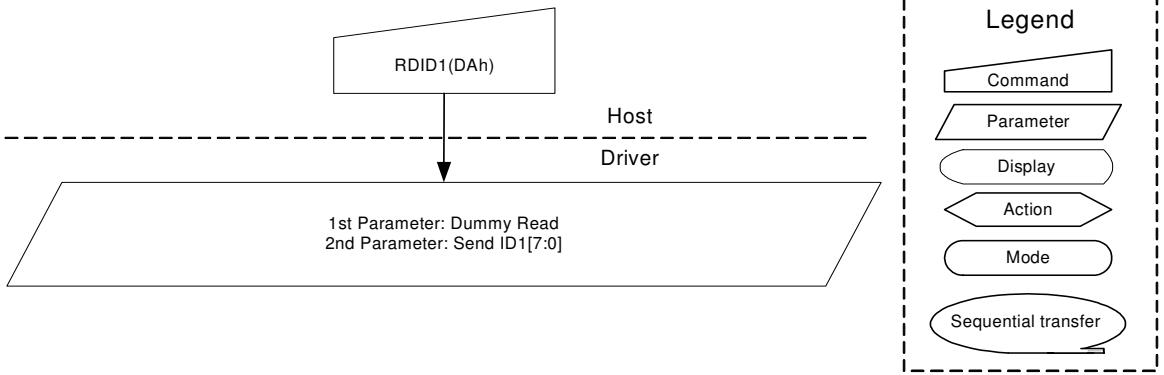
5Eh		Backlight Control 1												
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		0	1	↑	XX	0	1	0	1	1	1	1	0	5Eh
Parameter		1	1	↑	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]	00

Description	<p>This command is used to set the minimum brightness value of the display for CABC function.</p> <p>CMB[7:0]: CABC minimum brightness control, this parameter is used to avoid too much brightness reduction.</p> <p>When CABC is active, CABC cannot reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness cannot be changed.</p> <p>This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.</p> <p>When display brightness is turned off (BCTRL=0 of "Write CTRL Display (53h)", CABC minimum brightness setting is ignored.</p> <p>In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value																								
	CMB [7:0]																								
Power On Sequence	8'h00h																								
SW Reset	No Change																								
HW Reset	8'h00h																								

8.2.45. Read CABC Minimum Brightness (5Fh)

5Fh		Backlight Control 1																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	0	1	0	1	1	1	1	1	1	5Fh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	CMB [7]	CMB [6]	CMB [5]	CMB [4]	CMB [3]	CMB [2]	CMB [1]	CMB [0]		00												
Description	<p>This command returns the minimum brightness value of CABC function.</p> <p>In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness.</p> <p>CMB[7:0] is CABC minimum brightness specified with “Write CABC minimum brightness (5Eh)” command. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC.</p>																									
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Power On Sequence	8'h00h																									
SW Reset	No Change																									
HW Reset	8'h00h																									

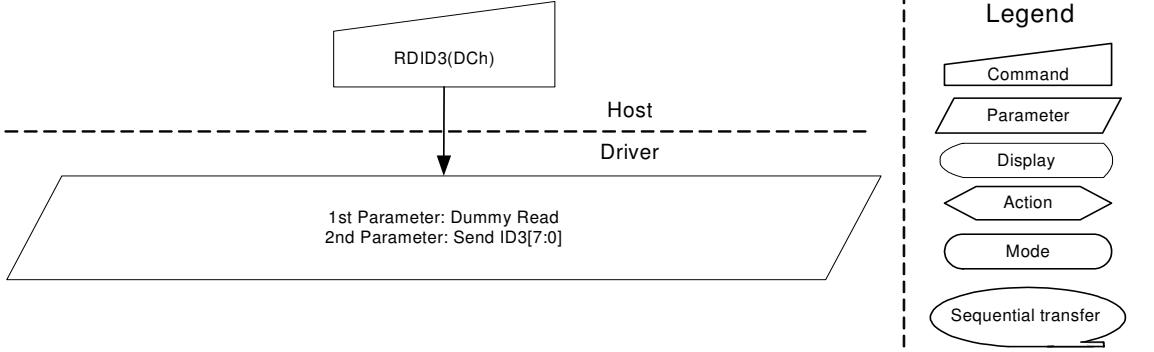
8.2.46. Read ID1 (DAh)

DAh	RDID1 (Read ID1)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	0	1	0	DAh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	ID1 [7:0]								00												
Description	<p>This read byte identifies the LCD module's manufacturer ID and it is specified by User</p> <p>The 1st parameter is dummy data.</p> <p>The 2nd parameter is LCD module's manufacturer ID.</p> <p>X = Don't care</p>																								
Restriction																									
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Status	Default Value (Before MTP program)	Default Value (After MTP program)																							
Power On Sequence	8'h00h	MTP value																							
SW Reset	8'h00h	MTP value																							
HW Reset	8'h00h	MTP value																							
Flow Chart	 <pre> graph TD RDID1["RDID1(DAh)"] --> Host[Host] Host --> Driver[Driver] subgraph Legend [Legend] direction TB C1[Command] --- P1[Parameter] P1 --- D1[Display] D1 --- A1[Action] A1 --- M1[Mode] M1 --- ST1[Sequential transfer] end subgraph Host [Host] direction TB P1_1[1st Parameter: Dummy Read] P2_1[2nd Parameter: Send ID1[7:0]] end subgraph Driver [Driver] direction TB P1_2[1st Parameter: Dummy Read] P2_2[2nd Parameter: Send ID1[7:0]] end </pre>																								

8.2.47. Read ID2 (DBh)

DBh	RDID2 (Read ID2)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	0	1	1	DBh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	ID2 [7:0]								00												
Description	<p>This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications.</p> <p>The 1st parameter is dummy data.</p> <p>The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.</p> <p>The ID2 can be programmed by MTP function.</p> <p>X = Don't care</p>																								
Restriction																									
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Status	Default Value (Before MTP program)	Default Value (After MTP program)																							
Power On Sequence	8'h80h	MTP value																							
SW Reset	8'h80h	MTP value																							
HW Reset	8'h80h	MTP value																							
Flow Chart	<p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer <p>1st Parameter: Dummy Read 2nd Parameter: Send ID2[7:0]</p>																								

8.2.48. Read ID3 (DCh)

RDID3 (Read ID3)																									
DCh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	1	1	0	0	DCh												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	ID3 [7:0]								00												
Description	This read byte identifies the LCD module/driver and It is specified by User. The 1 st parameter is dummy data. The 2 nd parameter is LCD module/driver ID. The ID3 can be programmed by MTP function. X = Don't care																								
Restriction																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes
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Status	Default Value (Before MTP program)	Default Value (After MTP program)																							
Power On Sequence	8'h00h	MTP value																							
SW Reset	8'h00h	MTP value																							
HW Reset	8'h00h	MTP value																							
Flow Chart	 <p>The flowchart illustrates the communication sequence. It starts with a rectangular box labeled "RDID3(DCh)" representing a command. An arrow points from this box down to a dashed horizontal line separating the "Host" from the "Driver". Below the line, a trapezoidal box contains the text "1st Parameter: Dummy Read" and "2nd Parameter: Send ID3[7:0]". To the right of the driver, a legend provides key symbols: a rectangle for "Command", a trapezoid for "Parameter", an oval for "Display", a diamond for "Action", a hexagon for "Mode", and an elliptical arrow for "Sequential transfer".</p>																								

8.3. Description of Level 2 Command

8.3.1. RGB Interface Signal Control (B0h)

B0h		IFMODE (Interface Mode Control)																																														
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																		
Command		0	1	↑	XX	1	0	1	1	0	0	0	0	B0h																																		
Parameter		1	1	↑	XX	ByPass_MODE	RCM [1]	RCM [0]	0	VSPL	HSPL	DPL	EPL	40																																		
Description	Sets the operation status of the display interface. The setting becomes effective as soon as the command is received. EPL: DE polarity ("0"= High enable for RGB interface, "1"= Low enable for RGB interface) DPL: DOTCLK polarity set ("0"= data fetched at the rising time, "1"= data fetched at the falling time) HSPL: HSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) VSPL: VSYNC polarity ("0"= Low level sync clock, "1"= High level sync clock) RCM [1:0]: RGB interface selection (refer to the RGB interface section). ByPass_MODE: Select display data path whether Memory or Direct to Shift register when RGB Interface is used.																																															
Restriction	EXTC should be high to enable this command																																															
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Status	Default Value																																															
	ByPass_MODE	RCM [1:0]	VSPL	HSPL	DPL	EPL																																										
Power ON Sequence	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1																																										
SW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1																																										
HW Reset	1'b0	2'b10	1'b0	1'b0	1'b0	1'b1																																										

8.3.2. Frame Rate Control (In Normal Mode/Full Colors) (B1h)

B1h	FRMCTR1 (Frame Rate Control (In Normal Mode / Full colors))													
	D/CX	RDX	WRX	D17-8		D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX		1	0	1	1	0	0	0	1	B1h
1 st Parameter	1	1	↑	XX		0	0	0	0	0	0	DIVA [1:0]	00	
2 nd Parameter	1	1	↑	XX		0	0	0	RTNA [4:0]					1B

Formula to calculate frame frequency:

$$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$$

Sets the division ratio for internal clocks of Normal mode at MCU interface.

fosc : internal oscillator frequency

Clocks per line : RTNA setting

Division ratio : DIVA setting

Lines : total driving line number

VBP : back porch line number

VFP : front porch line number

RTNA [4:0]					Frame Rate (Hz)
1	0	0	0	0	119
1	0	0	0	1	112
1	0	0	1	0	106
1	0	0	1	1	100
1	0	1	0	0	95
1	0	1	0	1	90
1	0	1	1	0	86
1	0	1	1	1	83

RTNA [4:0]					Frame Rate (Hz)
1	1	0	0	0	79
1	1	0	0	1	76
1	1	0	1	0	73
1	1	0	1	1	70(default)
1	1	1	0	0	68
1	1	1	0	1	65
1	1	1	0	1	63
1	1	1	1	1	61

DIVA [1:0] : division ratio for internal clocks when Normal mode.

DIVA [1:0]		Division Ratio
0	0	fosc
0	1	fosc / 2
1	0	fosc / 4
1	1	fosc / 8

RTNA [4:0] : RTNA[4:0] is used to set 1H (line) period of Normal mode at MCU interface.

RTNA [4:0]					Clock per Line	RTNA [4:0]					Clock per Line	RTNA [4:0]					Clock per Line
0	0	0	0	0	Setting prohibited	0	1	0	1	1	Setting prohibited	1	0	1	1	0	22 clocks
0	0	0	0	1	Setting prohibited	0	1	1	0	0	Setting prohibited	1	0	1	1	1	23 clocks
0	0	0	1	0	Setting prohibited	0	1	1	0	1	Setting prohibited	1	1	0	0	0	24 clocks
0	0	0	1	1	Setting prohibited	0	1	1	1	0	Setting prohibited	1	1	0	0	1	25 clocks
0	0	1	0	0	Setting prohibited	0	1	1	1	1	Setting prohibited	1	1	0	1	0	26 clocks
0	0	1	0	1	Setting prohibited	1	0	0	0	0	16 clocks	1	1	0	1	1	27 clocks
0	0	1	1	0	Setting prohibited	1	0	0	0	1	17 clocks	1	1	1	0	0	28 clocks
0	0	1	1	1	Setting prohibited	1	0	0	1	0	18 clocks	1	1	1	0	1	29 clocks
0	1	0	0	0	Setting prohibited	1	0	0	1	1	19 clocks	1	1	1	1	0	30 clocks
0	1	0	0	1	Setting prohibited	1	0	1	0	0	20 clocks	1	1	1	1	1	31 clocks
0	1	0	1	0	Setting prohibited	1	0	1	0	1	21 clocks						

Restriction	EXTC should be high to enable this command															
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes															
Sleep IN	Yes															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>DIVA [1:0]</th><th>RTNA [4:0]</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>2'b00</td><td>5'h1Bh</td></tr> <tr> <td>SW Reset</td><td>2'b00</td><td>5'h1Bh</td></tr> <tr> <td>HW Reset</td><td>2'b00</td><td>5'h1Bh</td></tr> </tbody> </table>	Status	Default Value		DIVA [1:0]	RTNA [4:0]	Power ON Sequence	2'b00	5'h1Bh	SW Reset	2'b00	5'h1Bh	HW Reset	2'b00	5'h1Bh	
Status	Default Value															
	DIVA [1:0]	RTNA [4:0]														
Power ON Sequence	2'b00	5'h1Bh														
SW Reset	2'b00	5'h1Bh														
HW Reset	2'b00	5'h1Bh														

8.3.3. Frame Rate Control (In Idle Mode/8 colors) (B2h)

B2h	FRMCTR2 (Frame Rate Control (In Idle Mode / 8I colors))																																			
	D/CX	RDX	WRX	D17-8		D7	D6	D5	D4	D3	D2	D1	D0	HEX																						
Command	0	1	↑	XX		1	0	1	1	0	0	1	0	B2h																						
1 st Parameter	1	1	↑	XX		0	0	0	0	0	0	0	DIVB [1:0]	00																						
2 nd Parameter	1	1	↑	XX		0	0	0	RTNB [4:0]					1B																						
Description	Formula to calculate frame frequency																																			
	Frame Rate = $\frac{fosc}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$																																			
	Sets the division ratio for internal clocks of Idle mode at MCU interface.																																			
	fosc : internal oscillator frequency																																			
	Clocks per line : RTNB setting																																			
	Division ratio : DIVB setting																																			
	Lines : total driving line number																																			
	VBP : back porch line number																																			
	VFP : front porch line number																																			
	RTNB [4:0]				Frame Rate (Hz)																															
					1 0 0 0 0	119																														
					1 0 0 0 1	112																														
					1 0 0 1 0	106																														
					1 0 0 1 1	100																														
					1 0 1 0 0	95																														
					1 0 1 0 1	90																														
					1 0 1 1 0	86																														
					1 0 1 1 1	83																														
RTNB [4:0]													Frame Rate (Hz)																							
					1 1 0 0 0	79																														
					1 1 0 0 1	76																														
					1 1 0 1 0	73																														
					1 1 0 1 1	70(default)																														
					1 1 1 0 0	68																														
					1 1 1 0 1	65																														
					1 1 1 0 1	63																														
					1 1 1 1 1	61																														
DIVB [1:0]: division ratio for internal clocks when Idle mode.																																				
<table border="1"> <thead> <tr> <th>DIVB [1:0]</th> <th>Division Ratio</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>fosc</td> </tr> <tr> <td>0 1</td> <td>fosc / 2</td> </tr> <tr> <td>1 0</td> <td>fosc / 4</td> </tr> <tr> <td>1 1</td> <td>fosc / 8</td> </tr> </tbody> </table>													DIVB [1:0]	Division Ratio	0 0	fosc	0 1	fosc / 2	1 0	fosc / 4	1 1	fosc / 8														
DIVB [1:0]	Division Ratio																																			
0 0	fosc																																			
0 1	fosc / 2																																			
1 0	fosc / 4																																			
1 1	fosc / 8																																			
RTNB [4:0]: RTNB[4:0] is used to set 1H (line) period of Idle mode at MCU interface.																																				
RTNB [4:0]				Clock per Line																																
					0 1 0 1 1	Setting prohibited																														
					0 1 1 0 0	Setting prohibited																														
					0 1 1 0 1	Setting prohibited																														
					0 1 1 1 0	Setting prohibited																														
					0 1 1 1 1	Setting prohibited																														
					1 0 0 0 0	16 clocks																														
					1 0 0 0 1	17 clocks																														
					1 0 0 1 0	18 clocks																														
					1 0 0 1 1	19 clocks																														
					1 0 1 0 0	20 clocks																														
					1 0 1 0 1	21 clocks																														
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RTNB [4:0]	Clock per Line																																			
1 0 1 1 0	22 clocks																																			
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1 1 1 1 0	30 clocks																																			
1 1 1 1 1	31 clocks																																			

Restriction	EXTC should be high to enable this command															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes			
Status	Availability															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes															
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes															
Sleep IN	Yes															
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Status	Default Value															
	DIVB [1:0]	RTNB [4:0]														
Power ON Sequence	2'b00	5'h1Bh														
SW Reset	2'b00	5'h1Bh														
HW Reset	2'b00	5'h1Bh														

8.3.4. Frame Rate control (In Partial Mode/Full Colors) (B3h)

B3h	FRMCTR3 (Frame Rate Control (In Partial Mode / Full colors))																																																																																																																																																											
	D/CX	RDX	WRX	D17-8		D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																														
Command	0	1	↑	XX		1	0	1	1	0	0	1	1	B3h																																																																																																																																														
1 st Parameter	1	1	↑	XX		0	0	0	0	0	0	DIVC [1:0]		00																																																																																																																																														
2 nd Parameter	1	1	↑	XX		0	0	0	RTNC [4:0]					1B																																																																																																																																														
Description	Formula to calculate frame frequency:																																																																																																																																																											
	$\text{Frame Rate} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{Division ratio} \times (\text{Lines} + \text{VBP} + \text{VFP})}$																																																																																																																																																											
	Sets the division ratio for internal clocks of Partial mode (Idle mode off) at MCU interface.																																																																																																																																																											
	fosc : internal oscillator frequency																																																																																																																																																											
	Clocks per line : RTNC setting																																																																																																																																																											
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<table border="1"> <thead> <tr> <th colspan="5">RTNC [4:0]</th> <th>Clock per Line</th> </tr> </thead> <tbody> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>Setting prohibited</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Setting prohibited</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>Setting prohibited</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>Setting prohibited</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>Setting prohibited</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>16 clocks</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>17 clocks</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>18 clocks</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>19 clocks</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>20 clocks</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>21 clocks</td></tr> </tbody> </table>													RTNC [4:0]					Clock per Line	0	1	0	1	1	Setting prohibited	0	1	1	0	0	Setting prohibited	0	1	1	0	1	Setting prohibited	0	1	1	1	0	Setting prohibited	0	1	1	1	1	Setting prohibited	1	0	0	0	0	16 clocks	1	0	0	0	1	17 clocks	1	0	0	1	0	18 clocks	1	0	0	1	1	19 clocks	1	0	1	0	0	20 clocks	1	0	1	0	1	21 clocks																																																																								
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Restriction	EXTC should be high to enable this command														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes			
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Status	Default Value														
	DIVC [1:0]	RTNC [4:0]													
Power ON Sequence	2'b00	5'h1Bh													
SW Reset	2'b00	5'h1Bh													
HW Reset	2'b00	5'h1Bh													

8.3.5. Display Inversion Control (B4h)

B4h		INVTR (Display Inversion Control)																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	0	1	1	0	1	0	0	B4h																			
1 st Parameter	1	1	↑	XX	0	0	0	0	0	NLA	NLB	NLC	02																			
Description	Display inversion mode set NLA: Inversion setting in full colors normal mode (Normal mode on) NLB: Inversion setting in Idle mode (Idle mode on) NLC: Inversion setting in full colors partial mode (Partial mode on / Idle mode off) <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>NLA / NLB / NLC</th> <th>Inversion</th> </tr> <tr> <td>0</td> <td>Line inversion</td> </tr> <tr> <td>1</td> <td>Frame inversion</td> </tr> </table>													NLA / NLB / NLC	Inversion	0	Line inversion	1	Frame inversion													
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1	Frame inversion																															
Restriction	EXTC should be high to enable this command																															
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Status		Availability																														
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Status	Default Value																															
	NLA	NLB	NLC																													
Power ON Sequence	1'b0	1'b1	1'b0																													
SW Reset	1'b0	1'b1	1'b0																													
H/W Reset	1'b0	1'b1	1'b0																													

8.3.6. Blanking Porch Control (B5h)

B5h	PRCTR (Blanking Porch)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	XX	1	0	1	1	0	1	0	1	B5h											
1 st Parameter	1	1	↑	XX	0				VFP [6:0]				02											
2 nd Parameter	1	1	↑	XX	0				VBP [6:0]				02											
3 rd Parameter	1	1	↑	XX	0	0	0		HFP [4:0]				0A											
4 th Parameter	1	1	↑	XX	0	0	0		HBP [4:0]				14											
Description	VFP [6:0] / VBP [6:0]: The VFP [6:0] and VBP [6:0] bits specify the line number of vertical front and back porch period respectively.																							
	VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch				VFP [6:0] VBP [6:0]	Number of HSYNC of front/back porch																	
	0000000	Setting inhibited				1000000	64																	
	0000001	Setting inhibited				1000001	65																	
	0000010	2				1000010	66																	
	0000011	3				1000011	67																	
	0000100	4				1000100	68																	
	0000101	5				1000101	69																	
	0000110	6				1000110	70																	
	0000111	7				1000111	71																	
	0001000	8				1001000	72																	
	0001001	9				1001001	73																	
	0001010	10				1001010	74																	
	0001011	11				1001011	75																	
	0001100	12				1001100	76																	
	0001101	13				1001101	77																	
	:	:				:	:																	
	0111101	61				1111101	125																	
	0111110	62				1111110	126																	
	0111111	63				1111111	127																	
<i>Note: VFP + VBP ≤ 254 HSYNC signals</i>																								
Description	HFP [4:0] / HBP [4:0]: The HFP [4:0] and HBP [4:0] bits specify the line number of horizontal front and back porch period respectively.																							
	HFP [4:0] HBP [4:0]	Number of DOTCLK of the front/back porch				HFP [4:0] HBP [4:0]	Number of DOTCLK of front/back porch																	
	00000	Setting prohibited				10000	16																	
	00001	Setting prohibited				10001	17																	
	00010	2				10010	18																	
	00011	3				10011	19																	
	00100	4				10100	20																	
	00101	5				10101	21																	
	00110	6				10110	22																	
	00111	7				10111	23																	
	01000	8				11000	24																	
	01001	9				11001	25																	
	01010	10				11010	26																	
	01011	11				11011	27																	
	01100	12				11100	28																	
	01101	13				11101	29																	
	01110	14				11110	30																	
	01111	15				11111	31																	

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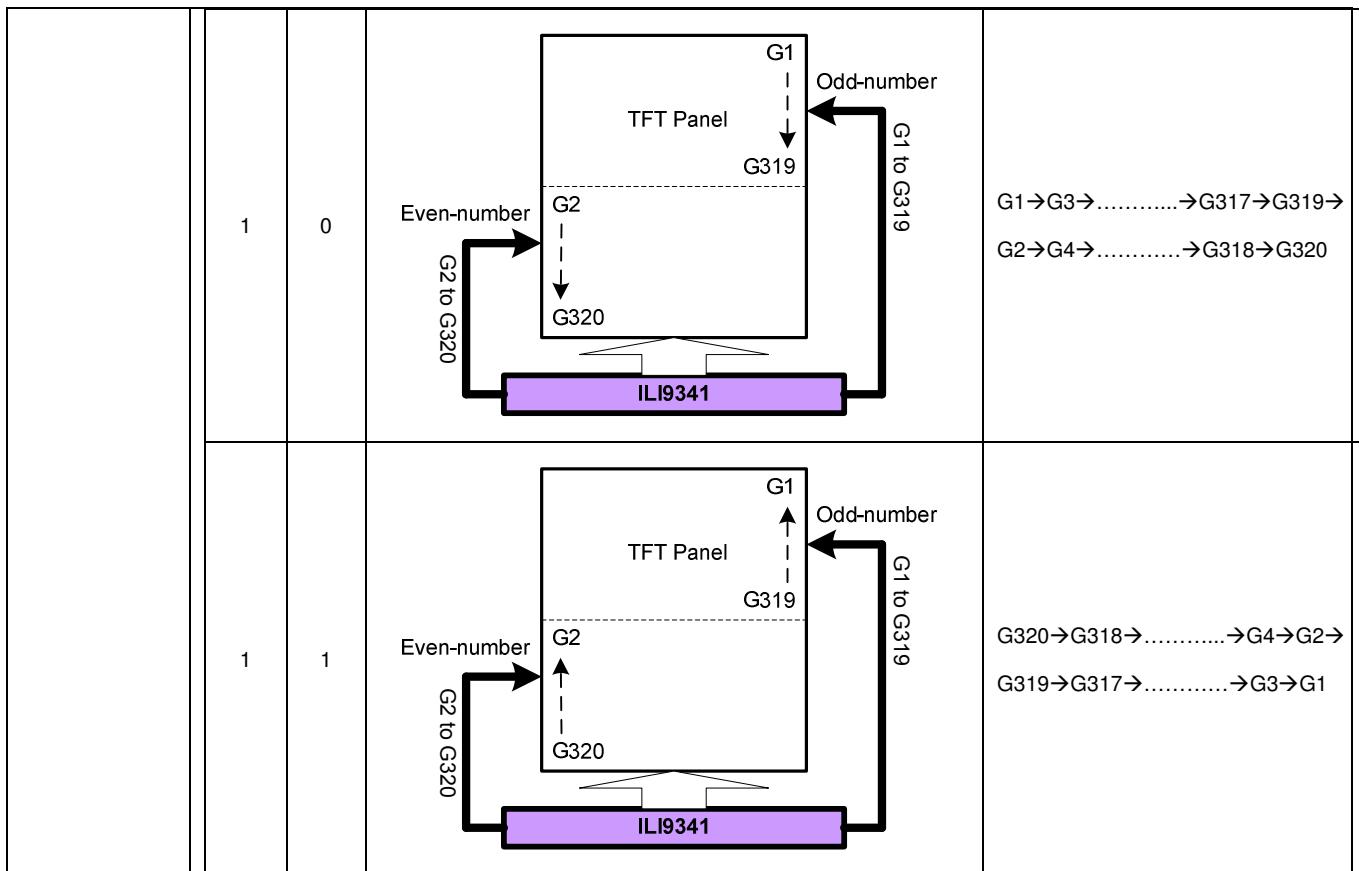
Restriction	EXTC should be high to enable this command																											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>				Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes												
Status	Availability																											
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Status	Default Value																											
	VFP [6:0]	VBP [6:0]	HFP [4:0]	HBP [4:0]																								
Power ON Sequence	7'h02h	7'h02h	5'h0Ah	5'h14h																								
SW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h																								
HW Reset	7'h02h	7'h02h	5'h0Ah	5'h14h																								

8.3.7. Display Function Control (B6h)

B6h	DISCTRL (Display Function Control)																																																																													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																	
Command	0	1	↑	XX	1	0	1	1	0	1	1	0	B6h																																																																	
1 st Parameter	1	1	↑	XX	0	0	0	0	PTG [1:0]		PT [1:0]		0A																																																																	
2 nd Parameter	1	1	↑	XX	REV	GS	SS	SM		ISC [3:0]			82																																																																	
3 rd Parameter	1	1	↑	XX	0	0			NL [5:0]				27																																																																	
4 th Parameter	1	1	↑	XX	0	0			PCDIV [5:0]				XX																																																																	
Description	PTG [1:0]: Set the scan mode in non-display area. <table border="1"> <tr> <th>PTG1</th> <th>PTG0</th> <th>Gate outputs in non-display area</th> <th>Source outputs in non-display area</th> <th>VCOM output</th> </tr> <tr> <td>0</td> <td>0</td> <td>Normal scan</td> <td>Set with the PT [2:0] bits</td> <td>VCOMH/VCOML</td> </tr> <tr> <td>0</td> <td>1</td> <td>Setting prohibited</td> <td>---</td> <td>---</td> </tr> <tr> <td>1</td> <td>0</td> <td>Interval scan</td> <td>Set with the PT [2:0] bits</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Setting prohibited</td> <td>---</td> <td>---</td> </tr> </table> PT [1:0]: Determine source/VCOM output in a non-display area in the partial display mode. <table border="1"> <tr> <th colspan="2" rowspan="2">PT [1:0]</th> <th colspan="2">Source output on non-display area</th> <th colspan="2">VCOM output on non-display area</th> </tr> <tr> <th>Positive polarity</th> <th>Negative polarity</th> <th>Positive polarity</th> <th>Negative polarity</th> </tr> <tr> <td>0</td> <td>0</td> <td>V63</td> <td>V0</td> <td>VCOML</td> <td>VCOMH</td> </tr> <tr> <td>0</td> <td>1</td> <td>V0</td> <td>V63</td> <td>VCOML</td> <td>VCOMH</td> </tr> <tr> <td>1</td> <td>0</td> <td>AGND</td> <td>AGND</td> <td>AGND</td> <td>AGND</td> </tr> <tr> <td>1</td> <td>1</td> <td>Hi-Z</td> <td>Hi-Z</td> <td>AGND</td> <td>AGND</td> </tr> </table> SS: Select the shift direction of outputs from the source driver. <table border="1"> <tr> <th>SS</th> <th>Source Output Scan Direction</th> </tr> <tr> <td>0</td> <td>S1 → S720</td> </tr> <tr> <td>1</td> <td>S720 → S1</td> </tr> </table> In addition to the shift direction, the settings for both SS and BGR bits are required to change the assignment of R, G, and B dots to the source driver pins. To assign R, G, B dots to the source driver pins from S1 to S720, set SS = 0. To assign R, G, B dots to the source driver pins from S720 to S1, set SS = 1.													PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output	0	0	Normal scan	Set with the PT [2:0] bits	VCOMH/VCOML	0	1	Setting prohibited	---	---	1	0	Interval scan	Set with the PT [2:0] bits		1	1	Setting prohibited	---	---	PT [1:0]		Source output on non-display area		VCOM output on non-display area		Positive polarity	Negative polarity	Positive polarity	Negative polarity	0	0	V63	V0	VCOML	VCOMH	0	1	V0	V63	VCOML	VCOMH	1	0	AGND	AGND	AGND	AGND	1	1	Hi-Z	Hi-Z	AGND	AGND	SS	Source Output Scan Direction	0	S1 → S720	1	S720 → S1
PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	VCOM output																																																																										
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PT [1:0]		Source output on non-display area		VCOM output on non-display area																																																																										
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REV: Select whether the liquid crystal type is normally white type or normally black type. <table border="1"> <tr> <th>REV</th> <th>Liquid crystal type</th> </tr> <tr> <td>0</td> <td>Normally black</td> </tr> <tr> <td>1</td> <td>Normally white</td> </tr> </table> ISC [3:0]: Specify the scan cycle interval of gate driver in non-display area when PTG [1:0] = "10" to select interval scan. Then scan cycle is set as odd number from 0~29 frame periods. The polarity is inverted every scan cycle.													REV	Liquid crystal type	0	Normally black	1	Normally white																																																												
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<table border="1"> <tr> <th>ISC [3:0]</th> <th>Scan Cycle</th> <th>f_{FLM} = 60Hz</th> </tr> <tr> <td>0000</td> <td>1 frame</td> <td>17ms</td> </tr> <tr> <td>0001</td> <td>3 frames</td> <td>51ms</td> </tr> <tr> <td>0010</td> <td>5 frames</td> <td>85ms</td> </tr> <tr> <td>0011</td> <td>7 frames</td> <td>119ms</td> </tr> <tr> <td>0100</td> <td>9 frames</td> <td>153ms</td> </tr> <tr> <td>0101</td> <td>11 frames</td> <td>187ms</td> </tr> <tr> <td>0110</td> <td>13 frames</td> <td>221ms</td> </tr> <tr> <td>0111</td> <td>15 frames</td> <td>255ms</td> </tr> </table>													ISC [3:0]	Scan Cycle	f _{FLM} = 60Hz	0000	1 frame	17ms	0001	3 frames	51ms	0010	5 frames	85ms	0011	7 frames	119ms	0100	9 frames	153ms	0101	11 frames	187ms	0110	13 frames	221ms	0111	15 frames	255ms																																							
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		<table border="1"> <tr><td>1000</td><td>17 frames</td><td>289ms</td></tr> <tr><td>1001</td><td>19 frames</td><td>323ms</td></tr> <tr><td>1010</td><td>21 frames</td><td>357ms</td></tr> <tr><td>1011</td><td>23 frames</td><td>391ms</td></tr> <tr><td>1100</td><td>25 frames</td><td>425ms</td></tr> <tr><td>1101</td><td>27 frames</td><td>459ms</td></tr> <tr><td>1110</td><td>29 frames</td><td>493ms</td></tr> <tr><td>1111</td><td>31 frames</td><td>527ms</td></tr> </table>	1000	17 frames	289ms	1001	19 frames	323ms	1010	21 frames	357ms	1011	23 frames	391ms	1100	25 frames	425ms	1101	27 frames	459ms	1110	29 frames	493ms	1111	31 frames	527ms	
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1110	29 frames	493ms																									
1111	31 frames	527ms																									
		<p>GS: Sets the direction of scan by the gate driver in the range determined by SCN [4:0] and NL [4:0]. The scan direction determined by GS = 0 can be reversed by setting GS = 1.</p> <table border="1"> <tr><td>GS</td><td>Gate Output Scan Direction</td></tr> <tr><td>0</td><td>G1 → G320</td></tr> <tr><td>1</td><td>G320 → G1</td></tr> </table>	GS	Gate Output Scan Direction	0	G1 → G320	1	G320 → G1																			
GS	Gate Output Scan Direction																										
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1	G320 → G1																										
		<p>SM: Sets the gate driver pin arrangement in combination with the GS bit to select the optimal scan mode for the module.</p> <table border="1"> <thead> <tr> <th>SM</th><th>GS</th><th>Scan Direction</th><th>Gate Output Sequence</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td> <p>Even-number G2 to G320</p> <p>TFT Panel</p> <p>G2, G4, G1, G3</p> <p>G318, G317, G319, G320</p> <p>G1 to G319</p> </td><td> <p>G1→G2→G3→G4→.....→G317→G318→G319→G320</p> </td></tr> <tr> <td>0</td><td>1</td><td> <p>Even-number G2 to G320</p> <p>TFT Panel</p> <p>G2, G4, G1, G3</p> <p>G318, G317, G319, G320</p> <p>G1 to G319</p> </td><td> <p>G320→G319→G318→G317→.....→G4→G3→G2→G1</p> </td></tr> </tbody> </table>	SM	GS	Scan Direction	Gate Output Sequence	0	0	<p>Even-number G2 to G320</p> <p>TFT Panel</p> <p>G2, G4, G1, G3</p> <p>G318, G317, G319, G320</p> <p>G1 to G319</p>	<p>G1→G2→G3→G4→.....→G317→G318→G319→G320</p>	0	1	<p>Even-number G2 to G320</p> <p>TFT Panel</p> <p>G2, G4, G1, G3</p> <p>G318, G317, G319, G320</p> <p>G1 to G319</p>	<p>G320→G319→G318→G317→.....→G4→G3→G2→G1</p>													
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NL [5:0]: Sets the number of lines to drive the LCD at an interval of 8 lines. The GRAM address mapping is not affected by the number of lines set by NL [5:0]. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.

NL [5:0]						LCD Drive Line
0	0	0	0	0	0	Setting prohibited
0	0	0	0	0	1	16 lines
0	0	0	0	1	0	24 lines
0	0	0	0	1	1	32 lines
0	0	0	1	0	0	40 lines
0	0	0	1	0	1	48 lines
0	0	0	1	1	0	56 lines
0	0	0	1	1	1	64 lines
0	0	1	0	0	0	72 lines
0	0	1	0	0	1	80 lines
0	0	1	0	1	0	88 lines
0	0	1	0	1	1	96 lines
0	0	1	1	0	0	104 lines
0	0	1	1	0	1	112 lines
0	0	1	1	1	0	120 lines
0	0	1	1	1	1	128 lines
0	1	0	0	0	0	136 lines
0	1	0	0	0	1	144 lines
0	1	0	0	1	0	152 lines
0	1	0	0	1	1	160 lines
0	1	0	1	0	0	168 lines

NL [5:0]						LCD Driver Line
0	1	0	1	0	1	176 lines
0	1	0	1	1	0	184 lines
0	1	0	1	1	1	192 lines
0	1	1	0	0	0	200 lines
0	1	1	0	0	1	208 lines
0	1	1	0	1	0	216 lines
0	1	1	0	1	1	224 lines
0	1	1	1	0	0	232 lines
0	1	1	1	0	1	240 lines
0	1	1	1	1	0	248 lines
0	1	1	1	1	1	256 lines
1	0	0	0	0	0	264 lines
1	0	0	0	0	1	272 lines
1	0	0	0	1	0	280 lines
1	0	0	0	1	1	288 lines
1	0	0	1	0	0	296 lines
1	0	0	1	0	1	304 lines
1	0	0	1	1	0	312 lines
1	0	0	1	1	1	320 lines
Others						Setting inhibited

PCDIV [5:0]:

	$\text{external fosc} = \frac{\text{DOTCLK}}{2 \times (\text{PCDIV} + 1)}$																																												
Restriction	EXTC should be high to enable this command																																												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse; text-align: center;"> <thead> <tr> <th style="background-color: #cccccc;">Status</th> <th style="background-color: #cccccc;">Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes																																
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SW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h																																					
HW Reset	2'b10	2'b10	1'b1	1'b0	1'b0	1'b0	4'b0010	6'h27h																																					

8.3.8. Entry Mode Set (B7h)

B7h		ETMOD (Entry Mode Set)																																						
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																											
Command	0	1	↑	XX	1	0	1	1	0	1	1	1	B7h																											
Parameter	1	1	↑	XX	0	0	0	0	0	GON	DTE	GAS	06																											
GAS: Low voltage detection control.																																								
Description	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="padding: 2px;">GAS</td><td style="padding: 2px;">Low voltage detection</td></tr> <tr> <td style="padding: 2px;">0</td><td style="padding: 2px;">Enable</td></tr> <tr> <td style="padding: 2px;">1</td><td style="padding: 2px;">Disable</td></tr> </table>														GAS	Low voltage detection	0	Enable	1	Disable																				
GAS	Low voltage detection																																							
0	Enable																																							
1	Disable																																							
GON/DTE: Set the output level of gate driver G1 ~ G320 as follows																																								
Restriction	EXTC should be high to enable this command																																							
	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th colspan="3" style="background-color: #cccccc;">Status</th> <th colspan="2" style="background-color: #cccccc;">Availability</th> </tr> <tr> <td colspan="3">Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="3">Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="3">Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="3">Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td colspan="2">Yes</td> </tr> <tr> <td colspan="3">Sleep IN</td> <td colspan="2">Yes</td> </tr> </table>											Status			Availability		Normal Mode ON, Idle Mode OFF, Sleep OUT			Yes		Normal Mode ON, Idle Mode ON, Sleep OUT			Yes		Partial Mode ON, Idle Mode OFF, Sleep OUT			Yes		Partial Mode ON, Idle Mode ON, Sleep OUT			Yes		Sleep IN			Yes
Status			Availability																																					
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Sleep IN			Yes																																					
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th rowspan="2" style="width: 15%;">Status</th> <th colspan="3" style="background-color: #cccccc;">Default Value</th> </tr> <tr> <th>GON</th> <th>DTE</th> <th>GAS</th> </tr> <tr> <td>Power ON Sequence</td> <td>1'b1</td> <td>1'b1</td> <td>1'b0</td> </tr> <tr> <td>SW Reset</td> <td>1'b1</td> <td>1'b1</td> <td>1'b0</td> </tr> <tr> <td>HW Reset</td> <td>1'b1</td> <td>1'b1</td> <td>1'b0</td> </tr> </table>														Status	Default Value			GON	DTE	GAS	Power ON Sequence	1'b1	1'b1	1'b0	SW Reset	1'b1	1'b1	1'b0	HW Reset	1'b1	1'b1	1'b0							
Status	Default Value																																							
	GON	DTE	GAS																																					
Power ON Sequence	1'b1	1'b1	1'b0																																					
SW Reset	1'b1	1'b1	1'b0																																					
HW Reset	1'b1	1'b1	1'b0																																					

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8.3.9. Backlight Control 1 (B8h)

B8h		Backlight Control 1																																																
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																					
Command	0	1	↑	XX	1	0	1	1	1	0	0	0	B8h																																					
Parameter		1	↑	XX	0	0	0	0	TH_UI [3]	TH_UI [2]	TH_UI [1]	TH_UI [0]	0C																																					
		<p>TH_UI [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the user interface (UI) mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.</p> <table border="1"> <thead> <tr> <th>TH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>4'0h</td> <td>99%</td> </tr> <tr> <td>4'1h</td> <td>98%</td> </tr> <tr> <td>4'2h</td> <td>96%</td> </tr> <tr> <td>4'3h</td> <td>94%</td> </tr> <tr> <td>4'4h</td> <td>92%</td> </tr> <tr> <td>4'5h</td> <td>90%</td> </tr> <tr> <td>4'6h</td> <td>88%</td> </tr> <tr> <td>4'7h</td> <td>86%</td> </tr> </tbody> </table> <table border="1"> <thead> <tr> <th>TH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>4'8h</td> <td>84%</td> </tr> <tr> <td>4'9h</td> <td>82%</td> </tr> <tr> <td>4'Ah</td> <td>80%</td> </tr> <tr> <td>4'Bh</td> <td>78%</td> </tr> <tr> <td>4'Ch</td> <td>76%</td> </tr> <tr> <td>4'Dh</td> <td>74%</td> </tr> <tr> <td>4'Eh</td> <td>72%</td> </tr> <tr> <td>4'Fh</td> <td>70%</td> </tr> </tbody> </table>													TH_UI [3:0]	Description	4'0h	99%	4'1h	98%	4'2h	96%	4'3h	94%	4'4h	92%	4'5h	90%	4'6h	88%	4'7h	86%	TH_UI [3:0]	Description	4'8h	84%	4'9h	82%	4'Ah	80%	4'Bh	78%	4'Ch	76%	4'Dh	74%	4'Eh	72%	4'Fh	70%
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Status	Default Value																																																	
TH_UI [3:0]																																																		
Power On Sequence	4'b0110																																																	
SW Reset	No change																																																	
HW Reset	4'b0110																																																	

8.3.10. Backlight Control 2 (B9h)

B9h		Backlight Control 2											
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	0	1	1	1	0	0	1	B9h
Parameter	1	1	↑	XX	TH_MV [3]	TH_MV [2]	TH_MV [1]	TH_MV [0]	TH_ST [3]	TH_ST [2]	TH_ST [1]	TH_ST [0]	CC

TH_ST [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the still picture mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_ST [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_ST [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

TH_MV [3:0]: These bits are used to set the percentage of grayscale data accumulate histogram value in the moving image mode. This ratio of maximum number of pixels that makes display image white (=data "255") to the total of pixels by image processing.

TH_MV [3:0]	Description
4'0h	99%
4'1h	98%
4'2h	96%
4'3h	94%
4'4h	92%
4'5h	90%
4'6h	88%
4'7h	86%

TH_MV [3:0]	Description
4'8h	84%
4'9h	82%
4'Ah	80%
4'Bh	78%
4'Ch	76%
4'Dh	74%
4'Eh	72%
4'Fh	70%

Description

The graph illustrates the cumulative distribution function (CDF) of grayscale values. The x-axis represents the grayscale levels from 0 to 255, with specific points marked as Dth and 255. The y-axis represents the percentage of pixels, ranging from 0% to 100%. A smooth black curve represents the histogram. A vertical red arrow originates from the text 'TH_MV[3:0], TH_ST[3:0], TH_UI[3:0]' and points to the point where the curve begins to rise sharply, indicating the threshold where most pixels are white (at approximately 255 grayscale).

Register Availability	Status		Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Partial Mode On, Idle Mode Off, Sleep Out	Yes	
	Partial Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In	Yes	
Default	Status	Default Value	
		TH_MV [3:0]	TH_ST [3:0]
		4'b1100	4'b1100
		No change	No change
		HW Reset	4'b1100

8.3.11. Backlight Control 3 (BAh)

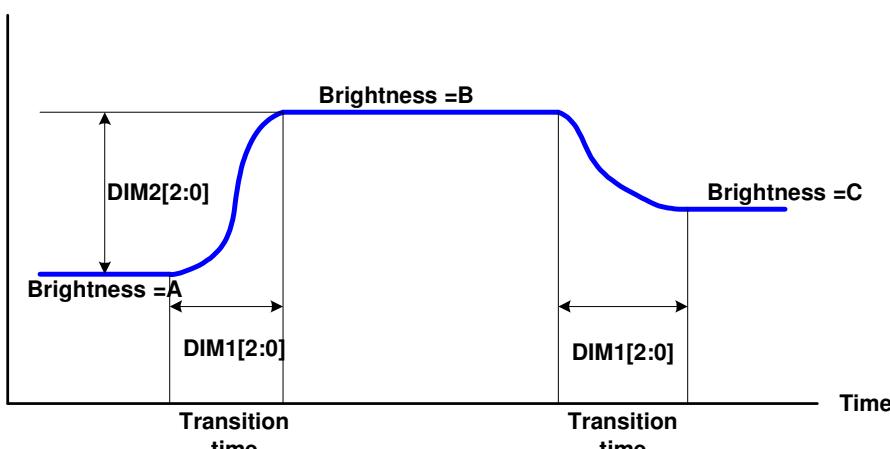
BAh	Backlight Control 3																																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																			
Command	0	1	↑	XX	1	0	1	1	1	0	1	0	BAh																																			
Parameter	1	1	↑	XX	0	0	0	0	DTH_UI [3]	DTH_UI [2]	DTH_UI [1]	DTH_UI [0]	04																																			
<p>DTH_UI [3:0]: This parameter is used set the minimum limitation of grayscale threshold value in User Icon (UI) image mode. This register setting will limit the minimum Dth value to prevent the display image from being too white and the display quality is not acceptable.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DTH_UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'0h</td><td>252</td></tr> <tr><td>4'1h</td><td>248</td></tr> <tr><td>4'2h</td><td>244</td></tr> <tr><td>4'3h</td><td>240</td></tr> <tr><td>4'4h</td><td>236</td></tr> <tr><td>4'5h</td><td>232</td></tr> <tr><td>4'6h</td><td>228</td></tr> <tr><td>4'7h</td><td>224</td></tr> </tbody> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>DTH UI [3:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr><td>4'8h</td><td>220</td></tr> <tr><td>4'9h</td><td>216</td></tr> <tr><td>4'Ah</td><td>212</td></tr> <tr><td>4'Bh</td><td>208</td></tr> <tr><td>4'C_h</td><td>204</td></tr> <tr><td>4'D_h</td><td>200</td></tr> <tr><td>4'E_h</td><td>196</td></tr> <tr><td>4'F_h</td><td>192</td></tr> </tbody> </table>													DTH_UI [3:0]	Description	4'0h	252	4'1h	248	4'2h	244	4'3h	240	4'4h	236	4'5h	232	4'6h	228	4'7h	224	DTH UI [3:0]	Description	4'8h	220	4'9h	216	4'Ah	212	4'Bh	208	4'C _h	204	4'D _h	200	4'E _h	196	4'F _h	192
DTH_UI [3:0]	Description																																															
4'0h	252																																															
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4'4h	236																																															
4'5h	232																																															
4'6h	228																																															
4'7h	224																																															
DTH UI [3:0]	Description																																															
4'8h	220																																															
4'9h	216																																															
4'Ah	212																																															
4'Bh	208																																															
4'C _h	204																																															
4'D _h	200																																															
4'E _h	196																																															
4'F _h	192																																															
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes																							
Status	Availability																																															
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																															
Normal Mode On, Idle Mode On, Sleep Out	Yes																																															
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																															
Sleep In	Yes																																															
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> <tr> <th>DTH UI [3:0]</th> <th></th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>4'b0100</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>4'b0100</td></tr> </tbody> </table>													Status	Default Value	DTH UI [3:0]		Power On Sequence	4'b0100	SW Reset	No change	HW Reset	4'b0100																									
Status	Default Value																																															
DTH UI [3:0]																																																
Power On Sequence	4'b0100																																															
SW Reset	No change																																															
HW Reset	4'b0100																																															

8.3.12. Backlight Control 4 (BBh)

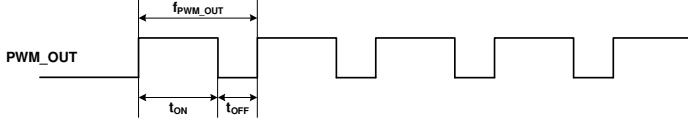
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Default			Default Value		
			Status		
			DTH_MV [3:0]	DTH_ST [3:0]	
			Power On Sequence	4'b0110	4'b0101
			SW Reset	No change	No change
			HW Reset	4'b0110	4'b0101

8.3.13. Backlight Control 5 (BCh)

BCh	Backlight Control 5																														
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XX	1	0	1	1	1	1	0	0	BCh																		
Parameter	1	1	↑	XX	DIM2 [3]	DIM2 [2]	DIM2 [1]	DIM2 [0]	0	DIM1 [2]	DIM1 [1]	DIM1 [0]	44																		
DIM1 [2:0]: This parameter is used to set the transition time of brightness level to avoid the sharp brightness transition on vision.																															
<table border="1"> <thead> <tr> <th>DIM1 [2:0]</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>3'0h</td> <td>1 frame</td> </tr> <tr> <td>3'1h</td> <td>1 frame</td> </tr> <tr> <td>3'2h</td> <td>2 frames</td> </tr> <tr> <td>3'3h</td> <td>4 frames</td> </tr> <tr> <td>3'4h</td> <td>8 frames</td> </tr> <tr> <td>3'5h</td> <td>16 frames</td> </tr> <tr> <td>3'6h</td> <td>32 frames</td> </tr> <tr> <td>3'7h</td> <td>64 frames</td> </tr> </tbody> </table>													DIM1 [2:0]	Description	3'0h	1 frame	3'1h	1 frame	3'2h	2 frames	3'3h	4 frames	3'4h	8 frames	3'5h	16 frames	3'6h	32 frames	3'7h	64 frames	
DIM1 [2:0]	Description																														
3'0h	1 frame																														
3'1h	1 frame																														
3'2h	2 frames																														
3'3h	4 frames																														
3'4h	8 frames																														
3'5h	16 frames																														
3'6h	32 frames																														
3'7h	64 frames																														
Description																															
	<p>DIM2 [3:0]: This parameter is used to set the threshold of brightness change. When the brightness transition difference is smaller than DIM2 [3:0], the brightness transition will be ignored. For example: If $\text{brightness B} - \text{brightness A} < \text{DIM2 [3:0]}$, the brightness transition will be ignored and keep the brightness A.</p>																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
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Partial Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In	Yes																														
<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>DIM2 [3:0]</th> <th>DIM1 [2:0]</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>4'b0100</td> <td>4'b0100</td> </tr> <tr> <td>SW Reset</td> <td>No change</td> <td>No change</td> </tr> <tr> <td>HW Reset</td> <td>4'b0100</td> <td>4'b0100</td> </tr> </tbody> </table>													Status	Default Value		DIM2 [3:0]	DIM1 [2:0]	Power On Sequence	4'b0100	4'b0100	SW Reset	No change	No change	HW Reset	4'b0100	4'b0100					
Status	Default Value																														
	DIM2 [3:0]	DIM1 [2:0]																													
Power On Sequence	4'b0100	4'b0100																													
SW Reset	No change	No change																													
HW Reset	4'b0100	4'b0100																													

8.3.14. Backlight Control 7 (BEh)

Backlight Control 7																																						
BEh	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
Command	0	1	↑	XX	1	0	1	1	1	1	1	0	BEh																									
Parameter	1	1	↑	XX	PWM_DIV[7]	PWM_DIV[6]	PWM_DIV[5]	PWM_DIV[4]	PWM_DIV[3]	PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	0F																									
PWM_DIV [7:0]: PWM_OUT output frequency control. This command is used to adjust the PWM waveform frequency of PWM_OUT. The PWM frequency can be calculated by using the following equation.																																						
Description	$f_{\text{PWM_OUT}} = \frac{16\text{MHz}}{(\text{PWM_DIV}[7:0] + 1) \times 255}$ <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PWM_DIV [7:0]</th> <th>f_{PWM OUT}</th> </tr> </thead> <tbody> <tr><td>8'h0</td><td>62.74 KHz</td></tr> <tr><td>8'h1</td><td>31.38 KHz</td></tr> <tr><td>8'h2</td><td>20.915 KHz</td></tr> <tr><td>8'h3</td><td>15.686 KHz</td></tr> <tr><td>8'h4</td><td>12.549 KHz</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>8'hFB</td><td>249Hz</td></tr> <tr><td>8'hFC</td><td>248Hz</td></tr> <tr><td>8'hFD</td><td>247Hz</td></tr> <tr><td>8'hFE</td><td>246Hz</td></tr> <tr><td>8'hFF</td><td>245Hz</td></tr> </tbody> </table>  <p>Note: The output frequency tolerance of internal frequency divider in CABC is ±10%</p>														PWM_DIV [7:0]	f _{PWM OUT}	8'h0	62.74 KHz	8'h1	31.38 KHz	8'h2	20.915 KHz	8'h3	15.686 KHz	8'h4	12.549 KHz	8'hFB	249Hz	8'hFC	248Hz	8'hFD	247Hz	8'hFE	246Hz	8'hFF	245Hz
PWM_DIV [7:0]	f _{PWM OUT}																																					
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8'h1	31.38 KHz																																					
8'h2	20.915 KHz																																					
8'h3	15.686 KHz																																					
8'h4	12.549 KHz																																					
...	...																																					
8'hFB	249Hz																																					
8'hFC	248Hz																																					
8'hFD	247Hz																																					
8'hFE	246Hz																																					
8'hFF	245Hz																																					
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In	Yes												
Status	Availability																																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																					
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Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr><td>Power On Sequence</td><td>PWM_DIV [7:0]=0Fh</td></tr> <tr><td>SW Reset</td><td>No change</td></tr> <tr><td>HW Reset</td><td>PWM_DIV [7:0]=0Fh</td></tr> </tbody> </table>														Status	Default Value	Power On Sequence	PWM_DIV [7:0]=0Fh	SW Reset	No change	HW Reset	PWM_DIV [7:0]=0Fh																
Status	Default Value																																					
Power On Sequence	PWM_DIV [7:0]=0Fh																																					
SW Reset	No change																																					
HW Reset	PWM_DIV [7:0]=0Fh																																					

8.3.15. Backlight Control 8 (BFh)

BFh		Backlight Control 2																													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	0	1	↑	XX	1	0	1	1	1	1	1	1	BFh																		
Parameter	1	1	↑	XX	0	0	0	0	0	LEDONR	LEDONPOL	LEDPWMMPOL	00																		
		LEDPWMMPOL: The bit is used to define polarity of LEDPWM signal.																													
Description	<table border="1"> <thead> <tr> <th>BL</th> <th>LEDPWMMPOL</th> <th>LEDPWM pin</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>Original polarity of PWM signal</td></tr> <tr> <td>1</td><td>1</td><td>Inversed polarity of PWM signal</td></tr> </tbody> </table> LEDONPOL: This bit is used to control LEDON pin.													BL	LEDPWMMPOL	LEDPWM pin	0	0	0	0	1	1	1	0	Original polarity of PWM signal	1	1	Inversed polarity of PWM signal			
BL	LEDPWMMPOL	LEDPWM pin																													
0	0	0																													
0	1	1																													
1	0	Original polarity of PWM signal																													
1	1	Inversed polarity of PWM signal																													
<table border="1"> <thead> <tr> <th>BL</th> <th>LEDONPOL</th> <th>LEDON pin</th> </tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td></tr> <tr> <td>0</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>LEDONR</td></tr> <tr> <td>1</td><td>1</td><td>Inversed LEDONR</td></tr> </tbody> </table> LEDONR: This bit is used to control LEDON pin.													BL	LEDONPOL	LEDON pin	0	0	0	0	1	1	1	0	LEDONR	1	1	Inversed LEDONR				
BL	LEDONPOL	LEDON pin																													
0	0	0																													
0	1	1																													
1	0	LEDONR																													
1	1	Inversed LEDONR																													
<table border="1"> <thead> <tr> <th>LEDONR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td><td>Low</td></tr> <tr> <td>1</td><td>High</td></tr> </tbody> </table>													LEDONR	Description	0	Low	1	High													
LEDONR	Description																														
0	Low																														
1	High																														
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Status	Availability																														
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Sleep In	Yes																														
<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>LEDONR</th> <th>LEDONPOL</th> <th>LEDPWMMPOL</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr> <tr> <td>SW Reset</td><td>No change</td><td>No change</td><td>No change</td></tr> <tr> <td>HW Reset</td><td>1'b0</td><td>1'b0</td><td>1'b0</td></tr> </tbody> </table>													Status	Default Value			LEDONR	LEDONPOL	LEDPWMMPOL	Power On Sequence	1'b0	1'b0	1'b0	SW Reset	No change	No change	No change	HW Reset	1'b0	1'b0	1'b0
Status	Default Value																														
	LEDONR	LEDONPOL	LEDPWMMPOL																												
Power On Sequence	1'b0	1'b0	1'b0																												
SW Reset	No change	No change	No change																												
HW Reset	1'b0	1'b0	1'b0																												

8.3.16. Power Control 1 (C0h)

C0h	PWCTRL 1 (Power Control 1)																							
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	XX	1	1	0	0	0	0	0	0	C0h											
1 st Parameter	1	1	↑	XX	0	0			VRH [5:0]				21											
VRH [5:0]: Set the GVDD level, which is a reference level for the VCOM level and the grayscale voltage level.																								
Description	VRH [5:0]					GVDD																		
	0	0	0	0	0	0	Setting prohibited																	
	0	0	0	0	0	1	Setting prohibited																	
	0	0	0	0	1	0	Setting prohibited																	
	0	0	0	0	1	1	3.00 V																	
	0	0	0	1	0	0	3.05 V																	
	0	0	0	1	0	1	3.10 V																	
	0	0	0	1	1	0	3.15 V																	
	0	0	0	1	1	1	3.20 V																	
	0	0	1	0	0	0	3.25 V																	
	0	0	1	0	0	1	3.30 V																	
	0	0	1	0	1	0	3.35 V																	
	0	0	1	0	1	1	3.40 V																	
	0	0	1	1	0	0	3.45 V																	
	0	0	1	1	0	1	3.50 V																	
	0	0	1	1	1	0	3.55 V																	
	0	0	1	1	1	1	3.60 V																	
	0	1	0	0	0	0	3.65 V																	
	0	1	0	0	0	1	3.70 V																	
	0	1	0	0	1	0	3.75 V																	
	0	1	0	0	1	1	3.80 V																	
	0	1	0	1	0	0	3.85 V																	
	0	1	0	1	0	1	3.90 V																	
	0	1	0	1	1	0	3.95 V																	
	0	1	0	1	1	1	4.00 V																	
	0	1	1	0	0	0	4.05 V																	
	0	1	1	0	0	1	4.10 V																	
	0	1	1	0	1	0	4.15 V																	
	0	1	1	0	1	1	4.20 V																	
	0	1	1	1	0	0	4.25 V																	
	0	1	1	1	0	1	4.30 V																	
	0	1	1	1	1	0	4.35 V																	
	0	1	1	1	1	1	4.40 V																	
<i>Note 1: Make sure that VC and VRH setting restriction: GVDD ≤ (DDVDH - 0.2) V.</i>																								
Restriction	EXTC should be high to enable this command																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																							
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																							
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																							
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																							
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																							
Sleep IN	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>VRH [5:0]</td> <td></td> </tr> <tr> <td>Power ON Sequence</td> <td>6'h21h</td> </tr> <tr> <td>SW Reset</td> <td>6'h21h</td> </tr> <tr> <td>HW Reset</td> <td>6'h21h</td> </tr> </tbody> </table>												Status	Default Value	VRH [5:0]		Power ON Sequence	6'h21h	SW Reset	6'h21h	HW Reset	6'h21h		
Status	Default Value																							
VRH [5:0]																								
Power ON Sequence	6'h21h																							
SW Reset	6'h21h																							
HW Reset	6'h21h																							

8.3.17. Power Control 2 (C1h)

C1h		PWCTRL 2 (Power Control 2)																																				
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																									
Command	0	1	↑	XX	1	1	0	0	0	0	0	1	C1h																									
Parameter	1	1	↑	XX	0	0	0	0	0	0	0	10	BT [2:0]																									
Description	<p>BT [2:0]: Sets the factor used in the step-up circuits.</p> <p>Select the optimal step-up factor for the operating voltage. To reduce power consumption, set a smaller factor.</p> <table border="1"> <tr> <th colspan="3">BT [2:0]</th> <th>DDVDH</th> <th>VGH</th> <th>VGL</th> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td rowspan="4">VCI x 2</td> <td rowspan="2">VCI x 7</td> <td>-VCI x 4</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>-VCI x 3</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td rowspan="2">VCI x 6</td> <td>-VCI x 4</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>-VCI x 3</td> </tr> </table> <p><i>Note 1:</i> Make sure that DDVDH setting restriction: DDVDH \leq 5.8 V.</p> <p><i>2:</i> Make sure that VGH and VGL setting restriction: VGH -VGL \leq 28 V.</p>													BT [2:0]			DDVDH	VGH	VGL	0	0	0	VCI x 2	VCI x 7	-VCI x 4	0	0	1	-VCI x 3	0	1	0	VCI x 6	-VCI x 4	0	1	1	-VCI x 3
BT [2:0]			DDVDH	VGH	VGL																																	
0	0	0	VCI x 2	VCI x 7	-VCI x 4																																	
0	0	1			-VCI x 3																																	
0	1	0		VCI x 6	-VCI x 4																																	
0	1	1			-VCI x 3																																	
Restriction	EXTC should be high to enable this command																																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes													
Status	Availability																																					
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																					
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																					
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																					
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																					
Sleep IN	Yes																																					
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>BT [2:0]</td> <td>3'b000</td> </tr> <tr> <td>Power ON Sequence</td> <td>3'b000</td> </tr> <tr> <td>SW Reset</td> <td>3'b000</td> </tr> <tr> <td>HW Reset</td> <td>3'b000</td> </tr> </tbody> </table>													Status	Default Value	BT [2:0]	3'b000	Power ON Sequence	3'b000	SW Reset	3'b000	HW Reset	3'b000															
Status	Default Value																																					
BT [2:0]	3'b000																																					
Power ON Sequence	3'b000																																					
SW Reset	3'b000																																					
HW Reset	3'b000																																					

8.3.18. VCOM Control 1(C5h)

C5h	VMCTRL1 (VCOM Control 1)													
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	0	1	↑	XX	1	1	0	0	0	1	0	1	C5h	
1 st Parameter	1	1	↑	XX	0				VMH [6:0]				31	
2 nd Parameter	1	1	↑	XX	0				VML [6:0]				3C	
Description	VMH [6:0] : Set the VCOMH voltage.													
	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)	VMH [6:0]	VCOMH(V)
	0000000	2.700	0100000	3.500	1000000	4.300	1100000	5.100	1000001	4.325	1100001	5.125	1000010	5.150
	0000001	2.725	0100001	3.525	1000011	4.375	1100011	5.175	1000100	4.400	1100100	5.200	1000101	5.225
	0000010	2.750	0100010	3.550	1000110	4.425	1100110	5.250	1000111	4.450	1100111	5.275	1001000	5.300
	0000011	2.775	0100011	3.575	1001001	4.525	1101001	5.325	1001010	4.550	1101010	5.350	1001011	5.375
	0000100	2.800	0100100	3.600	1001100	4.600	1101100	5.400	1001101	4.625	1101101	5.425	1001110	5.450
	0000101	2.825	0100101	3.625	1001111	4.650	1101111	5.475	1001110	4.675	1101110	5.500	1100000	5.525
	0000110	2.850	0100110	3.650	1010000	4.700	1100001	5.550	1010001	4.725	1100001	5.575	1010010	5.600
	0000111	2.875	0100111	3.675	1010010	4.750	1010011	4.775	1010011	4.795	1101010	5.625	1010110	5.650
	0001000	2.900	0101000	3.700	1010100	4.800	1010111	4.875	1010110	4.850	1101011	5.675	1011000	5.700
	0001001	2.925	0101001	3.725	1011000	4.900	1011001	4.925	1011010	4.950	1111000	5.725	1011011	5.750
	0001010	2.950	0101010	3.750	1011010	4.975	1011011	5.000	1011100	5.025	1111010	5.775	1011110	5.800
	0001011	2.975	0101011	3.775	1011100	5.050	1011110	5.075	1011111	5.075	1111100	5.825	1111110	5.850
	0001100	3.000	0101100	3.800							1111111	5.875		
	0001101	3.025	0101101	3.825										
	0001110	3.050	0101110	3.850										
	0001111	3.075	0101111	3.875										
	0010000	3.100	0110000	3.900										
	0010001	3.125	0110001	3.925										
	0010010	3.150	0110010	3.950										
	0010011	3.175	0110011	3.975										
	0010100	3.200	0110100	4.000										
	0010101	3.225	0110101	4.025										
	0010110	3.250	0110110	4.050										
	0010111	3.275	0110111	4.075										
	0011000	3.300	0111000	4.100										
	0011001	3.325	0111001	4.125										
	0011010	3.350	0111010	4.150										
	0011011	3.375	0111011	4.175										
	0011100	3.400	0111100	4.200										
	0011101	3.425	0111101	4.225										
	0011110	3.450	0111110	4.250										
	0011111	3.475	0111111	4.275										
Description	VML [6:0] : Set the VCOML voltage													
	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)	VML [6:0]	VCOML(V)
	0000000	-2.500	0100000	-1.700	1000000	-0.900	1100000	-0.100	1000001	-0.875	1100001	-0.075	1000010	-0.850
	0000001	-2.475	0100001	-1.675	1000011	-0.825	1100011	-0.025	1000100	-0.800	1100100	0	1000101	Reserved
	0000010	-2.450	0100010	-1.650	1000110	-0.775	1100110	Reserved	1000111	-0.750	1100111	Reserved	1001000	Reserved
	0000011	-2.425	0100011	-1.625	1001001	-0.725	1100111	Reserved	1001010	-0.700	1101000	Reserved	1001011	Reserved
	0000100	-2.400	0100100	-1.600	1001010	-0.675	1101001	Reserved	1001011	-0.650	1101010	Reserved	1001011	Reserved
	0000101	-2.375	0100101	-1.575	1001011	-0.625	1001100	-0.600	1001101	-0.575	1101100	Reserved	1101101	Reserved
	0000110	-2.350	0100110	-1.550	1001100	-0.550	1001110	-0.525	1001111	-0.500	1110000	Reserved	1110001	Reserved
	0000111	-2.325	0100111	-1.525	1001111	-0.475	1001110	-0.450	1010001	-0.425	1110010	Reserved	1110011	Reserved
	0001000	-2.300	0101000	-1.500	1010000	-0.400	1010001	-0.375	1010001	-0.350	1110011	Reserved	1110011	Reserved
	0001001	-2.275	0101001	-1.475	1010010	-0.325	1010011	-0.300	1010011	-0.275	1110100	Reserved	1110101	Reserved
	0001010	-2.250	0101010	-1.450	1010100	-0.275	1010101	-0.250	1010101	-0.225	1110110	Reserved	1110111	Reserved
	0001011	-2.225	0101011	-1.425	1010110	-0.225	1010111	-0.200	1010111	-0.175	1111000	Reserved	1111001	Reserved
	0001100	-2.200	0101100	-1.400	1011000	-0.175	1011001	-0.150	1011001	-0.125	1111010	Reserved	1111011	Reserved
	0001101	-2.175	0101101	-1.375	1011010	-0.125	1011011	-0.100	1011011	-0.075	1111100	Reserved	1111101	Reserved
	0001110	-2.150	0101110	-1.350	1011100	-0.075	1011101	-0.050	1011101	-0.025	1111110	Reserved	1111111	Reserved
	0001111	-2.125	0101111	-1.325	1011110	-0.025	1011111	-0.000	1011111	-0.025	1111111	Reserved		
	0010000	-2.100	0110000	-1.300	1010000	-0.500	1010001	-0.475	1010001	-0.450	1110000	Reserved	1110001	Reserved
	0010001	-2.075	0110001	-1.275	1010010	-0.425	1010011	-0.400	1010011	-0.375	1110010	Reserved	1110011	Reserved
	0010010	-2.050	0110010	-1.250	1010100	-0.375	1010101	-0.350	1010101	-0.325	1110110	Reserved	1110111	Reserved
	0010011	-2.025	0110011	-1.225	1010110	-0.325	1010111	-0.300	1010111	-0.275	1111000	Reserved	1111001	Reserved

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	0010100	-2.000	0110100	-1.200	1010100	-0.400	1110100	Reserved														
	0010101	-1.975	0110101	-1.175	1010101	-0.375	1110101	Reserved														
	0010110	-1.950	0110110	-1.150	1010110	-0.350	1110110	Reserved														
	0010111	-1.925	0110111	-1.125	1010111	-0.325	1110111	Reserved														
	0011000	-1.900	0111000	-1.100	1011000	-0.300	1111000	Reserved														
	0011001	-1.875	0111001	-1.075	1011001	-0.275	1111001	Reserved														
	0011010	-1.850	0111010	-1.050	1011010	-0.250	1111010	Reserved														
	0011011	-1.825	0111011	-1.025	1011011	-0.225	1111011	Reserved														
	0011100	-1.800	0111100	-1.000	1011100	-0.200	1111100	Reserved														
	0011101	-1.775	0111101	-0.975	1011101	-0.175	1111101	Reserved														
	0011110	-1.750	0111110	-0.950	1011110	-0.150	1111110	Reserved														
	0011111	-1.725	0111111	-0.925	1011111	-0.125	1111111	Reserved														
Restriction	EXTC should be high to enable this command																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>								Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																					
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																					
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																					
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																					
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																					
Sleep IN	Yes																					
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>VMH [6:0]</th> <th>VML [6:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>7'h31</td> <td>7'h3C</td> </tr> <tr> <td>SW Reset</td> <td>7'h31</td> <td>7'h3C</td> </tr> <tr> <td>HW Rest</td> <td>7'h31</td> <td>7'h3C</td> </tr> </tbody> </table>								Status	Default Value		VMH [6:0]	VML [6:0]	Power ON Sequence	7'h31	7'h3C	SW Reset	7'h31	7'h3C	HW Rest	7'h31	7'h3C
Status	Default Value																					
	VMH [6:0]	VML [6:0]																				
Power ON Sequence	7'h31	7'h3C																				
SW Reset	7'h31	7'h3C																				
HW Rest	7'h31	7'h3C																				

8.3.19. VCOM Control 2(C7h)

C7h	VMCTRL1 (VCOM Control 1)												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	1	1	0	0	0	1	1	1	C7h
Parameter	1	1	↑	XX	nVM	VMF [6:0]							
nVM: nVM equals to "0" after power on reset and VCOM offset equals to program MTP value. When nVM set to "1", setting of VMF [6:0] becomes valid and VCOMH/VCOML can be adjusted.													
Description	VMF [6:0]: Set the VCOM offset voltage.			VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML	VMF[6:0]	VCOMH	VCOML	VMF[6:0]
	0000000	VMH	VML	1000000	VMH	VML	1000000	VMH	VML	1000000	VMH	VML	1000000
	0000001	VMH - 63	VML - 63	1000001	VMH + 1	VML + 1	1000001	VMH + 1	VML + 1	1000001	VMH + 1	VML + 1	1000001
	0000010	VMH - 62	VML - 62	1000010	VMH + 2	VML + 2	1000010	VMH + 2	VML + 2	1000010	VMH + 2	VML + 2	1000010
	0000011	VMH - 61	VML - 61	1000011	VMH + 3	VML + 3	1000011	VMH + 3	VML + 3	1000011	VMH + 3	VML + 3	1000011
	0000100	VMH - 60	VML - 60	1000100	VMH + 4	VML + 4	1000100	VMH + 4	VML + 4	1000100	VMH + 4	VML + 4	1000100
	0000101	VMH - 58	VML - 58	1000101	VMH + 5	VML + 5	1000101	VMH + 5	VML + 5	1000101	VMH + 5	VML + 5	1000101
	0000110	VMH - 58	VML - 58	1000110	VMH + 6	VML + 6	1000110	VMH + 6	VML + 6	1000110	VMH + 6	VML + 6	1000110
	0000111	VMH - 57	VML - 57	1000111	VMH + 7	VML + 7	1000111	VMH + 7	VML + 7	1000111	VMH + 7	VML + 7	1000111
	0001000	VMH - 56	VML - 56	1001000	VMH + 8	VML + 8	1001000	VMH + 8	VML + 8	1001000	VMH + 8	VML + 8	1001000
	0001001	VMH - 55	VML - 55	1001001	VMH + 9	VML + 9	1001001	VMH + 9	VML + 9	1001001	VMH + 9	VML + 9	1001001
	0001010	VMH - 54	VML - 54	1001010	VMH + 10	VML + 10	1001010	VMH + 10	VML + 10	1001010	VMH + 10	VML + 10	1001010
	0001011	VMH - 53	VML - 53	1001011	VMH + 11	VML + 11	1001011	VMH + 11	VML + 11	1001011	VMH + 11	VML + 11	1001011
	0001100	VMH - 52	VML - 52	1001100	VMH + 12	VML + 12	1001100	VMH + 12	VML + 12	1001100	VMH + 12	VML + 12	1001100
	0001101	VMH - 51	VML - 51	1001101	VMH + 13	VML + 13	1001101	VMH + 13	VML + 13	1001101	VMH + 13	VML + 13	1001101
	0001110	VMH - 50	VML - 50	1001110	VMH + 14	VML + 14	1001110	VMH + 14	VML + 14	1001110	VMH + 14	VML + 14	1001110
	0001111	VMH - 49	VML - 49	1001111	VMH + 15	VML + 15	1001111	VMH + 15	VML + 15	1001111	VMH + 15	VML + 15	1001111
	0010000	VMH - 48	VML - 48	1010000	VMH + 16	VML + 16	1010000	VMH + 16	VML + 16	1010000	VMH + 16	VML + 16	1010000
	0010001	VMH - 47	VML - 47	1010001	VMH + 17	VML + 17	1010001	VMH + 17	VML + 17	1010001	VMH + 17	VML + 17	1010001
	0010010	VMH - 46	VML - 46	1010010	VMH + 18	VML + 18	1010010	VMH + 18	VML + 18	1010010	VMH + 18	VML + 18	1010010
	0010011	VMH - 45	VML - 45	1010011	VMH + 19	VML + 19	1010011	VMH + 19	VML + 19	1010011	VMH + 19	VML + 19	1010011
	0010100	VMH - 44	VML - 44	1010100	VMH + 20	VML + 20	1010100	VMH + 20	VML + 20	1010100	VMH + 20	VML + 20	1010100
	0010101	VMH - 43	VML - 43	1010101	VMH + 21	VML + 21	1010101	VMH + 21	VML + 21	1010101	VMH + 21	VML + 21	1010101
	0010110	VMH - 42	VML - 42	1010110	VMH + 22	VML + 22	1010110	VMH + 22	VML + 22	1010110	VMH + 22	VML + 22	1010110
	0010111	VMH - 41	VML - 41	1010111	VMH + 23	VML + 23	1010111	VMH + 23	VML + 23	1010111	VMH + 23	VML + 23	1010111
	0011000	VMH - 40	VML - 40	1011000	VMH + 24	VML + 24	1011000	VMH + 24	VML + 24	1011000	VMH + 24	VML + 24	1011000
	0011001	VMH - 39	VML - 39	1011001	VMH + 25	VML + 25	1011001	VMH + 25	VML + 25	1011001	VMH + 25	VML + 25	1011001
	0011010	VMH - 38	VML - 38	1011010	VMH + 26	VML + 26	1011010	VMH + 26	VML + 26	1011010	VMH + 26	VML + 26	1011010
	0011011	VMH - 37	VML - 37	1011011	VMH + 27	VML + 27	1011011	VMH + 27	VML + 27	1011011	VMH + 27	VML + 27	1011011
	0011100	VMH - 36	VML - 36	1011100	VMH + 28	VML + 28	1011100	VMH + 28	VML + 28	1011100	VMH + 28	VML + 28	1011100
	0011101	VMH - 35	VML - 35	1011101	VMH + 29	VML + 29	1011101	VMH + 29	VML + 29	1011101	VMH + 29	VML + 29	1011101
	0011110	VMH - 34	VML - 34	1011110	VMH + 30	VML + 30	1011110	VMH + 30	VML + 30	1011110	VMH + 30	VML + 30	1011110
	0011111	VMH - 33	VML - 33	1011111	VMH + 31	VML + 31	1011111	VMH + 31	VML + 31	1011111	VMH + 31	VML + 31	1011111
	0100000	VMH - 32	VML - 32	1100000	VMH + 32	VML + 32	1100000	VMH + 32	VML + 32	1100000	VMH + 32	VML + 32	1100000
	0100001	VMH - 31	VML - 31	1100001	VMH + 33	VML + 33	1100001	VMH + 33	VML + 33	1100001	VMH + 33	VML + 33	1100001
	0100010	VMH - 30	VML - 30	1100010	VMH + 34	VML + 34	1100010	VMH + 34	VML + 34	1100010	VMH + 34	VML + 34	1100010
	0100011	VMH - 29	VML - 29	1100011	VMH + 35	VML + 35	1100011	VMH + 35	VML + 35	1100011	VMH + 35	VML + 35	1100011
	0100100	VMH - 28	VML - 28	1100100	VMH + 36	VML + 36	1100100	VMH + 36	VML + 36	1100100	VMH + 36	VML + 36	1100100
	0100101	VMH - 27	VML - 27	1100101	VMH + 37	VML + 37	1100101	VMH + 37	VML + 37	1100101	VMH + 37	VML + 37	1100101
	0100110	VMH - 26	VML - 26	1100110	VMH + 38	VML + 38	1100110	VMH + 38	VML + 38	1100110	VMH + 38	VML + 38	1100110
	0100111	VMH - 25	VML - 25	1100111	VMH + 39	VML + 39	1100111	VMH + 39	VML + 39	1100111	VMH + 39	VML + 39	1100111
	0101000	VMH - 24	VML - 24	1101000	VMH + 40	VML + 40	1101000	VMH + 40	VML + 40	1101000	VMH + 40	VML + 40	1101000
	0101001	VMH - 23	VML - 23	1101001	VMH + 41	VML + 41	1101001	VMH + 41	VML + 41	1101001	VMH + 41	VML + 41	1101001
	0101010	VMH - 22	VML - 22	1101010	VMH + 42	VML + 42	1101010	VMH + 42	VML + 42	1101010	VMH + 42	VML + 42	1101010
	0101011	VMH - 21	VML - 21	1101011	VMH + 43	VML + 43	1101011	VMH + 43	VML + 43	1101011	VMH + 43	VML + 43	1101011
	0101100	VMH - 20	VML - 20	1101100	VMH + 44	VML + 44	1101100	VMH + 44	VML + 44	1101100	VMH + 44	VML + 44	1101100
	0101101	VMH - 19	VML - 19	1101101	VMH + 45	VML + 45	1101101	VMH + 45	VML + 45	1101101	VMH + 45	VML + 45	1101101
	0101110	VMH - 18	VML - 18	1101110	VMH + 46	VML + 46	1101110	VMH + 46	VML + 46	1101110	VMH + 46	VML + 46	1101110
	0101111	VMH - 17	VML - 17	1101111	VMH + 47	VML + 47	1101111	VMH + 47	VML + 47	1101111	VMH + 47	VML + 47	1101111
	0110000	VMH - 16	VML - 16	1110000	VMH + 48	VML + 48	1110000	VMH + 48	VML + 48	1110000	VMH + 48	VML + 48	1110000
	0110001	VMH - 15	VML - 15	1110001	VMH + 49	VML + 49	1110001	VMH + 49	VML + 49	1110001	VMH + 49	VML + 49	1110001
	0110010	VMH - 14	VML - 14	1110010	VMH + 50	VML + 50	1110010	VMH + 50	VML + 50	1110010	VMH + 50	VML + 50	1110010
	0110011	VMH - 13	VML - 13	1110011	VMH + 51	VML + 51	1110011	VMH + 51	VML + 51	1110011	VMH + 51	VML + 51	1110011
	0110100	VMH - 12	VML - 12	1110100	VMH + 52	VML + 52	1110100	VMH + 52	VML + 52	1110100	VMH + 52	VML + 52	1110100

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		0110101	VMH - 11	VML - 11	1110101	VMH + 53	VML + 53															
		0110110	VMH - 10	VML - 10	1110110	VMH + 54	VML + 54															
		0110111	VMH - 9	VML - 9	1110111	VMH + 55	VML + 55															
		0111000	VMH - 8	VML - 8	1111000	VMH + 56	VML + 56															
		0111001	VMH - 7	VML - 7	1111001	VMH + 57	VML + 57															
		0111010	VMH - 6	VML - 6	1111010	VMH + 58	VML + 58															
		0111011	VMH - 5	VML - 5	1111011	VMH + 59	VML + 59															
		0111100	VMH - 4	VML - 4	1111100	VMH + 60	VML + 60															
		0111101	VMH - 3	VML - 3	1111101	VMH + 61	VML + 61															
		0111110	VMH - 2	VML - 2	1111110	VMH + 62	VML + 62															
		0111111	VMH - 1	VML - 1	1111111	VMH + 63	VML + 63															
Restriction	EXTC should be high to enable this command																					
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>							Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																					
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																					
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																					
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																					
Sleep IN	Yes																					
Default		<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>nVM</th> <th>VMF [6:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>1'b1</td> <td>7'h40h</td> </tr> <tr> <td>SW Reset</td> <td>1'b1</td> <td>7'h40h</td> </tr> <tr> <td>HW Reset</td> <td>1'b1</td> <td>7'h40h</td> </tr> </tbody> </table>							Status	Default Value		nVM	VMF [6:0]	Power ON Sequence	1'b1	7'h40h	SW Reset	1'b1	7'h40h	HW Reset	1'b1	7'h40h
Status	Default Value																					
	nVM	VMF [6:0]																				
Power ON Sequence	1'b1	7'h40h																				
SW Reset	1'b1	7'h40h																				
HW Reset	1'b1	7'h40h																				

8.3.20. NV Memory Write (D0h)

NVMWR (NV Memory Write)																											
D0h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	0	1	0	0	0	0	D0h														
1 st Parameter	1	1	↑	XX	0	0	0	0	0	PGM_ADR [2:0]	00																
2 nd Parameter	1	1	↑	XX	PGM_DATA [7:0]								XX														
Description	<p>This command is used to program the NV memory data. After a successful MTP operation, the information of PGM_DATA [7:0] will be programmed to NV memory.</p> <p>PGM_ADR [2:0]: The select bits of ID1, ID2, ID3 and VMF [6:0] programming can be OTP x 3 times.</p> <table border="1"> <thead> <tr> <th>PGM_ADR [2:0]</th><th>Programmed NV Memory Selection</th></tr> </thead> <tbody> <tr> <td>0 0 0</td><td>ID1 programming</td></tr> <tr> <td>0 0 1</td><td>ID2 programming</td></tr> <tr> <td>0 1 0</td><td>ID3 programming</td></tr> <tr> <td>1 0 0</td><td>VMF [6:0] programming</td></tr> <tr> <td>Others</td><td>Reserved</td></tr> </tbody> </table> <p>PGM_DATA [7:0]: The programmed data.</p>													PGM_ADR [2:0]	Programmed NV Memory Selection	0 0 0	ID1 programming	0 0 1	ID2 programming	0 1 0	ID3 programming	1 0 0	VMF [6:0] programming	Others	Reserved		
PGM_ADR [2:0]	Programmed NV Memory Selection																										
0 0 0	ID1 programming																										
0 0 1	ID2 programming																										
0 1 0	ID3 programming																										
1 0 0	VMF [6:0] programming																										
Others	Reserved																										
Restriction	EXTC should be high to enable this command																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td><td>Yes</td></tr> <tr> <td>Sleep IN</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																										
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Sleep IN	Yes																										
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th><th colspan="2">Default Value</th></tr> <tr> <th>PGM_ADR [2:0]</th><th>PGM_DATA [7:0]</th></tr> </thead> <tbody> <tr> <td>Power ON Sequence</td><td>3'b000</td><td>MTP value</td></tr> <tr> <td>SW Reset</td><td>3'b000</td><td>MTP value</td></tr> <tr> <td>HW Reset</td><td>3'b000</td><td>MTP value</td></tr> </tbody> </table>													Status	Default Value		PGM_ADR [2:0]	PGM_DATA [7:0]	Power ON Sequence	3'b000	MTP value	SW Reset	3'b000	MTP value	HW Reset	3'b000	MTP value
Status	Default Value																										
	PGM_ADR [2:0]	PGM_DATA [7:0]																									
Power ON Sequence	3'b000	MTP value																									
SW Reset	3'b000	MTP value																									
HW Reset	3'b000	MTP value																									

8.3.21. NV Memory Protection Key (D1h)

D1h	NVMPKEY (NV Memory Protection Key)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	0	0	0	1	D1h												
1 st Parameter	1	1	↑	XX									55h												
2 nd Parameter	1	1	↑	XX									AAh												
3 rd Parameter	1	1	↑	XX									66h												
Description	KEY [23:0]: NV memory programming protection key. When writing MTP data to D1h, this register must be set to 0x55AA66h to enable MTP programming. If D1h register is not written with 0x55AA66h, then NV memory programming will be aborted.																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
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Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>KEY [23:0]=55AA66h</td> </tr> <tr> <td>SW Reset</td> <td>KEY [23:0]=55AA66h</td> </tr> <tr> <td>HW Reset</td> <td>KEY [23:0]=55AA66h</td> </tr> </tbody> </table>													Status	Default Value	Power ON Sequence	KEY [23:0]=55AA66h	SW Reset	KEY [23:0]=55AA66h	HW Reset	KEY [23:0]=55AA66h				
Status	Default Value																								
Power ON Sequence	KEY [23:0]=55AA66h																								
SW Reset	KEY [23:0]=55AA66h																								
HW Reset	KEY [23:0]=55AA66h																								

8.3.22. NV Memory Status Read (D2h)

RDNVM (NV Memory Status Read)																																											
D2h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																														
Command	0	1	↑	XX	1	1	0	1	0	0	1	0	D2h																														
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X																														
2 nd Parameter	1	↑	1	XX	0	ID2_CNT [2:0]			0	ID1_CNT [2:0]			XX																														
3 rd Parameter	1	↑	1	XX	BUSY	VMF_CNT [2:0]			0	ID3_CNT [2:0]			XX																														
Description	<p>ID1_CNT [2:0] / ID2_CNT [2:0] / ID3_CNT [2:0] / VMF_CNT [2:0]: ID and VMF all can be OPT x 3 times, NV memory program record. The bits will increase "+1" automatically after writing the PGM_DATA [7:0] to NV memory.</p> <table border="1"> <tr> <td>ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]</td><td>Description</td></tr> <tr> <td>Status</td><td>Availability</td></tr> <tr> <td>0 0 0</td><td>No Programmed</td></tr> <tr> <td>0 0 1</td><td>Programmed 1 time</td></tr> <tr> <td>0 1 1</td><td>Programmed 2 times</td></tr> <tr> <td>1 1 1</td><td>Programmed 3 times</td></tr> </table> <p>BUSY: The status bit of NV memory programming.</p> <table border="1"> <tr> <td>BUSY</td><td>The Status of NV Memory</td></tr> <tr> <td>0</td><td>Idle</td></tr> <tr> <td>1</td><td>Busy</td></tr> </table>														ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]	Description	Status	Availability	0 0 0	No Programmed	0 0 1	Programmed 1 time	0 1 1	Programmed 2 times	1 1 1	Programmed 3 times	BUSY	The Status of NV Memory	0	Idle	1	Busy											
ID1_CNT [2:0] / ID2_CNT [2:0] ID3_CNT [2:0] / VMF_CNT [2:0]	Description																																										
Status	Availability																																										
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1 1 1	Programmed 3 times																																										
BUSY	The Status of NV Memory																																										
0	Idle																																										
1	Busy																																										
Restriction	EXTC should be high to enable this command																																										
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Status	Availability																																										
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																										
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																										
Sleep IN	Yes																																										
Default	<table border="1"> <tr> <th rowspan="2">Status</th><th colspan="5">Default Value</th></tr> <tr> <th>ID3_CNT</th><th>ID2_CNT</th><th>ID1_CNT</th><th>VMF_CNT</th><th>BUSY</th></tr> <tr> <td>Power ON Sequence</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr> <tr> <td>SW Reset</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr> <tr> <td>HW Reset</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr> </table>														Status	Default Value					ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY	Power ON Sequence	X	X	X	X	X	SW Reset	X	X	X	X	X	HW Reset	X	X	X	X	X
Status	Default Value																																										
	ID3_CNT	ID2_CNT	ID1_CNT	VMF_CNT	BUSY																																						
Power ON Sequence	X	X	X	X	X																																						
SW Reset	X	X	X	X	X																																						
HW Reset	X	X	X	X	X																																						

8.3.23. Read ID4 (D3h)

D3h	RDID4 (Read ID4)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	0	1	0	0	1	1	D3h												
1 st Parameter	1	↑	1	XX	X	X	X	X	X	X	X	X	X												
2 nd Parameter	1	↑	1	XX	0	0	0	0	0	0	0	0	00h												
3 rd Parameter	1	↑	1	XX	1	0	0	1	0	0	1	1	93h												
4 th Parameter	1	↑	1	XX	0	1	0	0	0	0	0	1	41h												
Description	Read IC device code. The 1 st parameter is dummy read period. The 2 nd parameter means the IC version. The 3 rd and 4 th parameter mean the IC model name.																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
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Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>24'h009341h</td> </tr> <tr> <td>SW Reset</td> <td>24'h009341h</td> </tr> <tr> <td>HW Reset</td> <td>24'h009341h</td> </tr> </tbody> </table>													Status	Default Value	Power ON Sequence	24'h009341h	SW Reset	24'h009341h	HW Reset	24'h009341h				
Status	Default Value																								
Power ON Sequence	24'h009341h																								
SW Reset	24'h009341h																								
HW Reset	24'h009341h																								

8.3.24. Positive Gamma Correction (E0h)

PGAMCTRL (Positive Gamma Control)																									
E0h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	0	0	0	0	0	E0h												
1 st Parameter	1	1	↑	XX	0	0	0	0	VP63 [3:0]				08												
2 nd Parameter	1	1	↑	XX	0	0	VP62 [5:0]																		
3 rd Parameter	1	1	↑	XX	0	0	VP61 [5:0]																		
4 th Parameter	1	1	↑	X	0	0	0	0	VP59 [3:0]			05													
5 th Parameter	1	1	↑	XX	0	0	0	0	VP57 [4:0]																
6 th Parameter	1	1	↑	XX	0	0	0	0	VP50 [3:0]			09													
7 th Parameter	1	1	↑	XX	0	VP43 [6:0]																			
8 th Parameter	1	1	↑	XX	VP27 [3:0]				VP36 [3:0]																
9 th Parameter	1	1	↑	XX	0	VP20 [6:0]																			
10 th Parameter	1	1	↑	XX	0	0	0	0	VP13 [3:0]			0B													
11 th Parameter	1	1	↑	XX	0	0	0	0	VP6 [4:0]																
12 th Parameter	1	1	↑	XX	0	0	0	0	VP4 [3:0]			00													
13 th Parameter	1	1	↑	XX	0	0	VP2 [5:0]																		
14 th Parameter	1	1	↑	XX	0	0	VP1 [5:0]																		
15 th Parameter	1	1	↑	XX	0	0	0	0	VP0 [3:0]			00													
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default																									

8.3.25. Negative Gamma Correction (E1h)

E1h		NGAMCTRL (Negative Gamma Correction)																								
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	1	1	1	0	0	0	0	1	E1h													
1 st Parameter	1	1	↑	XX	0	0	0	0	VN63 [3:0]				08													
2 nd Parameter	1	1	↑	XX	0	0	VN62 [5:0]																			
3 rd Parameter	1	1	↑	XX	0	0	VN61 [5:0]																			
4 th Parameter	1	1	↑	XX	0	0	0	0	VN59 [3:0]				07													
5 th Parameter	1	1	↑	XX	0	0	0	0	VN57 [4:0]																	
6 th Parameter	1	1	↑	XX	0	0	0	0	VN50 [3:0]				05													
7 th Parameter	1	1	↑	XX	0	VN43 [6:0]																				
8 th Parameter	1	1	↑	XX	VN36 [3:0]				VN27 [3:0]																	
9 th Parameter	1	1	↑	XX	0	VN20 [6:0]																				
10 th Parameter	1	1	↑	XX	0	0	0	0	VN13 [3:0]				04													
11 th Parameter	1	1	↑	XX	0	0	0	0	VN6 [4:0]																	
12 th Parameter	1	1	↑	XX	0	0	0	0	VN4 [3:0]				0F													
13 th Parameter	1	1	↑	XX	0	0	VN2 [5:0]																			
14 th Parameter	1	1	↑	XX	0	0	VN1 [5:0]																			
15 th Parameter	1	1	↑	XX	0	0	0	0	VN0 [3:0]				0F													
Description	Set the gray scale voltage to adjust the gamma characteristics of the TFT panel.																									
Restriction	EXTC should be high to enable this command																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																									
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Sleep IN	Yes																									
Default																										

8.3.26. Digital Gamma Control 1 (E2h)

DGAMCTRL (Digital Gamma Control 1)																											
E2h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	1	0	0	0	1	0	E2h														
1 st Parameter	1	1	↑	XX	RCA0 [3:0]				BCA0 [3:0]				XX														
:	1	1	↑	XX	RCAx [3:0]				BCAx [3:0]				XX														
16 th Parameter	1	1	↑	XX	RCA15 [3:0]				BCA15 [3:0]				XX														
Description	RCAx [3:0]: Gamma Macro-adjustment registers for red gamma curve. BCAx [3:0]: Gamma Macro-adjustment registers for blue gamma curve.																										
Restriction	EXTC should be high to enable this command																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																										
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																										
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Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="2">Default Value</th> </tr> <tr> <th>RCAx [3:0]</th> <th>BCAx [3:0]</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>TBD</td> <td>TBD</td> </tr> <tr> <td>SW Reset</td> <td>TBD</td> <td>TBD</td> </tr> <tr> <td>HW Reset</td> <td>TBD</td> <td>TBD</td> </tr> </tbody> </table>													Status	Default Value		RCAx [3:0]	BCAx [3:0]	Power ON Sequence	TBD	TBD	SW Reset	TBD	TBD	HW Reset	TBD	TBD
Status	Default Value																										
	RCAx [3:0]	BCAx [3:0]																									
Power ON Sequence	TBD	TBD																									
SW Reset	TBD	TBD																									
HW Reset	TBD	TBD																									

8.3.27. Digital Gamma Control 2(E3h)

DGAMCTRL (Digital Gamma Control 2)																											
E3h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	1	0	0	0	1	1	E3h														
1 st Parameter	1	1	↑	XX	RFA0 [3:0]				BFA0 [3:0]				XX														
:	1	1	↑	XX	RFAX [3:0]				BFAX [3:0]				XX														
64 rd Parameter	1	1	↑	XX	RFA63 [3:0]				BFA63 [3:0]				XX														
Description	RFAX [3:0]: Gamma Micro-adjustment register for red gamma curve. BFAX [3:0]: Gamma Micro-adjustment register for blue gamma curve.																										
Restriction	EXTC should be high to enable this command																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																										
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																										
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																										
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																										
Sleep IN	Yes																										
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Status	Default Value																										
	RFAX [3:0]	BFAX [3:0]																									
Power ON Sequence	TBD	TBD																									
SW Reset	TBD	TBD																									
HW Reset	TBD	TBD																									

8.3.28. Interface Control (F6h)

IFCTL (16bits Data Format Selection)																													
F6h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F6h																
1 st Parameter	1	1	↑	XX	MY_EOR	MX_EOR	MV_EOR	0	BGR_EOR	0	0	WE MODE	01																
2 nd Parameter	1	1	↑	XX	0	0	EPF [1]	EPF [0]	0	0	MDT [1]	MDT [0]	00																
3 rd Parameter	1	1	↑	XX	0	0	ENDIAN	0	DM [1]	DM [0]	RM	RIM	00																
MY_EOR / MX_EOR / MV_EOR / BGR_EOR: The set value of MADCTL is used in the IC is derived as exclusive OR between 1st Parameter of IFCTL and MADCTL Parameter.																													
MDT [1:0]: Select the method of display data transferring. WEMODE: Memory write control WEMODE=0: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the exceeding data will be ignored. WEMODE=1: When the transfer number of data exceeds (EC-SC+1)*(EP-SP+1), the column and page number will be reset, and the exceeding data will be written into the following column and page.																													
ENDIAN: Select Little Endian Interface bit. At Little Endian mode, the host sends LSB data first.																													
<table border="1"> <thead> <tr> <th>ENDIAN</th><th>Data transfer Mode</th></tr> </thead> <tbody> <tr> <td>0</td><td>Normal (MSB first, default)</td></tr> <tr> <td>1</td><td>Little Endian (LSB first)</td></tr> </tbody> </table>															ENDIAN	Data transfer Mode	0	Normal (MSB first, default)	1	Little Endian (LSB first)									
ENDIAN	Data transfer Mode																												
0	Normal (MSB first, default)																												
1	Little Endian (LSB first)																												
Note: Little Endian is valid on only 65K 8-bit and 9-bit MCU interface mode.																													
Description																													
DM [1:0]: Select the display operation mode.																													
<table border="1"> <thead> <tr> <th>DM [1]</th><th>DM [0]</th><th>Display Operation Mode</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>Internal clock operation</td></tr> <tr> <td>0</td><td>1</td><td>RGB Interface Mode</td></tr> <tr> <td>1</td><td>0</td><td>VSYNC interface mode</td></tr> <tr> <td>1</td><td>1</td><td>Setting disabled</td></tr> </tbody> </table>															DM [1]	DM [0]	Display Operation Mode	0	0	Internal clock operation	0	1	RGB Interface Mode	1	0	VSYNC interface mode	1	1	Setting disabled
DM [1]	DM [0]	Display Operation Mode																											
0	0	Internal clock operation																											
0	1	RGB Interface Mode																											
1	0	VSYNC interface mode																											
1	1	Setting disabled																											
The DM [1:0] setting allows switching between internal clock operation mode and external display interface operation mode. However, switching between the RGB interface operation mode and the VSYNC interface operation mode is prohibited.																													

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RM: Select the interface to access the GRAM.

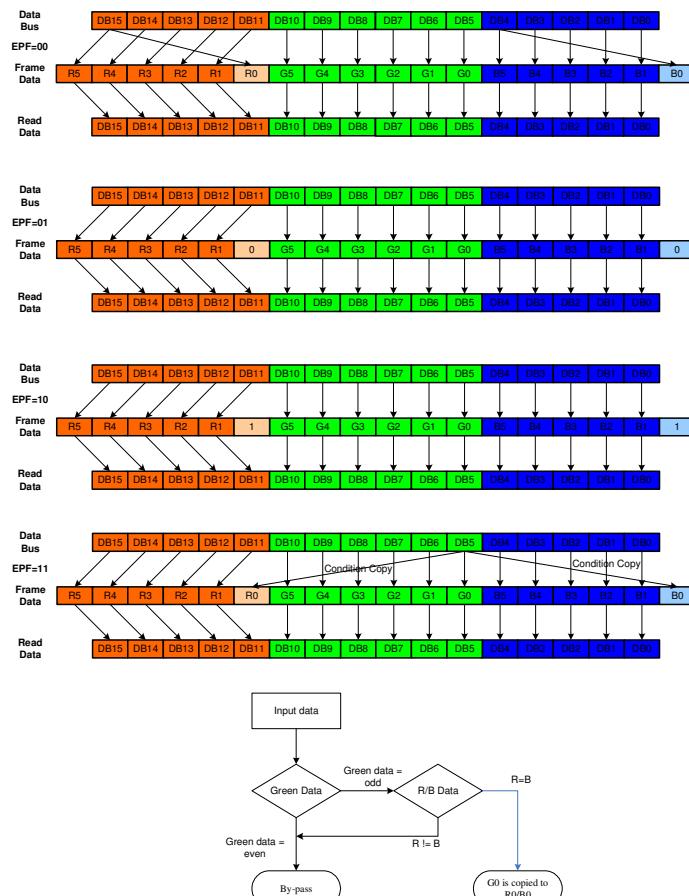
Set RM to "1" when writing display data by the RGB interface.

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

RIM: Specify the RGB interface mode when the RGB interface is used. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM	COLMOD [6:4]	RGB Interface Mode
0	110 (262K color)	18- bit RGB interface (1 transfer/pixel)
	101 (65K color)	16- bit RGB interface (1 transfer/pixel)
1	110 (262K color)	6- bit RGB interface (3 transfer/pixel)
	101 (65K color)	6- bit RGB interface (3 transfer/pixel)

EPF [1:0]: 65K color mode data format.



	<table border="1"> <thead> <tr> <th>EPF [1:0]</th><th>Expand 16 bbp (R,G,B) to 18bbp (R,G,B)</th></tr> </thead> <tbody> <tr> <td>00</td><td> <p>MSB is inputted to LSB $r[5:0] = \{R[4:0], R[4]\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], B[4]\}$</p> </td></tr> <tr> <td>01</td><td> <p>“0” is inputted to LSB $r[5:0] = \{R[4:0], 0\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 0\}$</p> <p>Exception: $R[4:0], B[4:0] = 5'h1F \rightarrow r[5:0], b[5:0] = 6'h3F$</p> </td></tr> <tr> <td>10</td><td> <p>“1” is inputted to LSB $r[5:0] = \{R[4:0], 1\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 1\}$</p> <p>Exception: $R[4:0], B[4:0] = 5'h00 \rightarrow r[5:0], b[5:0] = 6'h00$</p> </td></tr> <tr> <td>11</td><td> <p>Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → $r[5:0] = \{R[4:0], G[0]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], G[0]\}$ Case 2: R=B≠G → $r[5:0] = \{R[4:0], R[4]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], B[0]\}$ Case 3: R=G≠B → $r[5:0] = \{R[4:0], G[0]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], B[0]\}$ Case 4: B=G≠R → $r[5:0] = \{R[4:0], R[4]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], G[0]\}$</p> </td></tr> </tbody> </table>	EPF [1:0]	Expand 16 bbp (R,G,B) to 18bbp (R,G,B)	00	<p>MSB is inputted to LSB $r[5:0] = \{R[4:0], R[4]\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], B[4]\}$</p>	01	<p>“0” is inputted to LSB $r[5:0] = \{R[4:0], 0\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 0\}$</p> <p>Exception: $R[4:0], B[4:0] = 5'h1F \rightarrow r[5:0], b[5:0] = 6'h3F$</p>	10	<p>“1” is inputted to LSB $r[5:0] = \{R[4:0], 1\}$ $g[5:0] = \{G[5:0]\}$ $b[5:0] = \{B[4:0], 1\}$</p> <p>Exception: $R[4:0], B[4:0] = 5'h00 \rightarrow r[5:0], b[5:0] = 6'h00$</p>	11	<p>Compare R [4:0], G [5:1], B [4:0] case: Case 1: R=G=B → $r[5:0] = \{R[4:0], G[0]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], G[0]\}$ Case 2: R=B≠G → $r[5:0] = \{R[4:0], R[4]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], B[0]\}$ Case 3: R=G≠B → $r[5:0] = \{R[4:0], G[0]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], B[0]\}$ Case 4: B=G≠R → $r[5:0] = \{R[4:0], R[4]\}$, $g[5:0] = \{G[5:0]\}$, $b[5:0] = \{B[4:0], G[0]\}$</p>																													
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Status	Default Value																																							
	EPF [1:0]	MDT [1:0]	ENDIAN	WEMODE	DM [1:0]	RM	RIM																																	
Power ON Sequence	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0																																	
SW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0																																	
HW Reset	2'b00	2'b00	1'b0	1'b1	2'b00	1'b0	1'b0																																	

8.4 Description of Extend register command

8.4.1 Power control A (CBh)

CBh	Power control A																										
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	CBh														
1 st Parameter	1	1	↑	XX	0	0	1	1	1	0	0	1	39														
2 nd Parameter	1	1	↑	XX	0	0	1	0	1	1	0	0	2C														
3 rd Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00														
4 th Parameter	1	1	↑	XX	0	0	1	1	0	REG_VD[2:0]			34														
5 th Parameter	1	1	↑	XX	0	0	0	0	0	VBC[2:0]			02														
Description	REG_VD[2:0]: vcose control																										
	REG_VD[2:0]		Vcore(V)																								
	000		1.55																								
	001		1.4																								
	010		1.5																								
	011		1.65																								
	100		1.6																								
	101		1.7																								
	110		reserved																								
	111		reserved																								
Restriction	VBC[2:0]: dddvh control																										
	VBC[2:0]		DDVDH(V)																								
	000		5.8																								
	001		5.7																								
	010		5.6																								
	011		5.5																								
	100		5.4																								
	101		5.3																								
	110		5.2																								
	111		Reserved																								
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	Partial Mode ON, Idle Mode ON, Sleep OUT																										
	Sleep IN																										
Default	Status																										
	Parameter1																										
	Power ON Sequence																										
	SW Reset																										
	HW Reset																										

8.4.2 Power control B (CFh)

CFh	Power control B																															
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	1	0	0	1	1	1	1	CFh																			
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	0	0	00																			
2 nd Parameter	1	1	↑	XX	1	PCEQ	DRV_ena	Power control[1:0]		0	0	1	81																			
3 rd Parameter	1	1	↑	XX	DRV_vml[2:1]		1	DC_ena	DRV_vml[0]	DRV_vmh[2:0]		30																				
Description	<p>2nd parameter: power control[1:0]</p> <p>Only setting power control [1:0]=11, the VGH and VGL voltage level follow the table below.</p> <table border="1"> <tr> <th>BT [2:0]</th> <th>DDVDH</th> <th>VGH</th> <th>VGL</th> </tr> <tr> <td>0 0 0</td> <td rowspan="4">VCI x 2</td> <td>-VCI x 4</td> <td></td> </tr> <tr> <td>0 0 1</td> <td>-VCI x 3</td> <td></td> </tr> <tr> <td>0 1 0</td> <td>-VCI x 4</td> <td></td> </tr> <tr> <td>0 1 1</td> <td>-VCI x 3</td> <td></td> </tr> </table> <p>bit[5]: DRV_ena : For VCOM driving ability enhancement, DRV_ena = 1: Enable, and vice versa</p> <p>bit[6]: PCEQ: PC and EQ operation for power saving</p> <p>0:disable this function</p> <p>1:enable this function</p> <p>3rd parameter: default: 30h</p> <p>bit[2:0]: DRV_vmh[2:0] 3'b000 adjust over drive width for VMH(000: 1 op_clk ~111: 8 op_clk)</p> <p>bit[3]: DRV_vml[0] 1'b0</p> <p>bit[4]: DC_ena: Discharge path enable. Enable high for ESD protection, 1: enable and vice versa</p> <p>bit[7:6] : DRV_vml[2:1] 2'b00</p>													BT [2:0]	DDVDH	VGH	VGL	0 0 0	VCI x 2	-VCI x 4		0 0 1	-VCI x 3		0 1 0	-VCI x 4		0 1 1	-VCI x 3			
BT [2:0]	DDVDH	VGH	VGL																													
0 0 0	VCI x 2	-VCI x 4																														
0 0 1		-VCI x 3																														
0 1 0		-VCI x 4																														
0 1 1		-VCI x 3																														
Restriction	EXTC should be high to enable this command																															
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Status	Availability																															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Sleep IN	Yes																															
Default	<table border="1"> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>Parameter1</th> <th>Parameter2</th> <th>Parameter3</th> </tr> <tr> <td>Power ON Sequence</td> <td>00</td> <td>A2</td> <td>F0</td> </tr> <tr> <td>SW Reset</td> <td>00</td> <td>A2</td> <td>F0</td> </tr> <tr> <td>HW Reset</td> <td>00</td> <td>A2</td> <td>F0</td> </tr> </table>													Status	Default Value			Parameter1	Parameter2	Parameter3	Power ON Sequence	00	A2	F0	SW Reset	00	A2	F0	HW Reset	00	A2	F0
Status	Default Value																															
	Parameter1	Parameter2	Parameter3																													
Power ON Sequence	00	A2	F0																													
SW Reset	00	A2	F0																													
HW Reset	00	A2	F0																													

8.4.3 Driver timing control A (E8h)

F6h		Driver timing control A																															
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	1	1	0	1	0	0	0	0	E8h																			
1 st Parameter	1	1	↑	XX	1	0	0	0	0	1	0	NOW		84																			
2 nd Parameter	1	1	↑	XX	0	0	0	EQ	0	0	0	CR		11																			
3 rd Parameter	1	1	↑	XX	0	1	1	1	1	0	PC[1:0]			7A																			
Description	EQ timing for Internal clock 1 st parameter:gate driver non-overlap timing control 0:default non-overlap time 1:default + 1unit 2 nd parameter:EQ timing control 0: default – 1unit 1:default EQ timing parameter:CR timing control 0: default – 1unit 1:default CR timing 3 rd parameter:pre-charge timing control 11: reserved 10: default pre-charge timing 01:default – 1unit 00:default – 2unit																																
Restriction	EXTC should be high to enable this command																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes							
Status	Availability																																
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																																
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																																
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																
Sleep IN	Yes																																
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>Parameter1</th> <th>Parameter2</th> <th>Parameter3</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>84</td> <td>11</td> <td>7A</td> </tr> <tr> <td>SW Reset</td> <td>84</td> <td>11</td> <td>7A</td> </tr> <tr> <td>HW Reset</td> <td>84</td> <td>11</td> <td>7A</td> </tr> </tbody> </table>														Status	Default Value			Parameter1	Parameter2	Parameter3	Power ON Sequence	84	11	7A	SW Reset	84	11	7A	HW Reset	84	11	7A
Status	Default Value																																
	Parameter1	Parameter2	Parameter3																														
Power ON Sequence	84	11	7A																														
SW Reset	84	11	7A																														
HW Reset	84	11	7A																														

8.4.4 Driver timing control A (E9h)

Driver timing control A																																
F6h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	0	1	↑	XX	1	1	1	0	1	0	0	0	E8h																			
1 st Parameter	1	1	↑	XX	1	0	0	0	0	1	0	NOWE	84																			
2 nd Parameter	1	1	↑	XX	0	0	0	EQE	0	0	0	CRE	11																			
3 rd Parameter	1	1	↑	XX	0	1	1	1	1	0	PCE[1:0]		7A																			
Description	EQE timing for External clock 1 st parameter:gate driver non-overlap timing control 0:default non-overlap time 1:default + 1unit 2 nd parameter:EQE timing control 0: default – 1unit 1:default EQE timing parameter:CRE timing control 0: default – 1unit 1:default CRE timing 3 rd parameter:pre-charge timing control 11: reserved 10: default pre-charge timing 01:default – 1unit 00:default – 2unit																															
Restriction	EXTC should be high to enable this command																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes							
Status	Availability																															
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																															
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																															
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Status	Default Value																															
	Parameter1	Parameter2	Parameter3																													
Power ON Sequence	84	11	7A																													
SW Reset	84	11	7A																													
HW Reset	84	11	7A																													

8.4.5 Driver timing control B (EAh)

F6h		Driver timing control B																										
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command		0	1	↑	XX	1	1	1	0	1	0	1	0	EAh														
1 st Parameter		1	1	↑	XX	VG_SW_T4		VG_SW_T3		VG_SW_T2		VG_SW_T1		66														
2 nd Parameter		1	1	↑	XX	X	X	X	X	X	X	0	0	00														
Description		1 st parameter:gate driver timing control VG_SW_T1[1:0]:EQ to GND VG_SW_T2[1:0]:EQ to DDVDH VG_SW_T3[1:0]:EQ to DDVDH VG_SW_T4[1:0]:EQ to GND 00: 0 unit 01: 1 unit 10: 2 unit 11: 3 unit																										
Restriction		EXTC should be high to enable this command																										
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes		
Status	Availability																											
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																											
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																											
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																											
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																											
Sleep IN	Yes																											
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Status	Default Value																											
	Parameter1	Parameter2																										
Power ON Sequence	66	00																										
SW Reset	66	00																										
HW Reset	66	00																										

8.4.6 Power on sequence control (EDh)

F6h		Power on sequence control																																				
		D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																								
Command		0	1	↑	XX	1	1	1	0	1	1	0	1	EDh																								
1 st Parameter		1	1	↑	XX	X	1	CP1 soft start		X	1	CP23 soft start		55																								
2 nd Parameter		1	1	↑	XX	X	0	En_vcl		X	0	En_ddvdh		01																								
3 rd Parameter		1	1	↑	XX	X	0	En_vgh		X	0	En_vgl		23																								
4 th Parameter		1	1	↑	XX	DDVDH_ENH	0	0	0	0	0	0	1	1																								
Description		1 st parameter:soft start control 00:soft start keep 3 frame 01:soft start keep 2 frame 01:soft start keep 1 frame 11:disable 2 nd / 3 rd parameter:power on sequence control 00:1 st frame enable 01:2 nd frame enable 10:3 rd frame enable 11:4 th frame enable 4 th parameter:DDVDH enhance mode(only for 8 external capacitors) 0: disable 1: enable																																				
Restriction		EXTC should be high to enable this command																																				
Register Availability		<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes												
Status	Availability																																					
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																																					
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Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																																					
Sleep IN	Yes																																					
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Status	Default Value																																					
	Parameter1	Parameter2	Parameter3	Parameter4																																		
Power ON Sequence	55	01	23	01																																		
SW Reset	55	01	23	01																																		
HW Reset	55	01	23	01																																		

8.4.7 Enable 3G (F2h)

Enable_3G																									
F6h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	XX	1	1	1	1	0	0	1	0	F2h												
1 st Parameter	1	1	↑	XX	0	0	0	0	0	0	1	3G_enb	02												
Description	1 st Parameter: Enable 3 gamma control 3G_enb high for 3 gamma control enable																								
Restriction	EXTC should be high to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																								
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																								
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																								
Sleep IN	Yes																								
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>Parameter1</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>02</td> </tr> <tr> <td>SW Reset</td> <td>02</td> </tr> <tr> <td>HW Reset</td> <td>02</td> </tr> </tbody> </table>													Status	Default Value	Parameter1	Power ON Sequence	02	SW Reset	02	HW Reset	02			
Status	Default Value																								
	Parameter1																								
Power ON Sequence	02																								
SW Reset	02																								
HW Reset	02																								

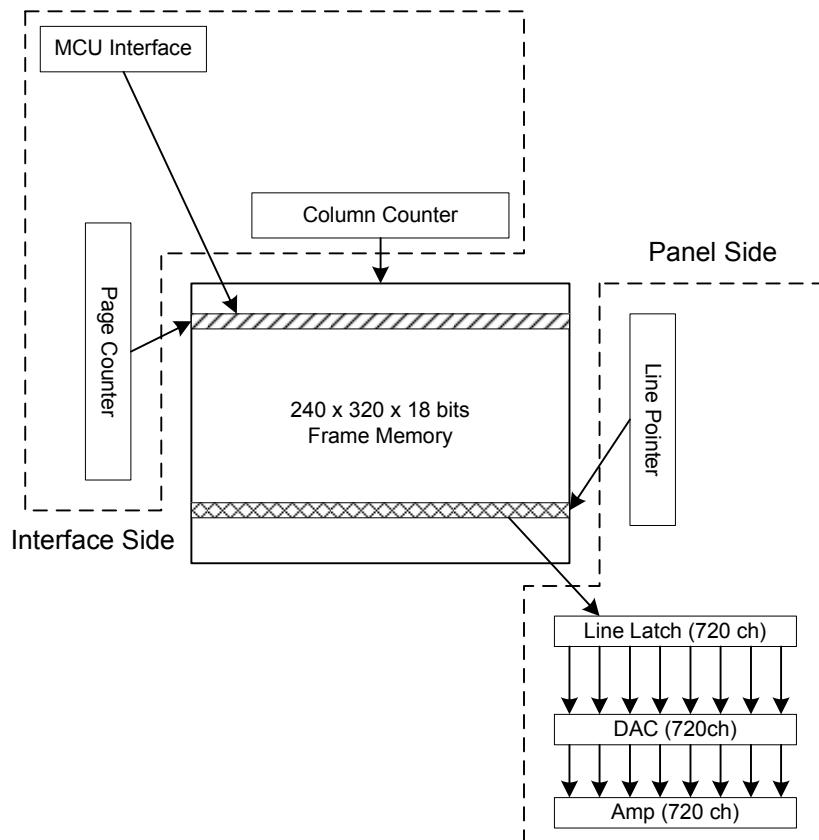
8.4.8 Pump ratio control (F7h)

Pump ratio control																										
F6h	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	XX	1	1	1	1	0	1	1	0	F7h													
1 st Parameter	1	1	↑	XX	X	X	Ratio[1:0]		0	0	0	0	10													
Description	1 st parameter:ratio control 00:reserved 01:reserved 10:DDVDH=2xVCI 11:DDVDH=3xVCI																									
Restriction	EXTC should be high to enable this command																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Normal Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode OFF, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Partial Mode ON, Idle Mode ON, Sleep OUT</td> <td>Yes</td> </tr> <tr> <td>Sleep IN</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes	Normal Mode ON, Idle Mode ON, Sleep OUT	Yes	Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes	Partial Mode ON, Idle Mode ON, Sleep OUT	Yes	Sleep IN	Yes
Status	Availability																									
Normal Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Normal Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode OFF, Sleep OUT	Yes																									
Partial Mode ON, Idle Mode ON, Sleep OUT	Yes																									
Sleep IN	Yes																									
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th>Default Value</th> </tr> <tr> <th>Parameter1</th> </tr> </thead> <tbody> <tr> <td>Power ON Sequence</td> <td>10</td> </tr> <tr> <td>SW Reset</td> <td>10</td> </tr> <tr> <td>HW Reset</td> <td>10</td> </tr> </tbody> </table>														Status	Default Value	Parameter1	Power ON Sequence	10	SW Reset	10	HW Reset	10			
Status	Default Value																									
	Parameter1																									
Power ON Sequence	10																									
SW Reset	10																									
HW Reset	10																									

9. Display Data RAM

9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

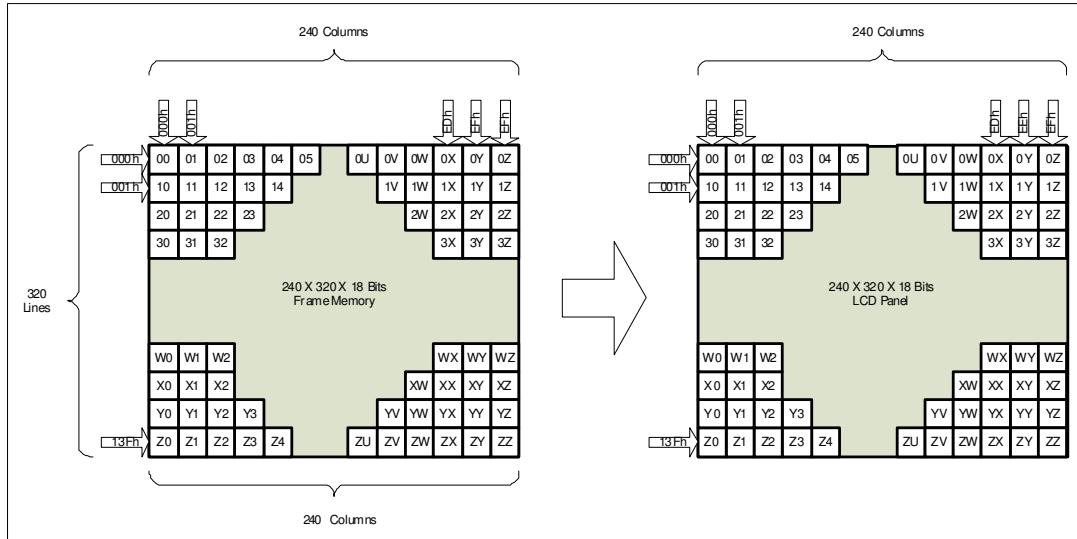


9.2. Memory to Display Address Mapping

9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

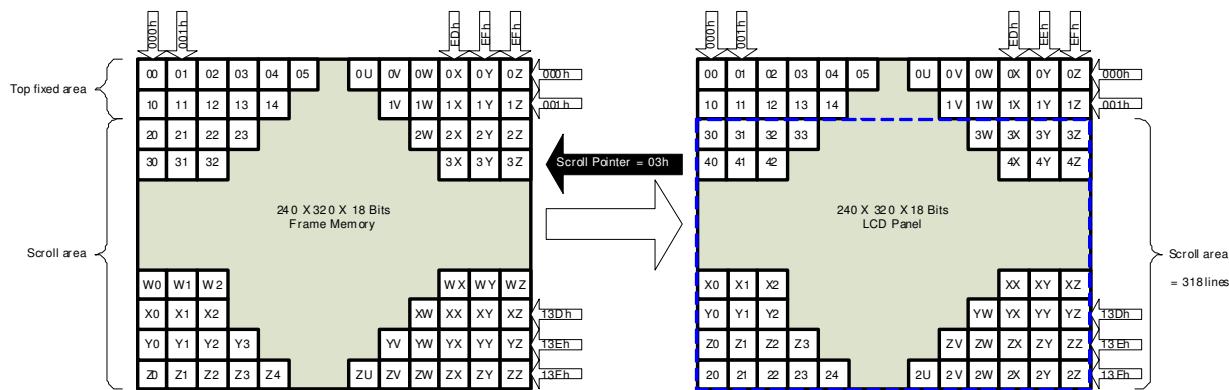


9.2.2. Vertical Scroll Mode

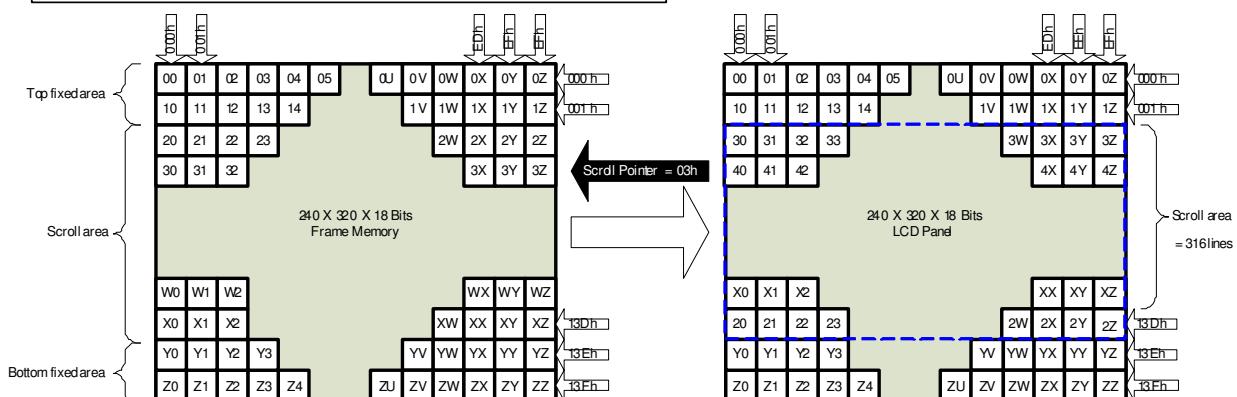
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

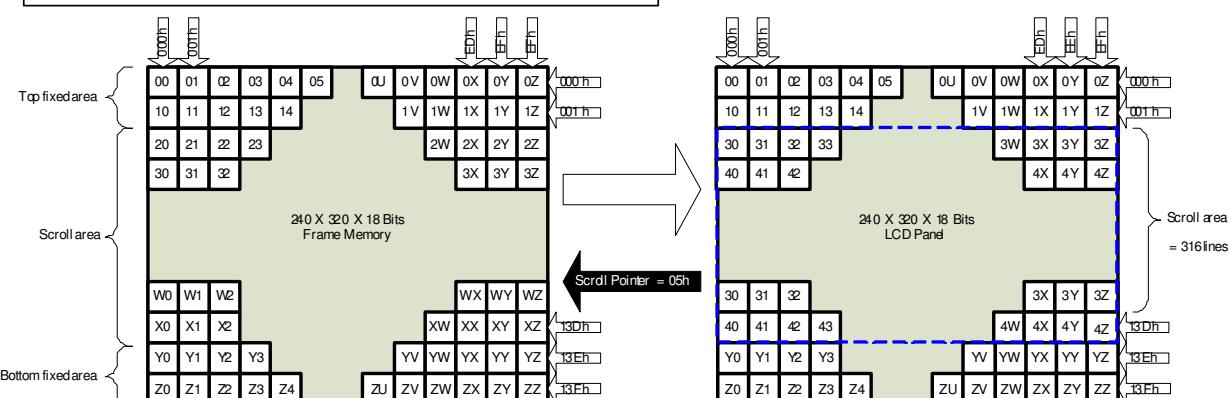
TFA=2, VSA=318, BFA=0 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=2 when MADCTL ML bit = 0



TFA=2, VSA=316, BFA=4 when MADCTL ML bit = 0



Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

9.2.3. Vertical Scroll Example

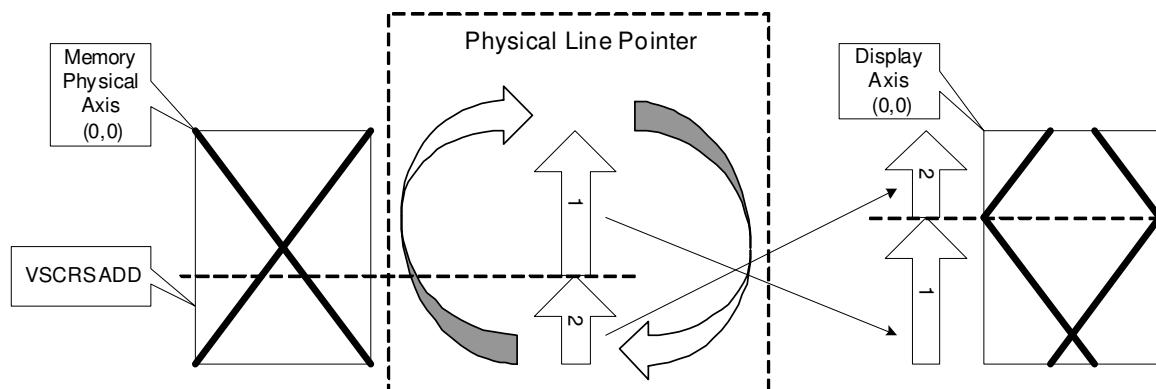
9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

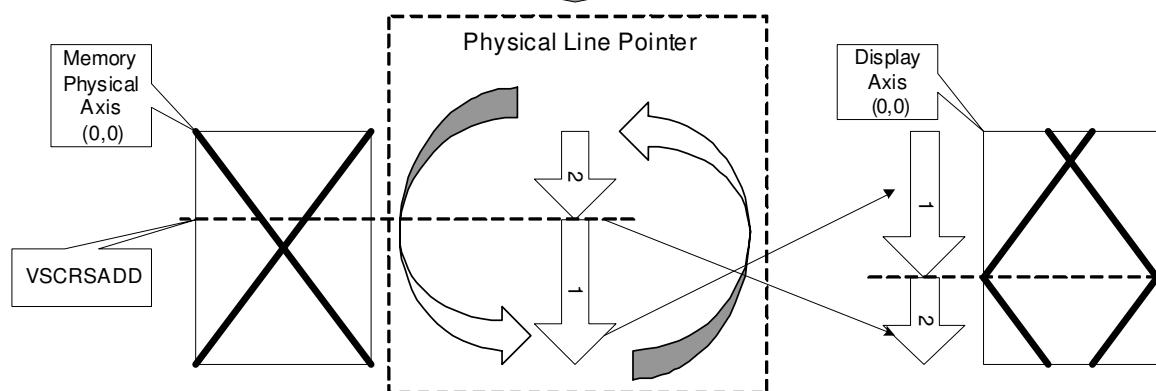
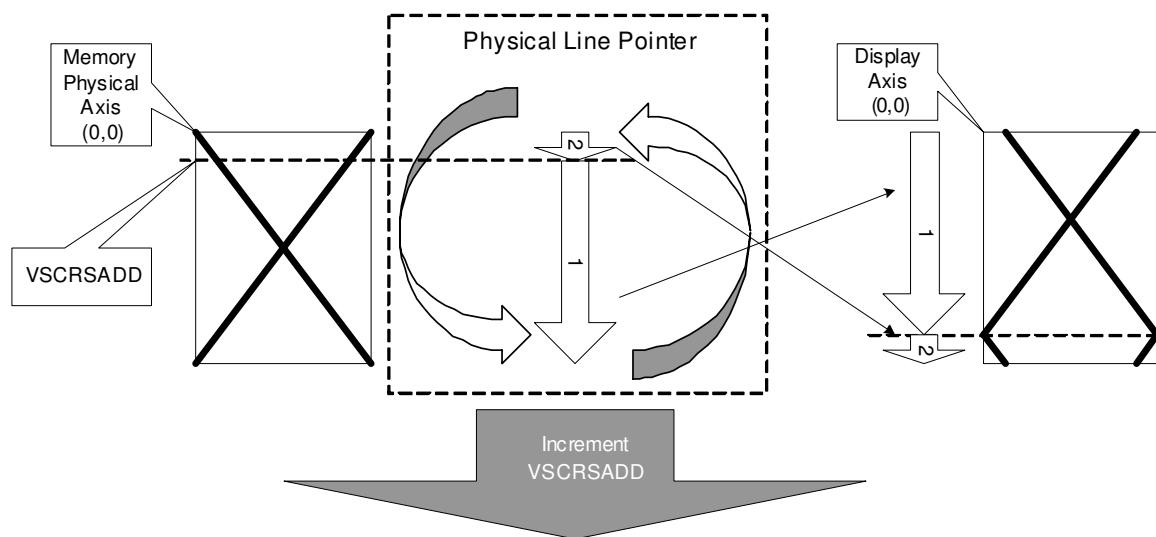
9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

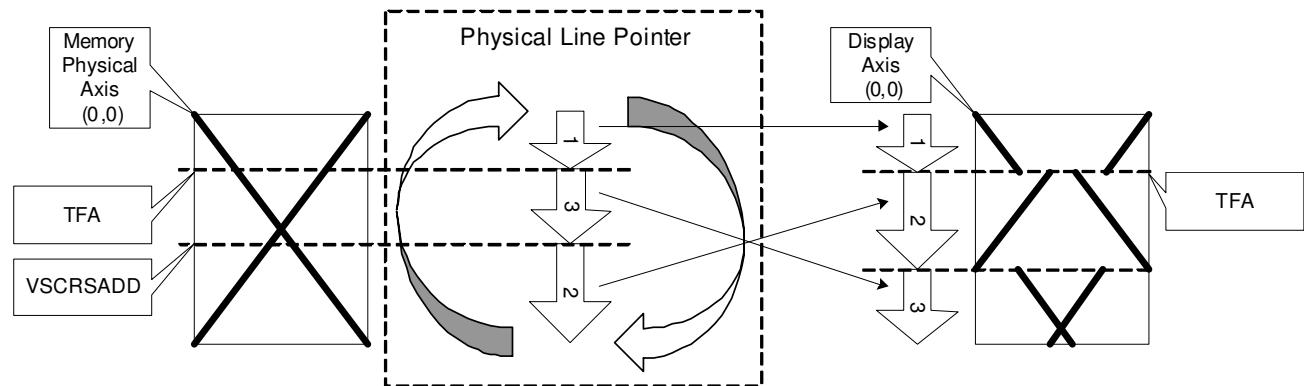
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 1



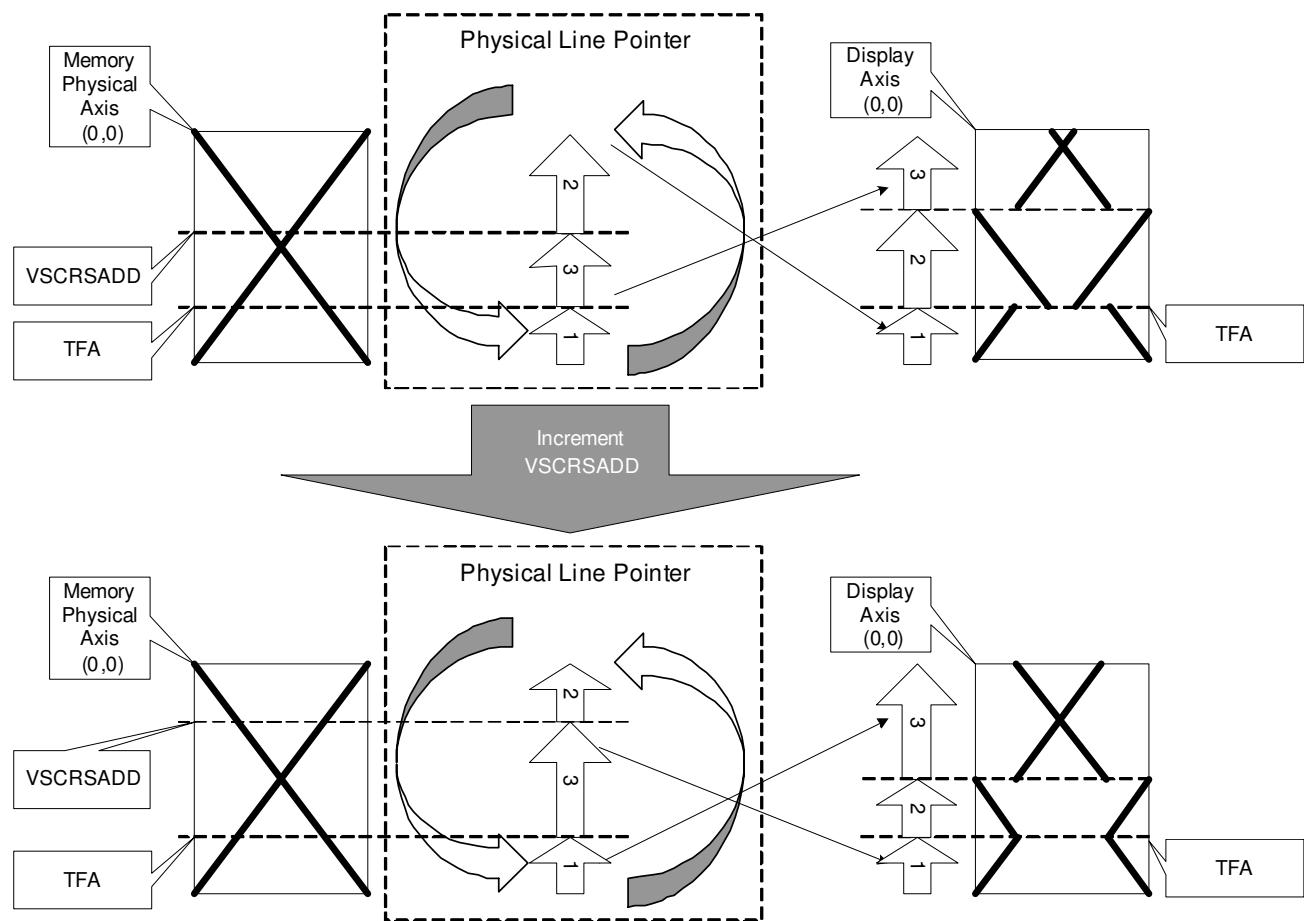
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



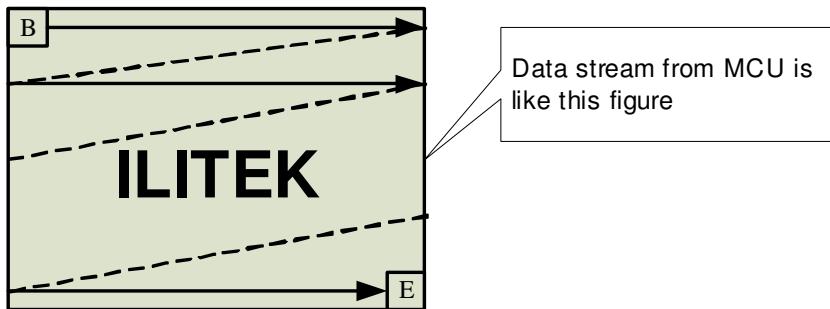
When TFA=30, VSA=290, BFA=0, VSCRADD=80 and MADCTL ML bit = 0



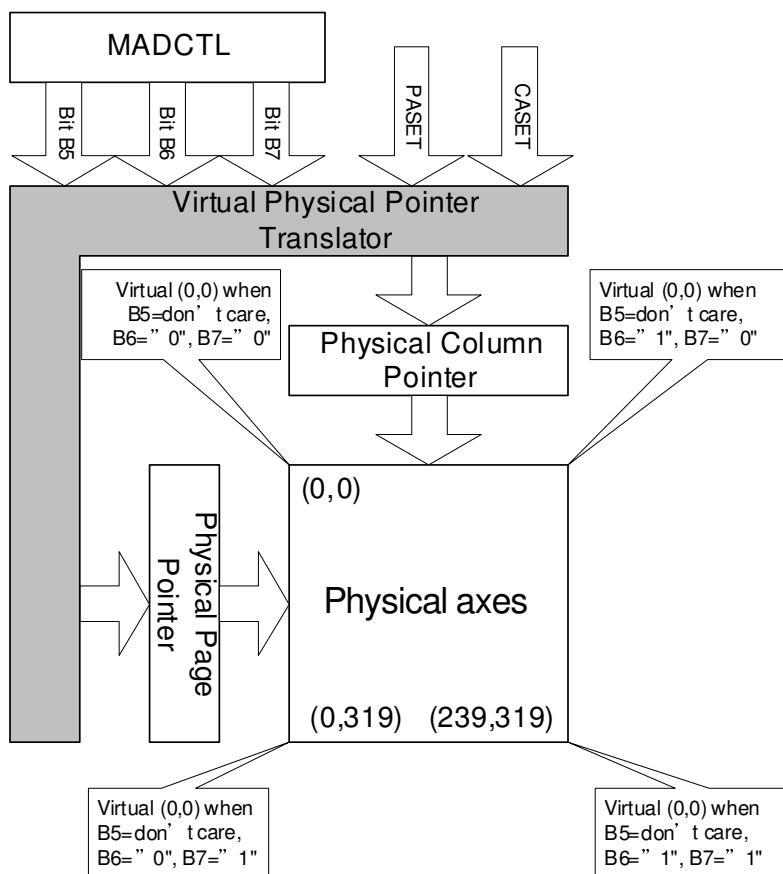
When TFA=30, VSA=290, BFA=0, VSCRADD=80 and MADCTL ML bit = 1



9.3. MCU to memory write/read direction



The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by "Memory Data Access Control" Command, Bits B5, B6, and B7 as described below.



B5	B6	B7	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (319-Physical Page Pointer)
0	1	0	Direct to (319-Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (319-Physical Column Pointer)	Direct to (319-Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (319-Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (319-Physical Column Pointer)
1	1	1	Direct to (319-Physical Page Pointer)	Direct to (319-Physical Column Pointer)
Condition			Column Counter	Page counter
When RAMWR/RAMRD command is accepted			Return to "Start column"	Return to "Start Page"
Complete Pixel Read/Write action			Increment by 1	No change
The Column values is large than "End Column"			Return to "Start column"	Increment by 1
The Page counter is large than "End Page"			Return to "Start column"	Return to "Start Page"

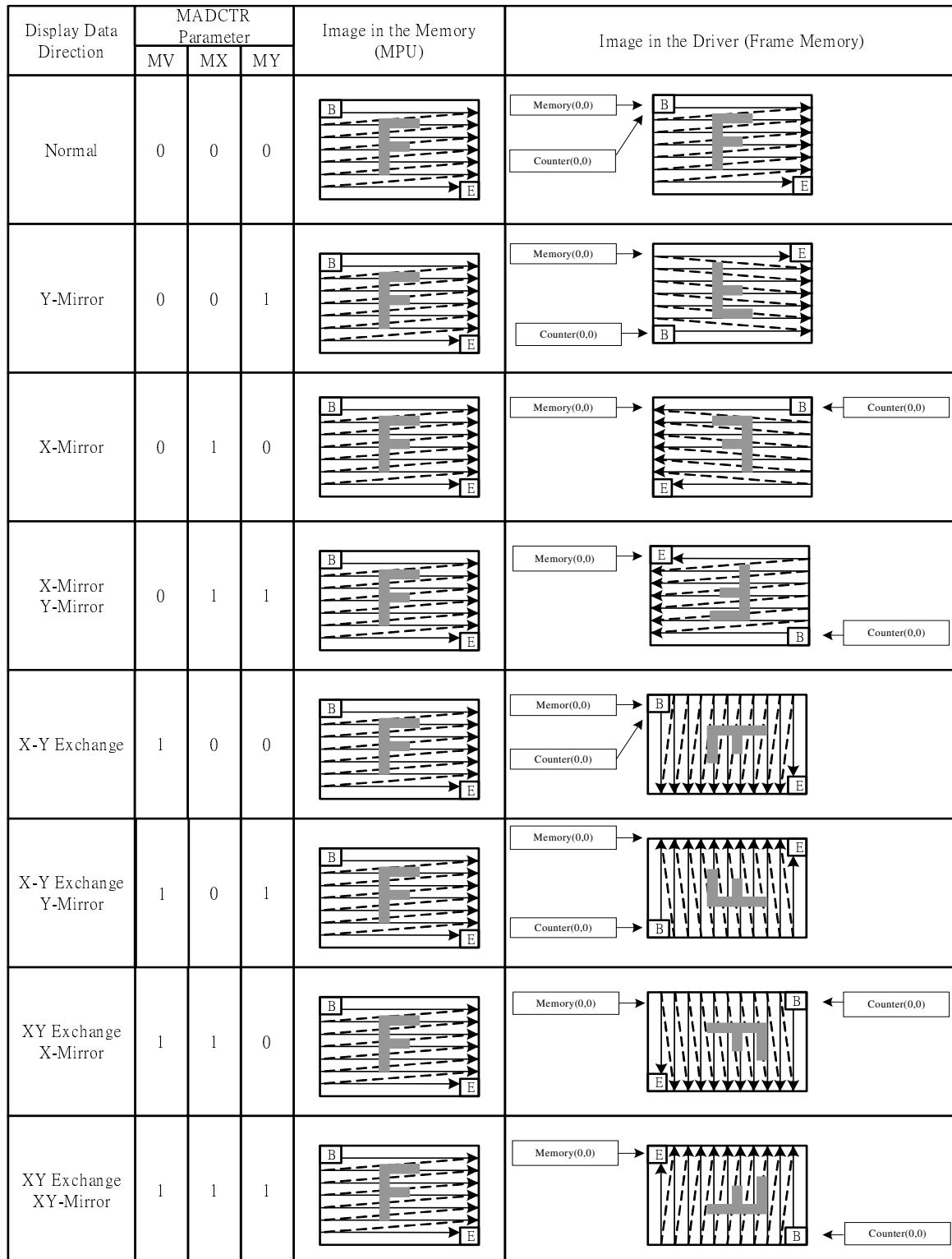
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Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.



10. Tearing Effect Output

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the parameter of the Tearing Effect Line Off & On commands.

The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

10.1. Tearing Effect Line Modes

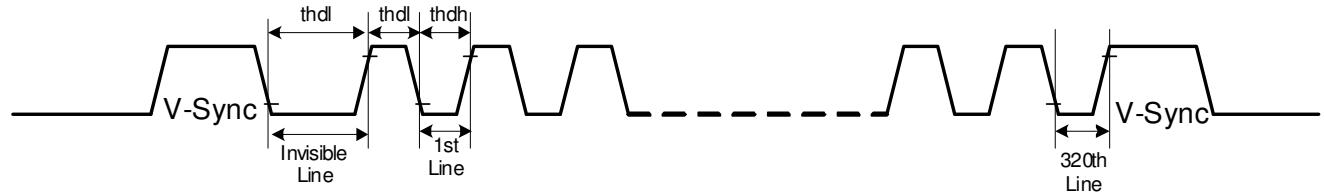
Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



tvdh = The LCD display is not updated from the Frame Memory.

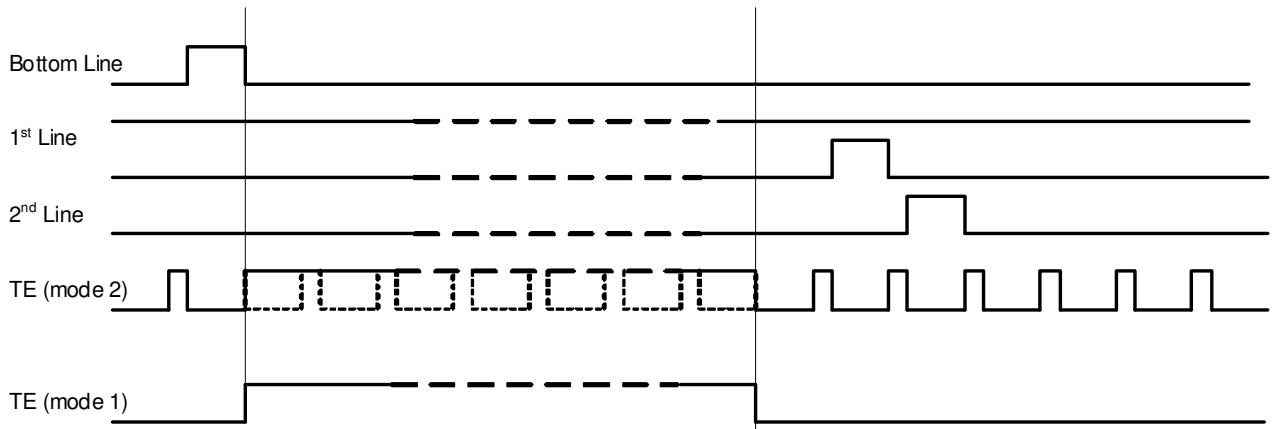
tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the tearing effect output signal consists of V-Sync and H-Sync information; there is one V-sync and 320 H-sync pulses per field:



thdh = The LCD display is not updated from the Frame Memory.

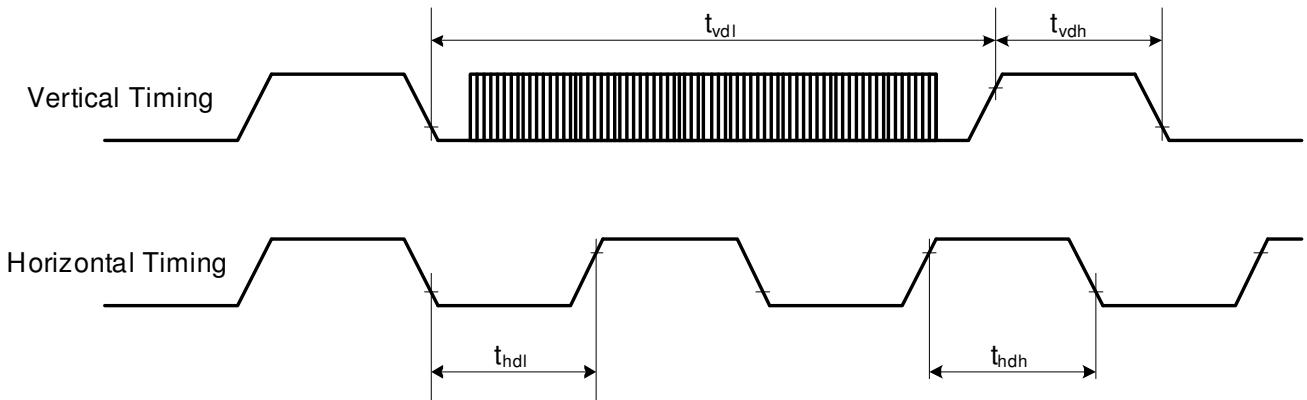
thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

10.2. Tearing Effect Line Timings

The tearing effect signal is described below:

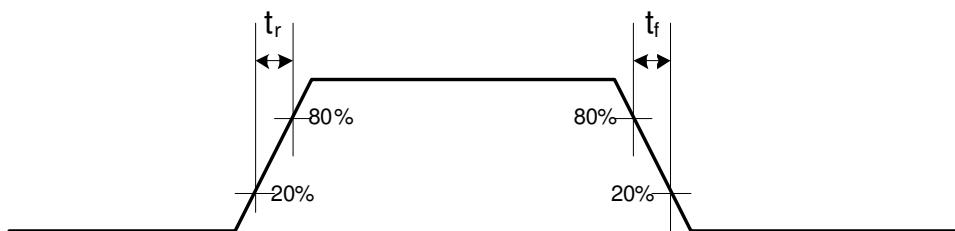


AC characteristics of Tearing Effect Signal (Frame Rate = 60Hz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{vdl}	Vertical timing low duration	--	--	--	ms	
t_{vdh}	Vertical timing high duration	1000	--	--	us	
t_{hdl}	Horizontal timing low duration	--	--	--	us	
t_{hdh}	Horizontal timing high duration	--	--	500	us	

Note:

1. The timings in Table as above apply when MADCTL B4=0 and B4=1
2. The signal's rise and fall times (t_f , t_r) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

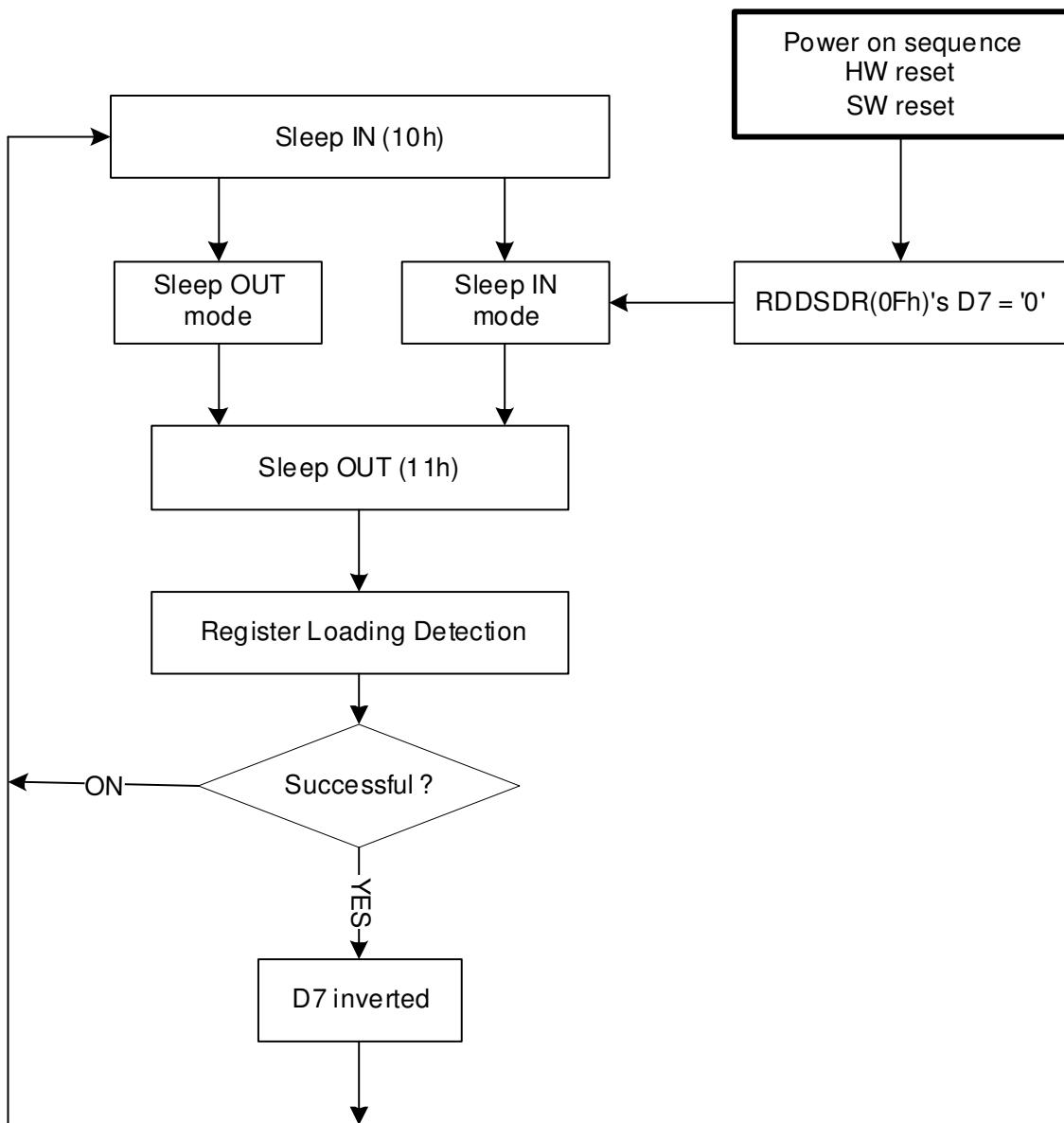
11. Sleep Out – Command and Self-Diagnostic Functions of the Display Module

11.1. Register loading Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from EV Memory(or similar device) to registers of the display controller is working properly.

If the register loading detection is successfully, there is inverted (= increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D7). If it is failure, this bit (D7) is not inverted (= not increased by 1).

The flow chart for this internal function is following:

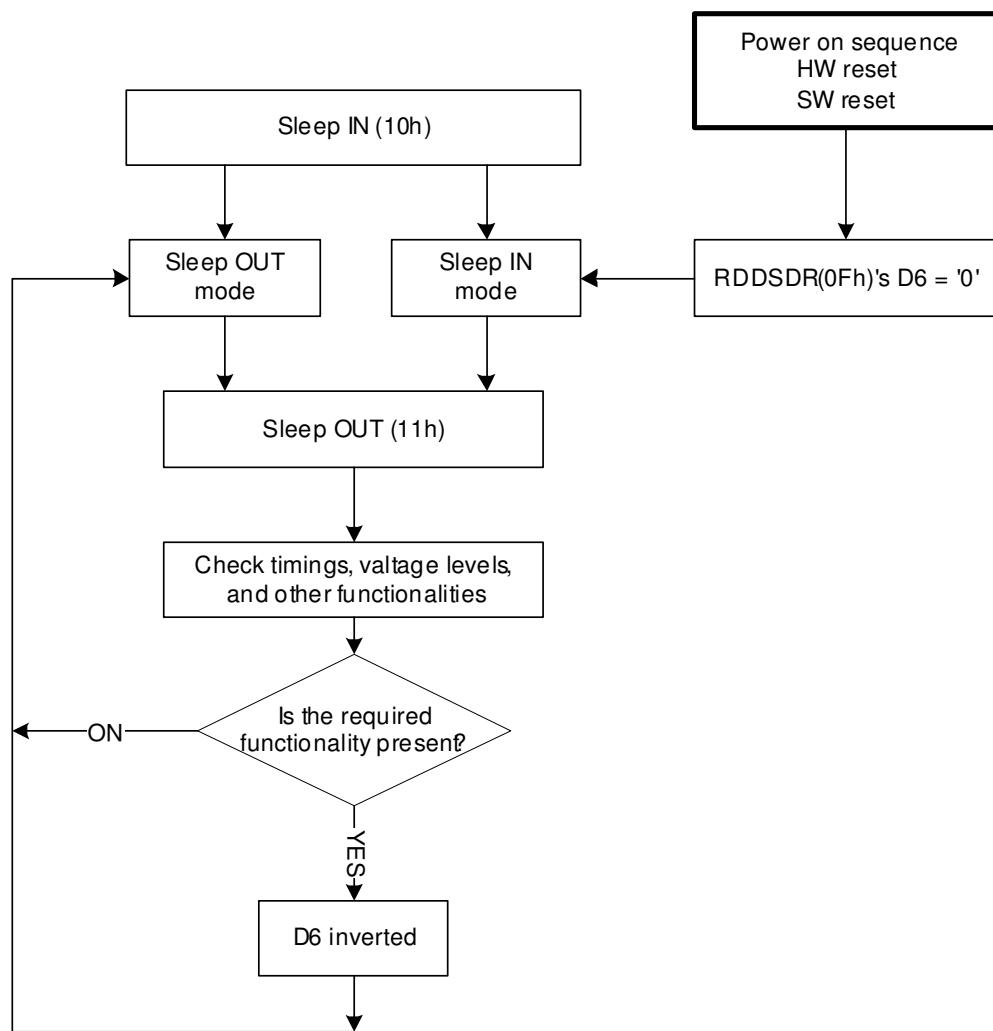


11.2. Functionality Detection

Sleep Out-command (Command “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (e.g. booster voltage levels, timings, etc.) If functionality requirement is met, there is an inverted (= increased by 1) bit, which defined in command “Read Display Self-Diagnostic Result (0Fh)” (= RDDSDR) (The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted (= increased by 1). The flow chart for this internal function is shown as below.

The flow chart for this internal function is following:



Note 1: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In –mode to Sleep Out -mode, before there is possible to check if User's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

12. Power ON/OFF Sequence

VDDI and VCI can be applied in any order.

VCI and VDDI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and VDDI must be powered down minimum 120msec after RESX has been released.

During power off, if LCD is in the Sleep In mode, VDDI or VCI can be powered down minimum 0msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no damage to the display module if the power sequences are not met.

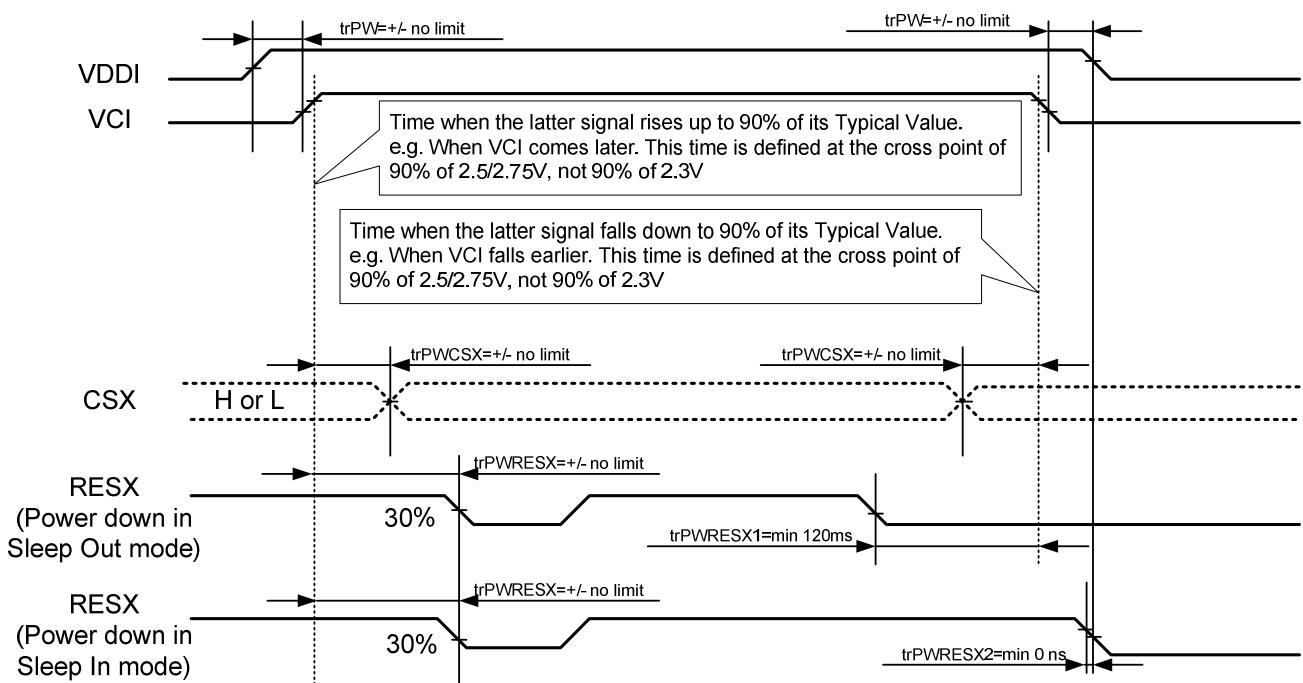
Note 2: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 3: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 4: If RESX line is not held stable by host during Power On Sequence as defined in Sections 12.1 and 12.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

12.1. Case 1 – RESX line is held High or Unstable by Host at Power ON

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



$trPWRESX1$ is applied to RESX falling in the Sleep Out Mode

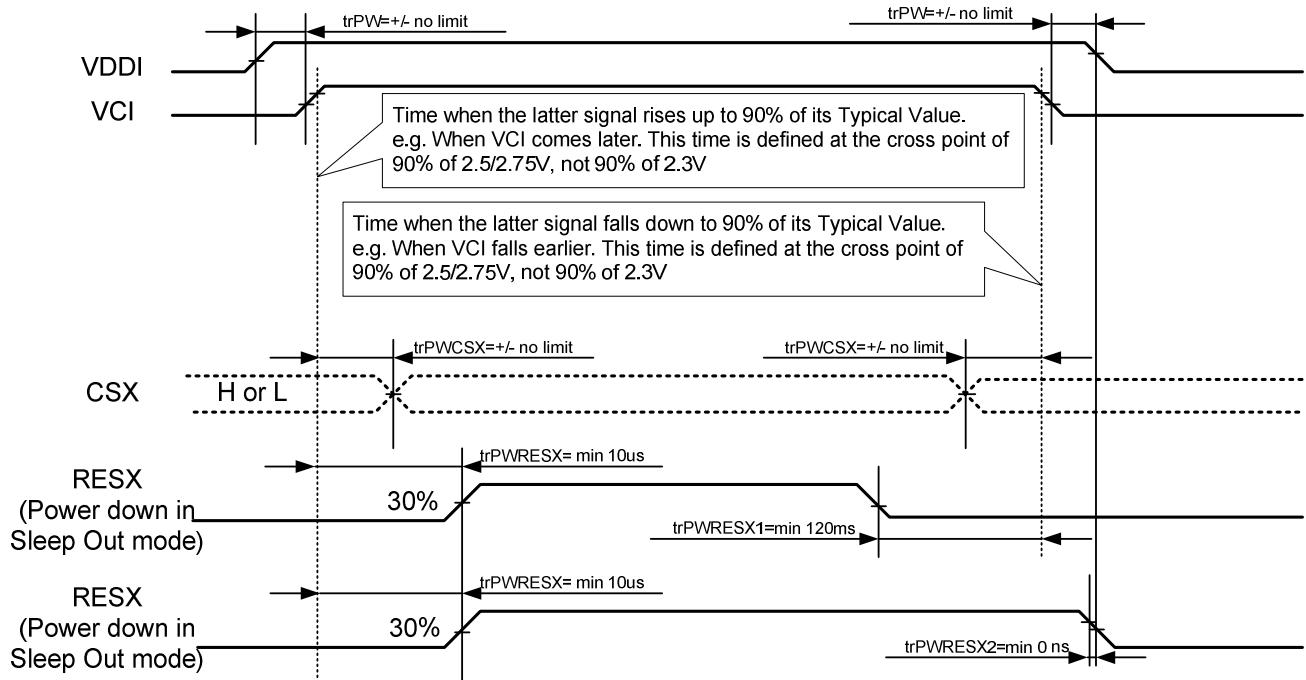
$trPWRESX2$ is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

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12.2. Case 2 – RESX line is held Low by Host at Power ON

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10 μ sec after both VCI and VDDI have been applied.



$t_{PWRESX1}$ is applied to RESX falling in the Sleep Out Mode
 $t_{PWRESX2}$ is applied to RESX falling in the Sleep In Mode

Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal power level.

12.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off event, ILI9341 will force the display to blank and will not be any abnormal visible effects within 1 second on the display and remains blank until "Power On Sequence" activates.

13. Power Level Definition

13.1. Power Levels

7 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.

In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.

In this mode part of the display is used with maximum 262,144 colors.

3. Normal Mode On (full display), Idle Mode On, Sleep Out.

In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.

In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode.

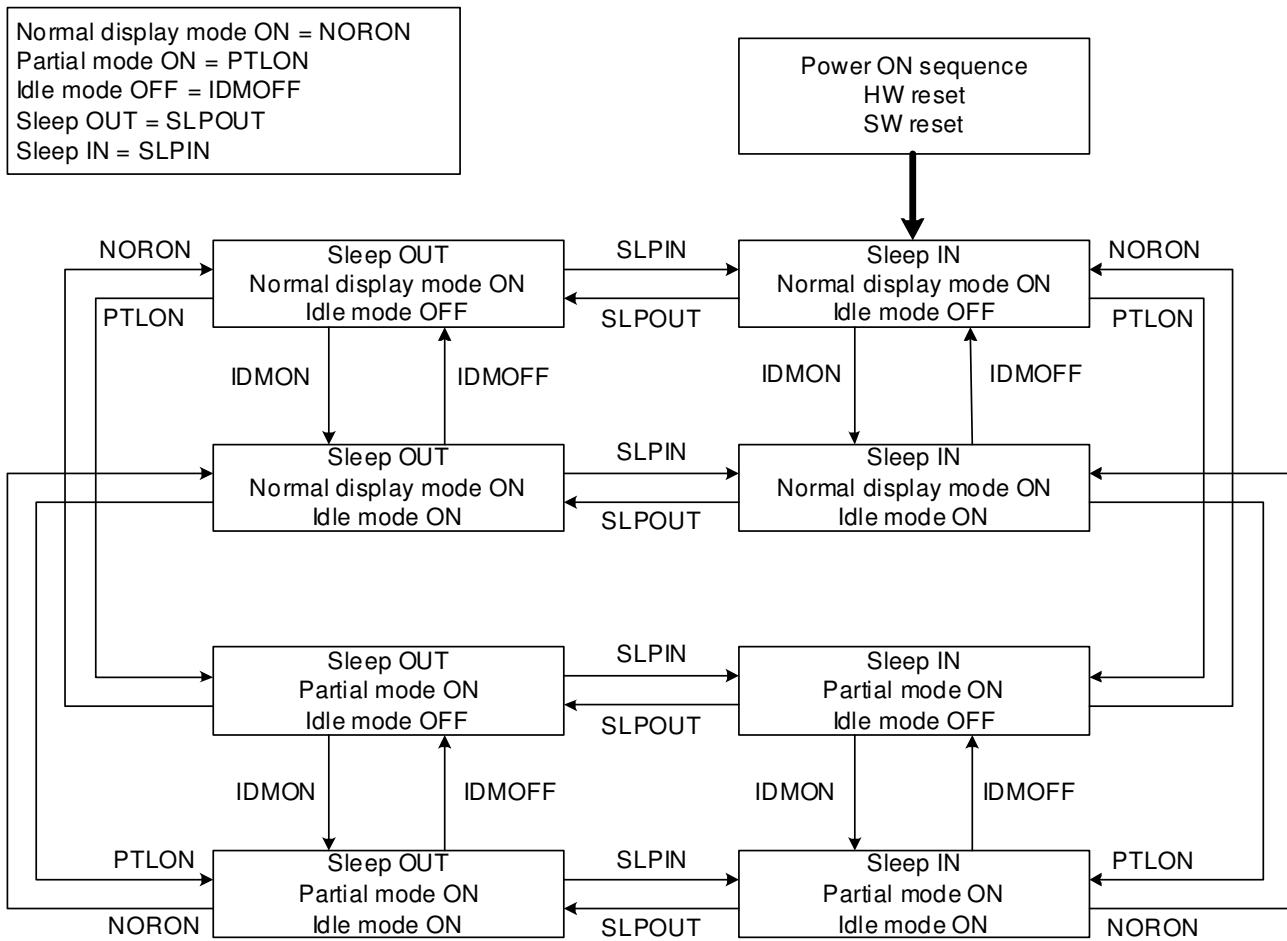
In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

6. Power Off Mode.

In this mode, both VCI and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands.

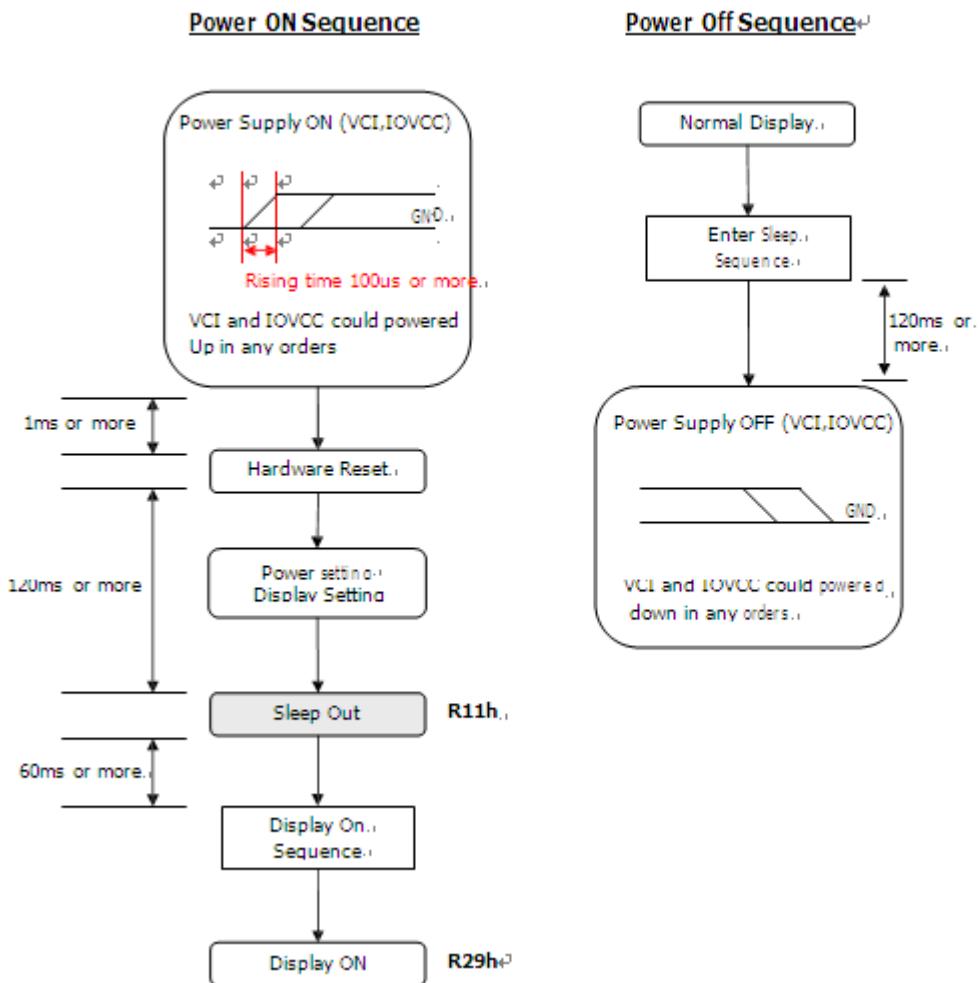
13.2. Power Flow Chart



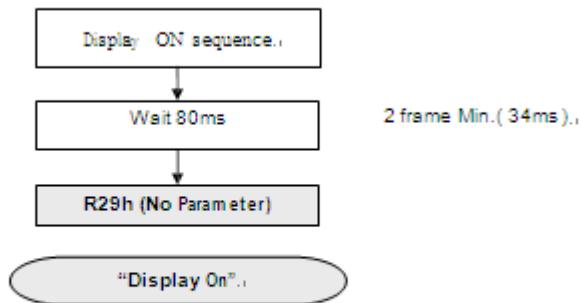
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

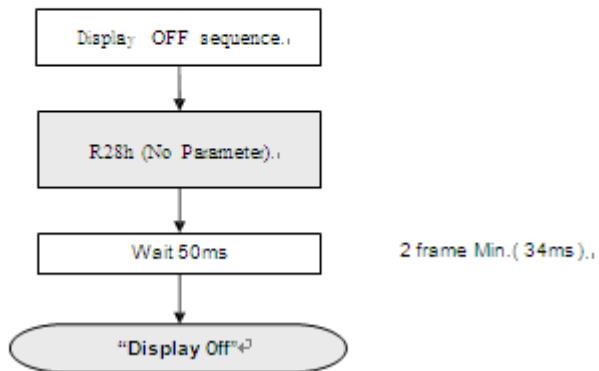
Power On / Off Sequence..



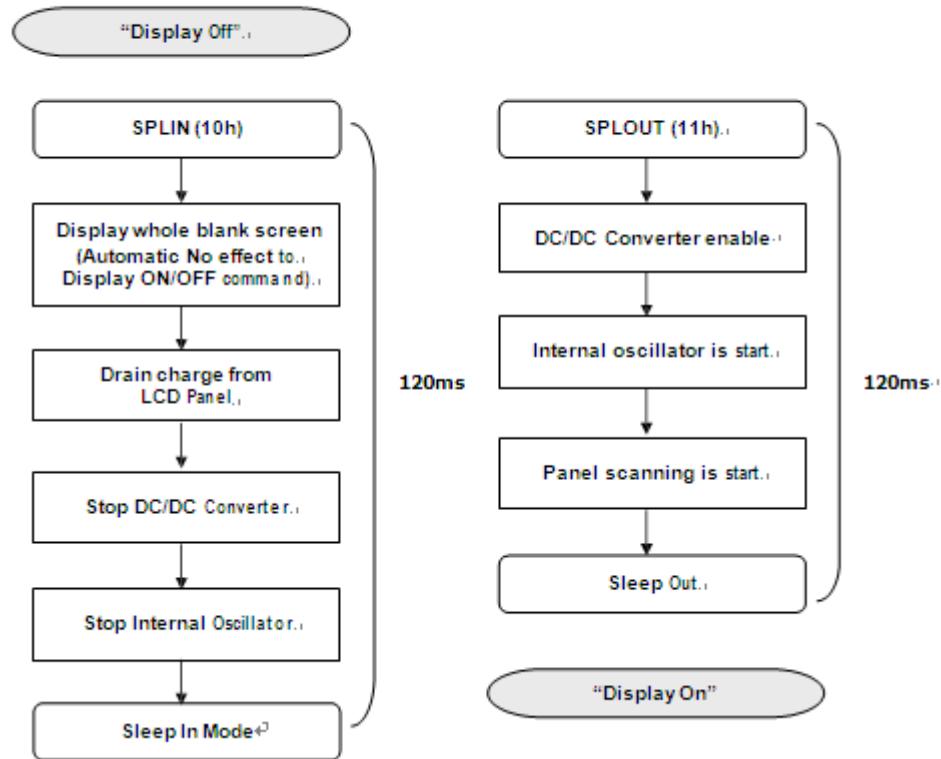
Display On Sequence Setting.:

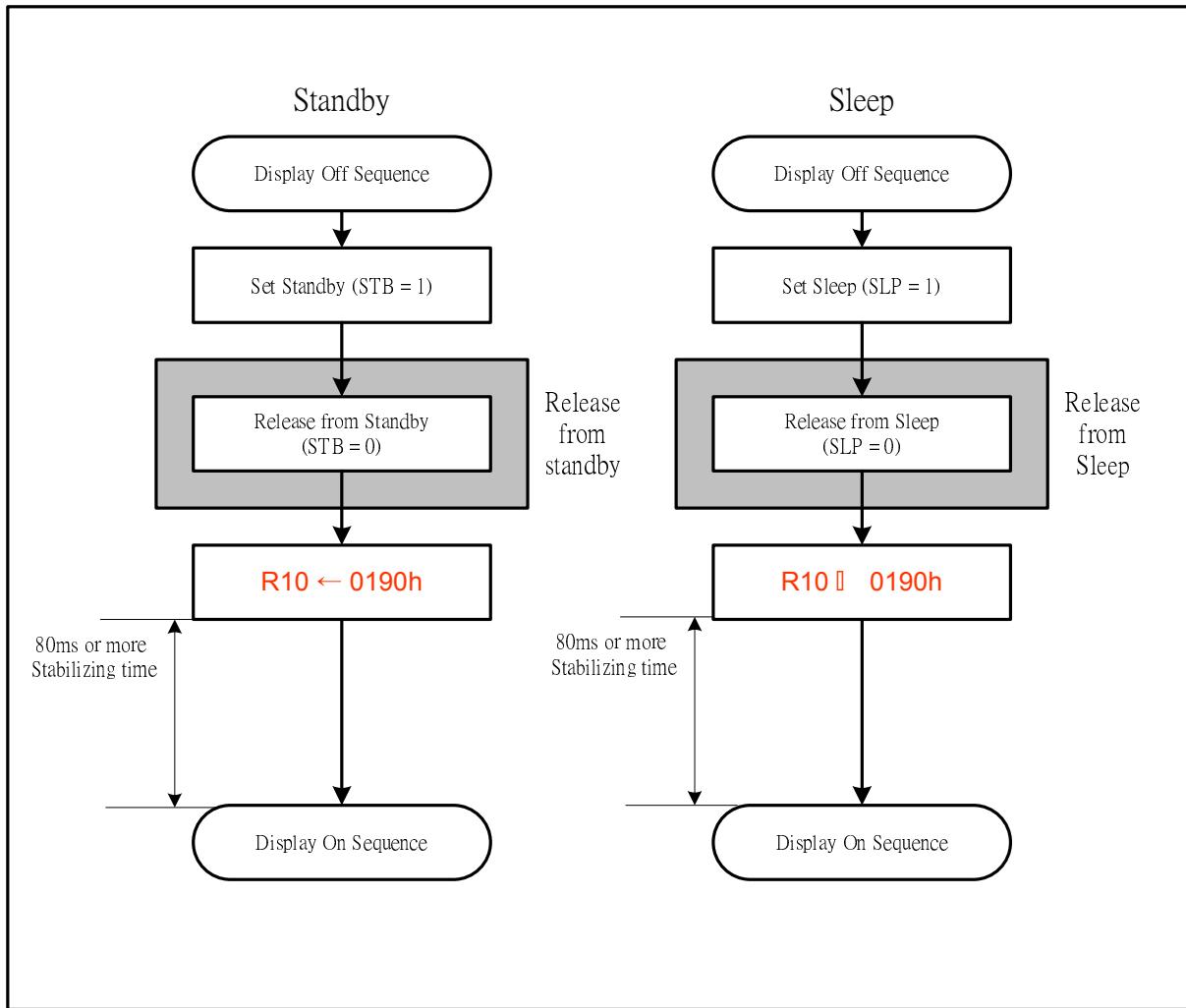


Display OFF Sequence Setting.:



LCD Sleep Mode In/Out..





14. Gamma Curves Selection

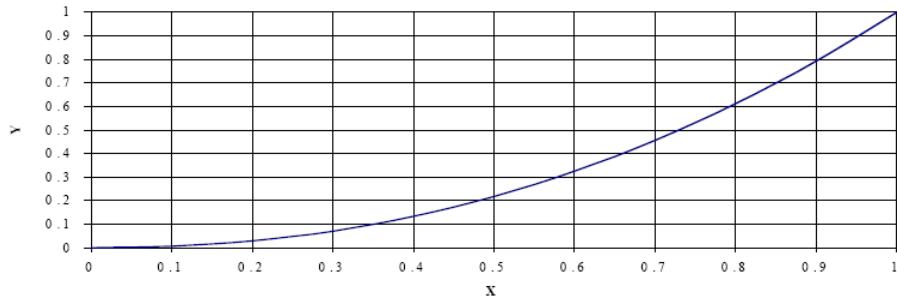
ILI9341 provide one gamma curve Gamma2.2. The gamma curve can be selected by the GC0 settings.

14.1. Gamma Default Values (for NW type LC)

Data	Output Voltage			
	VCOM = Low		VCOM = High	
	Gamma	2.2	Gamma	2.2
0	V0P	4.084	V0N	0.277
1	V1P	4.015	V1N	0.346
2	V2P	3.843	V2N	0.482
3	V3P	3.681	V3N	0.629
4	V4P	3.518	V4N	0.776
5	V5P	3.445	V5N	0.924
6	V6P	3.371	V6N	1.071
7	V7P	3.285	V7N	1.157
8	V8P	3.199	V8N	1.242
9	V9P	3.128	V9N	1.314
10	V10P	3.056	V10N	1.385
11	V11P	2.985	V11N	1.456
12	V12P	2.928	V12N	1.513
13	V13P	2.871	V13N	1.570
14	V14P	2.802	V14N	1.619
15	V15P	2.733	V15N	1.668
16	V16P	2.674	V16N	1.710
17	V17P	2.615	V17N	1.753
18	V18P	2.557	V18N	1.795
19	V19P	2.508	V19N	1.830
20	V20P	2.458	V20N	1.865
21	V21P	2.425	V21N	1.899
22	V22P	2.391	V22N	1.932
23	V23P	2.357	V23N	1.966
24	V24P	2.323	V24N	2.000
25	V25P	2.289	V25N	2.034
26	V26P	2.256	V26N	2.068
27	V27P	2.222	V27N	2.102
28	V28P	2.193	V28N	2.129
29	V29P	2.165	V29N	2.155
30	V30P	2.136	V30N	2.182
31	V31P	2.108	V31N	2.208
32	V32P	2.080	V32N	2.235
33	V33P	2.051	V33N	2.262
34	V34P	2.023	V34N	2.288
35	V35P	1.994	V35N	2.315
36	V36P	1.966	V36N	2.342
37	V37P	1.942	V37N	2.368
38	V38P	1.917	V38N	2.395
39	V39P	1.893	V39N	2.421
40	V40P	1.869	V40N	2.448
41	V41P	1.845	V41N	2.475
42	V42P	1.820	V42N	2.501
43	V43P	1.796	V43N	2.528
44	V44P	1.776	V44N	2.549
45	V45P	1.755	V45N	2.571
46	V46P	1.730	V46N	2.597
47	V47P	1.706	V47N	2.623
48	V48P	1.681	V48N	2.649
49	V49P	1.653	V49N	2.679
50	V50P	1.624	V50N	2.710
51	V51P	1.598	V51N	2.735
52	V52P	1.573	V52N	2.761
53	V53P	1.541	V53N	2.793
54	V54P	1.508	V54N	2.825
55	V55P	1.476	V55N	2.857
56	V56P	1.438	V56N	2.895
57	V57P	1.400	V57N	2.933
58	V58P	1.359	V58N	2.982
59	V59P	1.319	V59N	3.031
60	V60P	1.246	V60N	3.109
61	V61P	1.173	V61N	3.186
62	V62P	1.070	V62N	3.289
63	V63P	0.279	V63N	4.083

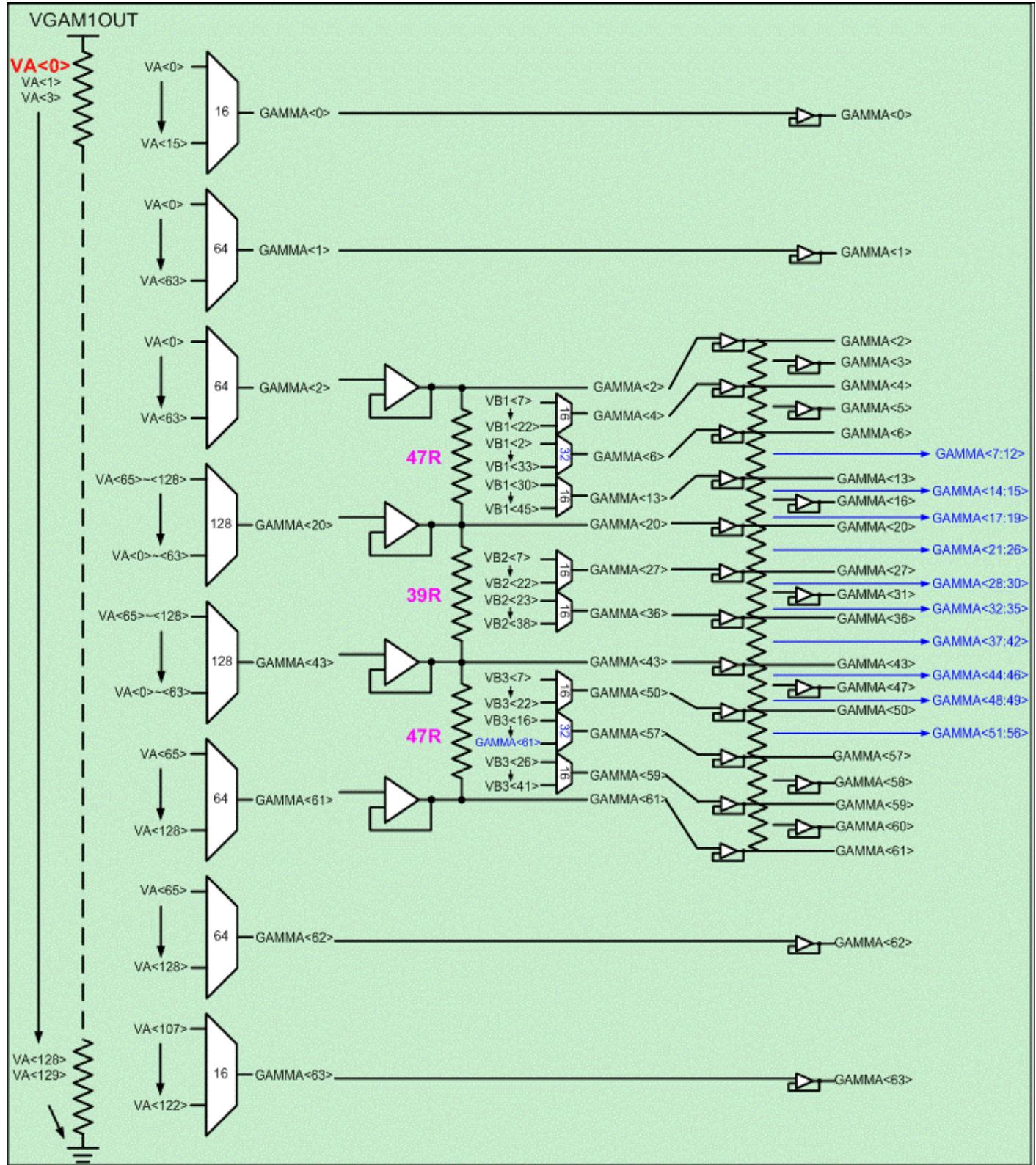
14.2. Gamma Curves

14.2.1. Gamma Curve 1 (GC0), applies the function $y=x^{2.2}$

Gamma $y = x^{2.2}$ 

14.3. Gamma Curves

14.3.1. Grayscale Voltage Generation



14.3.2. Positive Gamma Correction

Gamma Level	Value "X" in Formula	Formula						
VP0	VP0[3:0]	$(VREG1-VGS)*(130R-X*R)/130R$						
VP1	VP1[5:0]	$(VREG1-VGS)*(130R-X*R)/130R$						
VP2	VP2[5:0]	$(VREG1-VGS)*(130R-X*R)/130R$						
VP3	—	$(VP2-VP4)*35R/(35R^2)+VP4$						
VP4	VP4[3:0]	$(VP2-VP20)*(47R-X*R-7R)/47R+VP20$						
VP5	—	$(VP4-VP6)*35R/(35R^2)+VP6$						
VP6	VP6[4:0]	$(VP2-VP20)*(47R-X*R-2R)/47R+VP20$						
VP7	—	$(VP6-VP13)*(12R+10R^3+8R^2)/(12R^2+10R^3+8R^2)+VP13$						
VP8	—	$(VP6-VP13)*(10R^3+8R^2)/(12R^2+10R^3+8R^2)+VP13$						
VP9	—	$(VP6-VP13)*(10R^2+8R^2)/(12R^2+10R^3+8R^2)+VP13$						
VP10	—	$(VP6-VP13)*(10R+8R^2)/(12R^2+10R^3+8R^2)+VP13$						
VP11	—	$(VP6-VP13)*(8R^2)/(12R^2+10R^3+8R^2)+VP13$						
VP12	—	$(VP6-VP13)*8R/(12R^2+10R^3+8R^2)+VP13$						
VP13	VP13[3:0]	$(VP2-VP20)*(47R-X*R-30R)/47R+VP20$						
VP14	—	$(VP13-VP20)*(14R+12R^3+10R^2)/(14R^2+12R^3+10R^2)+VP20$						
VP15	—	$(VP13-VP20)*(12R^3+10R^2)/(14R^2+12R^3+10R^2)+VP20$						
VP16	—	$(VP13-VP20)*(12R^2+10R^2)/(14R^2+12R^3+10R^2)+VP20$						
VP17	—	$(VP13-VP20)*(12R+10R^2)/(14R^2+12R^3+10R^2)+VP20$						
VP18	—	$(VP13-VP20)*(10R^2)/(14R^2+12R^3+10R^2)+VP20$						
VP19	—	$(VP13-VP20)*10R/(14R^2+12R^3+10R^2)+VP20$						
VP20	VP20[6:0]	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center; padding: 2px;"><64</td> <td style="width: 10px;"></td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R)/130R</td> </tr> <tr> <td style="text-align: center; padding: 2px;">>=64</td> <td style="width: 10px;"></td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R-1R)/130R</td> </tr> </table>	<64		(VREG1-VGS)*(130R-X*R)/130R	>=64		(VREG1-VGS)*(130R-X*R-1R)/130R
<64		(VREG1-VGS)*(130R-X*R)/130R						
>=64		(VREG1-VGS)*(130R-X*R-1R)/130R						
VP21	—	$(VP20-VP27)*(12R^6)/(12R^7)+VP27$						
VP22	—	$(VP20-VP27)*(12R^5)/(12R^7)+VP27$						
VP23	—	$(VP20-VP27)*(12R^4)/(12R^7)+VP27$						
VP24	—	$(VP20-VP27)*(12R^3)/(12R^7)+VP27$						
VP25	—	$(VP20-VP27)*(12R^2)/(12R^7)+VP27$						
VP26	—	$(VP20-VP27)*12R/(12R^7)+VP27$						
VP27	VP27[3:0]	$(VP20-VP43)*(39R-X*R-7R)/39R+VP43$						
VP28	—	$(VP27-VP36)*(8R^8)/(8R^9)+VP36$						
VP29	—	$(VP27-VP36)*(8R^7)/(8R^9)+VP36$						
VP30	—	$(VP27-VP36)*(8R^6)/(8R^9)+VP36$						
VP31	—	$(VP27-VP36)*(8R^5)/(8R^9)+VP36$						
VP32	—	$(VP27-VP36)*(8R^4)/(8R^9)+VP36$						
VP33	—	$(VP27-VP36)*(8R^3)/(8R^9)+VP36$						
VP34	—	$(VP27-VP36)*(8R^2)/(8R^9)+VP36$						
VP35	—	$(VP27-VP36)*8R/(8R^9)+VP36$						
VP36	VP36[3:0]	$(VP20-VP43)*(39R-X*R-23R)/39R+VP43$						
VP37	—	$(VP36-VP43)*(12R^6)/(12R^7)+VP43$						
VP38	—	$(VP36-VP43)*(12R^5)/(12R^7)+VP43$						
VP39	—	$(VP36-VP43)*(12R^4)/(12R^7)+VP43$						
VP40	—	$(VP36-VP43)*(12R^3)/(12R^7)+VP43$						
VP41	—	$(VP36-VP43)*(12R^2)/(12R^7)+VP43$						
VP42	—	$(VP36-VP43)*12R/(12R^7)+VP43$						
VP43	VP43[6:0]	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center; padding: 2px;"><64</td> <td style="width: 10px;"></td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R)/130R</td> </tr> <tr> <td style="text-align: center; padding: 2px;">>=64</td> <td style="width: 10px;"></td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R-1R)/130R</td> </tr> </table>	<64		(VREG1-VGS)*(130R-X*R)/130R	>=64		(VREG1-VGS)*(130R-X*R-1R)/130R
<64		(VREG1-VGS)*(130R-X*R)/130R						
>=64		(VREG1-VGS)*(130R-X*R-1R)/130R						
VP44	—	$(VP43-VP50)*(14R^2+12R^3+10R)/(14R^2+12R^3+10R^2)+VP50$						
VP45	—	$(VP43-VP50)*(14R^2+12R^3)/(14R^2+12R^3+10R^2)+VP50$						
VP46	—	$(VP43-VP50)*(14R^2+12R^2)/(14R^2+12R^3+10R^2)+VP50$						
VP47	—	$(VP43-VP50)*(14R^2+12R)/(14R^2+12R^3+10R^2)+VP50$						
VP48	—	$(VP43-VP50)*(14R^2)/(14R^2+12R^3+10R^2)+VP50$						
VP49	—	$(VP43-VP50)*14R/(14R^2+12R^3+10R^2)+VP50$						
VP50	VP50[3:0]	$(VP43-VP61)*(47R-X*R-7R)/47R+VP61$						
VP51	—	$(VP50-VP57)*(12R^2+10R^3+8R)/(12R^2+10R^3+8R^2)+VP57$						
VP52	—	$(VP50-VP57)*(12R^2+10R^3)/(12R^2+10R^3+8R^2)+VP57$						
VP53	—	$(VP50-VP57)*(12R^2+10R^2)/(12R^2+10R^3+8R^2)+VP57$						
VP54	—	$(VP50-VP57)*(12R^2+10R)/(12R^2+10R^3+8R^2)+VP57$						
VP55	—	$(VP50-VP57)*(12R^2)/(12R^2+10R^3+8R^2)+VP57$						
VP56	—	$(VP50-VP57)*12R/(12R^2+10R^3+8R^2)+VP57$						
VP57	VP57[4:0]	$(VP43-VP61)*(47R-X*R-16R)/47R+VP61$						
VP58	—	$(VP57-VP59)*35R/(35R^2)+VP59$						
VP59	VP59[3:0]	$(VP43-VP61)*(47R-X*R-26R)/47R+VP61$						
VP60	—	$(VP59-VP61)*35R/(35R^2)+VP61$						
VP61	VP61[5:0]	$(VREG1-VGS)*(65R-X*R)/130R$						
VP62	VP62[5:0]	$(VREG1-VGS)*(65R-X*R)/130R$						
VP63	VP63[3:0]	$(VREG1-VGS)*(23R-X*R)/130R$						

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14.3.3. Negative Gamma Correction

Gamma Level	Value "X" in Formula	Formula				
VN63	VN63[3:0]	(VREG1-VGS)*(130R-X*R)/130R				
VN62	VN62[5:0]	(VREG1-VGS)*(130R-X*R)/130R				
VN61	VN61[5:0]	(VREG1-VGS)*(130R-X*R)/130R				
VN60	—	$(VN61-VN59)*35R/(35R^2)+VN59$				
VN59	VN59[3:0]	(VN61-VN43)*(47R-X*R-7R)/47R+VN43				
VN58	—	$(VN59-VN57)*35R/(35R^2)+VN57$				
VN57	VN57[4:0]	(VN61-VN43)*(47R-X*R-2R)/47R+VN43				
VN56	—	$(VN57-VN50)*(12R+10R^3+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
VN55	—	$(VN57-VN50)*(10R^3+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
VN54	—	$(VN57-VN50)*(10R^2+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
VN53	—	$(VN57-VN50)*(10R+8R^2)/(12R^2+10R^3+8R^2)+VN50$				
VN52	—	$(VN57-VN50)*(8R^2)/(12R^2+10R^3+8R^2)+VN50$				
VN51	—	$(VN57-VN50)*8R/(12R^2+10R^3+8R^2)+VN50$				
VN50	VN50[3:0]	(VN61-VN43)*(47R-X*R-30R)/47R+VN43				
VN49	—	$(VN50-VN43)*(14R+12R^3+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
VN48	—	$(VN50-VN43)*(12R^3+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
VN47	—	$(VN50-VN43)*(12R^2+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
VN46	—	$(VN50-VN43)*(12R+10R^2)/(14R^2+12R^3+10R^2)+VN43$				
VN45	—	$(VN50-VN43)*(10R^2)/(14R^2+12R^3+10R^2)+VN43$				
VN44	—	$(VN50-VN43)*10R/(14R^2+12R^3+10R^2)+VN43$				
VN43	VN43[6:0]	<table border="1"> <tr> <td style="text-align: center; padding: 2px;"><64</td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R)/130R</td> </tr> <tr> <td style="text-align: center; padding: 2px;">>=64</td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R-1R)/130R</td> </tr> </table>	<64	(VREG1-VGS)*(130R-X*R)/130R	>=64	(VREG1-VGS)*(130R-X*R-1R)/130R
<64	(VREG1-VGS)*(130R-X*R)/130R					
>=64	(VREG1-VGS)*(130R-X*R-1R)/130R					
VN42	—	$(VN43-VN36)*(12R^6)/(12R^7)+VN36$				
VN41	—	$(VN43-VN36)*(12R^5)/(12R^7)+VN36$				
VN40	—	$(VN43-VN36)*(12R^4)/(12R^7)+VN36$				
VN39	—	$(VN43-VN36)*(12R^3)/(12R^7)+VN36$				
VN38	—	$(VN43-VN36)*(12R^2)/(12R^7)+VN36$				
VN37	—	$(VN43-VN36)*12R/(12R^7)+VN36$				
VN36	VN36[3:0]	(VN43-VN20)*(39R-X*R-7R)/39R+VN20				
VN35	—	$(VN36-VN27)*(8R^8)/(8R^9)+VN27$				
VN34	—	$(VN36-VN27)*(8R^7)/(8R^9)+VN27$				
VN33	—	$(VN36-VN27)*(8R^6)/(8R^9)+VN27$				
VN32	—	$(VN36-VN27)*(8R^5)/(8R^9)+VN27$				
VN31	—	$(VN36-VN27)*(8R^4)/(8R^9)+VN27$				
VN30	—	$(VN36-VN27)*(8R^3)/(8R^9)+VN27$				
VN29	—	$(VN36-VN27)*(8R^2)/(8R^9)+VN27$				
VN28	—	$(VN36-VN27)*8R/(8R^9)+VN27$				
VN27	VN27[3:0]	(VN43-VN20)*(39R-X*R-23R)/39R+VN20				
VN26	—	$(VN27-VN20)*(12R^6)/(12R^7)+VN20$				
VN25	—	$(VN27-VN20)*(12R^5)/(12R^7)+VN20$				
VN24	—	$(VN27-VN20)*(12R^4)/(12R^7)+VN20$				
VN23	—	$(VN27-VN20)*(12R^3)/(12R^7)+VN20$				
VN22	—	$(VN27-VN20)*(12R^2)/(12R^7)+VN20$				
VN21	—	$(VN27-VN20)*12R/(12R^7)+VN20$				
VN20	VN20[6:0]	<table border="1"> <tr> <td style="text-align: center; padding: 2px;"><64</td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R)/130R</td> </tr> <tr> <td style="text-align: center; padding: 2px;">>=64</td> <td style="text-align: center; padding: 2px;">(VREG1-VGS)*(130R-X*R-1R)/130R</td> </tr> </table>	<64	(VREG1-VGS)*(130R-X*R)/130R	>=64	(VREG1-VGS)*(130R-X*R-1R)/130R
<64	(VREG1-VGS)*(130R-X*R)/130R					
>=64	(VREG1-VGS)*(130R-X*R-1R)/130R					
VN19	—	$(VN20-VN13)*(14R^2+12R^3+10R)/(14R^2+12R^3+10R^2)+VN13$				
VN18	—	$(VN20-VN13)*(14R^2+12R^3)/(14R^2+12R^3+10R^2)+VN13$				
VN17	—	$(VN20-VN13)*(14R^2+12R^2)/(14R^2+12R^3+10R^2)+VN13$				
VN16	—	$(VN20-VN13)*(14R^2+12R)/(14R^2+12R^3+10R^2)+VN13$				
VN15	—	$(VN20-VN13)*(14R^2)/(14R^2+12R^3+10R^2)+VN13$				
VN14	—	$(VN20-VN13)*14R/(14R^2+12R^3+10R^2)+VN13$				
VN13	VN13[3:0]	(VN20-VN2)*(47R-X*R-7R)/47R+VN2				
VN12	—	$(VN13-VN6)*(12R^2+10R^3+8R)/(12R^2+10R^3+8R^2)+VN6$				
VN11	—	$(VN13-VN6)*(12R^2+10R^3)/(12R^2+10R^3+8R^2)+VN6$				
VN10	—	$(VN13-VN6)*(12R^2+10R^2)/(12R^2+10R^3+8R^2)+VN6$				
VN9	—	$(VN13-VN6)*(12R^2+10R)/(12R^2+10R^3+8R^2)+VN6$				
VN8	—	$(VN13-VN6)*(12R^2)/(12R^2+10R^3+8R^2)+VN6$				
VN7	—	$(VN13-VN6)*12R/(12R^2+10R^3+8R^2)+VN6$				
VN6	VN6[4:0]	(VN20-VN2)*(47R-X*R-16R)/47R+VN2				
VN5	—	$(VN6-VN4)*35R/(35R^2)+VN4$				
VN4	VN4[3:0]	(VN20-VN2)*(47R-X*R-26R)/47R+VN2				
VN3	—	$(VN4-VN2)*35R/(35R^2)+VN2$				
VN2	VN2[5:0]	(VREG1-VGS)*(65R-X*R)/130R				
VN1	VN1[5:0]	(VREG1-VGS)*(65R-X*R)/130R				
VN0	VN0[3:0]	(VREG1-VGS)*(23R-X*R)/130R				

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15. Reset

15.1. Registers

The registers that are initialized are listed as below:

	After Powered ON	After Hardware Reset	After Software Reset
Frame Memory	Random	Repair data	No Change
Sleep	In	In	In
Display Mode	Normal	Normal	Normal
Display	Off	Off	Off
Idle	Off	Off	Off
Column Start Address	0000 h	0000 h	0000 h
Column End Address	00EF h	00EF h	If MADCTL's B5=0:00EF h If MADCTL's B5=1:013F h
Page Start Address	0000 h	0000 h	0000 h
Page End Address	013F h	013F h	If MADCTL's B5 = 0:013F h If MADCTL's B5=1:00EF h
Gamma Setting	GC0	GC0	GC0
Partial Area Start	0000 h	0000 h	0000 h
Partial Area End	013F h	013F h	013F h
Memory Data Access Control	00 h	00 h	No Change
RDDPM	08 h	08 h	08 h
RDDMADCTL	00 h	00 h	No Change
RDDCOLMOD	06 h	06 h	06 h
RDDIM	00 h	00 h	00 h
RDDSM	00 h	00 h	00 h
RDDSDR	00 h	00 h	00 h
TE Output Line	Off	Off	Off
TE Line Mode	Mode 1 (Note 3)	Mode 1 (Note 3)	Mode 1 (Note 3)

Note 1: There will be no abnormal visible effects on the display when S/W or H/W Resets are applied.

Note 2: After Powered-On Reset finishes within 10μs after both VCI & VDDI are applied.

Note 3: Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

15.2. Output Pins, I/O Pins

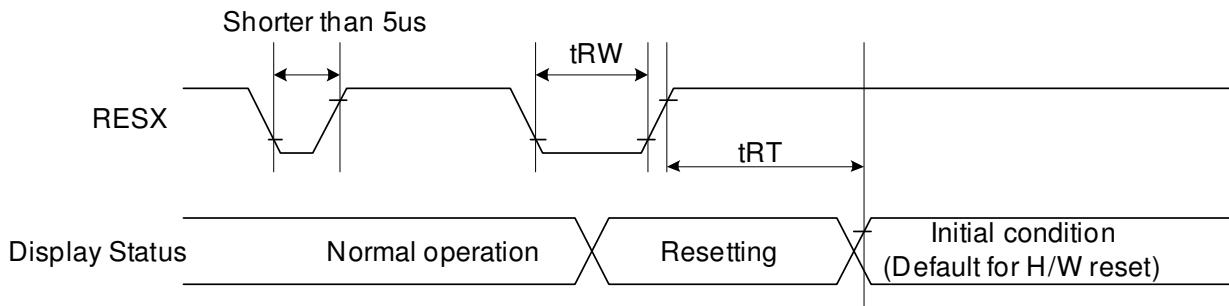
	After Power ON	After Hardware Reset	After Software Reset
TE line	Low	Low	Low
D[17:0] (output driver)	Hi-Z (Inactive)	Hi-Z (Inactive)	Hi-Z (Inactive)

Note 1: There will be no output from D [17:0] during Power ON/OFF sequence, hardware reset and software reset.

15.3. Input Pins

	During Power ON Process	After Power ON	After Hardware Reset	After Software Reset	During Power OFF Process
RESX	See Chapter 12	Input valid	Input valid	Input valid	See Chapter 12
CSX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D/CX	Input invalid	Input valid	Input valid	Input valid	Input invalid
WRX	Input invalid	Input valid	Input valid	Input valid	Input invalid
RDX	Input invalid	Input valid	Input valid	Input valid	Input invalid
D[17:0] (input driver)	Input invalid	Input valid	Input valid	Input valid	Input invalid

15.4. Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

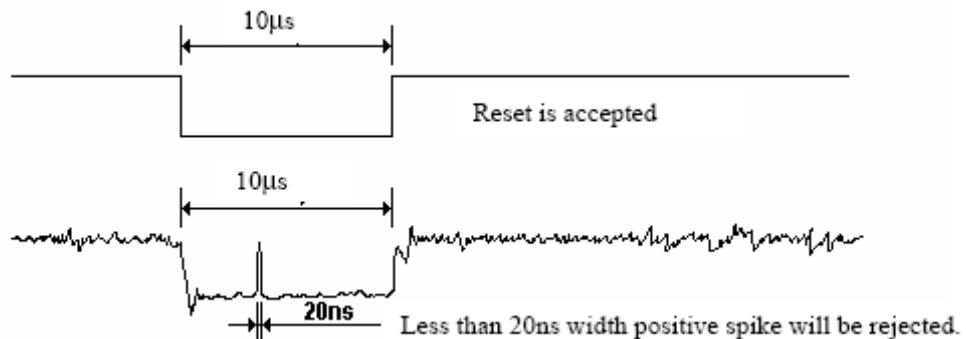
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

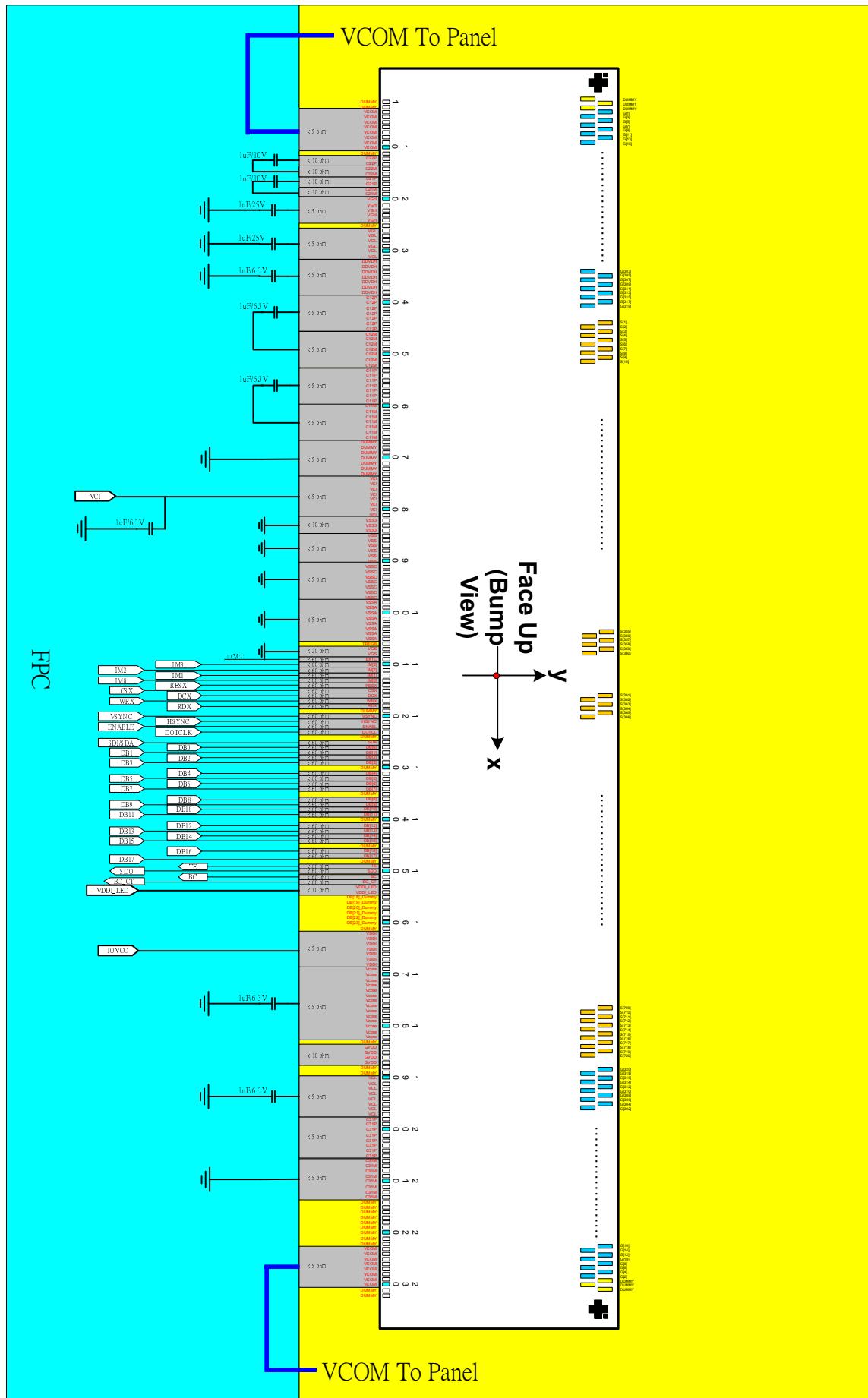


Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

16. Configuration of Power Supply Circuit

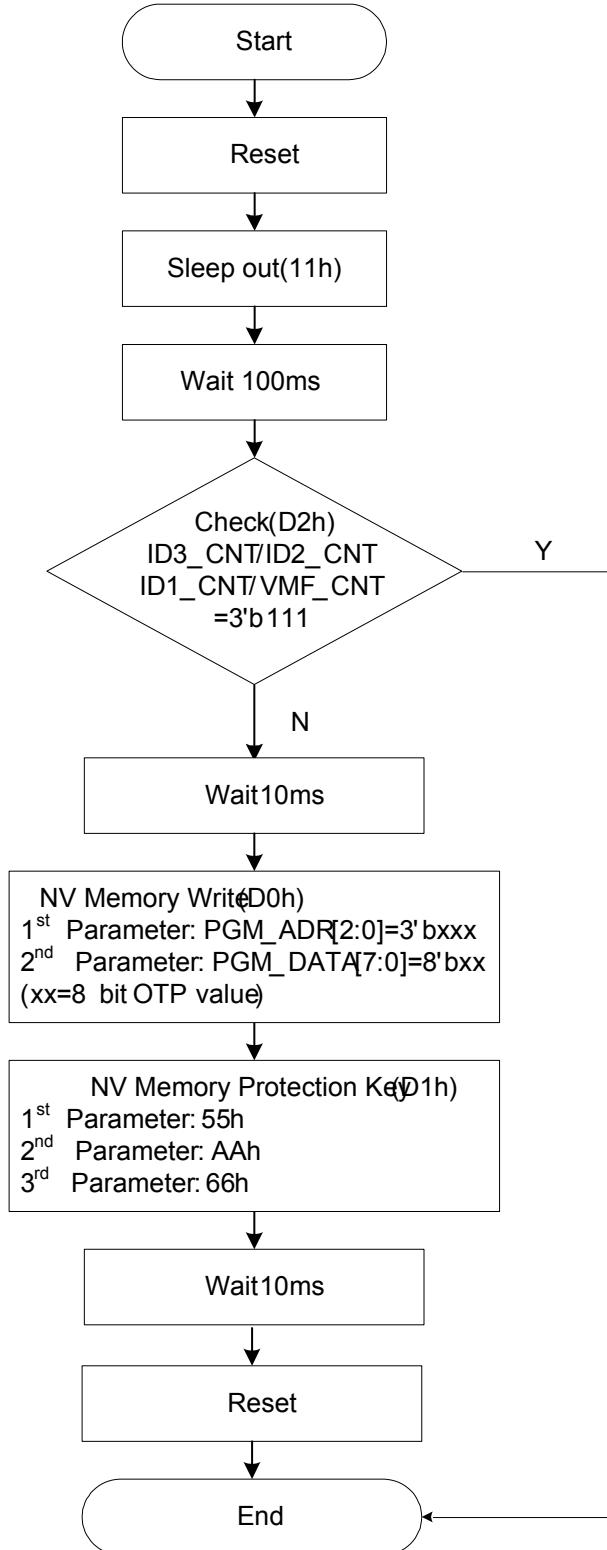


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The Following tables shows specifications of external elements connected to the ILI9341's power supply circuit.

Items	Recommended Specification	Pin connection
Capacity 1 μF (B characteristics)	6.3V	DDVDH ,VCL,C11P/M,C12P/M,Vcore,VCI
	10V	C21P/M,C22P/M
	25V	VGL, VGH

17. NV Memory Programming Flow



18. Electrical Characteristics

18.1 Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When ILI9341 is used out of the absolute maximum ratings, ILI9341 may be permanently damaged. To use ILI9341 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, ILI9341 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3 ~ +4.6
Supply voltage (Logic)	VDDI	V	-0.3 ~ +4.6
Supply voltage (Digital)	VCORE	V	-0.3 ~ +2.0
Driver supply voltage	VGH-VGL	V	-0.3 ~ +28.0
Logic input voltage range	VIN	V	-0.3 ~ VDDI + 0.3
Logic output voltage range	VO	V	-0.3 ~ VDDI + 0.3
Operating temperature	Topr	°C	-40 ~ +85
Storage temperature	Tstg	°C	-55 ~ +110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

18.2 DC Characteristics

18.2.1 General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	VDDI	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.5	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	18.0	Note3
Gate Driver Low Voltage	VGL	V	-	-10.0	-	-5.0	Note3
Driver Supply Voltage	-	V	VGH-VGL	15	-	28	Note3
Current consumption during standby mode	IST	µA	VCI=2.8V , Ta=25 °C	-	-	100	-
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSS	-0.1	-	+0.1	Note1,2,3
VCOM Operation							
VCOM High Voltage	VCOMH	V	Ccom=12nF	2.5	-	5.0	Note3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5	-	0.0	Note3
VCOM Amplitude Voltage	VCOMA	V	VCOMH-VCOML	4.0	-	5.5	Note3
Source Driver							
Source Output Range	Vsout	V	-	0.1	-	DDVDH-0.1	Note4
Gamma Reference Voltage	GVDD	V	-	3.0	-	5.0	Note3
Output Deviation Voltage (Source Output channel)	Vdev	mV	Sout>=4.2V Sout<=0.8V 4.2V>Sout>0.8V	-	-	20 15	Note4 -
Output Offset Voltage	VOFSET	mV	-	-	-	35	Note7
Booster Operation							
1 st Booster (VCIx2) Voltage	DDVDH	V	-	4.95 (Note 5)	-	5.8 (Note 6)	Note3
1 st Booster (VCIx2 Drop Voltage	VCIx2 drop	%	loading=1mA	-	-	5	Note3
Liner Range	Vliner	V	-	0.2	-	DDVDH-0.2	

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Note 1: $VDDI=1.65$ to $3.3V$, $VCI=2.5$ to $3.3V$, $AGND=VSS=0V$, $Ta=-30$ to 70 (to $+85$ no damage) $^{\circ}C$.

Note2: Please supply digital $VDDI$ voltage equal or less than analog VCI voltage.

Note3: CSX, RDX, WRX, D[17:0], D/CX, RESX, TE, DOTCLK, VSYNC, HSYNC, DE, SDA, SCL, IM3, IM2, IM1, IM0, and Test pins.

Note4: When the measurements are performed with LCD module. Measurement Points are like Note3.

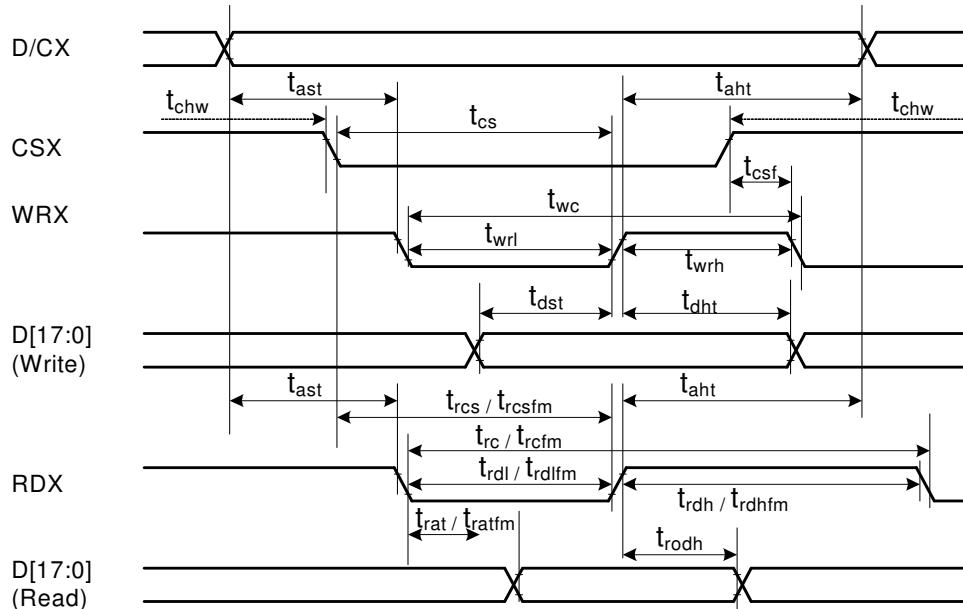
Note5: $VCI=2.6V$

Note6: $VCI=3.3V$

Note7: The Max. Value is between with Note 4 measure point and Gamma setting value

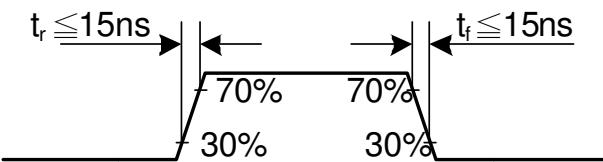
18.3 AC Characteristics

18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

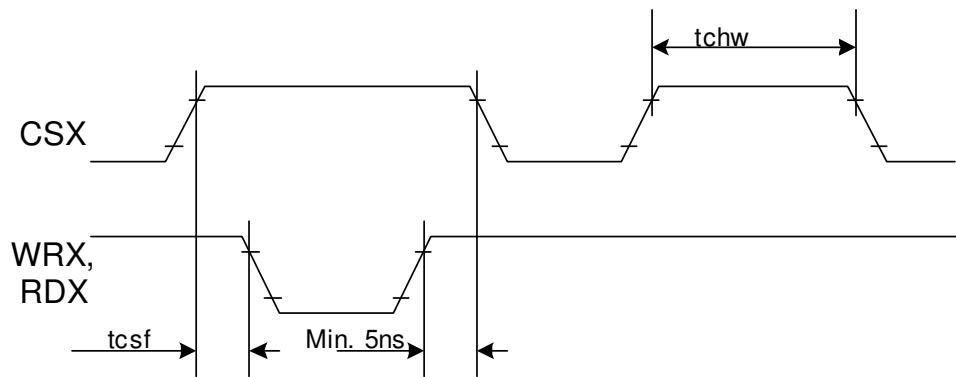


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tch _w	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	t _{wc}	Write cycle	66	-	ns	
	t _{wrh}	Write Control pulse H duration	15	-	ns	
	t _{wrl}	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	t _{dst}	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	t _{dht}	Write data hold time	10	-	ns	
	t _{rat}	Read access time	-	40	ns	
	t _{ratfm}	Read access time	-	340	ns	
	t _{rood}	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

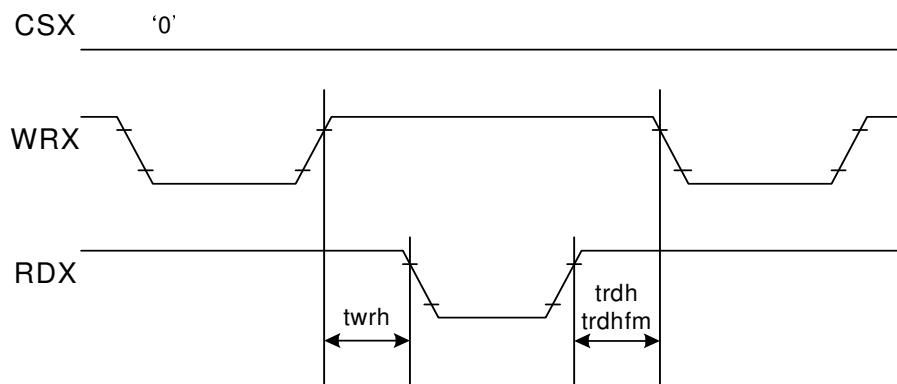


CSX timings :



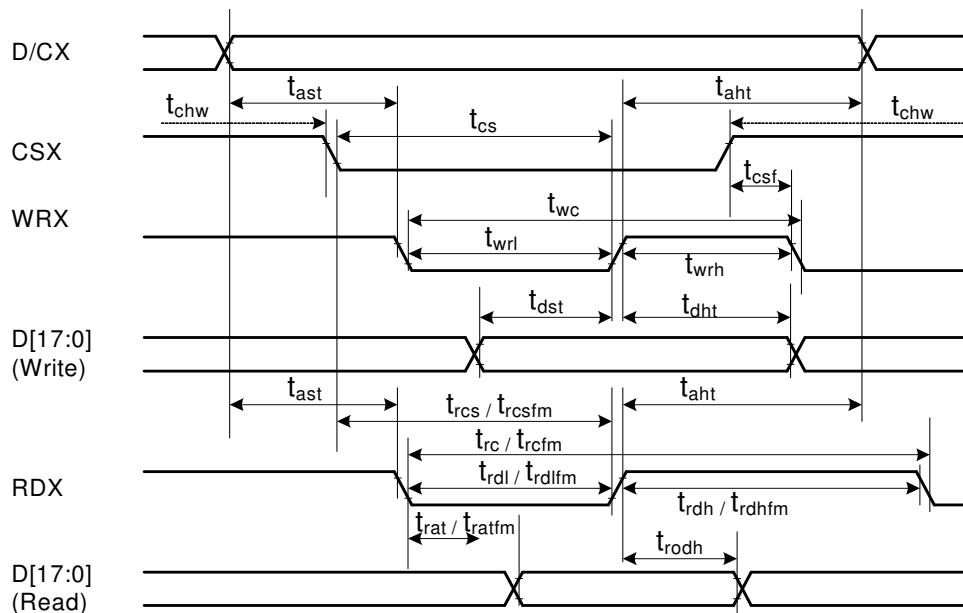
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



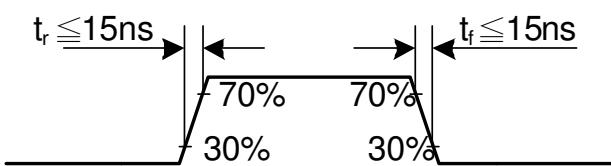
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-II system)

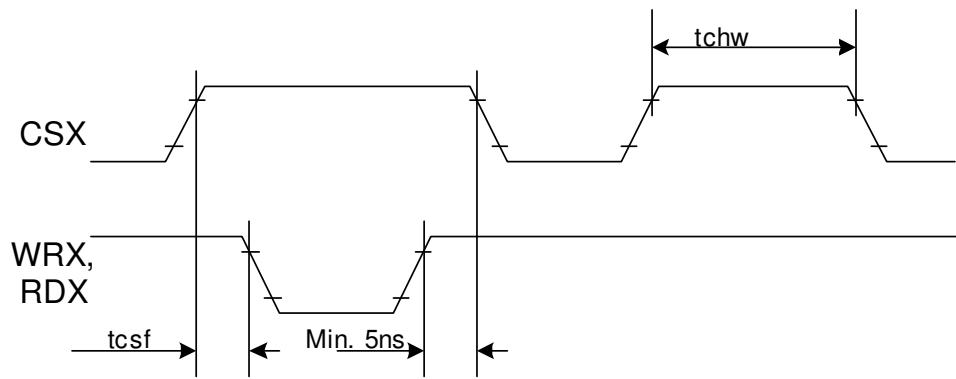


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: $T_a = -30$ to 70 °C, $VDDI=1.65V$ to $3.3V$, $VCI=2.5V$ to $3.3V$, $VSS=0V$.

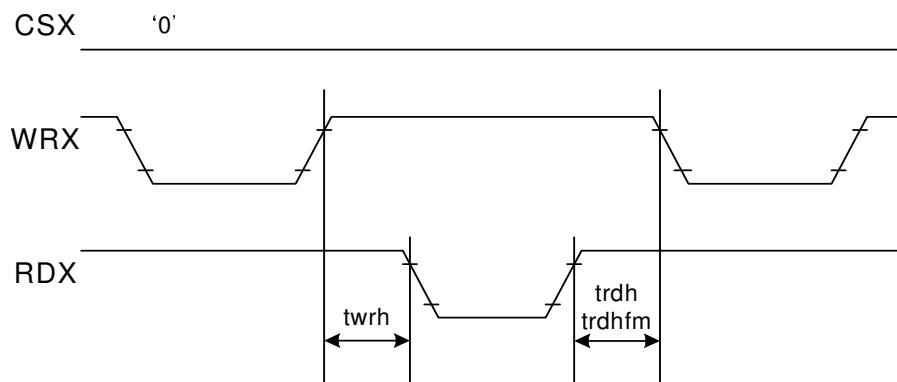


CSX timings :



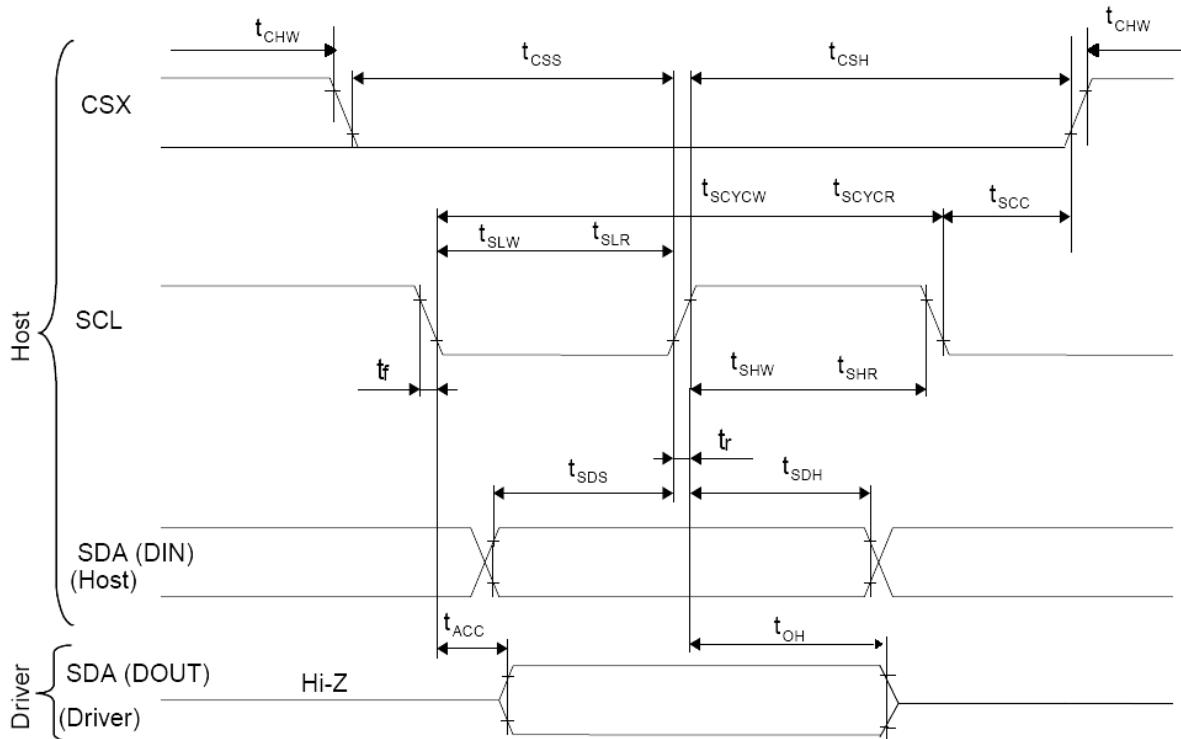
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



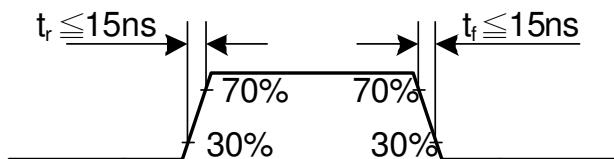
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)

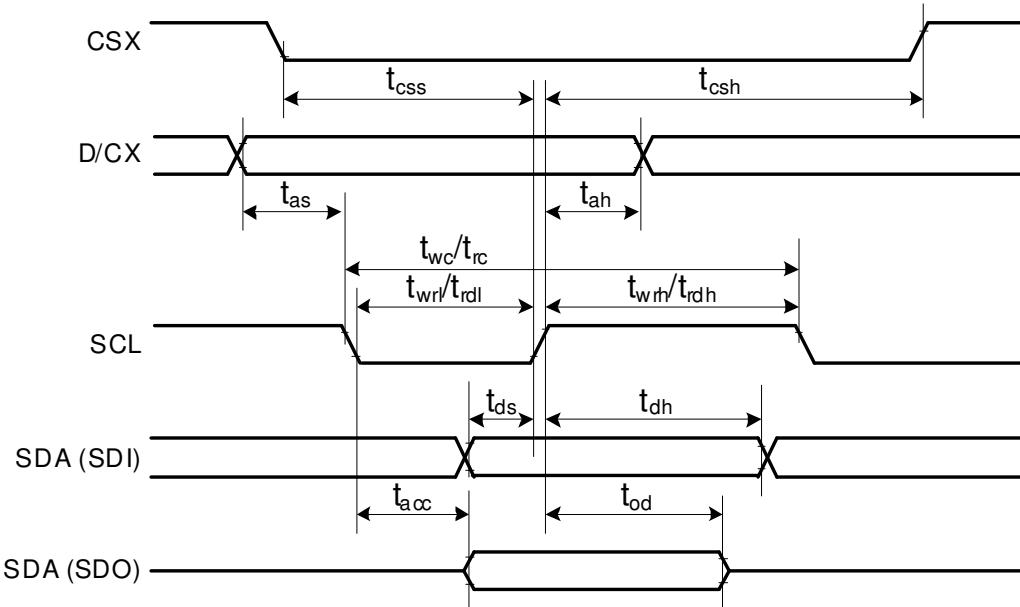


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: $T_a = 25^\circ C$, $VDDI=1.65V$ to $3.3V$, $VCI=2.5V$ to $3.3V$, $AGND=VSS=0V$

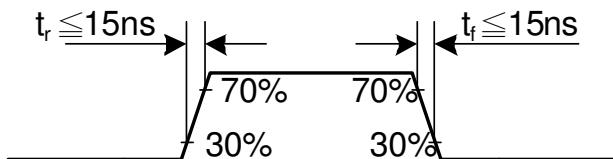


18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)

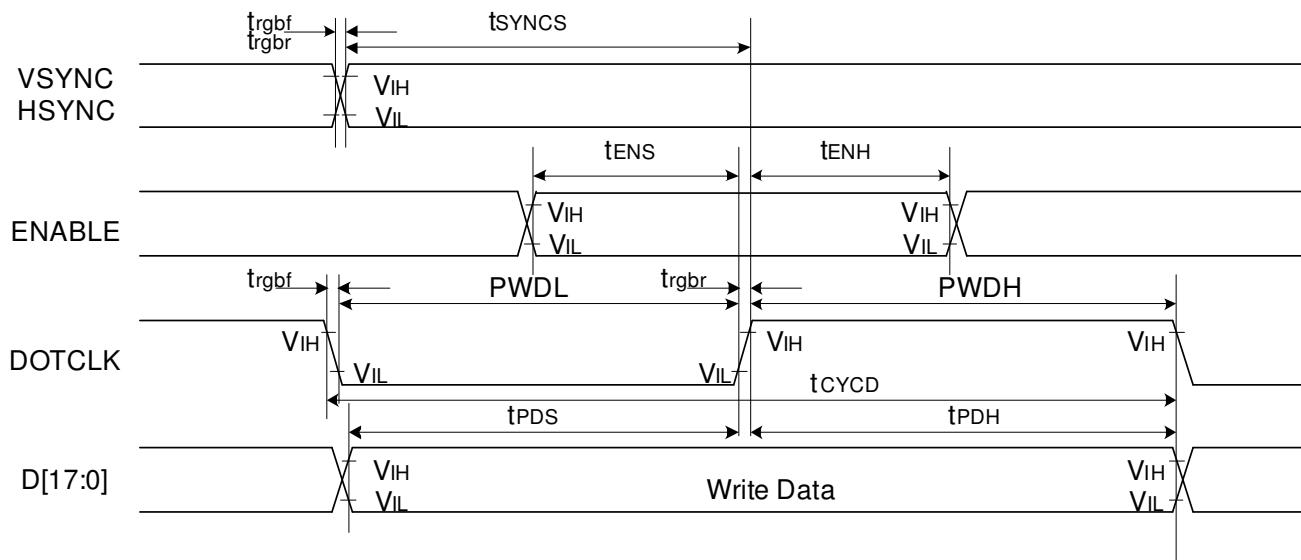


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	t _{wc}	Serial clock cycle (Write)	100	-	ns	
	t _{wrh}	SCL "H" pulse width (Write)	40	-	ns	
	t _{wrl}	SCL "L" pulse width (Write)	40	-	ns	
	t _{rc}	Serial clock cycle (Read)	150	-	ns	
	t _{rdh}	SCL "H" pulse width (Read)	60	-	ns	
	t _{rdl}	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tod	Output disable time (Read)	10	50	ns	

Note: $T_a = 25^\circ C$, $VDDI=1.65V$ to $3.3V$, $VCI=2.5V$ to $3.3V$, $AGND=VSS=0V$

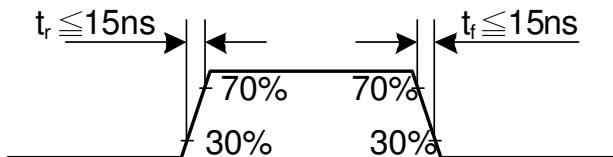


18.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics



Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t _{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t _{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ESENS}	DE setup time	15	-	ns	18/16-bit bus RGB interface mode
	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	6-bit bus RGB interface mode
	t _{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	18/16-bit bus RGB interface mode
	PWDL	DOTCLK low-level period	15	-	ns	
	t _{CYCD}	DOTCLK cycle time	100	-	ns	
	t _{rgrbf} , t _{rgrf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t _{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t _{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t _{ESENS}	DE setup time	15	-	ns	6-bit bus RGB interface mode
	t _{ENH}	DE hold time	15	-	ns	
D[17:0]	t _{POS}	Data setup time	15	-	ns	6-bit bus RGB interface mode
	t _{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	6-bit bus RGB interface mode
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t _{CYCD}	DOTCLK cycle time	100	-	ns	
	t _{rgrbf} , t _{rgrf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V



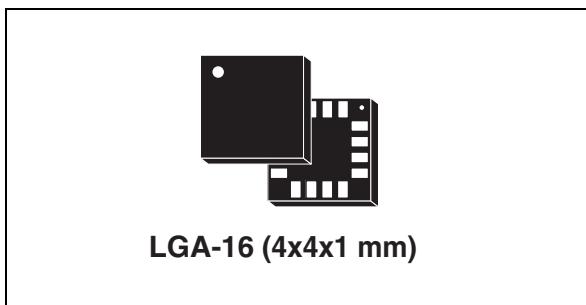
19 Revision History

Version No.	Date	Page	Description
V1.00	2010/10/12	All	New Created.
V1.01	2010/10/12	179	Update charge pump ratio
V1.02	2010/12/17	35,195~200	Add description of extend register command
V1.03	2010/12/20	196	Modify description of pumping
V1.04	2010/12/24	All	Update extend register and OTP flow
V1.05	2011/01/05	All	Update extend register
V1.06	2011/01/20	16,230	No.75 pad location, DC Characteristics
V1.07	2011/02/24	199,226,227	Modify register, external element.
V1.08	2011/03/04	179,196,227,228	Analog supply voltage naming, external element, DDVDH Max, Modify C1h,CFh default setting
V1.09	2011/03/15	9,159,197,199,226	Update clock timing, IC Configuration, E8h, EDh
V1.10	2011/04/15	226	Update for general FPC application
V1.11	2011/06/10	13	Rename pad 231, 232 as INT_TEST1 and INT_TEST2 (please leave these pins as open)
		15	Modify chip size 15860u x 650u
		166	Modify SM bit gate arrangement
V1.12	2011/07/15	8,14, 230, 231	Modify VGH from 16V to 18V
V1.13	2011/07/20	183, 185, 196,	Add OTP: ID and VMF x 3 times
		198, 219-222	Add "E9h register, Add power on sequence flow chart
			Add CFH, Bit[5], Bit[6] and all 3 rd parameter description

5.3. Hoja de datos del L3GD20

MEMS motion sensor: three-axis digital output gyroscope

Datasheet - production data



Features

- Three selectable full scales (250/500/2000 dps)
- I²C/SPI digital output interface
- 16 bit-rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low- and high-pass filters with user-selectable bandwidth
- Wide supply voltage: 2.4 V to 3.6 V
- Low voltage-compatible IOs (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- Embedded FIFO
- High shock survivability
- Extended operating temperature range (-40 °C to +85 °C)
- ECOPACK® RoHS and “Green” compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics

Description

The L3GD20 is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface capable of providing the measured angular rate to the external world through a digital interface (I²C/SPI).

The sensing element is manufactured using a dedicated micro-machining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics. The L3GD20 has a full scale of ±250/±500/ ±2000 dps and is capable of measuring rates with a user-selectable bandwidth.

The L3GD20 is available in a plastic land grid array (LGA) package and can operate within a temperature range of -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20	-40 to +85	LGA-16 (4x4x1 mm)	Tray
L3GD20TR	-40 to +85	LGA-16 (4x4x1 mm)	Tape and reel

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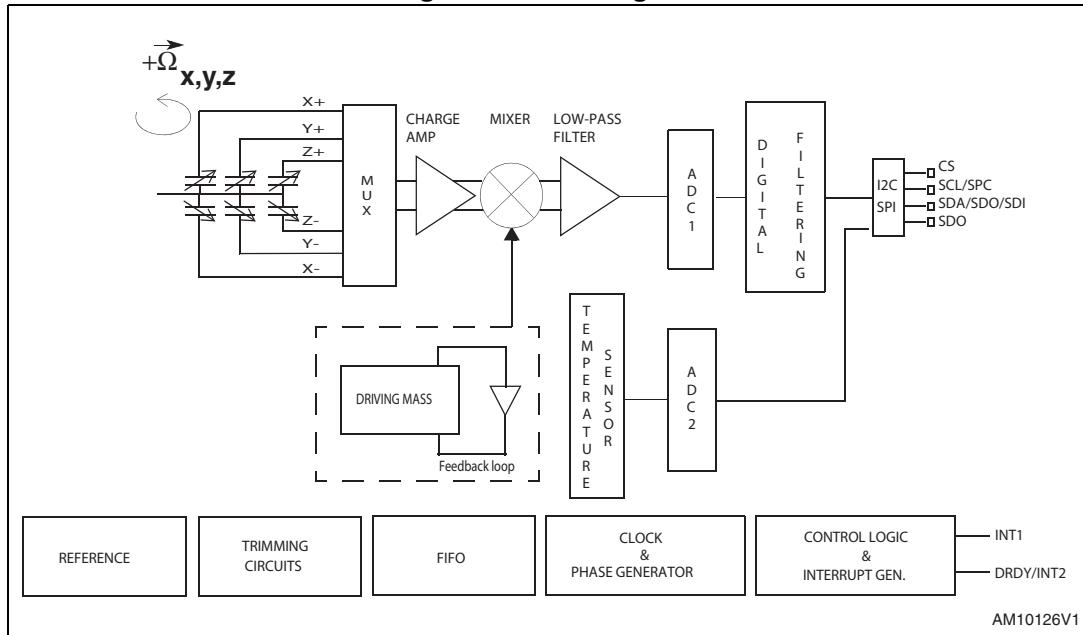
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1 Block diagram and pin description

Figure 1. Block diagram



Note: The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

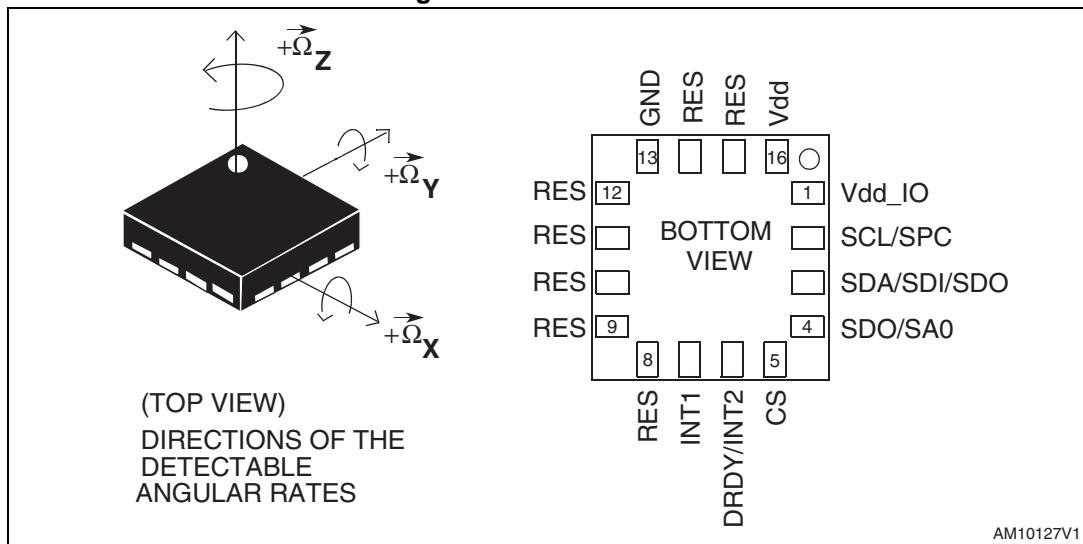


Table 2. Pin description**Table 3.**

Pin#	Name	Function
1	Vdd_IO ⁽¹⁾	Power supply for I/O pins
2	SCL SPC	I ² C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I ² C less significant bit of the device address (SA0)
5	CS	I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled)
6	DRDY/INT2	Data ready/FIFO interrupt (Watermark/Overrun/Empty)
7	INT1	Programmable interrupt
8	Reserved	Connect to GND
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	Reserved	Connect to GND
13	GND	0 V supply
14	Reserved	Connect to GND with ceramic capacitor ⁽²⁾
15	Reserved	Connect to Vdd
16	Vdd ⁽³⁾	Power supply

1. 100 nF filter capacitor recommended.
2. 1 nF min value must be guaranteed under 11 V bias condition.
3. 100 nF plus 10 μ F capacitors recommended.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

Table 4. Mechanical characteristics⁽¹⁾

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit
FS	Measurement range	User-selectable		±250		dps
				±500		
				±2000		
So	Sensitivity	FS = 250 dps		8.75		mdps/digit
		FS = 500 dps		17.50		
		FS = 2000 dps		70		
SoDr	Sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%
DVoff	Digital zero-rate level	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±75		
OffDr	Zero-rate level change vs. temperature	FS = 250 dps		±0.03		dps/°C
		FS = 2000 dps		±0.04		dps/°C
NL	Non linearity	Best fit straight line		0.2		% FS
Rn	Rate noise density			0.03		fps/(√Hz)
ODR	Digital output data rate			95/190/ 380/760		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V. The operational power supply range is specified in [Table 5](#).

2. Typical specifications are not guaranteed.

2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 5. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit
Vdd	Supply voltage		2.4	3.0	3.6	V
Vdd_IO	I/O pins supply voltage ⁽³⁾		1.71		Vdd+0.1	V
Idd	Supply current			6.1		mA
IddSL	Supply current in sleep mode ⁽⁴⁾	Selectable by digital interface		2		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		5		µA
VIH	Digital high level input voltage		0.8*Vdd_I_O			V
VIL	Digital low level input voltage				0.2*Vdd_I_O	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time relative to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 6. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

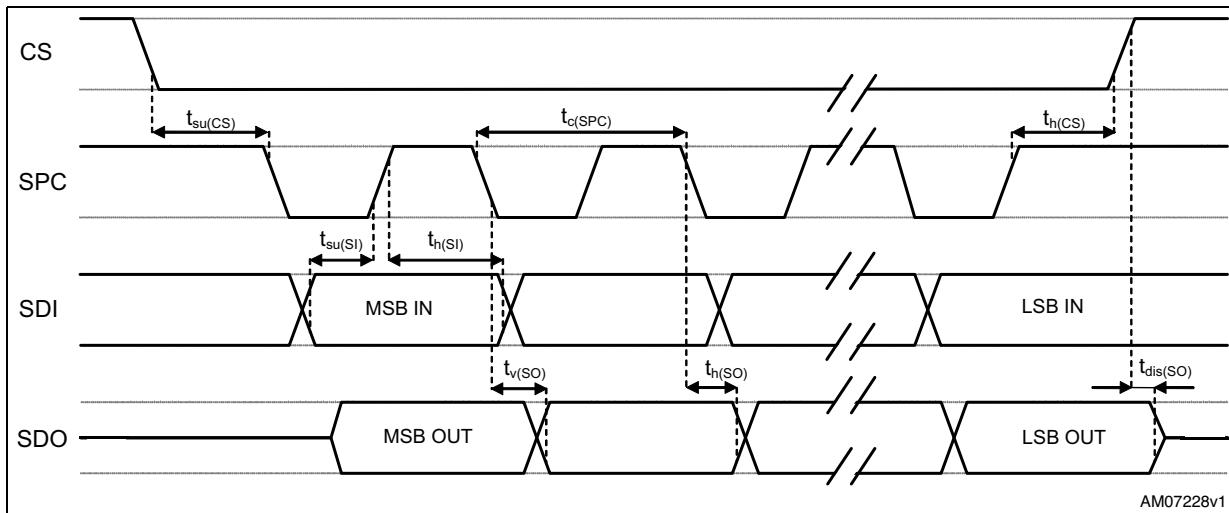
Subject to general operating conditions for Vdd and T_{op} .

Table 7. SPI slave timing values

Symbol	Parameter	Value ⁽¹⁾		Unit
		Min	Max	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	8		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	6		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at a 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results; not tested in production.

Figure 3. SPI slave timing diagram (a)



a. Measurement points are at $0.2 \cdot V_{dd_IO}$ and $0.8 \cdot V_{dd_IO}$, for both input and output port.

2.4.2 I²C - Inter IC control interface

Subject to general operating conditions for Vdd and T_{op}.

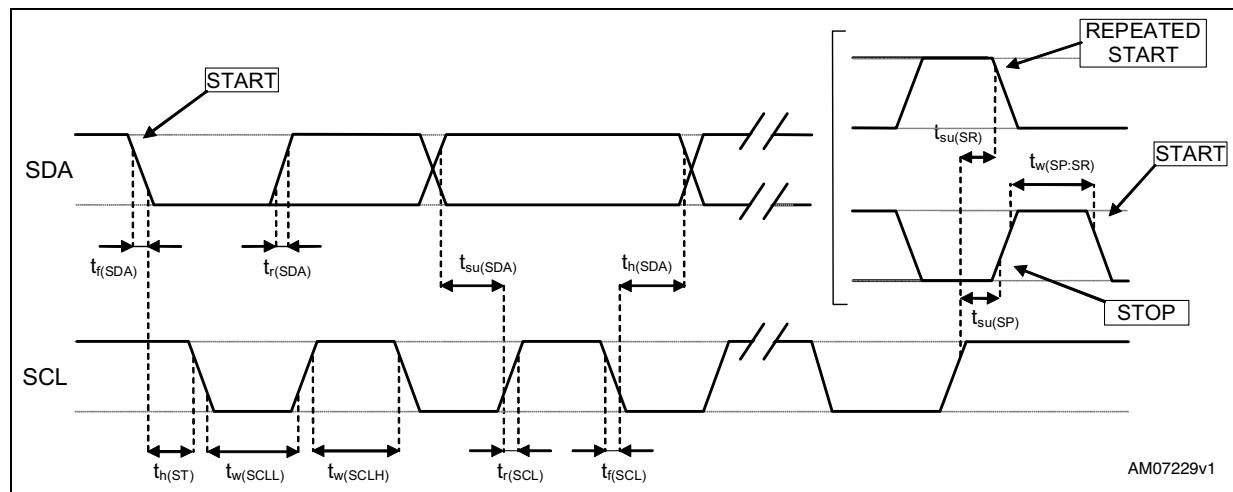
Table 8. I²C slave timing values (TBC)

Symbol	Parameter	I ² C standard mode ⁽¹⁾		I ² C fast mode ⁽¹⁾		Unit
		Min	Max	Min	Max	
f _(SCL)	SCL clock frequency	0	100	0	400	kHz
t _{w(SCLL)}	SCL clock low time	4.7		1.3		μ s
t _{w(SCLH)}	SCL clock high time	4.0		0.6		
t _{su(SDA)}	SDA setup time	250		100		ns
t _{h(SDA)}	SDA data hold time	0	3.45	0	0.9	μ s
t _{r(SDA)} t _{r(SCL)}	SDA and SCL rise time		1000	20 + 0.1C _b ⁽²⁾	300	ns
t _{f(SDA)} t _{f(SCL)}	SDA and SCL fall time		300	20 + 0.1C _b ⁽²⁾	300	
t _{h(ST)}	START condition hold time	4		0.6		μ s
t _{su(SR)}	Repeated START condition setup time	4.7		0.6		
t _{su(SP)}	STOP condition setup time	4		0.6		
t _{w(SP:SR)}	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement; not tested in production.

2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram (b)



b. Measurement points are at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T _{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	g
ESD	Electrostatic discharge protection	2 (HBM)	kV
		1.5 (CDM)	kV
		200 (MM)	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V



This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part



This is an ESD sensitive device, improper handling can cause permanent damage to the part

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

2.7 Soldering information

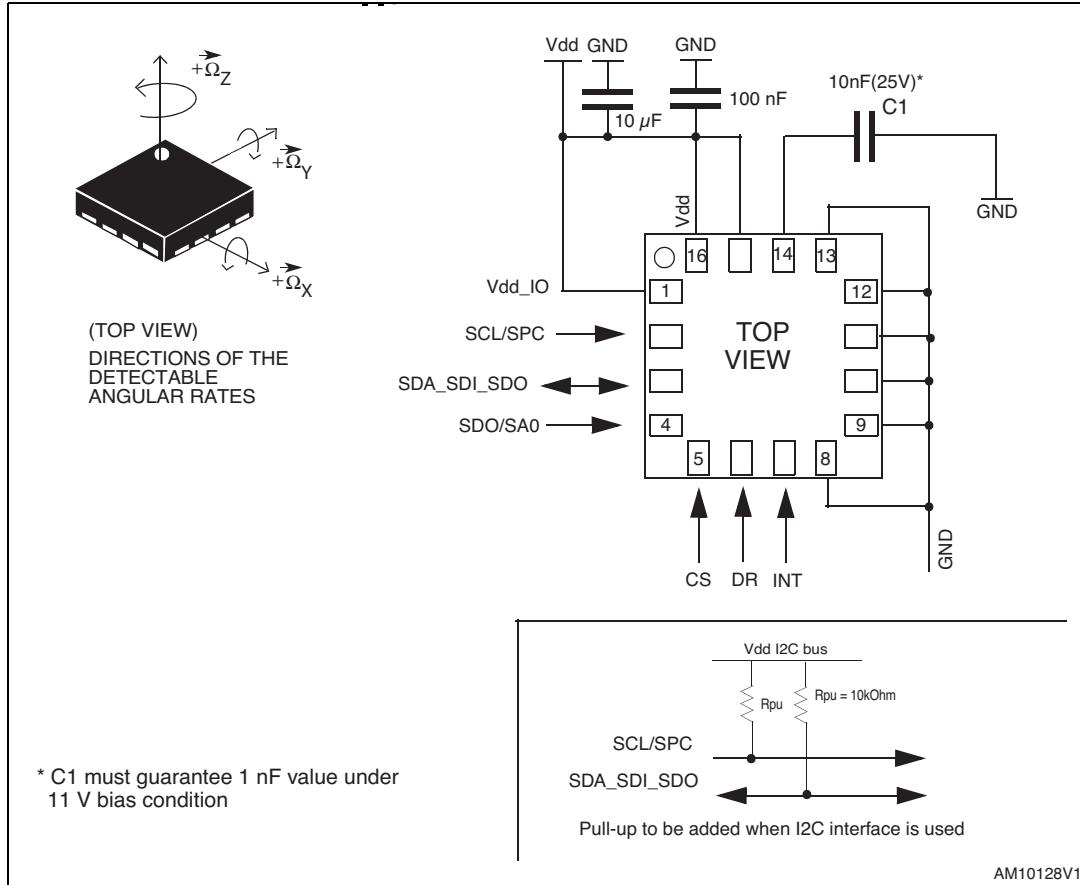
The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard. It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

3 Application hints

Figure 5. L3GD20 electrical connections and external component values



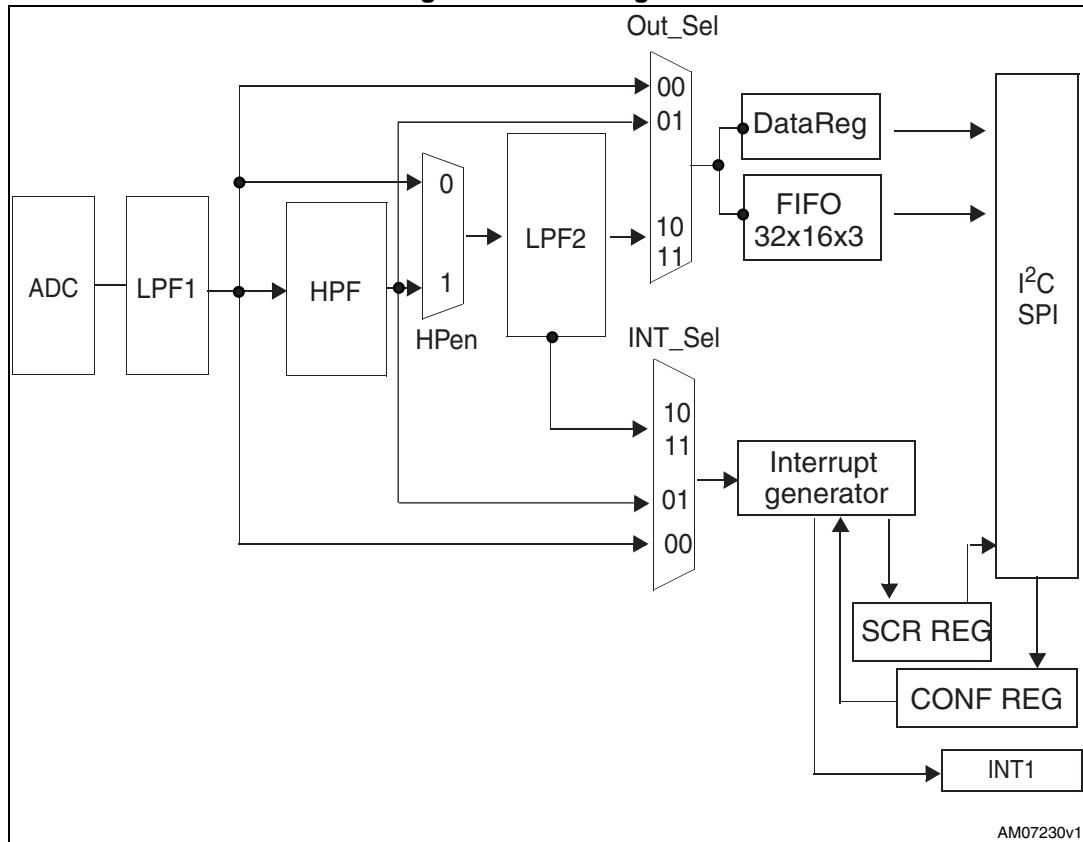
Power supply decoupling capacitors ($100\text{ nF} + 10\text{ }\mu\text{F}$) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, 100 nF and $10\text{ }\mu\text{F}$ decoupling capacitors must be placed between Vdd and common ground, and 100 nF between Vdd_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

4 Digital main blocks

4.1 Block diagram

Figure 6. Block diagram



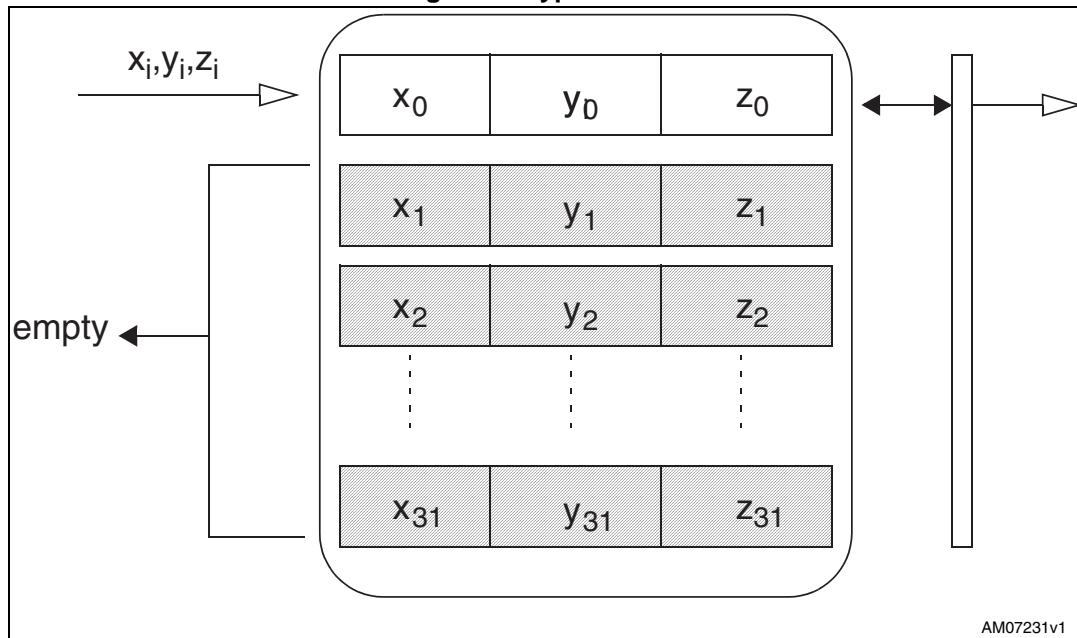
4.2 FIFO

The L3GD20 embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the FIFO_CTRL_REG (2Eh). Programmable Watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h)) and event detection information is available in FIFO_SRC_REG (2Fh). Watermark level can be configured to WTM4:0 in FIFO_CTRL_REG (2Eh).

4.2.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in [Figure 7](#) below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available, the old data is overwritten.

Figure 7. Bypass mode

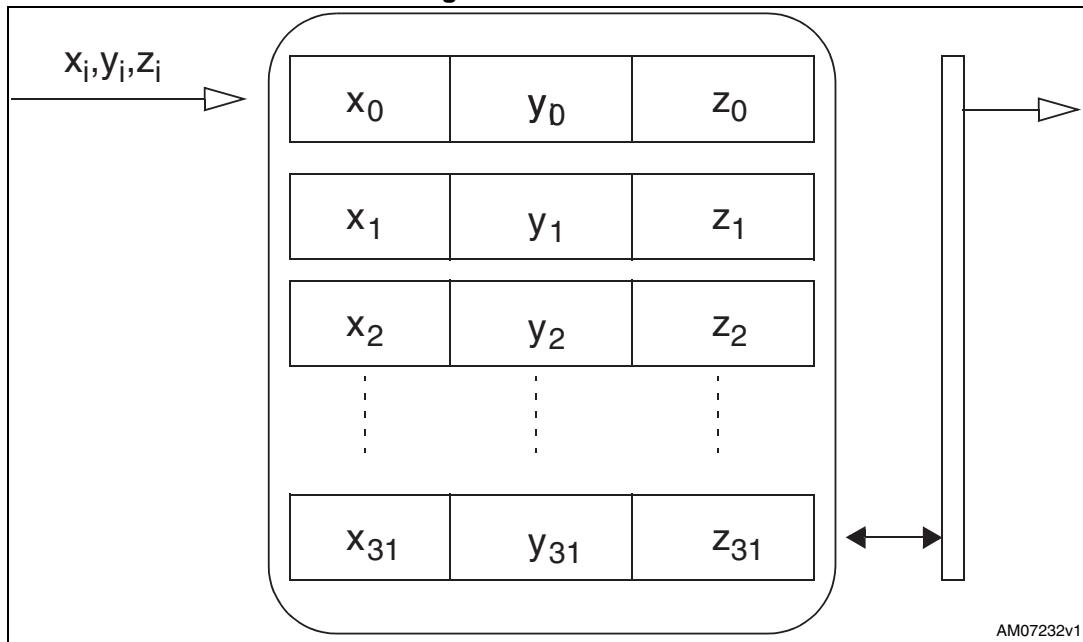


4.2.2 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit into CTRL_REG3 (22h)) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, the FIFO_CTRL_REG (2Eh) must be written back to Bypass mode.

FIFO mode is represented in [Figure 8: FIFO mode](#).

Figure 8. FIFO mode

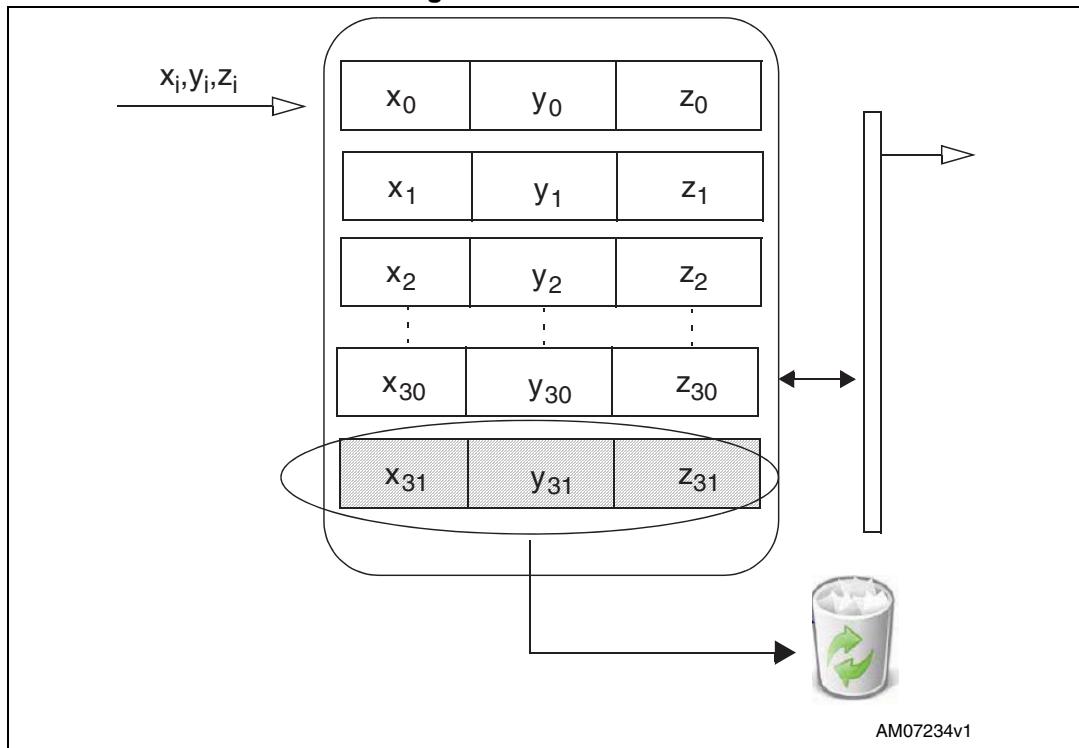


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4.2.3 Stream mode

In Stream mode, data from yaw, pitch and roll measurement are stored in the FIFO. A watermark interrupt can be enabled and set as in the FIFO mode. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY/INT2 pin (configured through CTRL_REG3 (22h)).

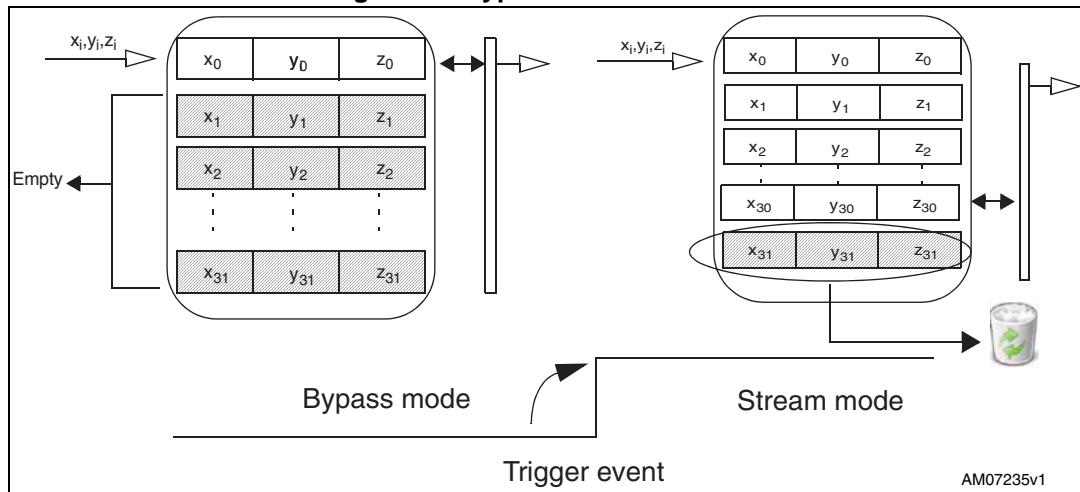
Stream mode is represented in [Figure 9: Stream mode](#).

Figure 9. Stream mode

4.2.4 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO begins operating in Bypass mode and once a trigger event occurs (related to INT1_CFG (30h) register events), the FIFO starts operating in Stream mode. Refer to [Figure 10](#) below.

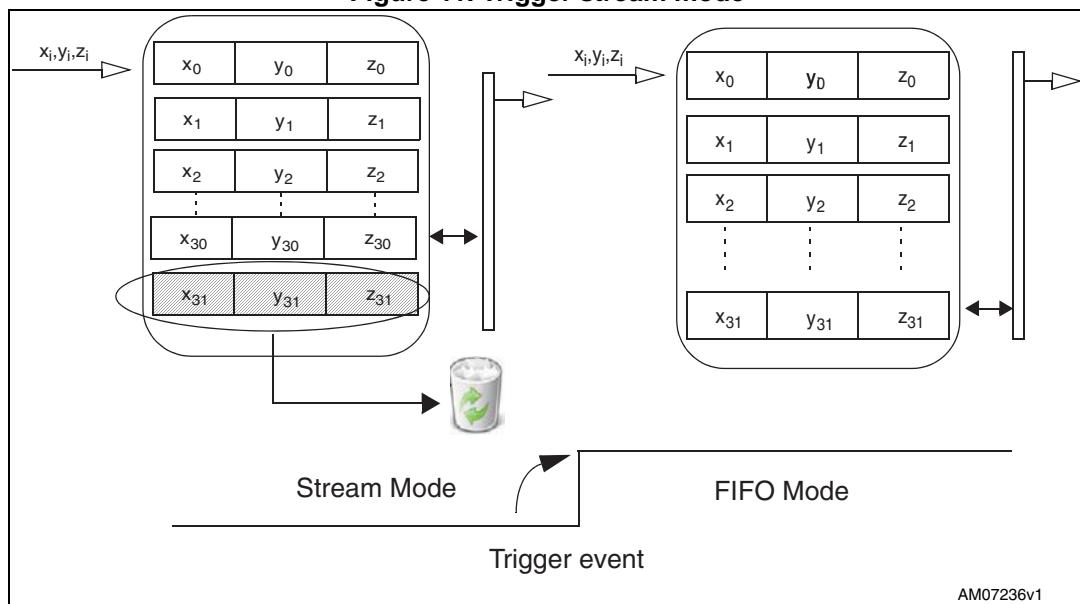
Figure 10. Bypass-to-stream mode



4.2.5 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2 by setting the I2_WTM bit in CTRL_REG3 (22h) in order to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of FIFO_CTRL_REG (2Eh). The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to INT1_CFG (30h) register events), the FIFO starts operating in FIFO mode. Refer to [Figure 11](#) below.

Figure 11. Trigger stream mode



4.2.6 Retrieve data from FIFO

FIFO data is read through OUT_X (Addr reg 28h,29h), OUT_Y (Addr reg 2Ah,2Bh) and OUT_Z (Addr reg 2Ch,2Dh). When the FIFO is in Stream, Trigger or FIFO mode, a read operation of the OUT_X, OUT_Y or OUT_Z registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data is placed in the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst (X,Y & Z with auto-incrementing address) operations can be used. When data included in OUT_Z_H (2Dh) is read, the system restarts to read information from addr OUT_X_L (28h).

5 Digital interfaces

The registers embedded in the L3GD20 may be accessed through both the I²C and SPI serial interfaces. The latter may be SW-configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I²C interface, the CS line must be tied high (i.e connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled)
SCL/SPC	I ² C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO	SPI serial data output (SDO) I ² C less significant bit of the device address

5.1 I²C serial interface

The L3GD20 I²C is a bus slave. The I²C is employed to write data into registers whose content can also be read back.

The relevant I²C terminology is given in the table below.

Table 11. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are high.

The I²C interface is compliant with fast mode (400 kHz) I²C standards as well as with normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated with the L3GD20 is 110101xb. The **SDO** pin can be used to modify the less significant bit of the device address. If the SDO pin is connected to voltage supply, LSb is '1' (address 1101011b). Otherwise, if the SDO pin is connected to ground, the LSb value is '0' (address 1101010b). This solution allows to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obligated to generate an acknowledge after each byte of data received.

The I²C embedded in the L3GD20 behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 12* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+read/write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5)
Write	110101	0	0	11010100 (D4)
Read	110101	1	1	11010111 (D7)
Write	110101	1	0	11010110 (D6)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R		MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA	

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to '1' while SUB(6-0) represents the address of the first register to be read.

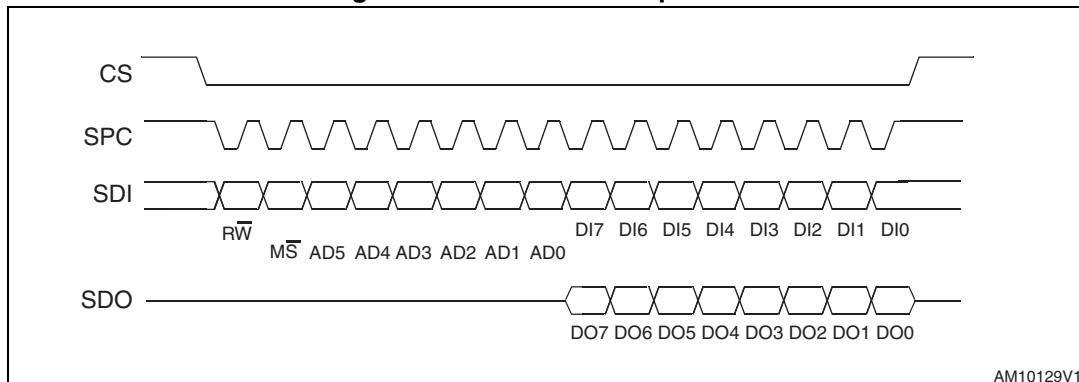
In the communication format presented, MAK is Master Acknowledge and NMAK is No Master Acknowledge.

5.2 SPI bus interface

The SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 12. Read and write protocol



CS is the Serial Port Enable and is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: **RW** bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: **MS** bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address will be auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

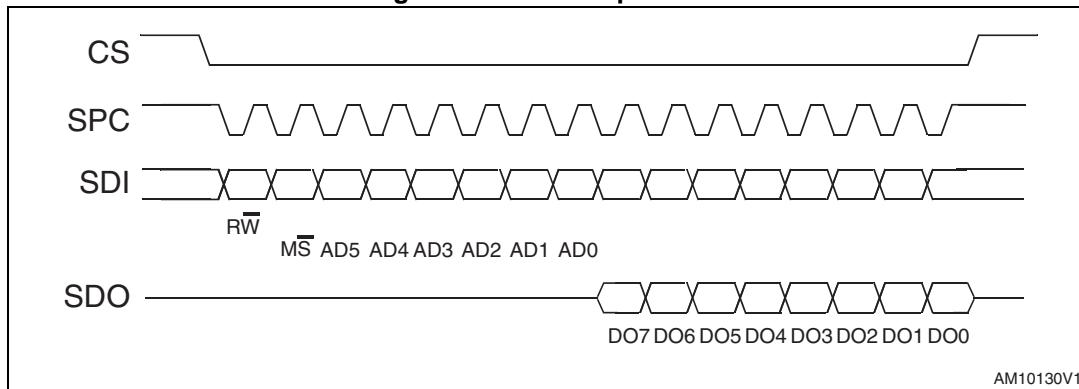
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods will be added. When the **MS** bit is 0, the address used to read/write data remains the same for every block. When the **MS** bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 13. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

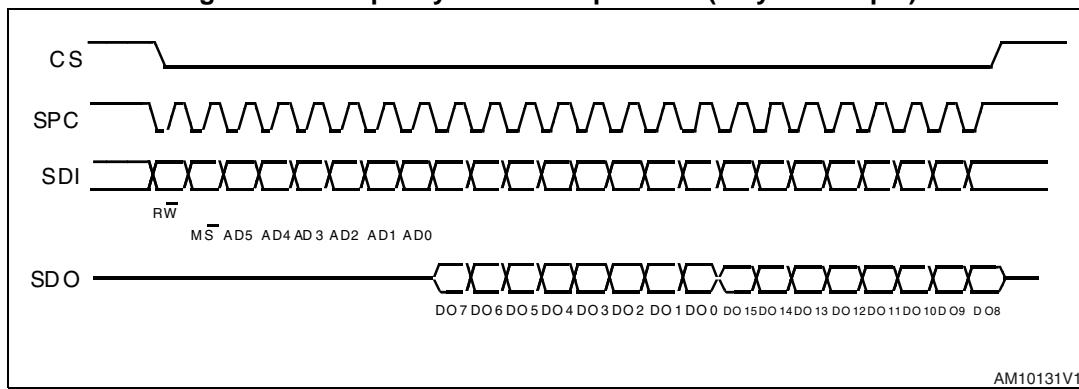
bit 1: MS̄ bit. When 0 do not increment address; when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

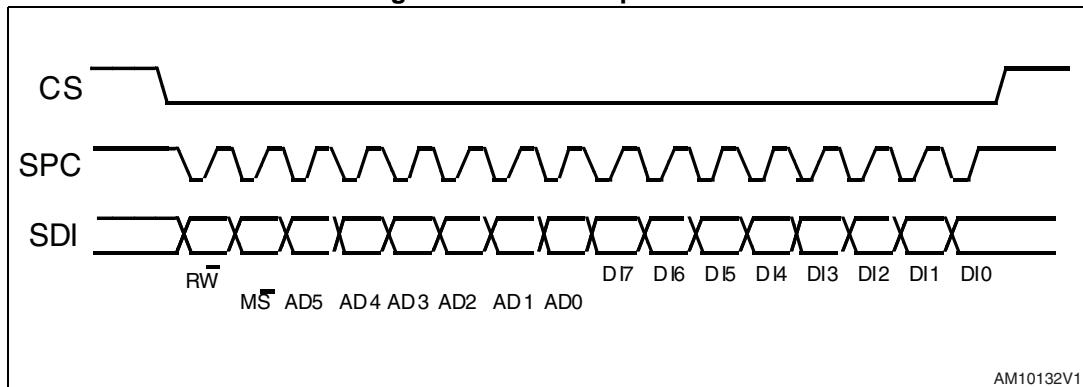
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 14. Multiple byte SPI read protocol (2-byte example)



5.2.2 SPI write

Figure 15. SPI write protocol



The SPI Write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

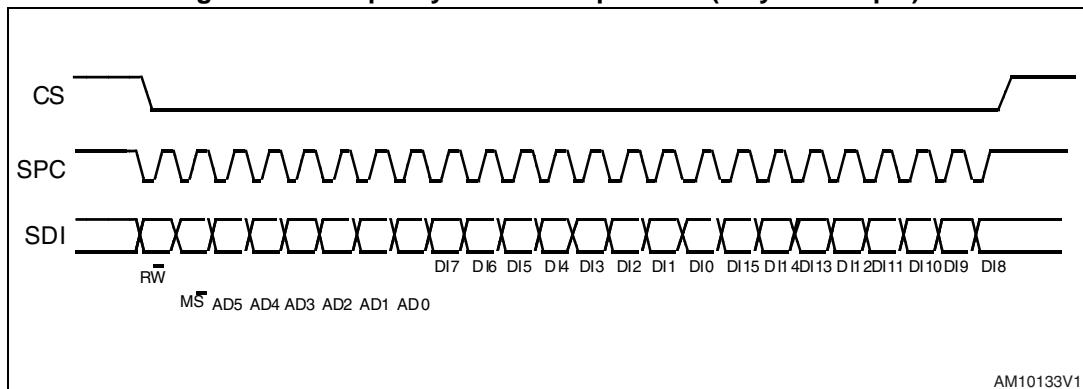
bit 1: MS̄ bit. When 0, do not increment address; when 1, increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written to the device (MSb first).

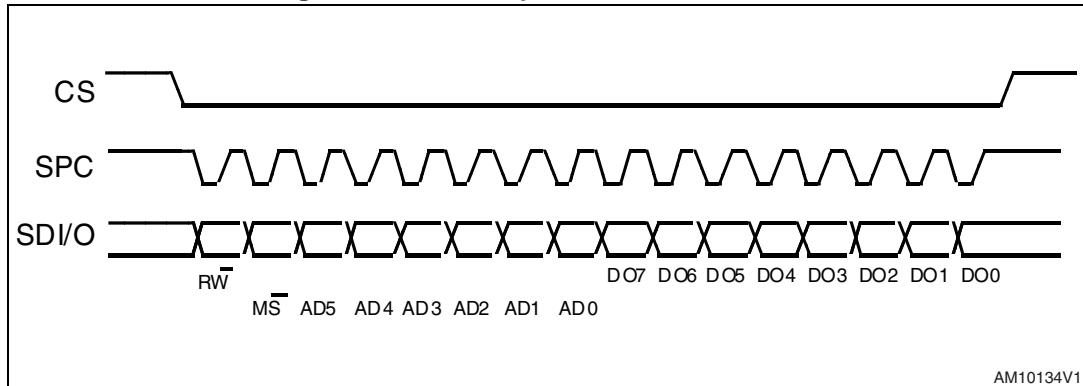
bit 16-... : data DI(...-8). Further data in multiple byte writing.

Figure 16. Multiple byte SPI write protocol (2-byte example)



5.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to '1' in CTRL_REG2.

Figure 17. SPI read protocol in 3-wire mode

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The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: \bar{MS} bit. When 0, do not increment address; when 1, increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

6 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device, and the related addresses:

Table 17. Register address map

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	r	0F	000 1111	11010100
Reserved	-	10-1F	-	-
CTRL_REG1	rw	20	010 0000	00000111
CTRL_REG2	rw	21	010 0001	00000000
CTRL_REG3	rw	22	010 0010	00000000
CTRL_REG4	rw	23	010 0011	00000000
CTRL_REG5	rw	24	010 0100	00000000
REFERENCE	rw	25	010 0101	00000000
OUT_TEMP	r	26	010 0110	output
STATUS_REG	r	27	010 0111	output
OUT_X_L	r	28	010 1000	output
OUT_X_H	r	29	010 1001	output
OUT_Y_L	r	2A	010 1010	output
OUT_Y_H	r	2B	010 1011	output
OUT_Z_L	r	2C	010 1100	output
OUT_Z_H	r	2D	010 1101	output
FIFO_CTRL_REG	rw	2E	010 1110	00000000
FIFO_SRC_REG	r	2F	010 1111	output
INT1_CFG	rw	30	011 0000	00000000
INT1_SRC	r	31	011 0001	output
INT1_TSH_XH	rw	32	011 0010	00000000
INT1_TSH_XL	rw	33	011 0011	00000000
INT1_TSH_YH	rw	34	011 0100	00000000
INT1_TSH_YL	rw	35	011 0101	00000000
INT1_TSH_ZH	rw	36	011 0110	00000000
INT1_TSH_ZL	rw	37	011 0111	00000000
INT1_DURATION	rw	38	011 1000	00000000

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Table 18. WHO_AM_I register

1	1	0	1	0	1	0	0
---	---	---	---	---	---	---	---

Device identification register.

7.2 CTRL_REG1 (20h)

Table 19. CTRL_REG1 register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen
-----	-----	-----	-----	----	-----	-----	-----

Table 20. CTRL_REG1 description

DR1-DR0	Output data rate selection. Refer to Table 21
BW1-BW0	Bandwidth selection. Refer to Table 21
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used for ODR selection. **BW <1:0>** is used for Bandwidth selection.

In the [Table 21](#) all frequencies resulting in combinations of DR / BW bits are reported.

Table 21. DR and BW configuration setting

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	00	95	12.5
00	01	95	25
00	10	95	25

Table 21. DR and BW configuration setting (continued)

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD**, **Zen**, **Yen**, **Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with [Table 22](#) below.

Table 22. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

7.3 CTRL_REG2 (21h)

Table 23. CTRL_REG2 register

0 ⁽¹⁾	0 ⁽¹⁾	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0
------------------	------------------	------	------	-------	-------	-------	-------

- These bits must be set to '0' to ensure proper operation of the device

Table 24. CTRL_REG2 description

HPM1- HPM0	High-pass filter mode selection. Default value: 00 Refer to Table 25
HPCF3- HPCF0	High-pass filter cutoff frequency selection Refer to Table 26

Table 25. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 26. High-pass filter cut off frequency configuration [Hz]

HPCF3-0	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

7.4 CTRL_REG3 (22h)

Table 27. CTRL_REG1 register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty
---------	---------	-----------	-------	---------	--------	---------	----------

Table 28. CTRL_REG3 description

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1:low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: push-pull; 1: open drain)
I2_DRDY	Date-ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

7.5 CTRL_REG4 (23h)

Table 29. CTRL_REG4 register

BDU	BLE	FS1	FS0	-	0 ⁽¹⁾	0 ⁽¹⁾	SIM
-----	-----	-----	-----	---	------------------	------------------	-----

1. This value must not be changed.

Table 30. CTRL_REG4 description

BDU	Block data update. Default value: 0 (0: continuos update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

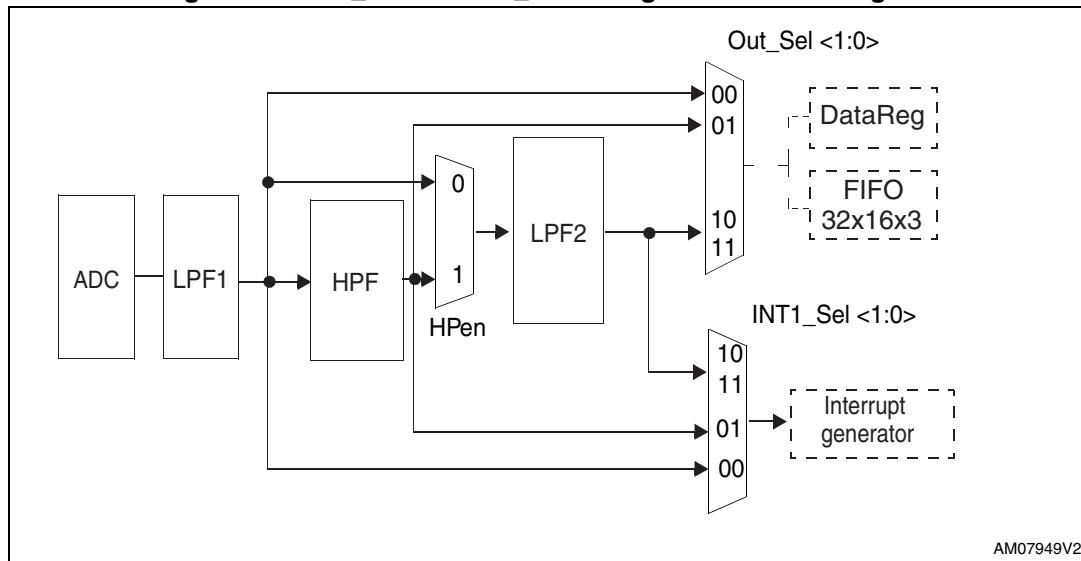
7.6 CTRL_REG5 (24h)

Table 31. CTRL_REG5 register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0
------	---------	----	------	-----------	-----------	----------	----------

Table 32. CTRL_REG5 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled See Figure 20)
INT1_Sel1-INT1_-Sel0	INT1 selection configuration. Default value: 0 (See Figure 20)
Out_Sel1-Out_-Sel1	Out selection configuration. Default value: 0 (See Figure 20)

Figure 18. INT1_Sel and Out_Sel configuration block diagram

7.7 REFERENCE/DATACAPTURE (25h)

Table 33. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0
------	------	------	------	------	------	------	------

Table 34. REFERENCE register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0
------------	--

7.8 OUT_TEMP (26h)

Table 35. OUT_TEMP register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
-------	-------	-------	-------	-------	-------	-------	-------

Table 36. OUT_TEMP register description

Temp7-Temp0	Temperature data
-------------	------------------

Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

7.9 STATUS_REG (27h)

Table 37. STATUS_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
-------	-----	-----	-----	-------	-----	-----	-----

Table 38. STATUS_REG description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

7.13 FIFO_CTRL_REG (2Eh)

Table 39. REFERENCE register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0
-----	-----	-----	------	------	------	------	------

Table 40. REFERENCE register description

FM2-FM0	FIFO mode selection. Default value: 00 (see Table 41)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 41. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

7.14 FIFO_SRC_REG (2Fh)

Table 42. FIFO_SRC register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0
-----	------	-------	------	------	------	------	------

Table 43. FIFO_SRC register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

7.15 INT1_CFG (30h)

Table 44. INT1_CFG register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
--------	-----	------	------	------	------	------	------

Table 45. INT1_CFG description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events)
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

7.16 INT1_SRC (31h)

Interrupt source register. Read only register.

Table 46. INT1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 47. INT1_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Reading at this address clears INT1_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

7.17 INT1_THS_XH (32h)

Table 48. INT1_THS_XH register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8
---	--------	--------	--------	--------	--------	-------	-------

Table 49. INT1_THS_XH description

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000
----------------	---

7.18 INT1_THS_XL (33h)

Table 50. INT1_THS_XL register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0
-------	-------	-------	-------	-------	-------	-------	-------

Table 51. INT1_THS_XL description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000
---------------	---

7.19 INT1_THS_YH (34h)

Table 52. INT1_THS_YH register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8
---	--------	--------	--------	--------	--------	-------	-------

Table 53. INT1_THS_YH description

THSY14 - THSY9	Interrupt threshold. Default value: 0000 0000
----------------	---

7.20 INT1_THS_YL (35h)

Table 54. INT1_THS_YL register

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0
-------	-------	-------	-------	-------	-------	-------	-------

Table 55. INT1_THS_YL description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000
---------------	---

7.21 INT1_THS_ZH (36h)

Table 56. INT1_THS_ZH register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8
---	--------	--------	--------	--------	--------	-------	-------

Table 57. INT1_THS_ZH description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000
----------------	---

7.22 INT1_THS_ZL (37h)

Table 58. INT1_THS_ZL register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
-------	-------	-------	-------	-------	-------	-------	-------

Table 59. INT1_THS_ZL description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000
---------------	---

7.23 INT1_DURATION (38h)

Table 60. INT1_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0
------	----	----	----	----	----	----	----

Table 61. INT1_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = '0': the interrupt falls immediately if the signal crosses the selected threshold

Wait = '1': if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 19. Wait disabled

- Wait-bit = '0' → Interrupt disabled as soon as condition is no more valid (ex: Rate value below threshold)

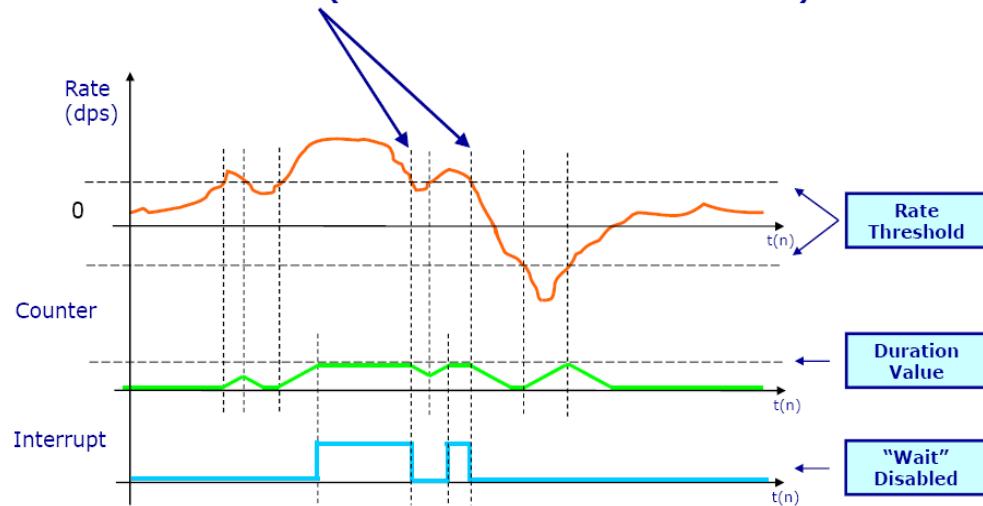
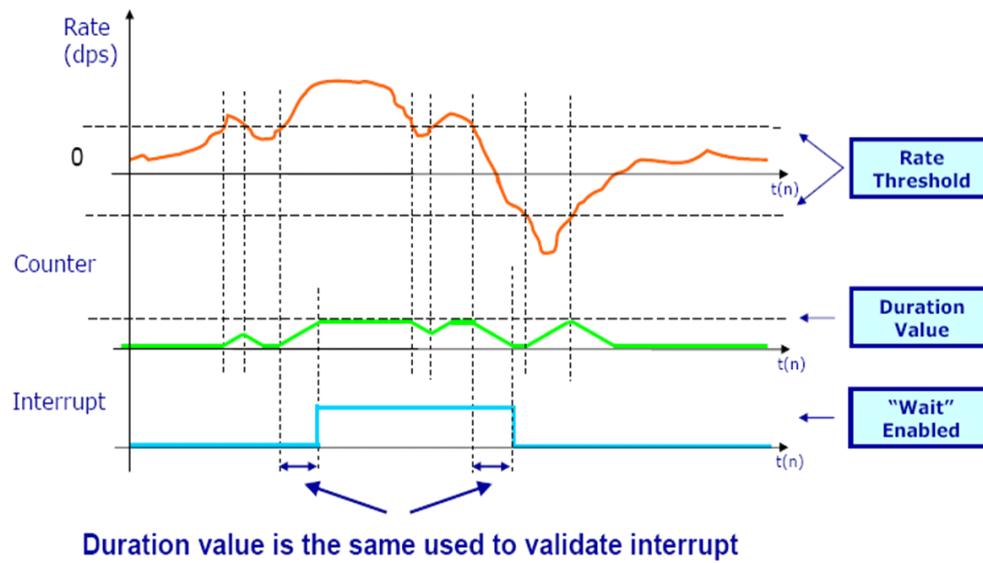


Figure 20. Wait enabled

- Wait-bit = '1' → Interrupt disabled after duration sample (sort of hysteresis)



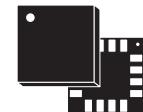
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.
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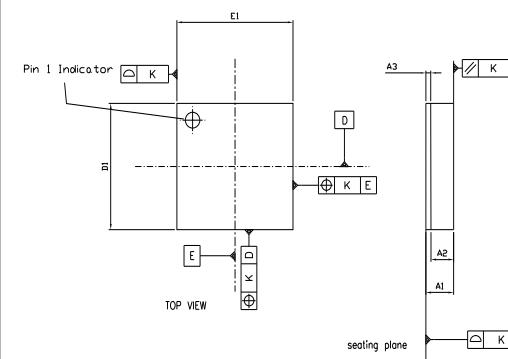
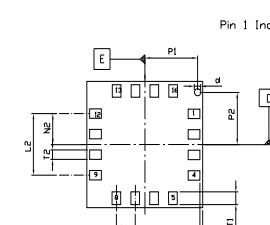
Figure 21. LGA-16: mechanical data and package dimensions

Ref.	Dimensions			inch		
	mm					
	Min.	Typ.	Max.	Min.	Typ.	Max.
A1			1.000			0.0394
A2		0.785			0.0309	
A3		0.200			0.0079	
d		0.300			0.0118	
D1	3.850	4.000	4.150	0.1516	0.1575	0.1634
E1	3.850	4.000	4.150	0.1516	0.1575	0.1634
L2		1.950			0.0768	
M		0.100			0.0039	
N1		0.650			0.0256	
N2		0.975			0.0384	
P1		1.750			0.0689	
P2		1.525			0.0600	
T1		0.400			0.0157	
T2		0.300			0.0118	
k		0.050			0.0020	

Outline and mechanical data



**LGA-16 (4x4x1mm)
Land Grid Array Package**

8125097_A

9 Revision history

Table 62. Document revision history

Date	Revision	Changes
18-Aug-2011	1	Initial release.
27-Feb-2013	2	Updated Table 12: SAD+read/write patterns and Table 23: CTRL_REG2 register .

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5.4. Estructura del Proyecto

El proyecto se organizó de la siguiente manera:

```
.  
src  
  clock.c  
  clock.h  
  console.c  
  console.h  
  dashboard_sismografo.json  
  enviar_iot.py  
  Makefile  
  sismografo.c
```

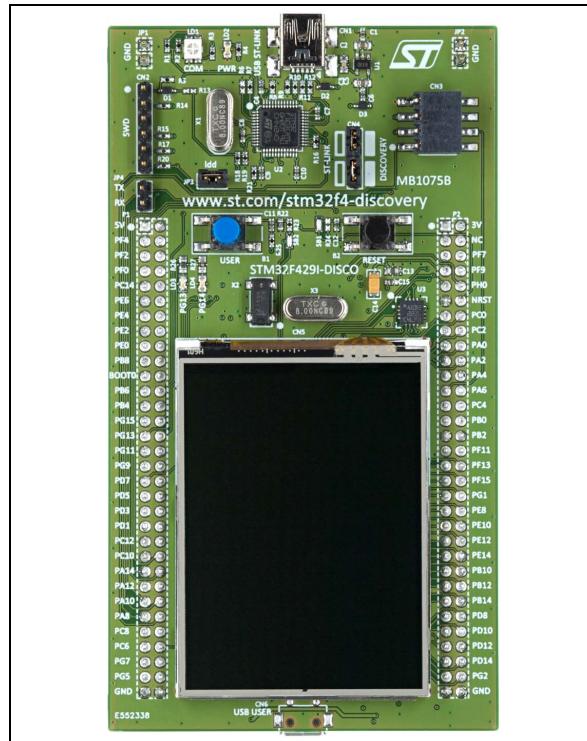
5.5. Hoja de datos STM32F429

Discovery kit with STM32F429ZI MCU

Data brief

Features

- STM32F429ZIT6 microcontroller featuring 2 Mbytes of Flash memory, 256 Kbytes of RAM in an LQFP144 package
- On-board ST-LINK/V2 on STM32F429I-DISCO or ST-LINK/V2-B on STM32F429I-DISC1
- mbed™ -enabled (mbed.org) with ST-LINK/V2-B only
- USB functions:
 - debug port
 - virtual COM port with ST-LINK/V2-B only
 - mass storage with ST-LINK/V2-B only
- Board power supply: through the USB bus or from an external 3 V or 5 V supply voltage
- 2.4" QVGA TFT LCD
- 64-Mbit SDRAM
- L3GD20, ST MEMS motion sensor 3-axis digital output gyroscope
- Six LEDs:
 - LD1 (red/green) for USB communication
 - LD2 (red) for 3.3 V power-on
 - Two user LEDs: LD3 (green), LD4 (red)
 - Two USB OTG LEDs: LD5 (green) VBUS and LD6 (red) OC (over-current)
- Two push-buttons (user and reset)
- USB OTG with micro-AB connector
- Extension header for LQFP144 I/Os for a quick connection to the prototyping board and an easy probing
- Comprehensive free software including a variety of examples, part of STM32CubeF4 package or STSW-STM32138 for legacy standard libraries usage



1. Picture not contractual.

Description

The STM32F429 Discovery kit (32F429IDISCOVERY) allows users to easily develop applications with the STM32F429 high-performance MCUs with ARM® Cortex®-M4 core.

It includes an ST-LINK/V2 or ST-LINK/V2-B embedded debug tool, a 2.4" QVGA TFT LCD, an external 64-Mbit SDRAM, an ST MEMS gyroscope, a USB OTG micro-AB connector, LEDs and push-buttons.



System requirements

- Windows® OS (XP, 7, 8)
- USB type A to Mini-B cable

Development toolchains

- IAR EWARM (IAR Embedded Workbench®)
- Keil® MDK-ARM™
- GCC-based IDEs (free AC6: SW4STM32, Atollic® TrueSTUDIO®,...)
- ARM® mbed™ online

Demonstration software

The demonstration software is preloaded in the board Flash memory. It displays on the screen icons to run different applications: clock/calendar, a game, a video player and an image browser, performance monitoring and system information.

The latest versions of the demonstration source code and associated documentation can be downloaded from the www.st.com/stm32f4-discovery webpage.

Ordering information

To order the Discovery kit for the STM32F429 line of microcontrollers, refer to [Table 1](#).

Table 1. List of the order codes

Order code	ST-LINK version
STM32F429I-DISCO	ST-LINK/V2
STM32F429I-DISC1	ST-LINK/V2-B (mbed-enabled)

Revision history

Table 2. Document revision history

Date	Revision	Changes
06-Sep-2013	1	Initial version.
29-Sep-2014	2	Updated Section : Features and Section : Description to introduce STM32cubeF4 and STSW-STM32138. Updated ST MEMS feature. Updated Section : System requirements and Section : Development toolchains .
23-Oct-2015	3	Updated Section : Features , Section : Description , Section : Ordering information .

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