Implementation of NEMS Interconnect Relays for Reconfigurable Circuits

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Abstract

In recent years, there has been much attention on bringing mechanical systems to the nanoscale. Reconfigurable computing for AI and Machine Learning has also sparked lots of growth in the tech industry. Recently, CMOS compatible Back-End-Of-Line mechanical systems have been proposed to create denser reconfigurable systems. In this project, we propose the design of a BEOL 5T standard cell switch and its implementation in a complex digital system for reduced die area and increased circuit complexity in a 7nm process (ASAP7). Example applications where these would be most pertinent include reconfigurable digital logic, reconfigurable hi-fidelity analog frontend, or compute-in-memory for AI/ML. Our goal is to perform the first step of Design-Technology Co-Optimization by integrating the switch standard cell into the hammer-vlsi flow alongside other devices from the ASAP7 library.

I. Introduction

Field Programmable Gate Arrays (FPGAs) have long been used to enable rapid prototyping of digital systems pre-tapeout of Application Specific Integrated Circuits (ASICs). The framework they provide for high-performance reconfigurable digital systems is now proving useful for end-use applications including ML-acceleration, cryptocurrency mining, high-frequency stock trading, and software-defined radios. FPGA demand is predicted to continue rising as these protoyping and end-use markets increase in demand.

To enable this flexibility, FPGA-based systems are much more demanding than their ASIC counterparts. FPGAs come with larger die area requirements, delay, and dynamic power consumption. These factors increase the cost of FPGA-based systems and lower their potential performance over ASIC-based systems. Recently, CMOS compatible devices have been developed that could mitigate these area/power/performance drawbacks. Nano-Electro-Mechanical-Systems (NEMS) provide a promising, easily-integratable way to further FPGA-based systems. But first, a look at where all this overhead comes from in FPGAs.

The Island-Style FPGA architecture

FPGAs general consist of a general logic fabric as well as application-specific components, such as block RAM, DSPs, clocking, I/O, and serial I/O. This project will tackle the general logic fabric, since it makes up the majority of the FPGA.

Island-Style logic fabric can be divided into two major components: Configurable Logic Blocks and Reconfigurable Interconnects. Configurable Logic Blocks (CLBs) are used to implement arbitrary combinational and sequential logic circuits. They consist of Lookup Tables, Flip Flops, and Multiplexers. Each CLB can be programmed to perform an arithmetic or state-based portion of a larger logic sys-

tem. CLBs are connected together using reconfigurable interconnects. Reconfigurable Interconnects, made up of Connection Blocks and Switch Boxes, are the âĂIJbreadboardâĂİ of the FPGA. They allow the portions of the digital system to communicate. In an Island-Style Architecture, Connection Blocks connect CLBs to routing wires that run throughout the fabric. Those wires are then connected to each other via Switch Boxes. These routing elements are primarily made up of muxes and SRAM, a setup that is readily implementable using NEM relays.

These Reconfigurable Interconnects dominate the area/power overhead incurred by FPGAs [Altera 08]. In an ASIC, interconnects are simple, passive elements; circuits are connected using fixed metal lines paths above the transistor devices. To enable design flexibility, FPGAs add SRAM configuration storage as well as the mux circuitry required to connect blocks and wires. Not only does this additional circuitry incur a large power/delay overhead, it also must be implemented completely in the Front-End-Of-Line alongside logic transistors, adding significantly to die area.

Obviously, FPGAs are awesome, and have many compelling applications. But how to mitigate the performance/area/power hits? ASIC circuits are connected solely via Back-End-Of-Line (BEOL) Metal lines. If FPGAs could emulate this structure, much of the overhead incurred from reconfigurable interconnects could be eliminated.

NEM Relays

Nanoelectromechanical Relays are electrically actuated mechanical switches. Notably, they experience zero leakage, have the potential for lower on-state resistance than NMOS pass gate, and can be implemented in the BEOL in a CMOS-compatible process flow. The major disadvantages of NEM relays are large mechanical switching delay (> 1ns) and lower reliability with respect to transistors ($\tilde{1}0\hat{9}10\hat{1}0$ cycles). The two relay device architectures examined in this work are lateral âĂIJcrab styleâĂİ relays and vertical interconnect relays. Due to their hysteretic properties, they can be implemented to replace both the interconnect pass-gates and their corresponding SRAM cells.

The lateral âĂIJcrab-styleâĂİ relays are the result of many years of development at Stanford and UC Berkeley to create an efficient CMOS compatible NEM relay. These relays are switched on/off using the gate to body voltage difference. When âĂIJoffâĂİ, no current flows across the air gap. When âĂIJonâĂİ, current flows between the drain and source with low on-state resistance. With this design, the device can be body-biased to have an extremely small switching voltage, experimentally shown to be sub- 50mV range.

The vertical relays are designed to be more compact and compatible with existing CMOS process flows. Rather than using deposited metal or polysilicon as the structural material, these vertical relays use the already-present metal vias/interconnects in a CMOS process flow. These relays can be implemented as single-pole double-throw switches or simpler single-pole single-throw switches (like the lateral relays). Both have their own drawbacks and benefits. While the lateral relays involve a âĂIJcustomâĂİ structure, these vertical ones are designed within the constraints of standard CMOS BEOL design rules; i.e, they use standard metal line/via structures, and dimensions are standard for the process node.

II. Proposed Techniques

III. Methods (A/B comparison)

SRAM-based island-style FPGAs represent the vast majority of commercial and academic FPGA implementations [**?**]. For this reason, this architecture will be used to construct three functionally equivalent FPGAs using the three different routing schemes discussed in the previous Section II.

To create an island-style FPGA a basic *tile* must first be constructed. Each tile consists of one *configurable logic block* (CLB), two *connection boxes* (CBs), and one *switch box* (SB). The CLB contains N basic logic elements (BLEs) which each contain a K-input look-up-table (LUT) and

a flip-flop. In addition, CLBs provide an intra-cluster routing network to connect the CLB I/O to the individual BLE I/O. The CBs connect the CLBs to their adjacent routing channels, while the SBs provide the connections between intersecting routing channels. It is common to fold the output portion of the CBs into the SB [**?**]. Thus, the same MUXes used for connecting routing channels can be enlarged to accomodate the additional CLB output connections.

To ensure that our results are consistent with previous works, we will create a very similar tile to the one described in [**?**]. This tile consists of 10 4-LUT BLEs w/ 22 input pins and 10 output pins. In order to simplify the design, the CBs in our tile will connect both the outputs and inputs of the CLB to the adjacent routing channel. The intra-CLB routing network will be fully populated, allowing for connection between any BLE input and CLB input as well as between any BLE output and CLB output. The SB flexibility will be set to 3 ($f_{SB} = 3$), allowing all incoming signals to the SB to be switched left, right, or straight through. The CB input and output flexibilities will be set to 0.2 ($f_{CB-in} = 0.2$) and 0.1 respectively ($f_{CB-out} = 0.1$). These flexibilities determine the proportion of signals within the adjacent routing channels that the CB can connect an input or output signal to.

The CMOS-only FPGA will serve as a baseline for the NEMs designs. Because the programmable interconnect (PI) will be replaced with NEMs relays, the make up of our baseline's PI will significantly impact the perceived benefits. We will use simple NMOS pass-transistors to build the MUXes used for the PI and the LUTs. While transmission gates show promise for scaled nodes, commercial FPGAs continue to use pass-transistors with gate-boosting and internal buffering to achieve a slightly lower area-delay product [**?**].

The NEMs relays can be modeled as simple RC circuits when configured in the ON-state [**?**] [**?**] and can be ignored, because they are physically disconnected from the circuit, when in the OFF-state. Modeling the dynamics of the NEMs relays as they switch on and off is not as important as this steady-state behavior for this analysis. As long as the configuration times are not prohibitively long, and they have been shown not to be [**?**] [**?**], then the dynamics of the switches can be ignored.

Preliminary area analysis can be done by comparing each FPGA tile. It is important to account for the additional metal area used by the relays as this will significantly impact the place-and-route quality due to higher routing congestion. Further analysis can be performed on the full FPGAs to determine the dissipated power and maximum operating frequency for each design for a given set of test circuits.

IV. Hypothesis

V. Conclusion

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