Control iD

PCB Stack-up and Technical Requirements

Our minimum specifications are as follow:

Number of layers:	**2 layers**
Minimum line width (<=):	**8 mils**
Minimum line spacing/gap (<=):	**8 mils**
Minimum Annular Ring (<=):	**8 mils**
Minimum mechanical hole size (<=):	**0,3mm**
Surface finish:	**HASL**
Electrical Test:	**100% Electrical Test (E-Test)**
Substrate type:	**FR-4**

PCB Stack-up and files:

Layer name	Thickness (mm)	File extension
Silkscreen Top (White)	-	*.GTL
Soldermask Top (Red)	-	*.GTS
Copper Top	0,036	*.GTL
Dielectric	1,5	-
Copper Bottom	0,036	*.GBL
Soldermask Bottom (Red)	-	*.GBS
Silkscreen Bottom (White)	-	*.GBO
Total thickness	1,572	

File type	File Extension
Stencil top	*.GTP
Board outline	*.GM1
Drill information (2.5 / Leading zero suppression) (All vias are 100% pass through)	*.TXT