

Week 3 - Sequential Logic

Combinatorial logic ignores the issue of time.

Results (output) are computed instantaneously.

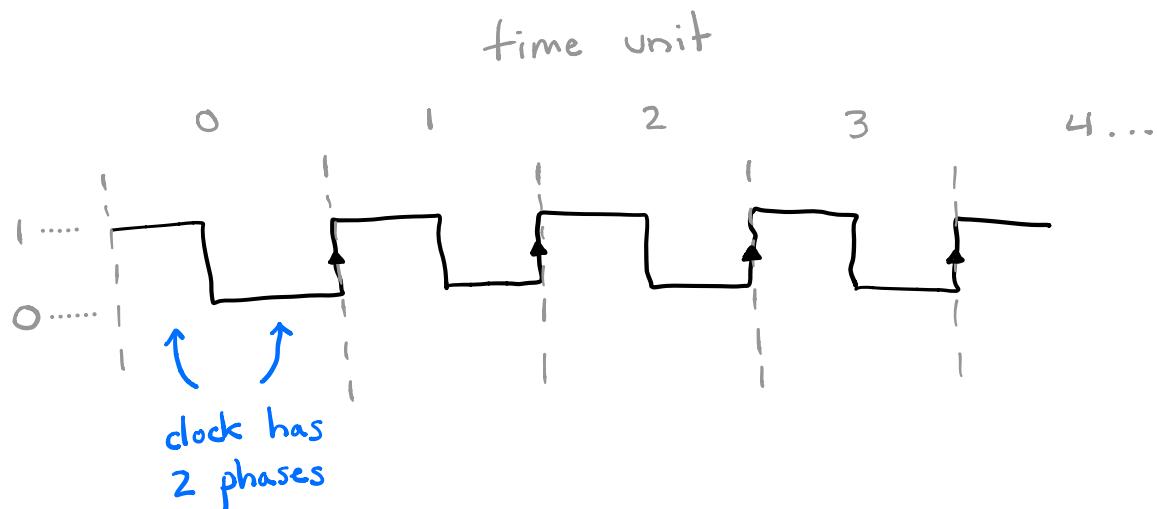
There are two issues with this: (like an adder)

1) How to "re-use" hardware?

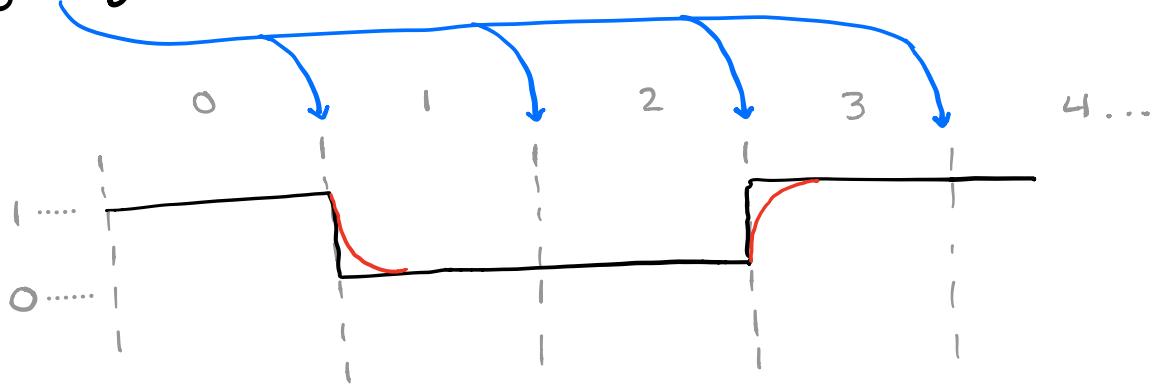
2) How to maintain state?

this is the important one! Computers need to remember things to compute!

Time is handled in digital systems using a discrete clock.



Obviously, real electrical signals do not change instantaneously. But the abstraction of the clock allows us to only care about the state of signals at the beginning of a new clock cycle.



→ a clock period must be long enough to account for the longest of these real "propagation delays" and other electrical effects.

A discrete clock allows synchronization + stability.

Combinatorial:

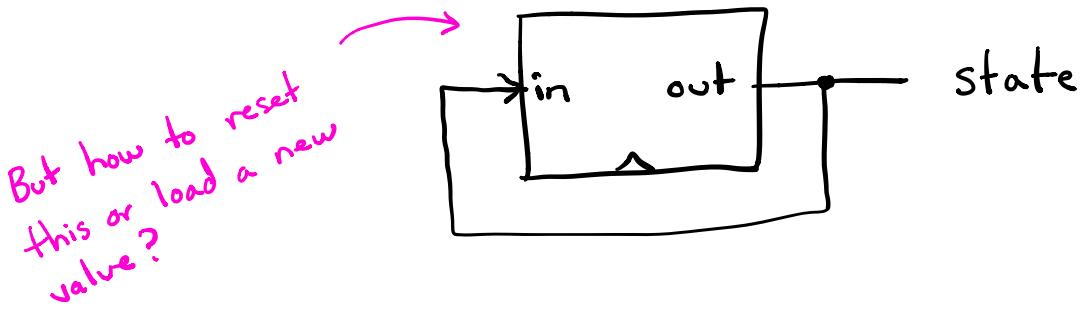
$$\text{out}[+] = f(\text{in}[+])$$

$$\text{out}[+] = f(\text{in}[+1])$$

Sequential:

could also be $f(\text{in}[+], \text{in}[+1])$, but the course discourages this and defines sequential logic as depending on inputs from the previous time step only - not the current time step ↗ related: Mealy vs Moore design

By looping the output back to the input, you get a circuit that can **maintain state**.



$$\text{state}[t] = f(\text{state}[t-1])$$

On to the chips...

The core chip is the **data flip flop (DFF)**



$$\text{out}[t] = \text{in}[t-1]$$

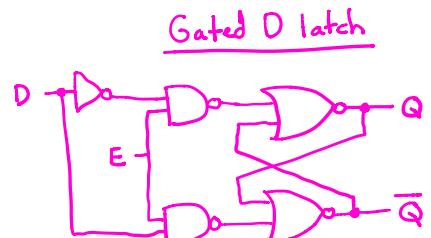
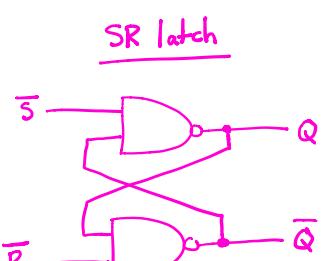
Really, this course should be called "(NAND + DFF)2Tetris"

The elemental DFF is just as critical as the primitive NAND gate!

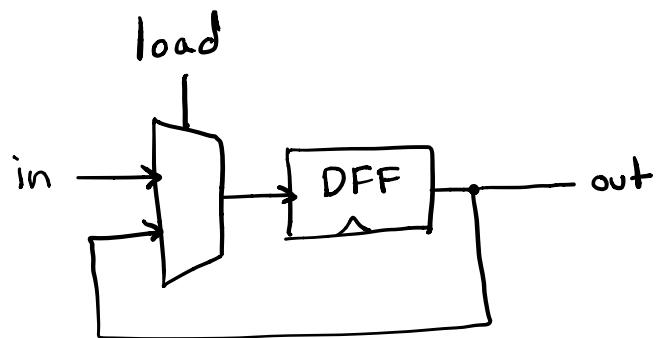
This is a primitive/provided circuit!

However, a DFF can be constructed physically using NAND gates and feedback loops.

- 1) Construct a gated D latch
- 2) Chain two latches together to isolate across time steps.

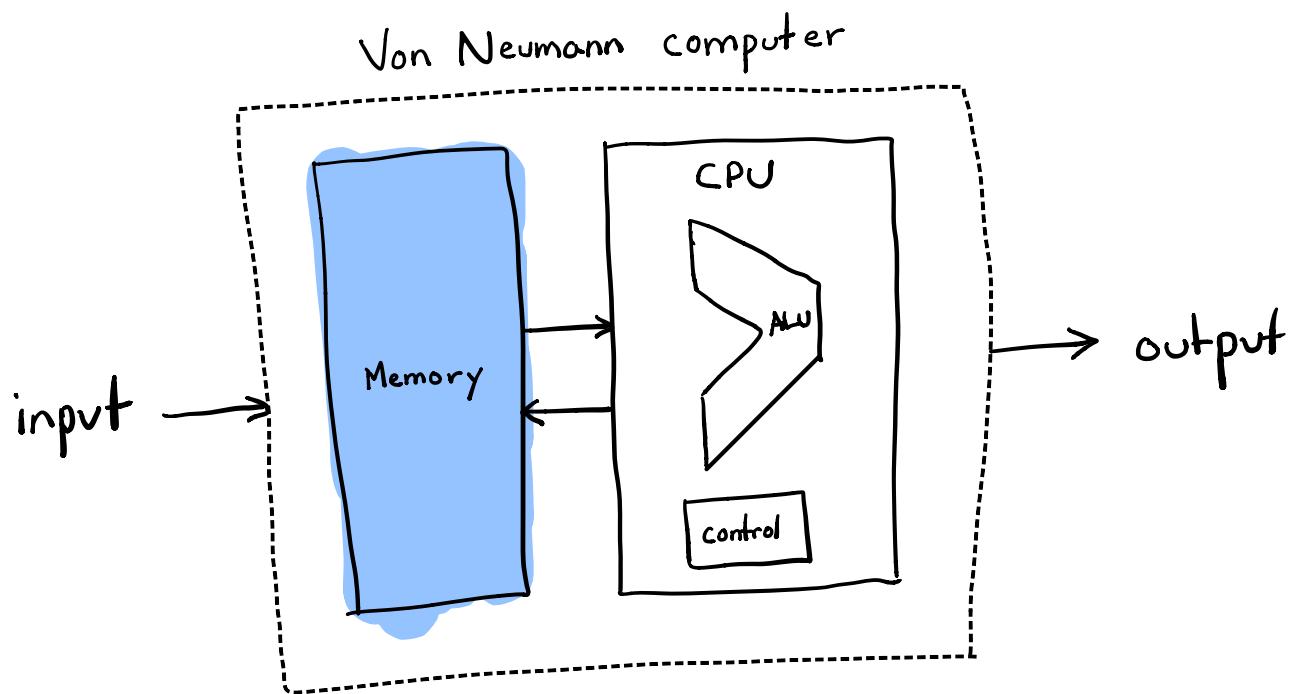


1-bit register ("Bit")



Memory units

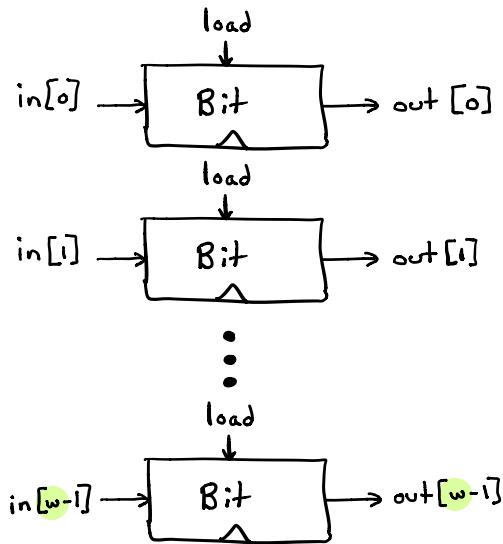
In the Von Neumann architecture, the main system memory contains both **instructions** and **data**.



This course mostly focuses on **logical** descriptions of blocks, not the physical implementations.

16-bit Register

A w -bit wide register can be constructed from w 1-bit registers in parallel.

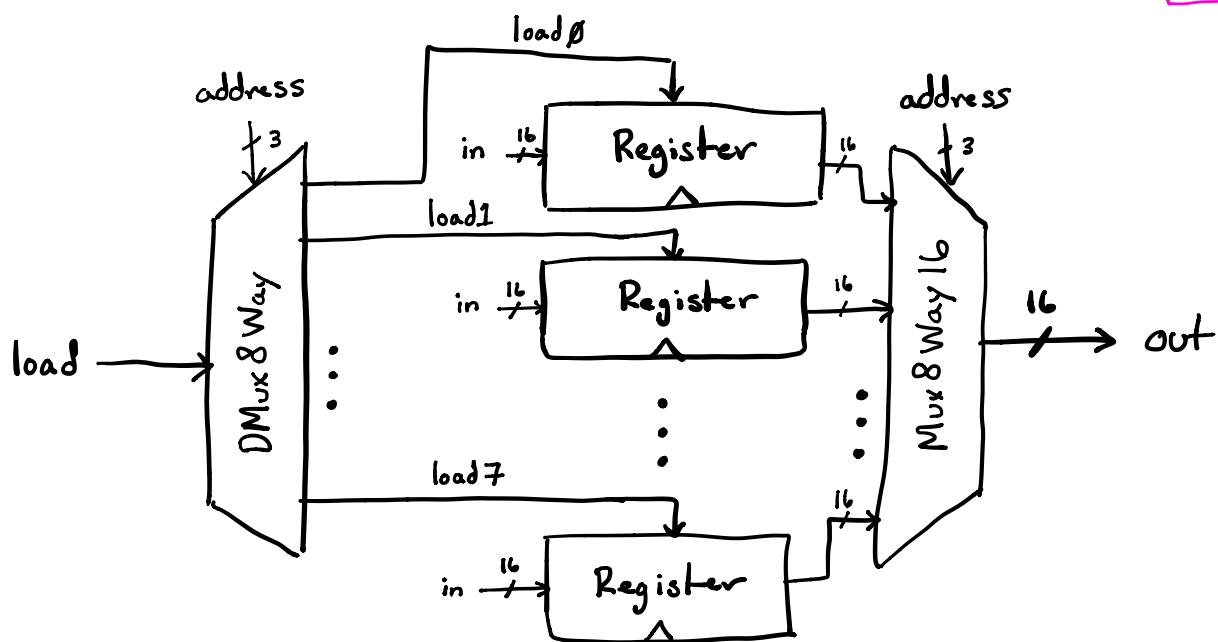


RAM unit abstraction:

A sequence of n addressable w -bit wide registers.

RAM8

↓
 size
 of the RAM ↓
 width
 of the RAM For the Hack computer
 architecture, $w = 16$



RAM64, RAM512, RAM4k, and RAM16k can be constructed hierarchically using the same topology as RAM8, but using smaller, previously constructed RAM units in place of Registers.

PC (counter)

