

Example : TLB och Cacheinteraktion

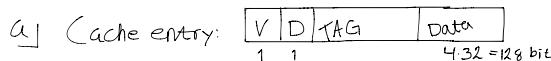
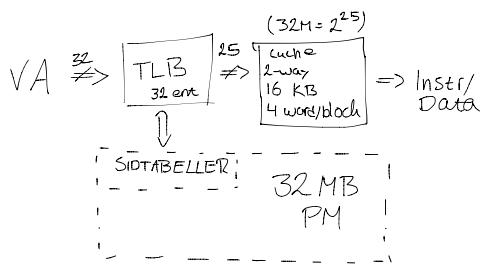
Virtuellt minne exempel (tentamensfråga 4 2010-08-16)

- Assume a computer system with the following characteristics: The CPU uses virtual memory (unified data- and instructions) using 32-bit virtual addresses. There is a maximum of 32 MB of physical primary memory, and a two-way set associative 16 KB cache. The hit-time in this cache is 1.5 ns. A 32-entry fully associative TLB is used for virtual-to-physical address translations. The TLB hit-time is 1 ns. The page size is 16 KB, and the cache uses a block size of 4 words.
- The cache, the TLB, and the virtual memory uses a "write-back" ("copy-back") strategy. The replacement algorithm used by the cache is "Random", and for the virtual memory an approximative "LRU" using 2-bit time "time stamps" per page. Virtual memory pages that belong to the OS are marked with a "protection bit" to protect it from user process accesses. In maximum, 16 processes are active at any given time. The Page Tables do not store secondary storage addresses when the pages are not in primary memory.

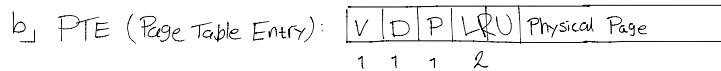
2010-08-16, uppg.4 , forts

- a. How many bits must the cache memory be able to store ? (4 p)
- b. How many bytes is needed to store the Page Tables ? (4 p)
- c. How many bits must the TLB be able to store ? (4 p)
- d. What is the maximum clock frequency the processor can have (assuming the critical timing path is constrained by TLB and cache) (6 p)?

Chapter 5 — Large and Fast: Exploiting Memory Hierarchy — 27



$$\begin{aligned} \text{Offset: } & 2^4 \Rightarrow 16 \text{ byte} \\ \text{Index: } & \frac{16 \text{ KB}}{16 \text{ B}} = 1 \text{ K blocks} \quad \left. \begin{array}{l} 2-\text{way} \\ \end{array} \right\} \frac{1 \text{ K}}{2} = 512 = 2^9 \Rightarrow 9 \text{ bitar} \\ \text{Tag: } & 25 - 9 - 4 = 12 \text{ bitar} \\ & 1 + 1 + 12 + 128 = 142 \text{ bitar/block} \Rightarrow 142 \cdot 1024 = 145408 \text{ bitar} \end{aligned}$$



Page offset: 16 KB $\Rightarrow 2^{14}$ bits

Physical Page: $25 - 14 = 11$

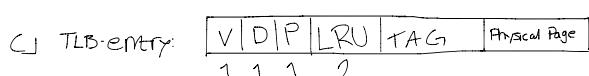
PTE = $1+1+1+2+11=16$ bitar

There's one PTE for each virtual page.

How many pages? $2^{32-14} \cdot 32 \cdot \text{VA}, 14: \text{Page offset} = 2^{18} = 256 \text{ K}$

$$256 \text{ K} \cdot 2 \text{ B} \cdot 16 = 8 \text{ MB}$$

#processes



Tag in TLB = Virtuell page number = 18

Physical Page = 11

Totalt: $1+1+1+2+18+11=34 \Rightarrow 32$ entries in TLB $34 = 1088$ bitar i TLB

d) Physically addressed cache: $VA \rightarrow \boxed{\text{TLB}} \xrightarrow{\text{FA}} \boxed{\$} \xrightarrow{1 \text{ ns}} \boxed{\text{Data}} \xrightarrow{7.5 \text{ ns}} \text{Instr/ Data}$ $f_{max} = \frac{1}{1+1.5} = 400 \text{ MHz}$

Pipelined: $VA \rightarrow \boxed{\text{TLB}} \rightarrow \boxed{_} \rightarrow \boxed{\$} \rightarrow \boxed{\text{Data}}$ $f_{max} = \frac{1}{1.5} = 667 \text{ MHz}$

Virtually addressed: $VA \rightarrow \boxed{\$} \rightarrow \boxed{\text{Data}}$ TLB is not in CP \Rightarrow TLB is only used if cache miss. $f_{max} = \frac{1}{1.5} = 667 \text{ MHz}$

Mipsaritmetik

Multiplikation: Två 32-bitars register för produkten

H1 (32 MSB)

LO (32 LSB)

Division: Använder HI/LO registeren för resultat

HI: Rest

LO: Kvot

Flyttal

Representation av icker-hälftal.

Binärt: $\pm 1.xxxxxx_2 \cdot 2^m$ ← Normaliserat

Det är
jämför...

Standardiserad enl IEEE

S	Exp	Fraction
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$$x = (-1)^s \cdot (1 + \text{Fraction}) \cdot 2^{(\text{Exponent} - \text{Bias})}$$

Exponent: Excess representation: aktuell exponent+Bias

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