15.6 A 20b Clockless DAC with Sub-ppm-Linearity 7.5nV/√Hz-Noise and 0.05ppm/°C-Stability

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DACs without continuous clocking are often favored in applications such as medical imaging and scientific instrumentation. The DACs in these high-precision systems are commonly endpoint-calibrated. After this calibration, a non-ideal DAC contributes three main sources of error: noise, temperature drift, and INL. The segmented voltage-mode R-2R DAC is an attractive architecture for reducing the first two of these error sources. Resistor Johnson noise is fixed by the DAC's code-independent output resistance, which is readily lowered by the combination of several parallel segments. The complete signal path can be built using opamps that have a minimal noise gain of unity. This architecture also benefits from inherently zero endpoint error, avoiding any gain or offset drift over temperature. However, this preferred architecture for noise and temperature drift suffers from several sources of INL including: resistor mismatch, voltage losses across CMOS switches, and the nonlinearity of each resistor.

This paper describes methods for overcoming these three sources of INL without compromising noise and drift, and provides silicon results from a ±10V implementation in 0.6µm BiCMOS.

Figure 15.6.1 shows the architecture. The main DAC core consists of a 20b thin-film resistor divider that interpolates between two endpoint voltages. The 6 MSBs control the thermometer-encoded switching of 63 equally weighted MSB segments. The 14 LSBs control the remaining 1/64th of the DAC range with a 14b binary-weighted R-2R network. Each parallel segment has a resistance of 220kΩ to give a DAC output resistance of 3.4kΩ. This resistance determines wideband thermal noise and settling time into capacitive loads.

The first source of INL is resistor mismatch. An error in the DAC output voltage from this mismatch is corrected by injecting a correction current from a calibration DAC into resistors in the main DAC [1]. This CALDAC injects a current within ±10µA into upper LSB resistors, which is more practical than injection of smaller currents into the MSBs or larger currents into the lower LSBs. The calibration current can be injected into a choice of three different nodes in order to allow greater trim range at the expense of coarser correction resolution. Both MSB and LSB resistors contribute INL. These contributions are independent. This means that at any particular DAC code, independent correction coefficients for the MSBs and LSBs can be digitally summed to provide an overall correction code. This code is sent to the CALDAC, which has 10b resolution and 9b accuracy. This CALDAC linearity requirement is a disadvantage compared to previous work [2], but allows efficient correction of MSB and LSB errors simultaneously. Mismatch nonlinearity in the main DAC within ±16 LSB at the 20b level can be corrected with a CALDAC step size of 1/32 LSB. The calibration is kept stable over a range of reference voltages by scaling the calibration current in proportion to the reference voltage. The correction ROM contains 64 MSB coefficients for the upper 6b. The inherent matching of the resistors allows LSB correction to be limited to the upper 5 LSBs. An additional 32 coefficients cover all combinations of these 5b. These 10b correction coefficients are programmed into a 1kb fuse ROM in each packaged part after measurement during factory test.

The next major source of INL in a typical voltage-mode R-2R DAC arises from voltage drops across MOS switches. Each resistor leg is switched to either the positive or negative reference voltage using PMOS or NMOS switches respectively. Any switch resistance mismatch between these different MOS types causes INL. The most practical approach to matching these CMOS resistances [3] leaves a residual error. This error can worsen when a higher-voltage process with less conductive switches is chosen to increase the DAC's voltage span.

This work eliminates the INL due to switch resistance by using force and sense switches around a pair of reference opamps [4]. Each single NMOS and PMOS switch in a conventional voltage-mode DAC architecture is replaced by a pair of force and sense switches that are switched in tandem. This method is exemplified in Fig. 15.6.2, which shows a segmented 2b DAC at midcode. The two upper PMOS sense switches with resistance Rps ensure that the average voltage on nodes N0 and N1 is correct even if force switches Rpf mismatch. If instead switches Rpf have no mismatch, then there is no voltage across switches Rps, allowing these Rps switches to have arbitrary mismatch. This segmented circuit eliminates 1st-order dependence of VOUT on any switch resistance.

To realise a practical 20b DAC, a binary-weighted sub-ranging circuit becomes necessary, as shown in Fig. 15.6.3. The sense switches are scaled in a binary manner. Each resistor leg may be forced to a slightly incorrect voltage, but a binary-weighted sense feedback network ensures that a weighted average of these voltages is correct, ensuring that the overall DAC output voltage is also correct. Using binary-scaled sense switches over a large range of bits increases DAC INL due to the inherent nonlinearity of CMOS switches. To mitigate this, the 20b span is divided into three ranges of 9 upper bits, 5 mid-range bits and 6 lower bits. With 6 MSBs of segmentation, the ratio of maximum to minimum switch resistance in the upper 9b range is 8:1, increasing to 16:1, and then to 32:1 in the lowest range.

An input offset voltage in the two opamps for the upper range does not cause INL but does shift the DAC endpoint voltages. External precision opamps are preferred to minimise this error. Linearity is sensitive to the input bias current of all opamps shown in Fig. 15.6.3. Opamps with bipolar input transistors and base-current cancellation provide acceptable low-frequency noise and low input bias current.

The third source of INL considered here arises from the nonlinearity of each resistor. The dominant nonlinear mechanism in these resistors arises from their non-zero temperature coefficient and the thermal resistance from the conductive film to thermal ground. The geometry of the resistor causes most heat conduction to be vertical and the nonlinearity to depend on the ratio of power to area. This power density is smaller for large resistors: each 220kΩ segment resistor is 1000µm/4.7µm. We model these nonlinear resistors using: $R(V) = R_0(1+kV^2)$. The value k is calculated from the thermal resistance per unit area through the silicon oxide to the substrate (θ_A), the resistor's 1st-order temperature coefficient (T_{CR}), its sheet resistivity (ρ), and its length (L) by: $k = \theta_A T_{CR}/\rho L^2$.

Assuming an entirely segmented DAC, an analytical calculation of the DAC nonlinearity that results from these nonlinear resistors takes the form $INL = \kappa(-D+3D^2-2D^3)$, where D is the DAC code as a fraction of full scale. This nonlinearity has a consistent shape but a magnitude with a square-law dependence on reference voltage, as shown in Fig. 15.6.4. An additional 'S' ROM within Fig. 15.6.1 corrects for this resistor self-heating nonlinearity as a function of DAC code and a digital representation of the reference voltage. Measurements of silicon confirm this improves INL by 0.35ppm.

Measured linearity of 0.3 LSB after calibration is shown in Fig. 15.6.5. This is a fourfold improvement over previous work. A performance summary is shown in Fig. 15.6.6 and a photo of the 3465×2465µm^2 die is shown in Fig. 15.6.7.

References:

[1] R. McLachlan and S. Blackburn, "Voltage Mode DAC with Calibration Circuit using Current Mode DAC and ROM Lookup," U.S. Patent 8089380, Jan. 3, 2012.
[2] G. A. Miller, M. C. W. Coln, L. A. Singer, and P. R. Oaklander, "A True 16b Self-Calibrating BiCMOS DAC", *ISSCC Dig. Tech. Papers*, pp. 58-59, 263, Feb. 1993.
[3] R. A. Meaney and R. J. Speer, "Voltage-Switching D/A Converter using P- and N-Channel MOSFETS," U.S. Patent 5075677, Dec. 24, 1991.
[4] R. McLachlan, "Digital to Analog Converters having Circuit Architectures to overcome Switch Losses," U.S. patent 7884747, Feb. 8, 2011.

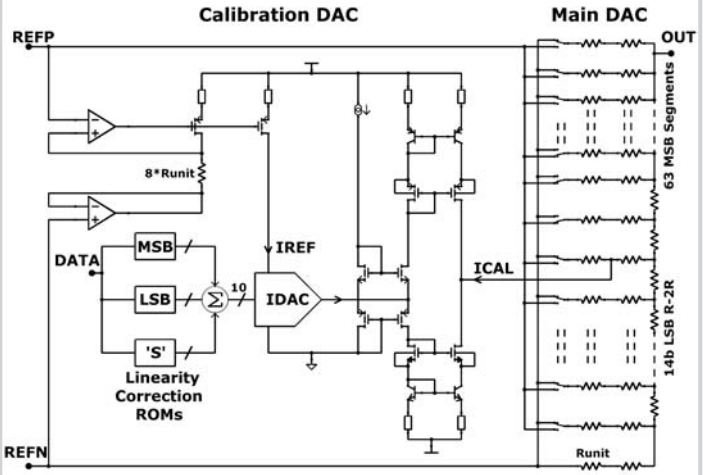

Figure 15.6.1: The 20b DAC architecture.

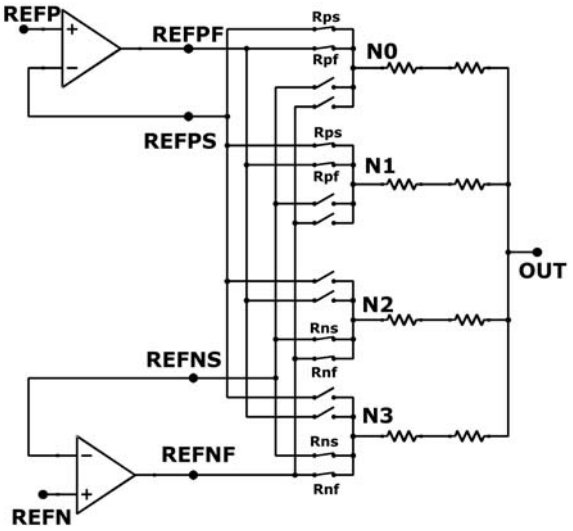

Figure 15.6.2: Force and sense technique applied to a 2b DAC.

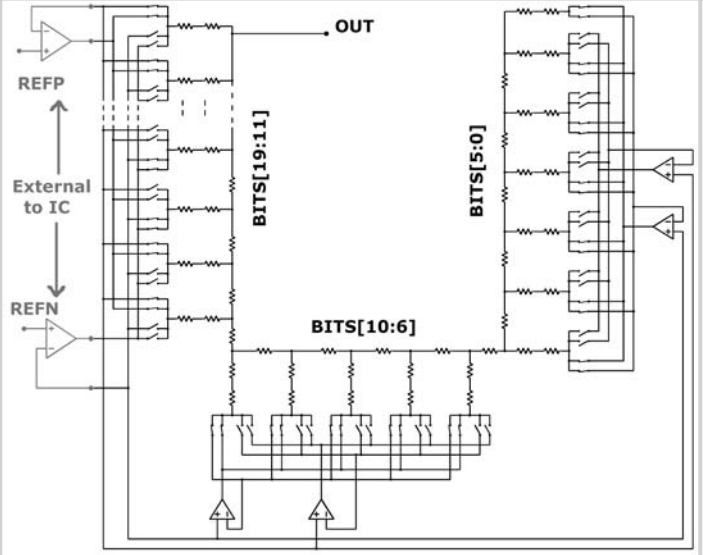

Figure 15.6.3: Complete 20b DAC with force and sense switches.

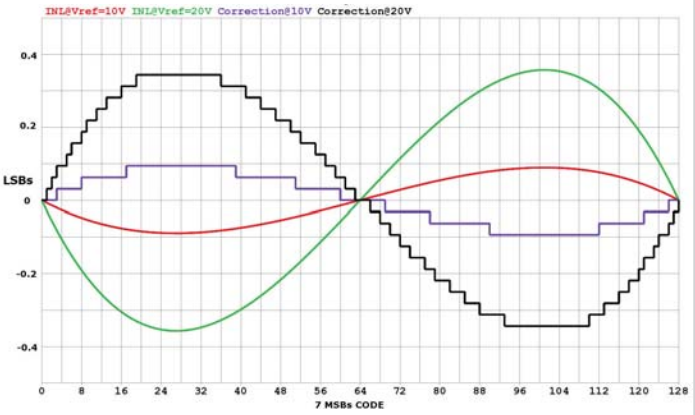

Figure 15.6.4: Nonlinearity from resistor self-heating and digital correction.

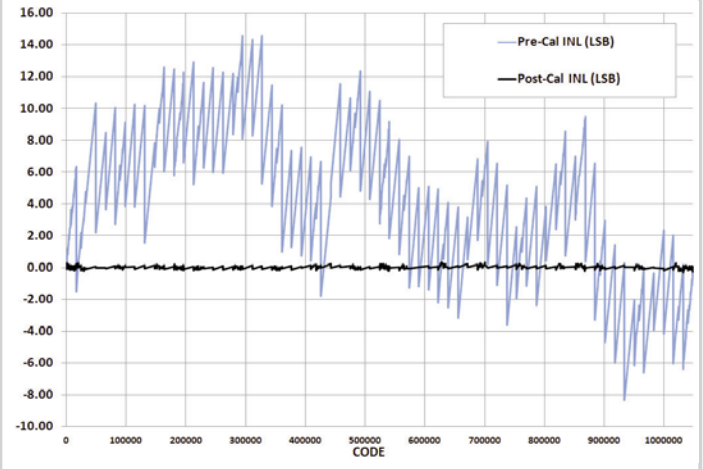

Figure 15.6.5: Pre and post-calibration INL at the 20b level.

Resolution	20 bits
Output Range	± 10V
INL	0.35 LSB
DNL	0.30 LSB
Output resistance	3.4 kΩ
Output noise > 10Hz	7.5 nV/√Hz
Output noise at 1Hz	14 nV/√Hz
Noise 0.1 - 10 Hz	1.1 μV_{pp}
Temperature Stability	0.05 ppm/°C
DC PSRR	0.03 ppm/V
Settling Time	1 µs
Technology	0.6 µm BiCMOS
Total Die Area	3465 µm x 2465 µm
Current	4.2 mA

Figure 15.6.6: Performance summary.

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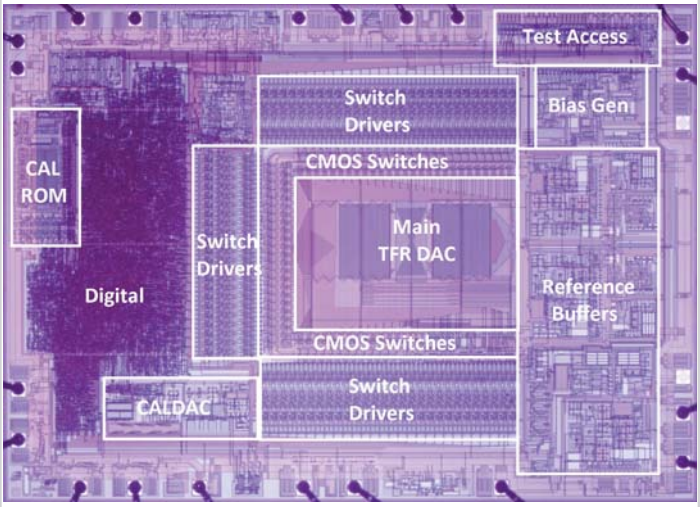

Figure 15.6.7: Die photograph. The complete die is 3465 x 2465µm

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