Homework Assignment #3

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WESTERN MICHIGAN UNIVERSITY
ECE 5510 APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN
Homework Assignment #3

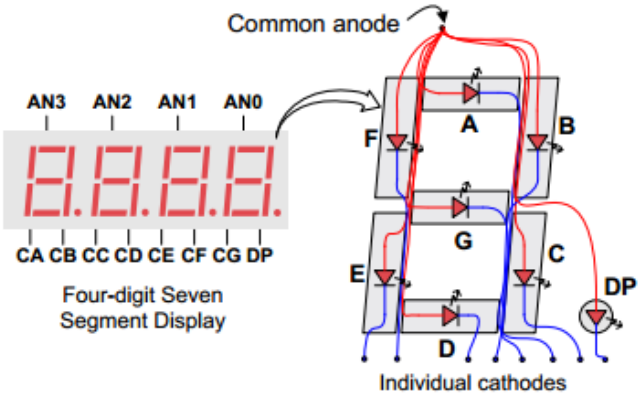
Task 1:

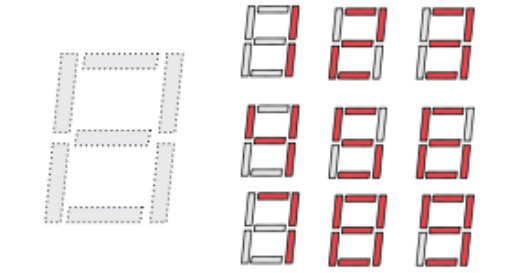
Develop a behavioral VHDL program for a **synchronous (clocked) 2-digit, modulo-32 binary-coded-decimal (BCD) up counter.** The counter should **count from 0 up to 31** and then continue from 0 again. The counter should have an **active high CLR** signal to reset its contents to 0 at any time. The counter's state should be displayed on the **7-segment display module** of the Nexys 3 Board. Both the CLK and the CLR signals should be mapped to pushbuttons, respectively. You should pick a push button for the CLK signal that is connected to a **GCLK pin** of your FPGA. You should implement this counter using the FPGA, the 7-segment display and push-buttons on your Nexys 3 Board. Note: you should use the 100MHz clock available on the Nexys 3 Board for creating the required signal timings for the 7-Segment Display module. Introduce a **suitable delay** to make the CLK signal **bounce free, if needed**.

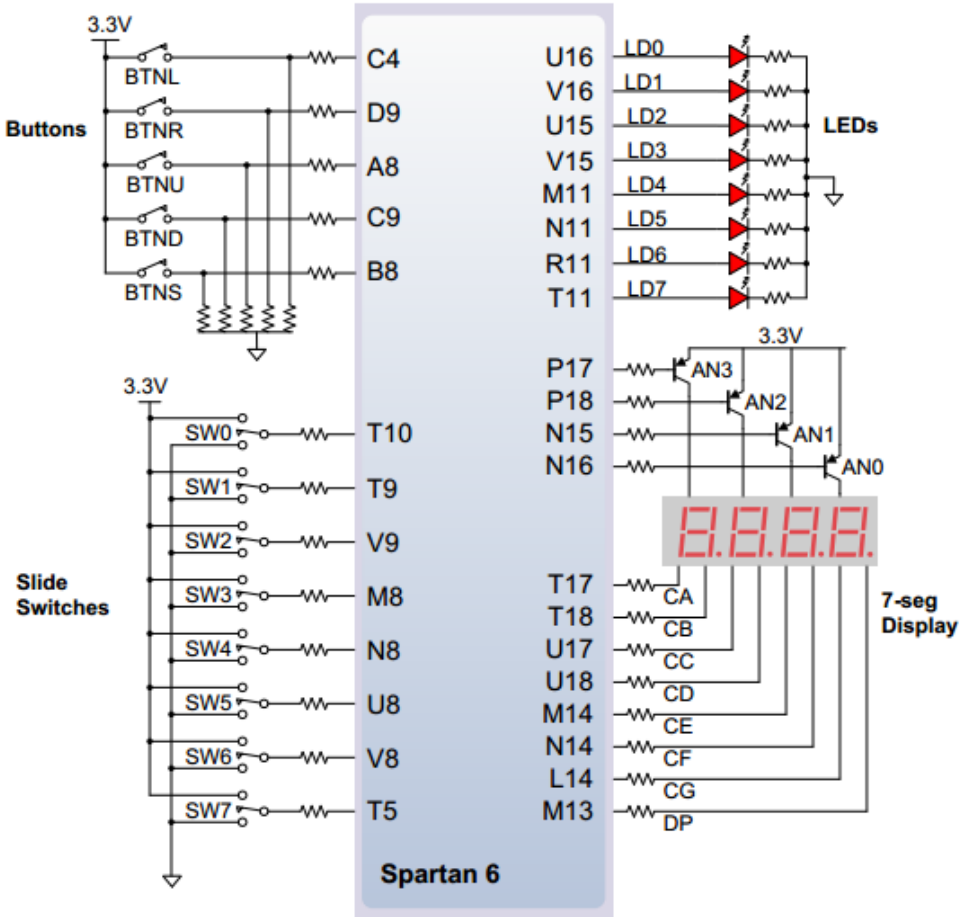
Task

The task of “synchronous (clocked) 2-digit, modulo-32, binary-coded-decimal (BCD) up counter” is a counter 0-31 that shows in the display of 7-segment LEDS. The Nexys3 board contains four-digit; however, for this activity will be utilized only 2 display.

Check above the connection of seven-segment:


Common anode
AN3 AN2 AN1 AN0
CA CB CC CD CE CF CG DP
Four-digit Seven Segment Display
A
B
C
D
E
F
G
DP
Individual cathodes


An un-illuminated seven-segment display, and nine illumination patterns corresponding to decimal digits


3.3V
BTNL
BTNR
BTNU
BTND
BTNS
Buttons
C4
D9
A8
C9
B8
U16
V16
U15
V15
M11
N11
R11
T11
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LEDs
3.3V
SW0
SW1
SW2
SW3
SW4
SW5
SW6
SW7
Slide Switches
T10
T9
V9
M8
N8
U8
V8
T5
P17
P18
N15
N16
AN3
AN2
AN1
AN0
T17
T18
U17
U18
M14
N14
L14
M13
CA
CB
CC
CD
CE
CF
CG
DP
7-seg Display
Spartan 6

An un-illuminated seven-segment display, and 10 patterns corresponding to decimal digits

Numeric Number	CA CB CC CD CE CF CG DP
0	00000011
1	10011111
2	00100101
3	00001101
4	10011001
5	01001001
6	01000001
7	00011111
8	00000001
9	00001001

Simulation: macro.do

```
restart

# For simulation I dived in two projects because there is a issue about the low frequency

force CLK 0 0, 1 10ns -r 20ns
force CLR 0

# Test the CLR
run 155ns
force CLR 1
run 155ns
force CLR 0

# Count the numbers
run 3000ns
```

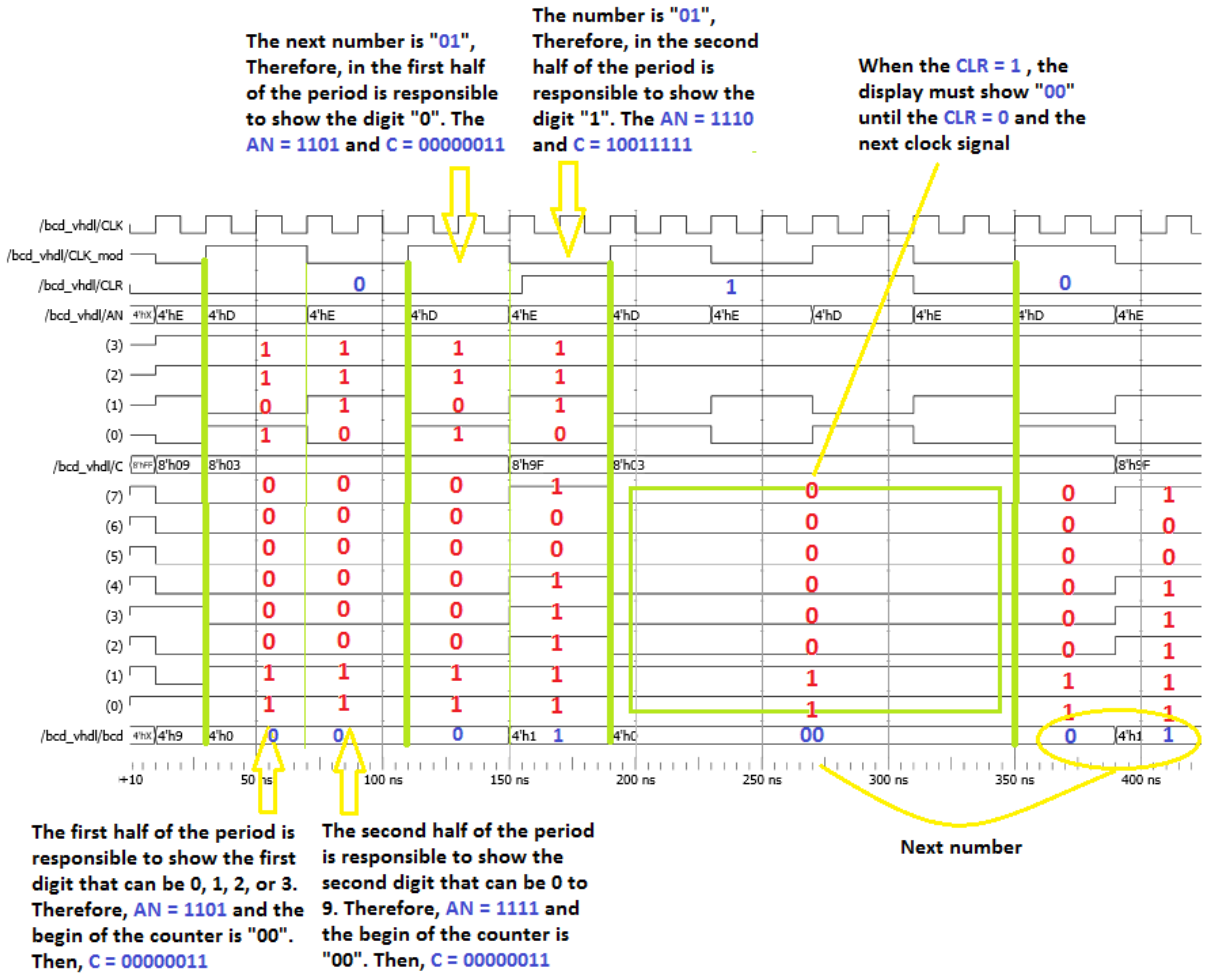
File .ucf

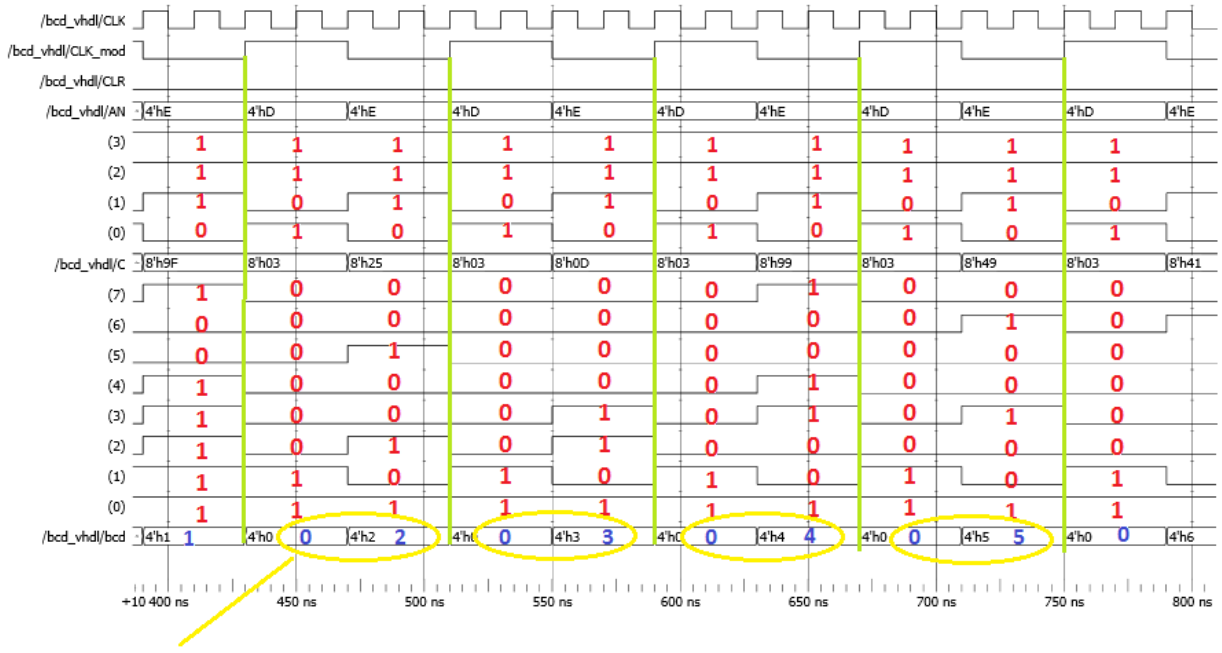
```
# PlanAhead Generated physical constraints

NET "AN[3]" LOC = P17;

# PlanAhead Generated IO constraints

NET "AN[3]" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "AN[0]" LOC = N16;
NET "AN[1]" LOC = N15;
NET "AN[2]" LOC = P18;

# PlanAhead Generated IO constraints

NET "AN[2]" IOSTANDARD = LVCMOS33;
NET "AN[1]" IOSTANDARD = LVCMOS33;
NET "AN[0]" IOSTANDARD = LVCMOS33;
NET "C[7]" IOSTANDARD = LVCMOS33;
NET "C[6]" IOSTANDARD = LVCMOS33;
NET "C[5]" IOSTANDARD = LVCMOS33;
NET "C[4]" IOSTANDARD = LVCMOS33;
NET "C[3]" IOSTANDARD = LVCMOS33;
NET "C[2]" IOSTANDARD = LVCMOS33;
NET "C[1]" IOSTANDARD = LVCMOS33;
NET "C[0]" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "C[7]" LOC = T17;
NET "C[6]" LOC = T18;
NET "C[5]" LOC = U17;
NET "C[4]" LOC = U18;
NET "C[3]" LOC = M14;
NET "C[2]" LOC = N14;
NET "C[1]" LOC = L14;
NET "C[0]" LOC = M13;
```

```
NET "CLR" LOC = C4;

# PlanAhead Generated IO constraints

NET "CLR" IOSTANDARD = LVCMOS33;
NET "CLK" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "CLK" LOC = V10;
```

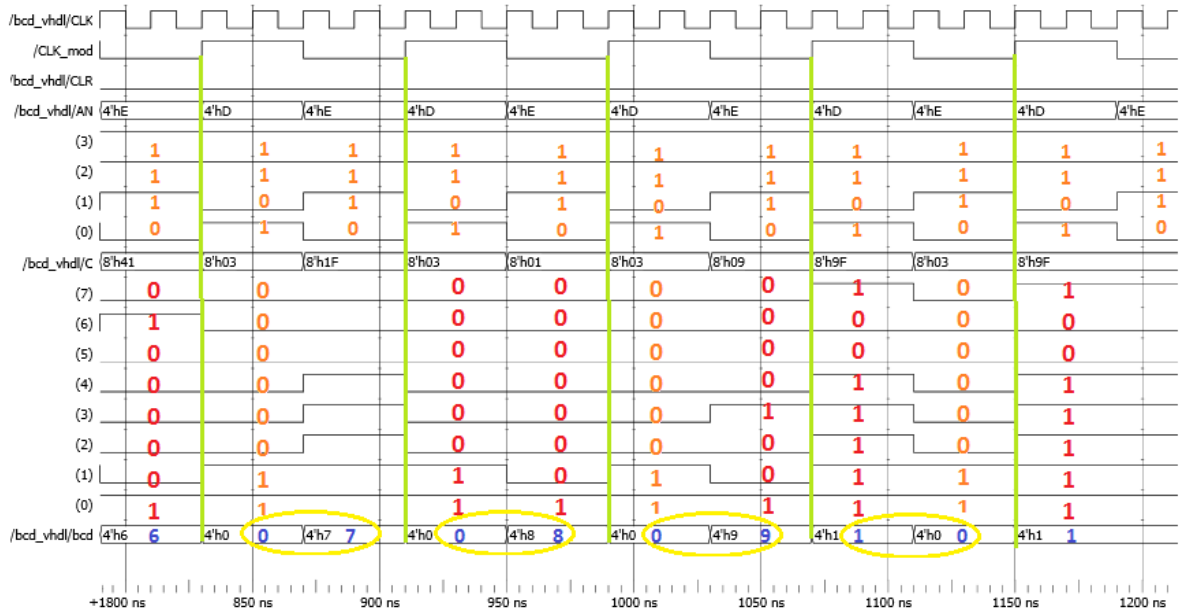
Wave

The simulation has adapt for the simulation because the frequency is too low.

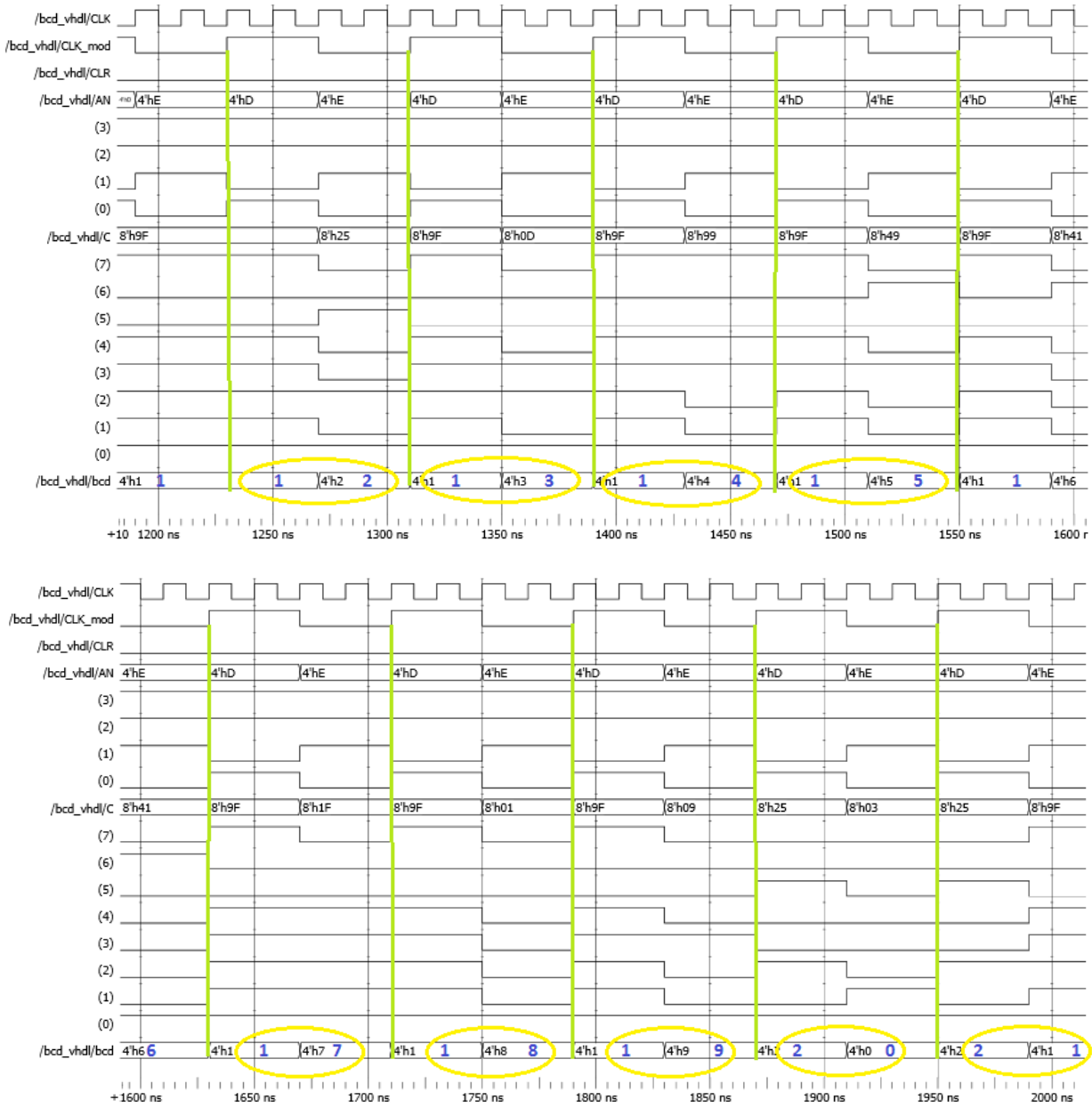


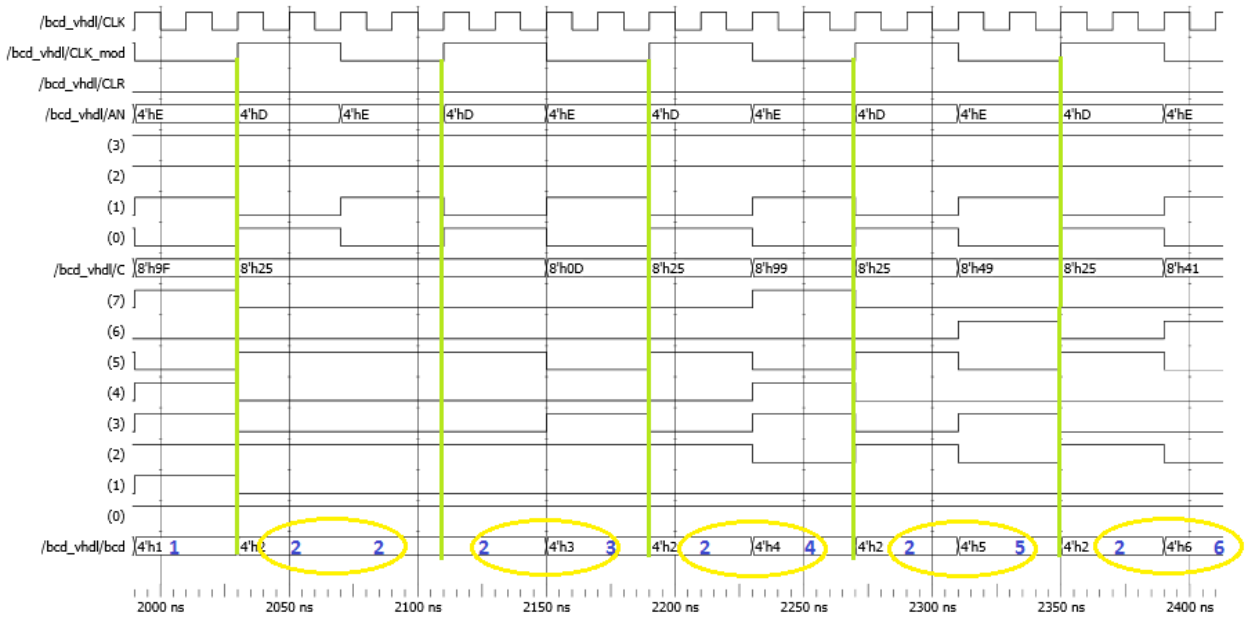


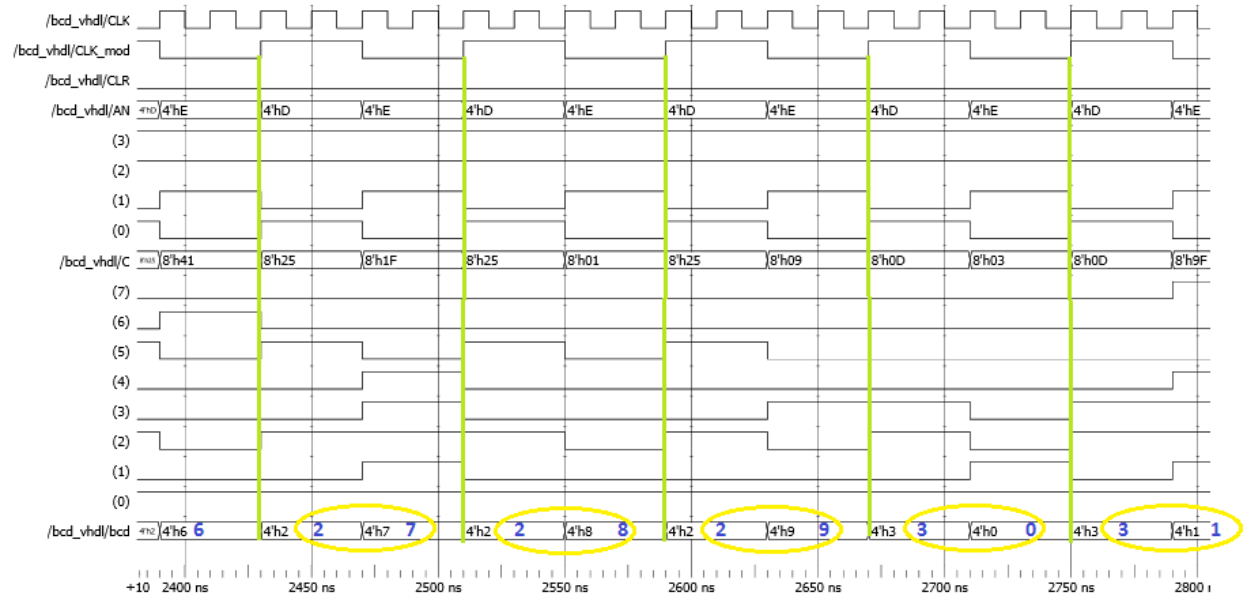
Counter working

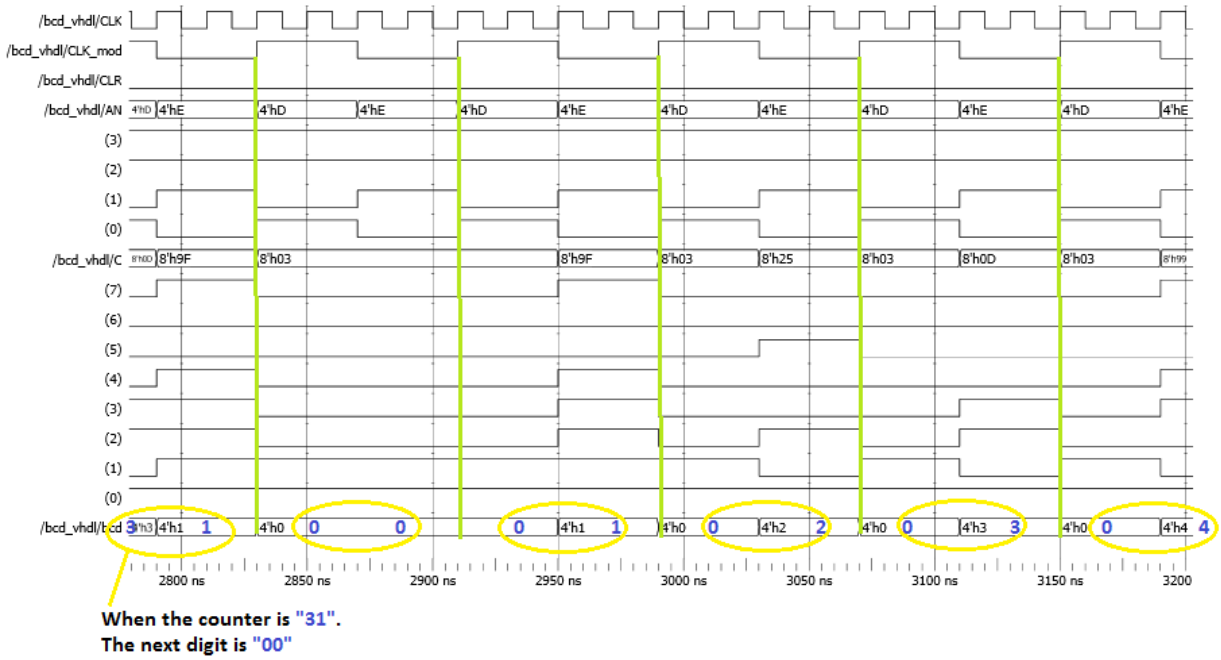


The counter keep going working normally




/bcd_vhdl/CLK
/bcd_vhdl/CLK_mod
/bcd_vhdl/CLR
/bcd_vhdl/AN
/bcd_vhdl/C
/bcd_vhdl/bcd
2000 ns
2050 ns
2100 ns
2150 ns
2200 ns
2250 ns
2300 ns
2350 ns
2400 ns


/bcd_vhdl/CLK
/bcd_vhdl/CLK_mod
/bcd_vhdl/CLR
/bcd_vhdl/AN
/bcd_vhdl/C
/bcd_vhdl/bcd
+10 2400 ns
2450 ns
2500 ns
2550 ns
2600 ns
2650 ns
2700 ns
2750 ns
2800


/bcd_vhdl/CLK
/bcd_vhdl/CLK_mod
/bcd_vhdl/CLR
/bcd_vhdl/AN
(3)
(2)
(1)
(0)
/bcd_vhdl/C
(7)
(6)
(5)
(4)
(3)
(2)
(1)
(0)
/bcd_vhdl/bcd
4'hE
4'hD
8'h9F
8'h03
8'h25
8'h0D
8'h99
4'h1
4'h0
4'h2
4'h3
4'h4
2800 ns
2850 ns
2900 ns
2950 ns
3000 ns
3050 ns
3100 ns
3150 ns
3200
When the counter is "31".
The next digit is "00"

BCD_vhdl.vhd

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;  -- include functions to perform logical
3   use IEEE.NUMERIC_STD.ALL;     -- arithmetic functions with Signed or Unsigned
    values
4
5   entity BCD_vhdl is
6       Port ( CLK : in  STD_LOGIC;                          -- Clock signal
7              CLR : in  STD_LOGIC;                          -- Clear
8              AN  : out  STD_LOGIC_VECTOR (3 downto 0);  --
9              C   : out  STD_LOGIC_VECTOR (7 downto 0));
10  end BCD_vhdl;
11
12  architecture Behavioral of BCD_vhdl is
13     signal dozen: UNSIGNED (3 downto 0) := "0000";
14     signal unit : UNSIGNED (3 downto 0) := "1001";
15     signal bcd : UNSIGNED(3 downto 0);
16     signal counter,divide : integer := 0;
17     signal CLK_mod : std_logic;
18     signal mux : std_logic;
19
20     signal bcd_LastUnit  : UNSIGNED(3 downto 0);
21     signal bcd_LastDozen : UNSIGNED(3 downto 0);
22
23  begin
24
25  count_process: process(unit, dozen, CLR, CLK_mod)
26  begin
27     if (CLK_mod'event and CLK_mod = '1') then
28        if (CLR = '0') then
29           if ((unit = "0000" and dozen = "0011") or CLR = '1') then
30              dozen <= "0000";
31              unit <= "0001";
32           else
33              if (unit = "1001") then
34                 unit  <= "0000";
35              else
36                 unit  <= unit + 1;
37              end if;
38
39              if (unit = "1000") then
40                 dozen <= dozen + 1;
41              end if;
42           end if;
43        else
44           unit  <= "0000";
45           dozen <= "0000";
46        end if;
47        if (bcd_LastUnit = "0001" and bcd_LastDozen = "0011") then
48           unit <= "0000";
49           dozen <= "0000";
50        end if;
51     end if;
52
53     if (CLK_mod'event and CLK_mod = '1') then
54        AN <= "1101";
```

BCD_vhdl.vhd

```
55          bcd <= dozen;
56          bcd_LastDozen <= dozen;
57       elsif (CLK_mod'event and CLK_mod = '0') then
58          AN <= "1110";
59          bcd <= unit;
60          bcd_LastUnit  <= unit;
61       end if;
62
63    end process count_process;
64
65    segment_process: process(bcd)
66    begin
67       case  bcd is
68       when "0000"=> C <="00000011";  -- '0'
69       when "0001"=> C <="10011111";  -- '1'
70       when "0010"=> C <="00100101";  -- '2'
71       when "0011"=> C <="00001101";  -- '3'
72       when "0100"=> C <="10011001";  -- '4'
73       when "0101"=> C <="01001001";  -- '5'
74       when "0110"=> C <="01000001";  -- '6'
75       when "0111"=> C <="00011111";  -- '7'
76       when "1000"=> C <="00000001";  -- '8'
77       when "1001"=> C <="00001001";  -- '9'
78       --nothing is displayed when a number more than 9 is given as input.
79       when others=> C <="11111111";
80       end case;
81    end process segment_process;
82
83    clk_process: process(CLK)
84    begin
85       divide <= 100000;       -- Convert a 100Mhz signal into a 1Khz
86       if( rising_edge(CLK) ) then
87          if(counter < divide/2-1) then
88             counter <= counter + 1;
89             CLK_mod <= '0';
90          elsif(counter < divide-1) then
91             counter <= counter + 1;
92             CLK_mod <= '1';
93          else
94             CLK_mod <= '0';
95             counter <= 0;
96          end if;
97       end if;
98    end process clk_process;
99
100   end Behavioral;
101
102
```

Pinout Report - Wed May 28 14:36:02 2014

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank Number	Drive (mA)	Slew Rate	Termination	IOB Delay	Voltage	Constraint	IO Register	Signal Integrity
A1			GND											
A2		IOBS	IO_L2N_0	UNUSED		0								
A3		IOBS	IO_L4N_0	UNUSED		0								
A4		IOBS	IO_L5N_0	UNUSED		0								
A5		IOBS	IO_L6N_0	UNUSED		0								
A6		IOBS	IO_L8N_VREF_0	UNUSED		0								
A7		IOBS	IO_L10N_0	UNUSED		0								
A8		IOBS	IO_L33N_0	UNUSED		0								
A9		IOBS	IO_L35N_GCLK16_0	UNUSED		0								
A10		IOBS	IO_L37N_GCLK12_0	UNUSED		0								
A11		IOBS	IO_L39N_0	UNUSED		0								
A12		IOBS	IO_L41N_0	UNUSED		0								
A13		IOBS	IO_L50N_0	UNUSED		0								
A14		IOBS	IO_L62N_VREF_0	UNUSED		0								
A15		IOBS	IO_L64N_SCP4_0	UNUSED		0								
A16		IOBS	IO_L66N_SCP0_0	UNUSED		0								
A17			TCK											
A18			GND											
B1			VCCAUX								2.5			
B2		IOBM	IO_L2P_0	UNUSED		0								
B3		IOBM	IO_L4P_0	UNUSED		0								
B4		IOBM	IO_L5P_0	UNUSED		0								
B5			VCCO_0			0					any*****			
B6		IOBM	IO_L8P_0	UNUSED		0								
B7			GND											
B8		IOBM	IO_L33	UNUSE		0								

			P_0	D									
B9		IOBM	IO_L35P_GCLK17_0	UNUSED		0							
B10			VCCO_0			0					any*****		
B11		IOBM	IO_L39P_0	UNUSED		0							
B12		IOBM	IO_L41P_0	UNUSED		0							
B13			GND										
B14		IOBM	IO_L62P_0	UNUSED		0							
B15			VCCO_0			0					any*****		
B16		IOBM	IO_L66P_SCP1_0	UNUSED		0							
B17			VCCAUX								2.5		
B18			TMS										
C1		IOBS	IO_L83N_VREF_3	UNUSED		3							
C2		IOBM	IO_L83P_3	UNUSED		3							
C3			GND										
C4	CLR	IOB	IO_L1N_VREF_0	INPUT	LVCMOS33	0				NONE		LOCATED	NO	NONE
C5		IOBM	IO_L6P_0	UNUSED		0							
C6		IOBS	IO_L3N_0	UNUSED		0							
C7		IOBM	IO_L10P_0	UNUSED		0							
C8		IOBS	IO_L11N_0	UNUSED		0							
C9		IOBS	IO_L34N_GCLK18_0	UNUSED		0							
C10		IOBM	IO_L37P_GCLK13_0	UNUSED		0							
C11		IOBS	IO_L36N_GCLK14_0	UNUSED		0							
C12		IOBS	IO_L47N_0	UNUSED		0							
C13		IOBM	IO_L50P_0	UNUSED		0							
C14		IOBS	IO_L65N_SCP2_0	UNUSED		0							
C15		IOBM	IO_L64P_SCP5_0	UNUSED		0							
C16			GND										
C17		IOBM	IO_L29P_A23_M1A13_	UNUSED		1							

			1										
C18		IOBS	IO_L29N_A22_M1A14_1	UNUSED		1							
D1		IOBS	IO_L52N_M3A9_3	UNUSED		3							
D2		IOBM	IO_L52P_M3A8_3	UNUSED		3							
D3		IOBS	IO_L54N_M3A11_3	UNUSED		3							
D4		IOBM	IO_L1P_HSWAPEN_0	UNUSED		0							
D5			GND										
D6		IOBM	IO_L3P_0	UNUSED		0							
D7			VCCO_0			0					any*****		
D8		IOBM	IO_L11P_0	UNUSED		0							
D9		IOBM	IO_L34P_GCLK19_0	UNUSED		0							
D10			GND										
D11		IOBM	IO_L36P_GCLK15_0	UNUSED		0							
D12		IOBM	IO_L47P_0	UNUSED		0							
D13			VCCO_0			0					any*****		
D14		IOBM	IO_L65P_SCP3_0	UNUSED		0							
D15			TDI										
D16			TDO										
D17		IOBM	IO_L31P_A19_M1CKE_1	UNUSED		1							
D18		IOBS	IO_L31N_A18_M1A12_1	UNUSED		1							
E1		IOBS	IO_L50N_M3BA2_3	UNUSED		3							
E2			VCCO_3			3					any*****		
E3		IOBM	IO_L50P_M3WE_3	UNUSED		3							
E4		IOBM	IO_L54P_M3RESET_3	UNUSED		3							
E5			VCCAUX								2.5		

E6		IOBS	IO_L7N_0	UNUSED		0							
E7		IOBM	IO_L9P_0	UNUSED		0							
E8		IOBS	IO_L9N_0	UNUSED		0							
E9			VCCAUX							2.5			
E10			VCCO_0			0				any*****			
E11		IOBS	IO_L42N_0	UNUSED		0							
E12		IOBS	IO_L51N_0	UNUSED		0							
E13		IOBS	IO_L63N_SCP6_0	UNUSED		0							
E14			VCCAUX							2.5			
E15			GND										
E16		IOBM	IO_L33P_A15_M1A10_1	UNUSED		1							
E17			VCCO_1			1				3.30			
E18		IOBS	IO_L33N_A14_M1A4_1	UNUSED		1							
F1		IOBS	IO_L48N_M3BA1_3	UNUSED		3							
F2		IOBM	IO_L48P_M3BA0_3	UNUSED		3							
F3		IOBS	IO_L51N_M3A4_3	UNUSED		3							
F4		IOBM	IO_L51P_M3A10_3	UNUSED		3							
F5		IOBS	IO_L55N_M3A14_3	UNUSED		3							
F6		IOBM	IO_L55P_M3A13_3	UNUSED		3							
F7		IOBM	IO_L7P_0	UNUSED		0							
F8		IOBS	IO_L32N_0	UNUSED		0							
F9		IOBS	IO_L38N_VREF_0	UNUSED		0							
F10		IOBS	IO_L40N_0	UNUSED		0							
F11		IOBM	IO_L42P_0	UNUSED		0							
F12		IOBM	IO_L51P_0	UNUSED		0							
F13		IOBM	IO_L63P_SCP7_0	UNUSED		0							

F14		IOBM	IO_L30P_A21_M1RESET_1	UNUSED		1							
F15		IOBM	IO_L1P_A25_1	UNUSED		1							
F16		IOBS	IO_L1N_A24_VREF_1	UNUSED		1							
F17		IOBM	IO_L35P_A11_M1A7_1	UNUSED		1							
F18		IOBS	IO_L35N_A10_M1A2_1	UNUSED		1							
G1		IOBS	IO_L46N_M3CLKN_3	UNUSED		3							
G2			GND										
G3		IOBM	IO_L46P_M3CLK_3	UNUSED		3							
G4			VCCO_3			3					any*****		
G5			GND										
G6		IOBS	IO_L53N_M3A12_3	UNUSED		3							
G7			VCCINT								1.2		
G8		IOBM	IO_L32P_0	UNUSED		0							
G9		IOBM	IO_L38P_0	UNUSED		0							
G10			VCCAUX								2.5		
G11		IOBM	IO_L40P_0	UNUSED		0							
G12			GND										
G13		IOBS	IO_L32N_A16_M1A9_1	UNUSED		1							
G14		IOBS	IO_L30N_A20_M1A11_1	UNUSED		1							
G15			VCCO_1			1					3.30		
G16		IOBM	IO_L38P_A5_M1CLK_1	UNUSED		1							
G17			GND										
G18		IOBS	IO_L38N_A4_M1CLKN_1	UNUSED		1							
H1		IOBS	IO_L41N_GCLK26_M3DQ5_3	UNUSED		3							
H2		IOBM	IO_L41P_GCLK27_M3D	UNUSED		3							

			Q4_3										
H3		IOBS	IO_L44N_GCLK20_M3A6_3	UNUSED		3							
H4		IOBM	IO_L44P_GCLK21_M3A5_3	UNUSED		3							
H5		IOBS	IO_L49N_M3A2_3	UNUSED		3							
H6		IOBM	IO_L49P_M3A7_3	UNUSED		3							
H7		IOBM	IO_L53P_M3CKE_3	UNUSED		3							
H8			GND										
H9			VCCINT								1.2		
H10			GND										
H11			VCCINT								1.2		
H12		IOBM	IO_L32P_A17_M1A8_1	UNUSED		1							
H13		IOBM	IO_L36P_A9_M1BA0_1	UNUSED		1							
H14		IOBS	IO_L36N_A8_M1BA1_1	UNUSED		1							
H15		IOBM	IO_L37P_A7_M1A0_1	UNUSED		1							
H16		IOBS	IO_L37N_A6_M1A1_1	UNUSED		1							
H17		IOBM	IO_L43P_GCLK5_M1DQ4_1	UNUSED		1							
H18		IOBS	IO_L43N_GCLK4_M1DQ5_1	UNUSED		1							
J1		IOBS	IO_L40N_M3DQ7_3	UNUSED		3							
J2			VCCO_3			3					any*****		
J3		IOBM	IO_L40P_M3DQ6_3	UNUSED		3							
J4			GND										
J5			VCCO_3			3					any*****		
J6		IOBS	IO_L47N_M3A1_3	UNUSED		3							
J7		IOBM	IO_L47P_M3A0	UNUSED		3							

			_3											
J8			VCCINT								1.2			
J9			GND											
J10			VCCINT								1.2			
J11			GND											
J12			VCCAUX								2.5			
J13		IOBM	IO_L39P_M1A3_1	UNUSED		1								
J14			VCCO_1			1					3.30			
J15			GND											
J16		IOBM	IO_L44P_A3_M1DQ6_1	UNUSED		1								
J17			VCCO_1			1					3.30			
J18		IOBS	IO_L44N_A2_M1DQ7_1	UNUSED		1								
K1		IOBS	IO_L38N_M3DQ3_3	UNUSED		3								
K2		IOBM	IO_L38P_M3DQ2_3	UNUSED		3								
K3		IOBS	IO_L42N_GCLK24_M3LDM_3	UNUSED		3								
K4		IOBM	IO_L42P_GCLK25_TRDY2_M3UDM_3	UNUSED		3								
K5		IOBS	IO_L43N_GCLK22_IRDY2_M3CASN_3	UNUSED		3								
K6		IOBS	IO_L45N_M3ODT_3	UNUSED		3								
K7			VCCAUX								2.5			
K8			GND											
K9			VCCINT								1.2			
K10			GND											
K11			VCCINT								1.2			
K12		IOBM	IO_L34P_A13_M1WE_1	UNUSED		1								
K13		IOBS	IO_L34N_A12_M1BA2_1	UNUSED		1								
K14		IOBS	IO_L39N_M1ODT_1	UNUSED		1								
K15		IOBM	IO_L41P_GCLK9_IRDY	UNUSED		1								

			1_M1RASN_1										
K16		IOBS	IO_L41N_GCLK8_M1CASN_1	UNUSED		1							
K17		IOBM	IO_L45P_A1_M1LDQS_1	UNUSED		1							
K18		IOBS	IO_L45N_A0_M1LDQSN_1	UNUSED		1							
L1		IOBS	IO_L37N_M3DQ1_3	UNUSED		3							
L2		IOBM	IO_L37P_M3DQ0_3	UNUSED		3							
L3		IOBS	IO_L39N_M3LDQSN_3	UNUSED		3							
L4		IOBM	IO_L39P_M3LDQS_3	UNUSED		3							
L5		IOBM	IO_L43P_GCLK23_M3RASN_3	UNUSED		3							
L6		IOBM	IO_L31P_3	UNUSED		3							
L7		IOBM	IO_L45P_M3A3_3	UNUSED		3							
L8			VCCINT								1.2			
L9			GND											
L10			VCCINT								1.2			
L11			GND											
L12		IOBM	IO_L40P_GCLK11_M1A5_1	UNUSED		1							
L13		IOBS	IO_L40N_GCLK10_M1A6_1	UNUSED		1							
L14	C<1>	IOB	IO_L61P_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
L15		IOBM	IO_L42P_GCLK7_M1UDM_1	UNUSED		1							
L16		IOBS	IO_L42N_GCLK6_TRDY1_M1LDM_1	UNUSED		1							
L17		IOBM	IO_L46P_FCS_B_M1D	UNUSED		1							

			Q2_1											
L18		IOBS	IO_L46N_FOE_B_M1DQ3_1	UNUSED		1								
M1		IOBS	IO_L36N_M3DQ9_3	UNUSED		3								
M2			GND											
M3		IOBM	IO_L36P_M3DQ8_3	UNUSED		3								
M4			VCCO_3			3					any***			
M5		IOBS	IO_L31N_VREF_3	UNUSED		3								
M6			GND											
M7			VCCINT								1.2			
M8		IOBM	IO_L40P_2	UNUSED		2								
M9			VCCAUX								2.5			
M10		IOBM	IO_L22P_2	UNUSED		2								
M11		IOBM	IO_L15P_2	UNUSED		2								
M12			VCCINT								1.2			
M13	C<0>	IOB	IO_L61N_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
M14	C<3>	IOB	IO_L53P_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
M15			VCCO_1			1					3.30			
M16		IOBM	IO_L47P_FWE_B_M1DQ0_1	UNUSED		1								
M17			GND											
M18		IOBS	IO_L47N_LDC_M1DQ1_1	UNUSED		1								
N1		IOBS	IO_L35N_M3DQ11_3	UNUSED		3								
N2		IOBM	IO_L35P_M3DQ10_3	UNUSED		3								
N3		IOBS	IO_L1N_VREF_3	UNUSED		3								
N4		IOBM	IO_L1P_3	UNUSED		3								
N5		IOBM	IO_L64P_D8_2	UNUSED		2								
N6		IOBM	IO_L47P_2	UNUSED		2								
N7		IOBM	IO_L44P_2	UNUSED		2								
N8		IOBS	IO_L40N_2	UNUSED		2								

N9		IOBS	IO_L22N_2	UNUSED		2								
N10		IOBM	IO_L20P_2	UNUSED		2								
N11		IOBS	IO_L15N_2	UNUSED		2								
N12		IOBM	IO_L13P_M1_2	UNUSED		2								
N13			GND											
N14	C<2>	IOB	IO_L53N_VREF_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
N15	AN<1>	IOB	IO_L50P_M1UDQS_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
N16	AN<0>	IOB	IO_L50N_M1UDQSN_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
N17		IOBM	IO_L48P_HDC_M1DQ8_1	UNUSED		1								
N18		IOBS	IO_L48N_M1DQ9_1	UNUSED		1								
P1		IOBS	IO_L34N_M3UDQSN_3	UNUSED		3								
P2		IOBM	IO_L34P_M3UDQS_3	UNUSED		3								
P3		IOBS	IO_L2N_3	UNUSED		3								
P4		IOBM	IO_L2P_3	UNUSED		3								
P5			VCCAUX								2.5			
P6		IOBS	IO_L64N_D9_2	UNUSED		2								
P7		IOBS	IO_L47N_2	UNUSED		2								
P8		IOBS	IO_L44N_2	UNUSED		2								
P9			VCCO_2			2					any*****			
P10			VCCAUX								2.5			
P11		IOBS	IO_L20N_2	UNUSED		2								
P12		IOBS	IO_L13N_D10_2	UNUSED		2								
P13			CMPCS_B_2											
P14			VCCAUX								2.5			
P15		IOBM	IO_L74P_AWAKE_1	UNUSED		1								
P16		IOBS	IO_L74N_DOUT_BUSY_1	UNUSED		1								

P17	AN<3>	IOB	IO_L49P_M1DQ10_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
P18	AN<2>	IOB	IO_L49N_M1DQ11_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
R1			GND											
R2			VCCO_3			3					any*****			
R3		IOBM	IO_L62P_D5_2	UNUSED		2								
R4			GND											
R5		IOBM	IO_L48P_D7_2	UNUSED		2								
R6			VCCO_2			2					any*****			
R7		IOBM	IO_L46P_2	UNUSED		2								
R8		IOBM	IO_L31P_GCLK31_D14_2	UNUSED		2								
R9			GND											
R10		IOBM	IO_L29P_GCLK3_2	UNUSED		2								
R11		IOBM	IO_L16P_2	UNUSED		2								
R12			VCCO_2			2					any*****			
R13		IOBM	IO_L3P_D0_DIN_MISO_MISO1_2	UNUSED		2								
R14			GND											
R15		IOBM	IO_L1P_CCLK_2	UNUSED		2								
R16			SUSPEND											
R17			VCCO_1			1					3.30			
R18			GND											
T1		IOBS	IO_L33N_M3DQ13_3	UNUSED		3								
T2		IOBM	IO_L33P_M3DQ12_3	UNUSED		3								
T3		IOBS	IO_L62N_D6_2	UNUSED		2								
T4		IOBM	IO_L63P_2	UNUSED		2								
T5		IOBS	IO_L48N_RDWR_B_VREF_2	UNUSED		2								
T6		IOBM	IO_L45P_2	UNUSED		2								
T7		IOBS	IO_L46	UNUSE		2								

			N_2	D									
T8		IOBS	IO_L31N_GCLK30_D15_2	UNUSED		2							
T9		IOBM	IO_L32P_GCLK29_2	UNUSED		2							
T10		IOBS	IO_L29N_GCLK2_2	UNUSED		2							
T11		IOBS	IO_L16N_VREF_2	UNUSED		2							
T12		IOBM	IO_L19P_2	UNUSED		2							
T13		IOBS	IO_L3N_MOSI_CSI_B_MISO0_2	UNUSED		2							
T14		IOBM	IO_L12P_D1_MISO2_2	UNUSED		2							
T15		IOBS	IO_L1N_M0_CMPMISO_2	UNUSED		2							
T16			GND										
T17	C<7>	IOB	IO_L51P_M1DQ12_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
T18	C<6>	IOB	IO_L51N_M1DQ13_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
U1		IOBS	IO_L32N_M3DQ15_3	UNUSED		3							
U2		IOBM	IO_L32P_M3DQ14_3	UNUSED		3							
U3		IOBM	IO_L65P_INIT_B_2	UNUSED		2							
U4			VCCO_2			2					any*****		
U5		IOBM	IO_L49P_D3_2	UNUSED		2							
U6			GND										
U7		IOBM	IO_L43P_2	UNUSED		2							
U8		IOBM	IO_L41P_2	UNUSED		2							
U9			VCCO_2			2					any*****		
U10		IOBM	IO_L30P_GCLK1_D13_2	UNUSED		2							
U11		IOBM	IO_L23P_2	UNUSED		2							

U12			GND											
U13		IOBM	IO_L14P_D11_2	UNUSED		2								
U14			VCCO_2			2					any*****			
U15		IOBM	IO_L5P_2	UNUSED		2								
U16		IOBM	IO_L2P_CMPCLK_2	UNUSED		2								
U17	C<5>	IOB	IO_L52P_M1DQ14_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
U18	C<4>	IOB	IO_L52N_M1DQ15_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
V1			GND											
V2			PROGRAM_B_2											
V3		IOBS	IO_L65N_CSO_B_2	UNUSED		2								
V4		IOBS	IO_L63N_2	UNUSED		2								
V5		IOBS	IO_L49N_D4_2	UNUSED		2								
V6		IOBS	IO_L45N_2	UNUSED		2								
V7		IOBS	IO_L43N_2	UNUSED		2								
V8		IOBS	IO_L41N_VREF_2	UNUSED		2								
V9		IOBS	IO_L32N_GCLK28_2	UNUSED		2								
V10	CLK	IOB	IO_L30N_GCLK0_USERCCLK_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
V11		IOBS	IO_L23N_2	UNUSED		2								
V12		IOBS	IO_L19N_2	UNUSED		2								
V13		IOBS	IO_L14N_D12_2	UNUSED		2								
V14		IOBS	IO_L12N_D2_MISO3_2	UNUSED		2								
V15		IOBS	IO_L5N_2	UNUSED		2								
V16		IOBS	IO_L2N_CMPMOSI_2	UNUSED		2								
V17			DONE_2											
V18			GND											

IOB Properties - Wed May 28 14:37:08 2014

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
AN<0>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<1>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<2>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<3>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<0>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<1>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<2>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<3>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<4>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<5>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<6>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<7>	IOB	OUTPUT	LVCMOS33		12	SLOW			
CLK	IOB	INPUT	LVCMOS33						
CLR	IOB	INPUT	LVCMOS33						

BCD_vhdl Project Status (05/28/2014 - 14:34:46)			
Project File:	BCD.xise	**Parser Errors:**	No Errors
Module Name:	BCD_vhdl	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.3	• **Warnings:**	3 Warnings (3 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	49	18,224	1%	
Number used as Flip Flops	49			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	77	9,112	1%	
Number used as logic	76	9,112	1%	
Number using O6 output only	14			
Number using O5 output only	30			
Number using O5 and O6	32			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	24	2,278	1%	
Nummber of MUXCYs used	48	4,556	1%	
Number of LUT Flip Flop pairs used	82			
Number with an unused Flip Flop	45	82	54%	
Number with an unused LUT	5	82	6%	
Number of fully used LUT-FF pairs	32	82	39%	
Number of unique control sets	4			
Number of slice register sites lost to control set restrictions	15	18,224	1%	
Number of bonded IOBs	14	232	6%	
Number of LOCed IOBs	14	14	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.61			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed May 28 14:33:29 2014	0	3 Warnings (3 new)	2 Infos (2 new)
Translation Report	Current	Wed May 28 14:33:34 2014	0	0	0
Map Report	Current	Wed May 28 14:33:58 2014	0	0	6 Infos (6 new)
Place and Route Report	Current	Wed May 28 14:34:08 2014	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed May 28 14:34:13 2014	0	0	4 Infos (4 new)
Bitgen Report	Current	Wed May 28 14:34:41 2014	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	Wed May 28 14:34:41 2014	
WebTalk Log File	Current	Wed May 28 14:34:46 2014	

Date Generated: 05/28/2014 - 14:34:46