WESTERN MICHIGAN UNIVERSITY
ECE 5510 APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN

Assignment #4

STOPWATCH USING NEXYS3

By:

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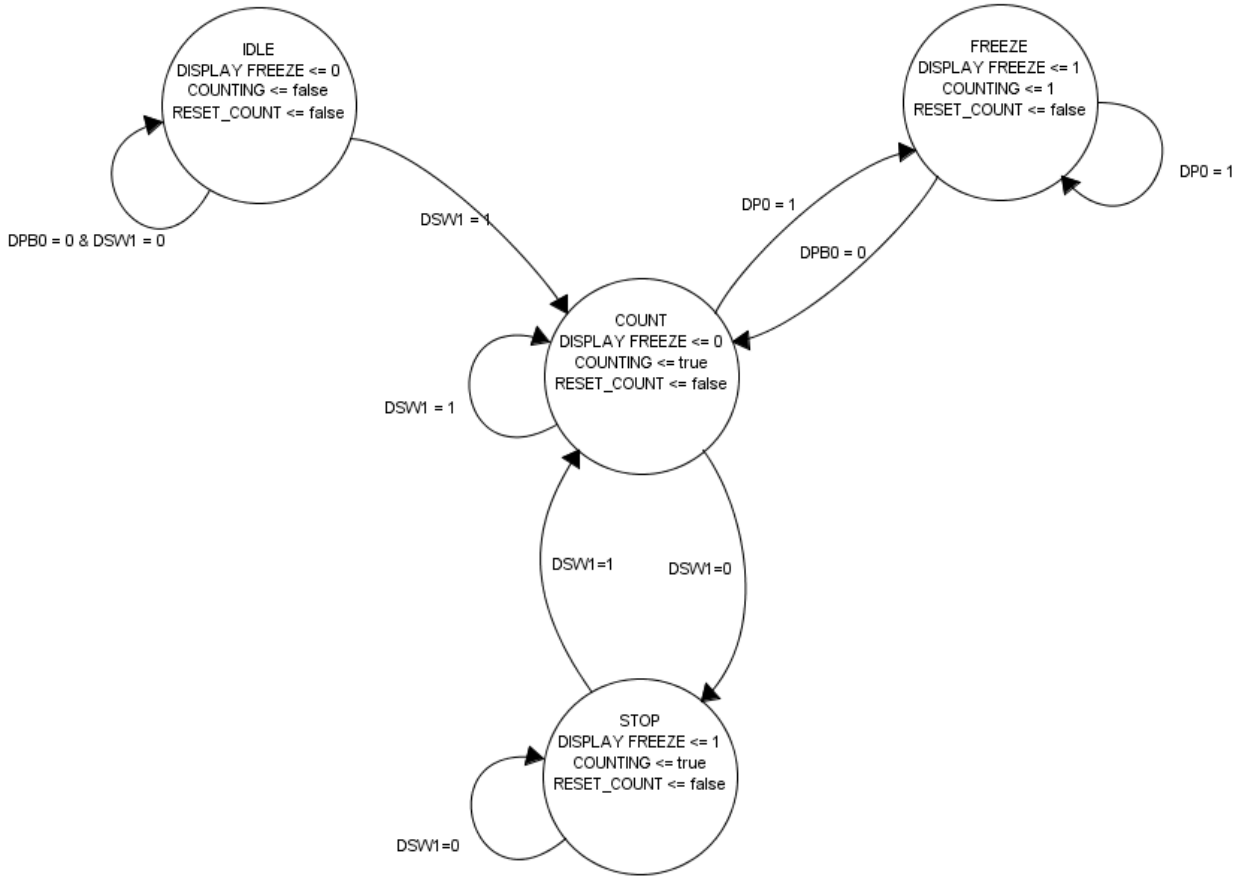
1.Introduction

A stopwatch is an instrument to measure the amount of time. Generally, there are differences scales of range; however, I am using a range of 1 minute. The scale of the stopwatch is 0.01s. The first digit in the left shows, leftmost, shows hundredth of second, the second digit shows the tenth of a second, and the first and second; rightmost, shows the seconds.

Our stopwatch is controlled by a push buttons PB0 and a slid switches SW1. When SW1 is switched the watch resets and starts to count from 0. When SW1 is low-level, the watch stops and the final time is displayed. The function of the push button is to frozen the display, but the watch is not stoped; therefore, when PB0 is released, the display shows the current time.

2.FMS



3. File.do

restart

force CLK 0 0, 1 10ns -r 20ns

force PB0 0
force SW1 1

force SW1 0 @5000ns
force SW1 1 @7000ns

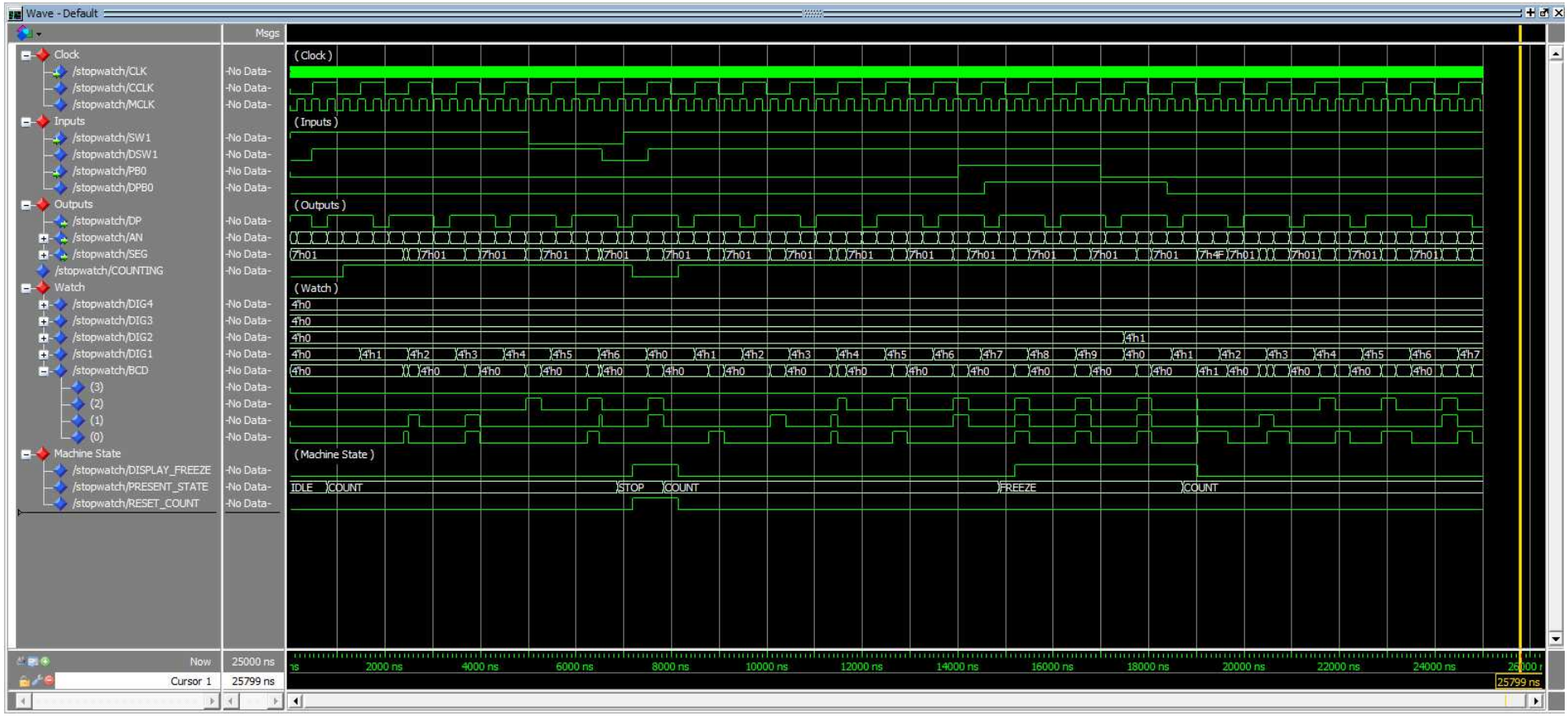
force PB0 1 @14000ns
force PB0 0 @17000ns

run 25000ns

In this simulation, there is a different clock signal because is not viable to work with real clock. Also, it is testing the all conditions of the STOPWATCH.

Initially, the slide switch is turn ON (SW1) and the watch is initialized. You can see in the signals DIG4, DIG3, DIG2, DIG1 the corresponding values: 0000, 0001, 0002, 0003, 0004, 0005, and 0006. I can continue until 5999 because the next value is 0000. However, the SW1 is turn OFF for a short time, then turn ON. Note that the value was frozen and when SW1 was turned ON, the watch started to work from the 00.00.

Also, I simulated the push button PB0 that has the function to fix the value on the display when pushed. Therefore, in the moment that the PB0 is pressed the last value in the displayed is showed; in this case is 0007. However, the watch is working normally, and when it is released the display shows the current time; in this case is 00.10.


Wave - Default
Msgs
Clock
/stopwatch/CLK
/stopwatch/CCLK
/stopwatch/MCLK
Inputs
/stopwatch/SW1
/stopwatch/DSW1
/stopwatch/PB0
/stopwatch/DPB0
Outputs
/stopwatch/DP
/stopwatch/AN
/stopwatch/SEG
/stopwatch/COUNTING
Watch
/stopwatch/DIG4
/stopwatch/DIG3
/stopwatch/DIG2
/stopwatch/DIG1
/stopwatch/BCD
(3)
(2)
(1)
(0)
Machine State
/stopwatch/DISPLAY_FREEZE
/stopwatch/PRESENT_STATE
/stopwatch/RESET_COUNT
-No Data-
(Clock)
(Inputs)
(Outputs)
(Watch)
(Machine State)
IDLE
COUNT
STOP
FREEZE
Now
25000 ns
Cursor 1
25799 ns
2000 ns
4000 ns
6000 ns
8000 ns
10000 ns
12000 ns
14000 ns
16000 ns
18000 ns
20000 ns
22000 ns
24000 ns

```
1   ----------------------------------------------------------------------------------
2   -- Company: Western Michigan University
3   -- Engineer: Erivelton Gualter dos Santos
4   --
5   -- Create Date:    21:50:25 06/03/2014
6   -- Design Name:
7   -- Module Name:    stopwatch - Behavioral
8   -- Project Name:
9   -- Target Devices:
10  -- Tool versions:
11  -- Description:
12  --
13  -- Dependencies:
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.STD_LOGIC_ARITH.ALL;
23  use IEEE.STD_LOGIC_UNSIGNED.ALL;
24
25  -- Uncomment the following library declaration if using
26  -- arithmetic functions with Signed or Unsigned values
27  --use IEEE.NUMERIC_STD.ALL;
28
29  -- Uncomment the following library declaration if instantiating
30  -- any Xilinx primitives in this code.
31  --library UNISIM;
32  --use UNISIM.VComponents.all;
33
34  entity stopwatch is
35     port (   CLK : in std_logic;
36              SW1 : in std_logic;
37              PB0 : in std_logic;
38              DP  : out std_logic;
39              AN  : out std_logic_vector (3 downto 0);
40              SEG : out std_logic_vector (6 downto 0));
41  end stopwatch;
42
43  architecture Behavioral of stopwatch is
44
45     signal CCLK : std_logic;
46     signal MCLK : std_logic;
47
48     signal SHIFTR1,SHIFTR2 : std_logic_vector (3 downto 0) := "0000";
49     signal DPB0 : std_logic := '0';
50     signal DSW1 : std_logic := '0';
51
52     type state is (IDLE, COUNT, STOP, FREEZE);
53     signal PRESENT_STATE : state:=IDLE;
54
55     signal DIG1: std_logic_vector (3 downto 0) := "0000";
56     signal DIG2: std_logic_vector (3 downto 0) := "0000";
57     signal DIG3: std_logic_vector (3 downto 0) := "0000";
```

```
58      signal DIG4: std_logic_vector (3 downto 0) := "0000";
59
60      signal BCD: std_logic_vector (3 downto 0);
61
62      signal COUNTING   : boolean := false;
63      signal RESET_COUNT: boolean := false;
64      signal DISPLAY_FREEZE: std_logic := '0';
65
66    begin
67
68    ------------------------------------------------
69    --------         Count Clock       ---------------
70    ------------------------------------------------
71    clk_main: process(CLK, CCLK)
72       variable DIVIDE : integer := 1000000;
73       variable COUNTER_DIV : integer :=0;
74    begin
75       if (rising_edge(CLK)) then
76          if(COUNTER_DIV < DIVIDE/2-1) then
77             COUNTER_DIV := COUNTER_DIV + 1;
78             CCLK <= '0';
79          elsif (COUNTER_DIV < DIVIDE-1) then
80             COUNTER_DIV := COUNTER_DIV + 1;
81             CCLK <= '1';
82          else
83             CCLK <= '0';
84             COUNTER_DIV := 0;
85          end if;
86       end if;
87    end process clk_main;
88
89    ------------------------------------------------
90    --------         Main Clock        ---------------
91    ------------------------------------------------
92    clk_segment: process(CLK, MCLK)
93       variable DIVIDE : integer := 1600;
94       variable COUNTER_DIV : integer :=0;
95    begin
96       if (rising_edge(CLK)) then
97          if(COUNTER_DIV < DIVIDE/2-1) then
98             COUNTER_DIV := COUNTER_DIV + 1;
99             MCLK <= '0';
100         elsif (COUNTER_DIV < DIVIDE-1) then
101            COUNTER_DIV := COUNTER_DIV + 1;
102            MCLK <= '1';
103         else
104            MCLK <= '0';
105            COUNTER_DIV := 0;
106         end if;
107      end if;
108   end process clk_segment;
109
110   ------------------------------------------------
111   --------      Debouncing SW1           -----------
112   ------------------------------------------------
113
114   process(MCLK,SW1)
```

```
115   begin
116      if (MCLK='1' and MCLK'event) then
117         SHIFTR1(2 downto 0) <= SHIFTR1(3 downto 1);
118         SHIFTR1(3) <= SW1;
119         if (SHIFTR1 = "0000") then
120            DSW1 <= '0';
121         else
122            DSW1 <= '1';
123         end if;
124      end if;
125      -- simulaco
126      -- DSW1 <= SW1;
127   end process;
128
129   ------------------------------------------------
130   --------      Debouncing PB0           -----------
131   ------------------------------------------------
132
133   process(MCLK,PB0)
134   begin
135      if (MCLK='1' and MCLK'event) then
136         SHIFTR2(2 downto 0) <= SHIFTR2(3 downto 1);
137         SHIFTR2(3) <= PB0;
138         if (SHIFTR2 = "0000") then
139            DPB0 <= '0';
140         else
141            DPB0 <= '1';
142         end if;
143      end if;
144      -- simulaco
145      -- DPB0 <= PB0;
146   end process;
147
148   ------------------------------------------------
149   --------      Display Controller       -----------
150   ------------------------------------------------
151
152   process(MCLK, DISPLAY_FREEZE, DIG1, DIG2, DIG3, DIG4)
153      variable SEL: STD_LOGIC_vector(1 downto 0) := "00";
154      variable FDIG1: std_logic_vector (3 downto 0) ;
155      variable FDIG2: std_logic_vector (3 downto 0) ;
156      variable FDIG3: std_logic_vector (3 downto 0) ;
157      variable FDIG4: std_logic_vector (3 downto 0) ;
158
159   begin
160      if (MCLK='1' and MCLK'event ) then
161         SEL:=SEL+1;
162      end if;
163      if (DISPLAY_FREEZE = '1' and DISPLAY_FREEZE'event) then
164         FDIG1 := DIG1;
165         FDIG2 := DIG2;
166         FDIG3 := DIG3;
167         FDIG4 := DIG4;
168      end if;
169
170      case SEL is
171         when "00" =>
```

```
172            if (DISPLAY_FREEZE = '1') then
173               BCD <= FDIG1;
174            else
175               BCD <= DIG1;
176            end if;
177            AN  <= "1110";
178            DP <= '1';
179         when "01"=>
180            if (DISPLAY_FREEZE = '1') then
181               BCD <= FDIG2;
182            else
183               BCD <= DIG2;
184            end if;
185            AN  <= "1101";
186            DP <= '1';
187         when "10"=>
188            if (DISPLAY_FREEZE = '1') then
189               BCD <= FDIG3;
190            else
191               BCD <= DIG3;
192            end if;
193            AN  <= "1011";
194            DP <= '0';
195         when others=>
196            if (DISPLAY_FREEZE = '1') then
197               BCD <= FDIG4;
198            else
199               BCD <= DIG4;
200            end if;
201            AN  <= "0111";
202            DP <= '1';
203      end case;
204
205   end process;
206
207   ----------------------------------------------------
208   --------     7 segments Decoder        -----------
209   ----------------------------------------------------
210   segment_process: process(BCD)
211   begin
212      case  BCD is
213      when "0000"=> SEG <="0000001";  -- '0'
214      when "0001"=> SEG <="1001111";  -- '1'
215      when "0010"=> SEG <="0010010";  -- '2'
216      when "0011"=> SEG <="0000110";  -- '3'
217      when "0100"=> SEG <="1001100";  -- '4'
218      when "0101"=> SEG <="0100100";  -- '5'
219      when "0110"=> SEG <="0100000";  -- '6'
220      when "0111"=> SEG <="0001111";  -- '7'
221      when "1000"=> SEG <="0000000";  -- '8'
222      when "1001"=> SEG <="0000100";  -- '9'
223      when others=> SEG <="1111111";
224      end case;
225   end process segment_process;
226
227   ----------------------------------------------------
228   --------          Counter          ---------------
```

```
229   ------------------------------------------------
230   counter: process(CCLK, DSW1, RESET_COUNT)
231
232   begin
233      if (CCLK'event and CCLK = '1') then
234         if (COUNTING = true) then
235            if (DIG4 = "0101" and DIG3 = "1001" and DIG2 = "1001" and DIG1 = "1001") then
       -- 59.99
236               DIG4 <= "0000";
237               DIG3 <= "0000";
238               DIG2 <= "0000";
239               DIG1 <= "0000";
240            elsif (DIG3 = "1001" and DIG2 = "1001" and DIG1 = "1001") then -- X9.99
241               DIG4 <= DIG4 + 1;
242               DIG3 <= "0000";
243               DIG2 <= "0000";
244               DIG1 <= "0000";
245            elsif (DIG2 = "1001" and DIG1 = "1001") then -- XX.99
246               DIG3 <= DIG3 + 1;
247               DIG2 <= "0000";
248               DIG1 <= "0000";
249            elsif (DIG1 = "1001") then -- XX.X9
250               DIG2 <= DIG2 + 1;
251               DIG1 <= "0000";
252            else -- XX.XX
253               DIG1 <= DIG1 + 1;
254            end if;
255         elsif (RESET_COUNT = true) then
256            DIG4 <= "0000";
257            DIG3 <= "0000";
258            DIG2 <= "0000";
259            DIG1 <= "0000";
260         end if;
261      end if;
262
263   end process counter;
264
265   ------------------------------------------------
266   --------         STATE MACHINE         -----------
267   ------------------------------------------------
268   machine: process(MCLK, DSW1, CCLK)
269      --variable reset: integer :=0;
270      --variable regreset: boolean := false;
271   begin
272      if (MCLK'event and MCLK = '1') then
273         case PRESENT_STATE is
274         when IDLE =>
275            DISPLAY_FREEZE <= '0';
276            COUNTING       <= false;
277
278            if (DPB0 = '1') then
279               PRESENT_STATE <= FREEZE;
280            elsif (DSW1 = '1') then
281               PRESENT_STATE <= COUNT;
282            else
283               PRESENT_STATE <= IDLE;
284            end if;
```

```
285
286         when COUNT =>
287            DISPLAY_FREEZE <= '0';
288            COUNTING       <= true;
289            RESET_COUNT    <= false;
290
291            if(DSW1 = '1' and DPB0 = '1') then
292               PRESENT_STATE <= FREEZE;
293            elsif (DSW1 = '1') then
294               PRESENT_STATE <= COUNT;
295            elsif (DSW1 = '0') then
296               PRESENT_STATE <= STOP;
297            end if;
298
299         when STOP =>
300            COUNTING       <= false;
301            RESET_COUNT    <= true;
302            DISPLAY_FREEZE <= '1';
303
304            if (DSW1 = '1') then
305               PRESENT_STATE <= COUNT;
306            else
307               PRESENT_STATE <= STOP;
308            end if;
309
310         when FREEZE =>
311            DISPLAY_FREEZE <= '1';
312            COUNTING       <= true;
313
314            if (DPB0 = '1') then
315               PRESENT_STATE <= FREEZE;
316            else
317               PRESENT_STATE <= COUNT;
318            end if;
319
320         end case;
321      end if;
322   end process machine;
323
324   end Behavioral;
325
326
```

```
1
2   # PlanAhead Generated IO constraints
3
4   NET "AN[3]" IOSTANDARD = LVCMOS33;
5   NET "AN[2]" IOSTANDARD = LVCMOS33;
6   NET "AN[1]" IOSTANDARD = LVCMOS33;
7   NET "AN[0]" IOSTANDARD = LVCMOS33;
8   NET "DP" IOSTANDARD = LVCMOS33;
9   NET "SEG[6]" IOSTANDARD = LVCMOS33;
10  NET "SEG[5]" IOSTANDARD = LVCMOS33;
11  NET "SEG[4]" IOSTANDARD = LVCMOS33;
12  NET "SEG[3]" IOSTANDARD = LVCMOS33;
13  NET "SEG[2]" IOSTANDARD = LVCMOS33;
14  NET "SEG[1]" IOSTANDARD = LVCMOS33;
15  NET "SEG[0]" IOSTANDARD = LVCMOS33;
16  NET "CLK" IOSTANDARD = LVCMOS33;
17  NET "PB0" IOSTANDARD = LVCMOS33;
18  NET "SW1" IOSTANDARD = LVCMOS33;
19
20  # PlanAhead Generated physical constraints
21
22  NET "AN[3]" LOC = P17;
23  NET "AN[2]" LOC = P18;
24  NET "AN[1]" LOC = N15;
25  NET "AN[0]" LOC = N16;
26  NET "DP" LOC = M13;
27  NET "SEG[6]" LOC = T17;
28  NET "SEG[5]" LOC = T18;
29  NET "SEG[4]" LOC = U17;
30  NET "SEG[3]" LOC = U18;
31  NET "SEG[2]" LOC = M14;
32  NET "SEG[1]" LOC = N14;
33  NET "SEG[0]" LOC = L14;
34  NET "CLK" LOC = V10;
35  NET "PB0" LOC = B8;
36  NET "SW1" LOC = T9;
37
```

IOB Properties - Tue Jun 10 22:09:17 2014

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
AN<0>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<1>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<2>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<3>	IOB	OUTPUT	LVCMOS33		12	SLOW			
CLK	IOB	INPUT	LVCMOS33						
DP	IOB	OUTPUT	LVCMOS33		12	SLOW			
PB0	IOB	INPUT	LVCMOS33						
SEG<0>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SEG<1>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SEG<2>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SEG<3>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SEG<4>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SEG<5>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SEG<6>	IOB	OUTPUT	LVCMOS33		12	SLOW			
SW1	IOB	INPUT	LVCMOS33						

stopwatch Project Status (06/10/2014 - 22:07:28)			
Project File:	STOPWATCH.xise	**Parser Errors:**	No Errors
Module Name:	stopwatch	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	19 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	147	18,224	1%	
Number used as Flip Flops	131			
Number used as Latches	16			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	232	9,112	2%	
Number used as logic	230	9,112	2%	
Number using O6 output only	118			
Number using O5 output only	60			
Number using O5 and O6	52			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	2			
Number with same-slice register load	0			
Number with same-slice carry load	2			
Number with other load	0			
Number of occupied Slices	108	2,278	4%	
Number of MUXCYs used	96	4,556	2%	
Number of LUT Flip Flop pairs used	275			
Number with an unused Flip Flop	131	275	47%	
Number with an unused LUT	43	275	15%	
Number of fully used LUT-FF pairs	101	275	36%	
Number of unique control sets	52			
Number of slice register sites lost to control set restrictions	357	18,224	1%	
Number of bonded IOBs	15	232	6%	
Number of LOCed IOBs	15	15	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	2	16	12%	
Number used as BUFGs	2			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.64			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Jun 10 22:05:52 2014	0	3 Warnings (0 new)	3 Infos (0 new)
Translation Report	Current	Tue Jun 10 22:06:47 2014	0	0	0
Map Report	Current	Tue Jun 10 22:07:01 2014	0	16 Warnings (0 new)	6 Infos (0 new)
Place and Route Report	Current	Tue Jun 10 22:07:19 2014	0	0	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Tue Jun 10 22:07:26 2014	0	0	4 Infos (0 new)
Bitgen Report	Out of Date	Tue Jun 10 21:55:11 2014	0	16 Warnings (16 new)	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Out of Date	Tue Jun 10 21:55:12 2014	
WebTalk Log File	Out of Date	Tue Jun 10 21:55:16 2014	

Date Generated: 06/10/2014 - 22:07:28

Pinout Report - Wed Jun 11 13:13:53 2014

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank Number	Drive (mA)	Slew Rate	Termination	IOB Delay	Voltage	Constraint	IO Register	Signal Integrity
A1			GND											
A2		IOBS	IO_L2N_0	UNUSED		0								
A3		IOBS	IO_L4N_0	UNUSED		0								
A4		IOBS	IO_L5N_0	UNUSED		0								
A5		IOBS	IO_L6N_0	UNUSED		0								
A6		IOBS	IO_L8N_VREF_0	UNUSED		0								
A7		IOBS	IO_L10N_0	UNUSED		0								
A8		IOBS	IO_L33N_0	UNUSED		0								
A9		IOBS	IO_L35N_GCLK16_0	UNUSED		0								
A10		IOBS	IO_L37N_GCLK12_0	UNUSED		0								
A11		IOBS	IO_L39N_0	UNUSED		0								
A12		IOBS	IO_L41N_0	UNUSED		0								
A13		IOBS	IO_L50N_0	UNUSED		0								
A14		IOBS	IO_L62N_VREF_0	UNUSED		0								
A15		IOBS	IO_L64N_SCP4_0	UNUSED		0								
A16		IOBS	IO_L66N_SCP0_0	UNUSED		0								
A17			TCK											
A18			GND											
B1			VCCAUX								2.5			
B2		IOBM	IO_L2P_0	UNUSED		0								
B3		IOBM	IO_L4P_0	UNUSED		0								
B4		IOBM	IO_L5P_0	UNUSED		0								
B5			VCCO_0			0					any*****			
B6		IOBM	IO_L8P_0	UNUSED		0								
B7			GND											
B8	PB0	IOB	IO_L33	INPUT	LVCMO	0				NONE		LOCATE	NO	NONE

			P_0		S33						D		
B9		IOBM	IO_L35P_GCLK17_0	UNUSED		0							
B10			VCCO_0			0					any*****		
B11		IOBM	IO_L39P_0	UNUSED		0							
B12		IOBM	IO_L41P_0	UNUSED		0							
B13			GND										
B14		IOBM	IO_L62P_0	UNUSED		0							
B15			VCCO_0			0					any*****		
B16		IOBM	IO_L66P_SCP1_0	UNUSED		0							
B17			VCCAUX								2.5		
B18			TMS										
C1		IOBS	IO_L83N_VREF_3	UNUSED		3							
C2		IOBM	IO_L83P_3	UNUSED		3							
C3			GND										
C4		IOBS	IO_L1N_VREF_0	UNUSED		0							
C5		IOBM	IO_L6P_0	UNUSED		0							
C6		IOBS	IO_L3N_0	UNUSED		0							
C7		IOBM	IO_L10P_0	UNUSED		0							
C8		IOBS	IO_L11N_0	UNUSED		0							
C9		IOBS	IO_L34N_GCLK18_0	UNUSED		0							
C10		IOBM	IO_L37P_GCLK13_0	UNUSED		0							
C11		IOBS	IO_L36N_GCLK14_0	UNUSED		0							
C12		IOBS	IO_L47N_0	UNUSED		0							
C13		IOBM	IO_L50P_0	UNUSED		0							
C14		IOBS	IO_L65N_SCP2_0	UNUSED		0							
C15		IOBM	IO_L64P_SCP5_0	UNUSED		0							
C16			GND										
C17		IOBM	IO_L29P_A23_M1A13_	UNUSED		1							

			1											
C18		IOBS	IO_L29N_A22_M1A14_1	UNUSED		1								
D1		IOBS	IO_L52N_M3A9_3	UNUSED		3								
D2		IOBM	IO_L52P_M3A8_3	UNUSED		3								
D3		IOBS	IO_L54N_M3A11_3	UNUSED		3								
D4		IOBM	IO_L1P_HSWAPEN_0	UNUSED		0								
D5			GND											
D6		IOBM	IO_L3P_0	UNUSED		0								
D7			VCCO_0			0					any*****			
D8		IOBM	IO_L11P_0	UNUSED		0								
D9		IOBM	IO_L34P_GCLK19_0	UNUSED		0								
D10			GND											
D11		IOBM	IO_L36P_GCLK15_0	UNUSED		0								
D12		IOBM	IO_L47P_0	UNUSED		0								
D13			VCCO_0			0					any*****			
D14		IOBM	IO_L65P_SCP3_0	UNUSED		0								
D15			TDI											
D16			TDO											
D17		IOBM	IO_L31P_A19_M1CKE_1	UNUSED		1								
D18		IOBS	IO_L31N_A18_M1A12_1	UNUSED		1								
E1		IOBS	IO_L50N_M3BA2_3	UNUSED		3								
E2			VCCO_3			3					any*****			
E3		IOBM	IO_L50P_M3WE_3	UNUSED		3								
E4		IOBM	IO_L54P_M3RESET_3	UNUSED		3								
E5			VCCAUX								2.5			

E6		IOBS	IO_L7N_0	UNUSED		0							
E7		IOBM	IO_L9P_0	UNUSED		0							
E8		IOBS	IO_L9N_0	UNUSED		0							
E9			VCCAUX								2.5		
E10			VCCO_0			0					any*****		
E11		IOBS	IO_L42N_0	UNUSED		0							
E12		IOBS	IO_L51N_0	UNUSED		0							
E13		IOBS	IO_L63N_SCP6_0	UNUSED		0							
E14			VCCAUX								2.5		
E15			GND										
E16		IOBM	IO_L33P_A15_M1A10_1	UNUSED		1							
E17			VCCO_1			1					3.30		
E18		IOBS	IO_L33N_A14_M1A4_1	UNUSED		1							
F1		IOBS	IO_L48N_M3BA1_3	UNUSED		3							
F2		IOBM	IO_L48P_M3BA0_3	UNUSED		3							
F3		IOBS	IO_L51N_M3A4_3	UNUSED		3							
F4		IOBM	IO_L51P_M3A10_3	UNUSED		3							
F5		IOBS	IO_L55N_M3A14_3	UNUSED		3							
F6		IOBM	IO_L55P_M3A13_3	UNUSED		3							
F7		IOBM	IO_L7P_0	UNUSED		0							
F8		IOBS	IO_L32N_0	UNUSED		0							
F9		IOBS	IO_L38N_VREF_0	UNUSED		0							
F10		IOBS	IO_L40N_0	UNUSED		0							
F11		IOBM	IO_L42P_0	UNUSED		0							
F12		IOBM	IO_L51P_0	UNUSED		0							
F13		IOBM	IO_L63P_SCP7_0	UNUSED		0							

F14		IOBM	IO_L30P_A21_M1RESET_1	UNUSED		1							
F15		IOBM	IO_L1P_A25_1	UNUSED		1							
F16		IOBS	IO_L1N_A24_VREF_1	UNUSED		1							
F17		IOBM	IO_L35P_A11_M1A7_1	UNUSED		1							
F18		IOBS	IO_L35N_A10_M1A2_1	UNUSED		1							
G1		IOBS	IO_L46N_M3CLKN_3	UNUSED		3							
G2			GND										
G3		IOBM	IO_L46P_M3CLK_3	UNUSED		3							
G4			VCCO_3			3					any*****		
G5			GND										
G6		IOBS	IO_L53N_M3A12_3	UNUSED		3							
G7			VCCINT								1.2		
G8		IOBM	IO_L32P_0	UNUSED		0							
G9		IOBM	IO_L38P_0	UNUSED		0							
G10			VCCAUX								2.5		
G11		IOBM	IO_L40P_0	UNUSED		0							
G12			GND										
G13		IOBS	IO_L32N_A16_M1A9_1	UNUSED		1							
G14		IOBS	IO_L30N_A20_M1A11_1	UNUSED		1							
G15			VCCO_1			1					3.30		
G16		IOBM	IO_L38P_A5_M1CLK_1	UNUSED		1							
G17			GND										
G18		IOBS	IO_L38N_A4_M1CLKN_1	UNUSED		1							
H1		IOBS	IO_L41N_GCLK26_M3DQ5_3	UNUSED		3							
H2		IOBM	IO_L41P_GCLK27_M3D	UNUSED		3							

			Q4_3											
H3		IOBS	IO_L44N_GCLK20_M3A6_3	UNUSED		3								
H4		IOBM	IO_L44P_GCLK21_M3A5_3	UNUSED		3								
H5		IOBS	IO_L49N_M3A2_3	UNUSED		3								
H6		IOBM	IO_L49P_M3A7_3	UNUSED		3								
H7		IOBM	IO_L53P_M3CKE_3	UNUSED		3								
H8			GND											
H9			VCCINT								1.2			
H10			GND											
H11			VCCINT								1.2			
H12		IOBM	IO_L32P_A17_M1A8_1	UNUSED		1								
H13		IOBM	IO_L36P_A9_M1BA0_1	UNUSED		1								
H14		IOBS	IO_L36N_A8_M1BA1_1	UNUSED		1								
H15		IOBM	IO_L37P_A7_M1A0_1	UNUSED		1								
H16		IOBS	IO_L37N_A6_M1A1_1	UNUSED		1								
H17		IOBM	IO_L43P_GCLK5_M1DQ4_1	UNUSED		1								
H18		IOBS	IO_L43N_GCLK4_M1DQ5_1	UNUSED		1								
J1		IOBS	IO_L40N_M3DQ7_3	UNUSED		3								
J2			VCCO_3			3					any*****			
J3		IOBM	IO_L40P_M3DQ6_3	UNUSED		3								
J4			GND											
J5			VCCO_3			3					any*****			
J6		IOBS	IO_L47N_M3A1_3	UNUSED		3								
J7		IOBM	IO_L47P_M3A0	UNUSED		3								

			_3											
J8			VCCINT								1.2			
J9			GND											
J10			VCCINT								1.2			
J11			GND											
J12			VCCAUX								2.5			
J13		IOBM	IO_L39P_M1A3_1	UNUSED		1								
J14			VCCO_1			1					3.30			
J15			GND											
J16		IOBM	IO_L44P_A3_M1DQ6_1	UNUSED		1								
J17			VCCO_1			1					3.30			
J18		IOBS	IO_L44N_A2_M1DQ7_1	UNUSED		1								
K1		IOBS	IO_L38N_M3DQ3_3	UNUSED		3								
K2		IOBM	IO_L38P_M3DQ2_3	UNUSED		3								
K3		IOBS	IO_L42N_GCLK24_M3LDM_3	UNUSED		3								
K4		IOBM	IO_L42P_GCLK25_TRDY2_M3UDM_3	UNUSED		3								
K5		IOBS	IO_L43N_GCLK22_IRDY2_M3CASN_3	UNUSED		3								
K6		IOBS	IO_L45N_M3ODT_3	UNUSED		3								
K7			VCCAUX								2.5			
K8			GND											
K9			VCCINT								1.2			
K10			GND											
K11			VCCINT								1.2			
K12		IOBM	IO_L34P_A13_M1WE_1	UNUSED		1								
K13		IOBS	IO_L34N_A12_M1BA2_1	UNUSED		1								
K14		IOBS	IO_L39N_M1ODT_1	UNUSED		1								
K15		IOBM	IO_L41P_GCLK9_IRDY	UNUSED		1								

			1_M1RASN_1											
K16		IOBS	IO_L41N_GCLK8_M1CASN_1	UNUSED		1								
K17		IOBM	IO_L45P_A1_M1LDQS_1	UNUSED		1								
K18		IOBS	IO_L45N_A0_M1LDQSN_1	UNUSED		1								
L1		IOBS	IO_L37N_M3DQ1_3	UNUSED		3								
L2		IOBM	IO_L37P_M3DQ0_3	UNUSED		3								
L3		IOBS	IO_L39N_M3LDQSN_3	UNUSED		3								
L4		IOBM	IO_L39P_M3LDQS_3	UNUSED		3								
L5		IOBM	IO_L43P_GCLK23_M3RASN_3	UNUSED		3								
L6		IOBM	IO_L31P_3	UNUSED		3								
L7		IOBM	IO_L45P_M3A3_3	UNUSED		3								
L8			VCCINT								1.2			
L9			GND											
L10			VCCINT								1.2			
L11			GND											
L12		IOBM	IO_L40P_GCLK11_M1A5_1	UNUSED		1								
L13		IOBS	IO_L40N_GCLK10_M1A6_1	UNUSED		1								
L14	SEG<0>	IOB	IO_L61P_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
L15		IOBM	IO_L42P_GCLK7_M1UDM_1	UNUSED		1								
L16		IOBS	IO_L42N_GCLK6_TRDY1_M1LDM_1	UNUSED		1								
L17		IOBM	IO_L46P_FCS_B_M1D	UNUSED		1								

			Q2_1											
L18		IOBS	IO_L46N_FOE_B_M1DQ3_1	UNUSED		1								
M1		IOBS	IO_L36N_M3DQ9_3	UNUSED		3								
M2			GND											
M3		IOBM	IO_L36P_M3DQ8_3	UNUSED		3								
M4			VCCO_3			3					any*****			
M5		IOBS	IO_L31N_VREF_3	UNUSED		3								
M6			GND											
M7			VCCINT								1.2			
M8		IOBM	IO_L40P_2	UNUSED		2								
M9			VCCAUX								2.5			
M10		IOBM	IO_L22P_2	UNUSED		2								
M11		IOBM	IO_L15P_2	UNUSED		2								
M12			VCCINT								1.2			
M13	DP	IOB	IO_L61N_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
M14	SEG<2>	IOB	IO_L53P_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
M15			VCCO_1			1					3.30			
M16		IOBM	IO_L47P_FWE_B_M1DQ0_1	UNUSED		1								
M17			GND											
M18		IOBS	IO_L47N_LDC_M1DQ1_1	UNUSED		1								
N1		IOBS	IO_L35N_M3DQ11_3	UNUSED		3								
N2		IOBM	IO_L35P_M3DQ10_3	UNUSED		3								
N3		IOBS	IO_L1N_VREF_3	UNUSED		3								
N4		IOBM	IO_L1P_3	UNUSED		3								
N5		IOBM	IO_L64P_D8_2	UNUSED		2								
N6		IOBM	IO_L47P_2	UNUSED		2								
N7		IOBM	IO_L44P_2	UNUSED		2								
N8		IOBS	IO_L40N_2	UNUSED		2								

N9		IOBS	IO_L22N_2	UNUSED		2								
N10		IOBM	IO_L20P_2	UNUSED		2								
N11		IOBS	IO_L15N_2	UNUSED		2								
N12		IOBM	IO_L13P_M1_2	UNUSED		2								
N13			GND											
N14	SEG<1>	IOB	IO_L53N_VREF_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
N15	AN<1>	IOB	IO_L50P_M1UDQS_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
N16	AN<0>	IOB	IO_L50N_M1UDQSN_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
N17		IOBM	IO_L48P_HDC_M1DQ8_1	UNUSED		1								
N18		IOBS	IO_L48N_M1DQ9_1	UNUSED		1								
P1		IOBS	IO_L34N_M3UDQSN_3	UNUSED		3								
P2		IOBM	IO_L34P_M3UDQS_3	UNUSED		3								
P3		IOBS	IO_L2N_3	UNUSED		3								
P4		IOBM	IO_L2P_3	UNUSED		3								
P5			VCCAUX								2.5			
P6		IOBS	IO_L64N_D9_2	UNUSED		2								
P7		IOBS	IO_L47N_2	UNUSED		2								
P8		IOBS	IO_L44N_2	UNUSED		2								
P9			VCCO_2			2					any*****			
P10			VCCAUX								2.5			
P11		IOBS	IO_L20N_2	UNUSED		2								
P12		IOBS	IO_L13N_D10_2	UNUSED		2								
P13			CMPCS_B_2											
P14			VCCAUX								2.5			
P15		IOBM	IO_L74P_AWAKE_1	UNUSED		1								
P16		IOBS	IO_L74N_DOUT_BUSY_1	UNUSED		1								

P17	AN<3>	IOB	IO_L49P_M1DQ10_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
P18	AN<2>	IOB	IO_L49N_M1DQ11_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
R1			GND											
R2			VCCO_3			3					any*****			
R3		IOBM	IO_L62P_D5_2	UNUSED		2								
R4			GND											
R5		IOBM	IO_L48P_D7_2	UNUSED		2								
R6			VCCO_2			2					any*****			
R7		IOBM	IO_L46P_2	UNUSED		2								
R8		IOBM	IO_L31P_GCLK31_D14_2	UNUSED		2								
R9			GND											
R10		IOBM	IO_L29P_GCLK3_2	UNUSED		2								
R11		IOBM	IO_L16P_2	UNUSED		2								
R12			VCCO_2			2					any*****			
R13		IOBM	IO_L3P_D0_DIN_MISO_MISO1_2	UNUSED		2								
R14			GND											
R15		IOBM	IO_L1P_CCLK_2	UNUSED		2								
R16			SUSPEND											
R17			VCCO_1			1					3.30			
R18			GND											
T1		IOBS	IO_L33N_M3DQ13_3	UNUSED		3								
T2		IOBM	IO_L33P_M3DQ12_3	UNUSED		3								
T3		IOBS	IO_L62N_D6_2	UNUSED		2								
T4		IOBM	IO_L63P_2	UNUSED		2								
T5		IOBS	IO_L48N_RDWR_B_VREF_2	UNUSED		2								
T6		IOBM	IO_L45P_2	UNUSED		2								
T7		IOBS	IO_L46	UNUSE		2								

			N_2	D									
T8		IOBS	IO_L31N_GCLK30_D15_2	UNUSED		2							
T9	SW1	IOB	IO_L32P_GCLK29_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
T10		IOBS	IO_L29N_GCLK2_2	UNUSED		2							
T11		IOBS	IO_L16N_VREF_2	UNUSED		2							
T12		IOBM	IO_L19P_2	UNUSED		2							
T13		IOBS	IO_L3N_MOSI_CSI_B_MISO0_2	UNUSED		2							
T14		IOBM	IO_L12P_D1_MISO2_2	UNUSED		2							
T15		IOBS	IO_L1N_M0_CMPMISO_2	UNUSED		2							
T16			GND										
T17	SEG<6>	IOB	IO_L51P_M1DQ12_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
T18	SEG<5>	IOB	IO_L51N_M1DQ13_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
U1		IOBS	IO_L32N_M3DQ15_3	UNUSED		3							
U2		IOBM	IO_L32P_M3DQ14_3	UNUSED		3							
U3		IOBM	IO_L65P_INIT_B_2	UNUSED		2							
U4			VCCO_2			2					any*****		
U5		IOBM	IO_L49P_D3_2	UNUSED		2							
U6			GND										
U7		IOBM	IO_L43P_2	UNUSED		2							
U8		IOBM	IO_L41P_2	UNUSED		2							
U9			VCCO_2			2					any*****		
U10		IOBM	IO_L30P_GCLK1_D13_2	UNUSED		2							
U11		IOBM	IO_L23P_2	UNUSED		2							

U12			GND											
U13		IOBM	IO_L14P_D11_2	UNUSED		2								
U14			VCCO_2			2					any*****			
U15		IOBM	IO_L5P_2	UNUSED		2								
U16		IOBM	IO_L2P_CMPCLK_2	UNUSED		2								
U17	SEG<4>	IOB	IO_L52P_M1DQ14_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
U18	SEG<3>	IOB	IO_L52N_M1DQ15_1	OUTPUT	LVCMOS33	1	12	SLOW				LOCATED	NO	NONE
V1			GND											
V2			PROGRAM_B_2											
V3		IOBS	IO_L65N_CSO_B_2	UNUSED		2								
V4		IOBS	IO_L63N_2	UNUSED		2								
V5		IOBS	IO_L49N_D4_2	UNUSED		2								
V6		IOBS	IO_L45N_2	UNUSED		2								
V7		IOBS	IO_L43N_2	UNUSED		2								
V8		IOBS	IO_L41N_VREF_2	UNUSED		2								
V9		IOBS	IO_L32N_GCLK28_2	UNUSED		2								
V10	CLK	IOB	IO_L30N_GCLK0_USERCCLK_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
V11		IOBS	IO_L23N_2	UNUSED		2								
V12		IOBS	IO_L19N_2	UNUSED		2								
V13		IOBS	IO_L14N_D12_2	UNUSED		2								
V14		IOBS	IO_L12N_D2_MISO3_2	UNUSED		2								
V15		IOBS	IO_L5N_2	UNUSED		2								
V16		IOBS	IO_L2N_CMPMOSI_2	UNUSED		2								
V17			DONE_2											
V18			GND											