Release 14.3 - xst P.40xd (nt64)

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs
Total CPU time to Xst completion: 0.08 secs

--> Reading design: BCD_vhdl.prj

TABLE OF CONTENTS

===
*   Synthesis Options Summary   *
===
---- Source Parameters
Input File Name   : "BCD_vhdl.prj"
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name   : "BCD_vhdl"
Output Format   : NGC
Target Device   : xc6slx16-3-csg324

---- Source Options
Top Module Name   : BCD_vhdl
Automatic FSM Extraction   : YES
FSM Encoding Algorithm   : Auto
Safe Implementation   : No
FSM Style   : LUT
RAM Extraction   : Yes
RAM Style   : Auto
ROM Extraction   : Yes
Shift Register Extraction   : YES
ROM Style   : Auto

```
Resource Sharing                  : YES
Asynchronous To Synchronous       : NO
Shift Register Minimum Size       : 2
Use DSP Block                     : Auto
Automatic Register Balancing      : No

---- Target Options
LUT Combining                     : Auto
Reduce Control Sets               : Auto
Add IO Buffers                    : YES
Global Maximum Fanout             : 100000
Add Generic Clock Buffer(BUFG)    : 16
Register Duplication              : YES
Optimize Instantiated Primitives  : NO
Use Clock Enable                  : Auto
Use Synchronous Set               : Auto
Use Synchronous Reset             : Auto
Pack IO Registers into IOBs       : Auto
Equivalent register Removal       : YES

---- General Options
Optimization Goal                 : Speed
Optimization Effort               : 1
Power Reduction                   : NO
Keep Hierarchy                    : No
Netlist Hierarchy                 : As_Optimized
RTL Output                        : Yes
Global Optimization               : AllClockNets
Read Cores                        : YES
Write Timing Constraints          : NO
Cross Clock Analysis              : NO
Hierarchy Separator               : /
Bus Delimiter                     : <>
Case Specifier                    : Maintain
Slice Utilization Ratio           : 100
BRAM Utilization Ratio            : 100
DSP48 Utilization Ratio           : 100
Auto BRAM Packing                 : NO
Slice Utilization Ratio Delta     : 5

=========================================================================


=========================================================================
*                          HDL Parsing                                  *
=========================================================================
Parsing VHDL file "C:\Users\ecelab\Desktop\Eri\BCD\BCD_vhdl.vhd" into library work
Parsing entity <BCD_vhdl>.
Parsing architecture <Behavioral> of entity <bcd_vhdl>.

=========================================================================
*                           HDL Elaboration                             *
=========================================================================

Elaborating entity <BCD_vhdl> (architecture <Behavioral>) from library <work>.

=========================================================================
*                          HDL Synthesis                                *
=========================================================================

Synthesizing Unit <BCD_vhdl>.
```

```
    Related source file is "C:\Users\ecelab\Desktop\Eri\BCD\BCD_vhdl.vhd".
    Register <bcd_LastDozen> equivalent to <bcd> has been removed
    Found 4-bit register for signal <unit>.
    Found 4-bit register for signal <bcd>.
    Found 4-bit register for signal <bcd_LastUnit>.
    Found 32-bit register for signal <counter>.
    Found 1-bit register for signal <CLK_mod>.
    Found 4-bit register for signal <dozen>.
    Found 4-bit adder for signal <unit[3]_GND_4_o_add_3_OUT> created at line 1241.
    Found 4-bit adder for signal <dozen[3]_GND_4_o_add_6_OUT> created at line 1241.
    Found 32-bit adder for signal <counter[31]_GND_4_o_add_34_OUT> created at line 110.
    Found 16x8-bit Read Only RAM for signal <C>
    Found 32-bit comparator greater for signal <divide[31]_counter[31]_LessThan_31_o>
created at line 106
    Found 32-bit comparator greater for signal <divide[31]_counter[31]_LessThan_34_o>
created at line 109
WARNING:Xst:2404 -  FFs/Latches <AN<1:2>> (without init value) have a constant value
of 1 in block <BCD_vhdl>.
WARNING:Xst:2404 -  FFs/Latches <AN<2:2>> (without init value) have a constant value
of 0 in block <BCD_vhdl>.
WARNING:Xst:2404 -  FFs/Latches <AN<2:2>> (without init value) have a constant value
of 1 in block <BCD_vhdl>.
    Summary:
        inferred   1 RAM(s).
        inferred   3 Adder/Subtractor(s).
        inferred  49 D-type flip-flop(s).
        inferred   2 Comparator(s).
        inferred   3 Multiplexer(s).
Unit <BCD_vhdl> synthesized.

=========================================================================
HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 16x8-bit single-port Read Only RAM                    : 1
# Adders/Subtractors                                   : 3
 32-bit adder                                          : 1
 4-bit adder                                           : 2
# Registers                                            : 6
 1-bit register                                        : 1
 32-bit register                                       : 1
 4-bit register                                        : 4
# Comparators                                          : 2
 32-bit comparator greater                             : 2
# Multiplexers                                         : 3
 4-bit 2-to-1 multiplexer                              : 3

=========================================================================

=========================================================================
*                      Advanced HDL Synthesis                           *
=========================================================================


Synthesizing (advanced) Unit <BCD_vhdl>.
The following registers are absorbed into counter <counter>: 1 register on signal <counter>.
The following registers are absorbed into counter <dozen>: 1 register on signal <dozen>.
INFO:Xst:3231 - The small RAM <Mram_C> will be implemented on LUTs in order to maximize
performance and save block RAM resources. If you want to force its implementation on
block, use option/constraint ram_style.
```

```
    ----------------------------------------------------------------------
    | ram_type           | Distributed                         |          |
    ----------------------------------------------------------------------
    | Port A                                                              |
    |     aspect ratio   | 16-word x 8-bit                     |          |
    |     weA            | connected to signal <GND>           | high     |
    |     addrA          | connected to signal <bcd>           |          |
    |     diA            | connected to signal <GND>           |          |
    |     doA            | connected to signal <C>             |          |
    ----------------------------------------------------------------------
Unit <BCD_vhdl> synthesized (advanced).

=========================================================================
Advanced HDL Synthesis Report

Macro Statistics
# RAMs                                                 : 1
 16x8-bit single-port distributed Read Only RAM        : 1
# Adders/Subtractors                                   : 1
 4-bit adder                                           : 1
# Counters                                             : 2
 32-bit up counter                                     : 1
 4-bit up counter                                      : 1
# Registers                                            : 13
 Flip-Flops                                            : 13
# Comparators                                          : 2
 32-bit comparator greater                             : 2
# Multiplexers                                         : 2
 4-bit 2-to-1 multiplexer                              : 2

=========================================================================

=========================================================================
*                         Low Level Synthesis                           *
=========================================================================

Optimizing unit <BCD_vhdl> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block BCD_vhdl, actual ratio is 1.

Final Macro Processing ...

=========================================================================
Final Register Report

Macro Statistics
# Registers                                            : 49
 Flip-Flops                                            : 49

=========================================================================

=========================================================================
*                           Partition Report                            *
=========================================================================

Partition Implementation Status
-------------------------------

  No Partitions were found in this design.
```

```
------------------------------

================================================================================
*                            Design Summary                                    *
================================================================================

Top Level Output File Name         : BCD_vhdl.ngc

Primitive and Black Box Usage:
------------------------------
# BELS                             : 186
#      GND                         : 1
#      INV                         : 2
#      LUT1                        : 31
#      LUT2                        : 7
#      LUT3                        : 27
#      LUT4                        : 13
#      LUT5                        : 21
#      LUT6                        : 6
#      MUXCY                       : 45
#      VCC                         : 1
#      XORCY                       : 32
# FlipFlops/Latches                : 49
#      FD                          : 36
#      FDE_1                       : 4
#      FDR                         : 9
# Clock Buffers                    : 1
#      BUFGP                       : 1
# IO Buffers                       : 13
#      IBUF                        : 1
#      OBUF                        : 12

Device utilization summary:
---------------------------

Selected Device : 6slx16csg324-3


Slice Logic Utilization:
 Number of Slice Registers:              49  out of  18224     0%
 Number of Slice LUTs:                  107  out of   9112     1%
    Number used as Logic:               107  out of   9112     1%

Slice Logic Distribution:
 Number of LUT Flip Flop pairs used:    114
   Number with an unused Flip Flop:      65  out of    114    57%
   Number with an unused LUT:             7  out of    114     6%
   Number of fully used LUT-FF pairs:    42  out of    114    36%
   Number of unique control sets:         4

IO Utilization:
 Number of IOs:                         14
 Number of bonded IOBs:                 14  out of    232     6%

Specific Feature Utilization:
 Number of BUFG/BUFGCTRLs:               1  out of     16     6%

---------------------------
Partition Resource Summary:
---------------------------
```

```
  No Partitions were found in this design.

--------------------------


=========================================================================
Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
CLK_mod                            | NONE(bcd_0)            | 16    |
CLK                                | BUFGP                  | 33    |
-----------------------------------+------------------------+-------+
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST
with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these
buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -3

   Minimum period: 5.200ns (Maximum Frequency: 192.308MHz)
   Minimum input arrival time before clock: 3.492ns
   Maximum output required time after clock: 4.849ns
   Maximum combinational path delay: No path found

Timing Details:
---------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'CLK_mod'
  Clock period: 5.200ns (frequency: 192.308MHz)
  Total number of paths / destination ports: 132 / 16
-------------------------------------------------------------------------
Delay:               2.600ns (Levels of Logic = 2)
  Source:            bcd_LastUnit_1 (FF)
  Destination:       unit_1 (FF)
  Source Clock:      CLK_mod falling
  Destination Clock: CLK_mod rising

  Data Path: bcd_LastUnit_1 to unit_1
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDE_1:C->Q            3   0.447   0.898  bcd_LastUnit_1 (bcd_LastUnit_1)
     LUT6:I2->O            6   0.203   0.745  Mcount_dozen_val (Mcount_dozen_val)
     LUT4:I3->O            1   0.205   0.000  dozen_2_rstpot (dozen_2_rstpot)
     FD:D                      0.102          dozen_2
```

```
    ----------------------------------------
    Total                      2.600ns (0.957ns logic, 1.643ns route)
                                       (36.8% logic, 63.2% route)

================================================================================
Timing constraint: Default period analysis for Clock 'CLK'
  Clock period: 4.928ns (frequency: 202.904MHz)
  Total number of paths / destination ports: 4323 / 42
--------------------------------------------------------------------------------
Delay:               4.928ns (Levels of Logic = 8)
  Source:            counter_6 (FF)
  Destination:       counter_23 (FF)
  Source Clock:      CLK rising
  Destination Clock: CLK rising

  Data Path: counter_6 to counter_23
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               5   0.447   1.059  counter_6 (counter_6)
     LUT5:I0->O            1   0.203   0.000
Mcompar_divide[31]_counter[31]_LessThan_31_o_lut<1>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_lut<1>)
     MUXCY:S->O            1   0.172   0.000
Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<1>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<1>)
     MUXCY:CI->O           1   0.019   0.000
Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<2>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<2>)
     MUXCY:CI->O           1   0.019   0.000
Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<3>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<3>)
     MUXCY:CI->O           1   0.019   0.000
Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<4>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<4>)
     MUXCY:CI->O           1   0.019   0.000
Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<5>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<5>)
     MUXCY:CI->O          25   0.213   1.297
Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<6>
(Mcompar_divide[31]_counter[31]_LessThan_31_o_cy<6>)
     LUT2:I0->O            9   0.203   0.829  _n00831 (_n0083)
     FDR:R                     0.430          counter_23
    ----------------------------------------
    Total                      4.928ns (1.744ns logic, 3.184ns route)
                                       (35.4% logic, 64.6% route)

================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'CLK_mod'
  Total number of paths / destination ports: 8 / 8
--------------------------------------------------------------------------------
Offset:              3.492ns (Levels of Logic = 3)
  Source:            CLR (PAD)
  Destination:       unit_1 (FF)
  Destination Clock: CLK_mod rising

  Data Path: CLR to unit_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   1.222   1.015  CLR_IBUF (CLR_IBUF)
```

```
     LUT6:I0->O            6   0.203   0.745  Mcount_dozen_val (Mcount_dozen_val)
     LUT4:I3->O            1   0.205   0.000  dozen_2_rstpot (dozen_2_rstpot)
     FD:D                      0.102          dozen_2
    ----------------------------------------
    Total                      3.492ns (1.732ns logic, 1.760ns route)
                                       (49.6% logic, 50.4% route)

==========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'CLK_mod'
  Total number of paths / destination ports: 28 / 7
--------------------------------------------------------------------------
Offset:              4.849ns (Levels of Logic = 2)
  Source:            bcd_1 (FF)
  Destination:       C<7> (PAD)
  Source Clock:      CLK_mod rising

  Data Path: bcd_1 to C<7>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               8   0.447   1.050  bcd_1 (bcd_1)
     LUT4:I0->O            1   0.203   0.579  Mram_C21 (C_2_OBUF)
     OBUF:I->O                 2.571          C_2_OBUF (C<2>)
    ----------------------------------------
    Total                      4.849ns (3.221ns logic, 1.628ns route)
                                       (66.4% logic, 33.6% route)

==========================================================================

Cross Clock Domains Report:
--------------------------

Clock to Setup on destination clock CLK
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
CLK            |    4.928|         |         |         |
---------------+---------+---------+---------+---------+

Clock to Setup on destination clock CLK_mod
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
CLK            |         |         |    2.684|         |
CLK_mod        |    3.950|    2.600|    1.322|         |
---------------+---------+---------+---------+---------+

==========================================================================


Total REAL time to Xst completion: 6.00 secs
Total CPU time to Xst completion: 5.22 secs

-->

Total memory usage is 266908 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    3 (   0 filtered)
```

Number of infos   :   2 (0 filtered)