```
1
2   # PlanAhead Generated IO constraints
3
4   NET "AN[3]" IOSTANDARD = LVCMOS33;
5   NET "AN[2]" IOSTANDARD = LVCMOS33;
6   NET "AN[1]" IOSTANDARD = LVCMOS33;
7   NET "AN[0]" IOSTANDARD = LVCMOS33;
8   NET "DP" IOSTANDARD = LVCMOS33;
9   NET "SEG[6]" IOSTANDARD = LVCMOS33;
10  NET "SEG[5]" IOSTANDARD = LVCMOS33;
11  NET "SEG[4]" IOSTANDARD = LVCMOS33;
12  NET "SEG[3]" IOSTANDARD = LVCMOS33;
13  NET "SEG[2]" IOSTANDARD = LVCMOS33;
14  NET "SEG[1]" IOSTANDARD = LVCMOS33;
15  NET "SEG[0]" IOSTANDARD = LVCMOS33;
16  NET "CLK" IOSTANDARD = LVCMOS33;
17  NET "PB0" IOSTANDARD = LVCMOS33;
18  NET "SW1" IOSTANDARD = LVCMOS33;
19
20  # PlanAhead Generated physical constraints
21
22  NET "AN[3]" LOC = P17;
23  NET "AN[2]" LOC = P18;
24  NET "AN[1]" LOC = N15;
25  NET "AN[0]" LOC = N16;
26  NET "DP" LOC = M13;
27  NET "SEG[6]" LOC = T17;
28  NET "SEG[5]" LOC = T18;
29  NET "SEG[4]" LOC = U17;
30  NET "SEG[3]" LOC = U18;
31  NET "SEG[2]" LOC = M14;
32  NET "SEG[1]" LOC = N14;
33  NET "SEG[0]" LOC = L14;
34  NET "CLK" LOC = V10;
35  NET "PB0" LOC = B8;
36  NET "SW1" LOC = T9;
37
```