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Release 14.3 Map P.40xd (nt64)
Xilinx Mapping Report File for Design 'BCD_vhdl'

Design Information
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Command Line   : map -intstyle ise -p xc6slx16-csg324-3 -w -logic_opt off -ol
high -t 1 -xt 0 -register_duplication off -r 4 -global_opt off -mt off -ir off
-pr off -lc off -power off -o BCD_vhdl_map.ncd BCD_vhdl.ngd BCD_vhdl.pcf
Target Device  : xc6slx16
Target Package : csg324
Target Speed   : -3
Mapper Version : spartan6 -- $Revision: 1.55 $
Mapped Date    : Wed May 28 14:33:52 2014

Design Summary
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Number of errors:      0
Number of warnings:    0
Slice Logic Utilization:
  Number of Slice Registers:                    49 out of  18,224    1%
    Number used as Flip Flops:                  49
    Number used as Latches:                      0
    Number used as Latch-thrus:                  0
    Number used as AND/OR logics:                0
  Number of Slice LUTs:                         77 out of   9,112    1%
    Number used as logic:                       76 out of   9,112    1%
      Number using O6 output only:              14
      Number using O5 output only:              30
      Number using O5 and O6:                   32
      Number used as ROM:                        0
    Number used as Memory:                       0 out of   2,176    0%
    Number used exclusively as route-thrus:      1
      Number with same-slice register load:      0
      Number with same-slice carry load:         1
      Number with other load:                    0

Slice Logic Distribution:
  Number of occupied Slices:                    24 out of   2,278    1%
  Nummber of MUXCYs used:                       48 out of   4,556    1%
  Number of LUT Flip Flop pairs used:           82
    Number with an unused Flip Flop:            45 out of      82   54%
    Number with an unused LUT:                   5 out of      82    6%
    Number of fully used LUT-FF pairs:          32 out of      82   39%
    Number of unique control sets:               4
    Number of slice register sites lost
      to control set restrictions:              15 out of  18,224    1%

  A LUT Flip Flop pair for this architecture represents one LUT paired with
  one Flip Flop within a slice.  A control set is a unique combination of
  clock, reset, set, and enable signals for a registered element.
  The Slice Logic Distribution report is not meaningful if the design is
  over-mapped for a non-slice resource or if Placement fails.

IO Utilization:
  Number of bonded IOBs:                        14 out of     232    6%
    Number of LOCed IOBs:                       14 out of      14  100%

Specific Feature Utilization:
  Number of RAMB16BWERs:                         0 out of      32    0%
  Number of RAMB8BWERs:                          0 out of      64    0%
  Number of BUFIO2/BUFIO2_2CLKs:                 0 out of      32    0%
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  Number of BUFIO2FB/BUFIO2FB_2CLKs:             0 out of      32    0%
  Number of BUFG/BUFGMUXs:                       1 out of      16    6%
    Number used as BUFGs:                        1
    Number used as BUFGMUX:                      0
  Number of DCM/DCM_CLKGENs:                     0 out of       4    0%
  Number of ILOGIC2/ISERDES2s:                   0 out of     248    0%
  Number of IODELAY2/IODRP2/IODRP2_MCBs:         0 out of     248    0%
  Number of OLOGIC2/OSERDES2s:                   0 out of     248    0%
  Number of BSCANs:                              0 out of       4    0%
  Number of BUFHs:                               0 out of     128    0%
  Number of BUFPLLs:                             0 out of       8    0%
  Number of BUFPLL_MCBs:                         0 out of       4    0%
  Number of DSP48A1s:                            0 out of      32    0%
  Number of ICAPs:                               0 out of       1    0%
  Number of MCBs:                                0 out of       2    0%
  Number of PCILOGICSEs:                         0 out of       2    0%
  Number of PLL_ADVs:                            0 out of       2    0%
  Number of PMVs:                                0 out of       1    0%
  Number of STARTUPs:                            0 out of       1    0%
  Number of SUSPEND_SYNCs:                       0 out of       1    0%

Average Fanout of Non-Clock Nets:                2.61

Peak Memory Usage:  370 MB
Total REAL time to MAP completion:  5 secs
Total CPU time to MAP completion:   4 secs

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Section 1 - Errors
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Section 2 - Warnings
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Section 3 - Informational
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INFO:MapLib:562 - No environment variables are currently set.
INFO:LIT:244 - All of the single ended outputs in this design are using slew
   rate limited output drivers. The delay on speed critical single ended outputs
   can be dramatically reduced by designating them as fast outputs.
INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:
   0.000 to 85.000 Celsius)
INFO:Pack:1720 - Initializing voltage to 1.140 Volts. (default - Range: 1.140 to
   1.260 Volts)
INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report
   (.mrp).
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INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary
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   2 block(s) optimized away

Section 5 - Removed Logic

Optimized Block(s):
TYPE BLOCK
GND XST_GND
VCC XST_VCC

To enable printing of redundant blocks removed and signals merged, set the
detailed map report option and rerun map.

Section 6 - IOB Properties

IOB Name	Type	Direction	IO Standard	Diff Term	Drive Strength	Slew Rate	Reg (s)	Resistor	IOB Delay
AN<0>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<1>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<2>	IOB	OUTPUT	LVCMOS33		12	SLOW			
AN<3>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<0>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<1>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<2>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<3>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<4>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<5>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<6>	IOB	OUTPUT	LVCMOS33		12	SLOW			
C<7>	IOB	OUTPUT	LVCMOS33		12	SLOW			
CLK	IOB	INPUT	LVCMOS33						
CLR	IOB	INPUT	LVCMOS33						

Section 7 - RPMs

Section 8 - Guide Report

Guide not run on this design.

Section 9 - Area Group and Partition Summary

Partition Implementation Status

No Partitions were found in this design.

Area Group Information

No area groups were found in this design.

Section 10 - Timing Report

A logic-level (pre-route) timing report can be generated by using Xilinx static timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the mapped NCD and PCF files. Please note that this timing report will be generated using estimated delay information. For accurate numbers, please generate a timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing Analyzer Reference Manual; for more information about TRCE, consult the Xilinx Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

Use the "-detail" map option to print out the Utilization by Hierarchy section.