BCD_vhdl Project Status (05/28/2014 - 14:34:46)			
Project File:	BCD.xise	**Parser Errors:**	No Errors
Module Name:	BCD_vhdl	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.3	• **Warnings:**	3 Warnings (3 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	49	18,224	1%	
Number used as Flip Flops	49			
Number used as Latches	0			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	77	9,112	1%	
Number used as logic	76	9,112	1%	
Number using O6 output only	14			
Number using O5 output only	30			
Number using O5 and O6	32			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	0			
Number with same-slice carry load	1			
Number with other load	0			
Number of occupied Slices	24	2,278	1%	
Nummber of MUXCYs used	48	4,556	1%	
Number of LUT Flip Flop pairs used	82			
Number with an unused Flip Flop	45	82	54%	
Number with an unused LUT	5	82	6%	
Number of fully used LUT-FF pairs	32	82	39%	
Number of unique control sets	4			
Number of slice register sites lost to control set restrictions	15	18,224	1%	
Number of bonded IOBs	14	232	6%	
Number of LOCed IOBs	14	14	100%	
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			

Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.61			

Performance Summary				[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report	
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report	
Timing Constraints:	All Constraints Met			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed May 28 14:33:29 2014	0	3 Warnings (3 new)	2 Infos (2 new)
Translation Report	Current	Wed May 28 14:33:34 2014	0	0	0
Map Report	Current	Wed May 28 14:33:58 2014	0	0	6 Infos (6 new)
Place and Route Report	Current	Wed May 28 14:34:08 2014	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed May 28 14:34:13 2014	0	0	4 Infos (4 new)
Bitgen Report	Current	Wed May 28 14:34:41 2014	0	0	0

Secondary Reports			[-]
Report Name	**Status**	**Generated**	
WebTalk Report	Current	Wed May 28 14:34:41 2014	
WebTalk Log File	Current	Wed May 28 14:34:46 2014	

Date Generated: 05/28/2014 - 14:34:46