ECE 5510 APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN
SUMMER I 2014

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Web Home Page:	http://homepages.wmich.edu/~grantner/ece5510
Class:	MW 6:30-9:00pm, in C-122, CEAS
Hours:	W 4:30-5:20pm, or by appointment

Course Description

The main objective of this course is to develop skills for designing digital circuits using VHDL and Programmable Logic Devices. The key features of semi-custom and full-custom ASIC devices will also be reviewed. Students are expected to have a background in digital logic design. The two design projects will be based upon Field Programmable Gate Arrays (FPGAs). Students will be designing their circuits in VHDL using professional CAD tools by Xilinx and Mentor Graphics. The subject matter is considered in the required text and the recommended texts. Additional materials will be posted on the Class Home Page. The Data Sheets of those chips that will be referred to in the homework assignments and design projects can be found in the respective manufacturers' Web sites.

Prerequisites by topic: Digital Design and Digital Electronics

Topics to be covered in this course include:

1. Review of the transient behavior of combinational logic and synchronous sequential logic circuits
2. Design of synchronous sequential logic Finite State Machines
3. Introduction to VHDL
4. Contemporary FPGA architectures
5. Digital circuit design with FPGAs using Xilinx and Mentor Graphics tools
6. Introduction to CMOS logic
7. Introduction to Programmable ASICs
8. ASIC construction
9. Floor planning, placement and routing

Required Textbook/Materials

1. *Application-Specific Integrated Circuits* by Michael John Sebastian Smith, Addison-Wesley Professional, 2008, ISBN 0321602757, **required**
2. Data sheets for selected FPGAs, FPGA Development Boards and other components. Students are expected to locate and download the needed information from either the vendor's or the class Web site, or from an on-line library.
3. **Xilinx ISE WebPack (14.7)** and the **ModelSim PE 10.3a Student Edition** software that can be downloaded from the Xilinx and Mentor Graphics Web sites, respectively, free of charge, **required**.

4. **Nexys 3 Spartan 6 FPGA Development Bo**ard by Digilentinc, **required**.

Recommended Textbook/Materials

1. *Digital System Design Using VHDL, Second Edition* by Charles H. Roth, Jr., Thomson Learning, 2008, ISBN 13: 978-0-534-38462-3, **recommended**, but not required, available in the University Bookstore, Bernhard Center
2. *The Student's Guide to VHDL*, by Peter J. Ashenden, Morgan Kaufmann Publishers, Inc., 1998, ISBN 1-55860-520-7, **recommended**, but not required
3. *Advanced Digital Logic Design*, by Sunggu Lee, Thomson, 2006, ISBN: 0-534-46602-8, **recommended**, but not required, available in the University Bookstore, Bernhard Center

Course Procedure

There will be **homework assignments** to work on and **two significant design projects** to be completed. No late homework will be accepted. Homework is **individual** assignment! Projects will be carried on in teams of two students each, or may be worked on individually. Project operational demonstrations must be made to the instructor prior to handing in the written project reports. Project demonstrations and written reports have **firm** due dates for full credit. Projects will be accepted up to **two** business days after due date but will be penalized by the loss of 15% credit for each day late. Failure to successfully complete a project will result in a failing grade for the course. Plagiarism and/or the copying/duplication of another student's homework, or another team's design or written reports will result in zero scores for the homework, or project, respectively, for **all** individuals involved.

If a student has a question regarding grading, he/she **must write a short statement** explaining his/her point and **send the statement via email to the course instructor**. Students will have **5 days** from the time the assignment is returned to do that.

Grading Policy

Grades will be determined on the following basis:

Homework	**30%**
Project 1	**30%**
Project 2	**40%**

It is expected that the breakdown for letter grades will be as follows:
100-92 A, **91-85 BA**, **84-78 B**, **77-71 CB**, **70-64 C**, **63-57 D**, **56 and below E**, missed project X. The boundaries between grades may be individually lowered at the instructor's discretion. In borderline cases, the second project may be given a higher weight, at the instructor's discretion.

Project Due Dates

Project demonstrations will be performed prior to the project due date and time either in class, or in the Microcomputer Lab (Room B-214). Both the demonstrations and the written project reports will be due on:

Project 1	**6:30pm, Wednesday, June 4, 2014**
Project 2	**6:30pm, Wednesday, June 25, 2014**

Permission to miss any due date may be granted by the instructor under extreme circumstances. If permission is desired, a request must be made before the due date and should include either a signed doctor's explanation or a written explanation signed by an appropriate WMU officer.

Codes and Policies

The ECE 5510 Web Home Page will be used as official communications media for the class.

The WMU College of Engineering and Applied Sciences Honesty Code will apply in this course.

You are responsible for making yourself aware of and understanding the policies and procedures in the Graduate Catalog that pertain to Academic Honesty. These policies include cheating, fabrication, falsification and forgery, multiple submission, plagiarism, complicity and computer misuse. The instructor will give you guidance to avoid problems of this kind. If there is reason to believe you have been involved in academic dishonesty, you will be referred to the Office of Student Conduct. You will be given the opportunity to review the charge(s). If you believe you are not responsible, you will have the opportunity for a hearing. You should consult with the course instructor if you are uncertain about an issue of academic honesty prior to the submission of an assignment or test.