Homework Assignment #2

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WESTERN MICHIGAN UNIVERSITY
ECE 5510 APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN
Homework Assignment #2

Task 1:

Construct a **behavioral** VHDL program for **a parity generator** of **7-bit words**. The parity bit (the 8^{th} bit) should be generated such that the **total number of 1s** of the 8-bit word will be an **even number**. Simulate your design and check for functional correctness.

Algorithm of parity generator of 7-bit words

The task of "parity generator of 7-bit words" consists in generate the 8^{th} bit such that the total number of 1s of the 8-bit word will be an even number. To execute this task, we have an input **A** that is a vector with 7 positions and another vector **p** with 8 positions for the output. Therefore, there is an algorithm that counts the number of 1s in the variable A. Then, there is a condition that adds '1' or '0' in the 8^{th} bit to form an even amount of number. I check the number if it is even or odd through modulo operator.

1. *Read the variable A*
2. *Create the variable "count" to count the number of '1s'*
3. *For I in 0 to 6 loop*
4. *If the A(I) = '1' -> count= count +1*
5. *End of loop*
6. *If the modulo of count is equal to 1, add '1' in the* 8^{th}
7. *If the modulo of count is equal to, add '0' in the* 8^{th}
8. *Finally, the vector P is a copy of the vector A, but there will be the last bit with the parity correctly*

Algorithm of parity generator of 7-bits words

For the simulation of this program, I created a file .do to test diverse of differents inputs.

Input	Output
0000000	00000000
0000001	00000011
0110011	01100110
0010100	00101000
0111000	01110001

1000100	10001000
0000001	00000011
1111000	11110000

Table of test

.VHD

parity_vhdl.vhd

```
1   library IEEE;                    -- Declaration of the library
2   use IEEE.STD_LOGIC_1164.ALL;     -- Declaration of the packages
3   use IEEE.NUMERIC_STD.ALL;
4
5   entity parity_vhdl is                          -- partity_vhdl entity
6      port( A  : in  std_logic_vector(6 downto 0); -- Input:  7-but words
7            p  : out std_logic_vector(7 downto 0));                    -- Output:
    parity bit
8   end parity_vhdl;
9
10  architecture Behavioral of parity_vhdl is
11  begin
12     process(A)
13     variable count: integer;   -- Count how many 1s there are
14
15     begin
16     count:=0;
17     for i in 0 to 6 loop
18        p(i+1) <= A(i);
19        if(A(i) = '1') then
20           count:=count+1;
21        end if;
22     end loop;
23
24     if ( (count mod 2) = 1) then  -- It means that the vector is even
25        p(0) <= '1';
26     else                          -- It means that the vector is odd
27        p(0) <= '0';
28     end if;
29
30     end process;
31  end Behavioral;
32
```

Program .vhd

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Simulation

```
#######################################
#     Macro for parity generator      #
#######################################



restart

# Test the wave for the input 0000000
# The answer should be 00000000
force A 0

# Test the wave for the input 0000001
# The answer should be 00000011
run 10ns
force A 2'h1

# Test the wave for the input 0110011
# The answer should be 01100110
run 10ns
force A 2'h33
run 10ns

# Test the wave for the input 0010100
# The answer should be 00101000
force A 2'h14
run 10ns

# Test the wave for the input 0111000
# The answer should be 01110001
force A 2'h38
run 10ns

# Test the wave for the input 1000100
# The answer should be 10001000
force A 2'h44
run 10ns

# Test the wave for the input 0000001
# The answer should be 00000011
force A 2'h1
run 10ns

# Test the wave for the input 1111000
# The answer should be 11110000
force A 2'h78
run 10ns
```

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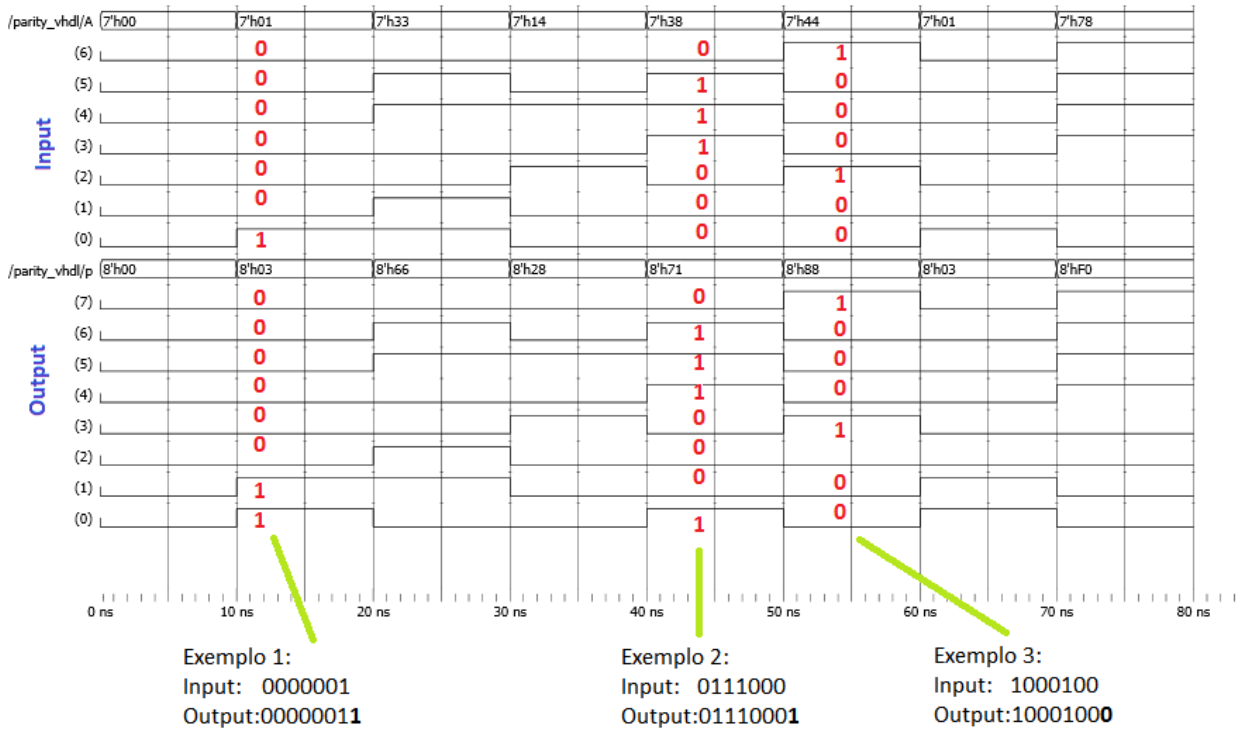
Wave



Some examples of the wave

File .ucf

```
# PlanAhead Generated physical constraints

NET "A[6]" LOC = T10;

# PlanAhead Generated IO constraints

NET "A[6]" IOSTANDARD = LVCMOS33;
NET "A[5]" IOSTANDARD = LVCMOS33;
NET "A[4]" IOSTANDARD = LVCMOS33;
NET "p[7]" IOSTANDARD = LVCMOS33;
NET "p[6]" IOSTANDARD = LVCMOS33;
NET "p[5]" IOSTANDARD = LVCMOS33;
NET "p[4]" IOSTANDARD = LVCMOS33;
NET "p[3]" IOSTANDARD = LVCMOS33;
NET "p[2]" IOSTANDARD = LVCMOS33;
```

```
NET "p[1]" IOSTANDARD = LVCMOS33;
NET "p[0]" IOSTANDARD = LVCMOS33;
NET "A[0]" IOSTANDARD = LVCMOS33;
NET "A[1]" IOSTANDARD = LVCMOS33;
NET "A[2]" IOSTANDARD = LVCMOS33;
NET "A[3]" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "A[5]" LOC = T9;
NET "A[4]" LOC = V9;
NET "A[3]" LOC = M8;
NET "A[2]" LOC = N8;
NET "A[1]" LOC = U8;
NET "A[0]" LOC = V8;
NET "p[7]" LOC = T11;
NET "p[6]" LOC = R11;
NET "p[5]" LOC = N11;
NET "p[4]" LOC = M11;
NET "p[3]" LOC = V15;
NET "p[2]" LOC = U15;
NET "p[1]" LOC = V16;
NET "p[0]" LOC = U16;
```

parity_vhdl Project Status (05/21/2014 - 11:11:34)			
Project File:	parity.xise	**Parser Errors:**	No Errors
Module Name:	parity_vhdl	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.3	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	18,224	0%	
Number of Slice LUTs	2	9,112	1%	
Number used as logic	2	9,112	1%	
Number using O6 output only	2			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	1	2,278	1%	
Nummber of MUXCYs used	0	4,556	0%	
Number of LUT Flip Flop pairs used	2			
Number with an unused Flip Flop	2	2	100%	
Number with an unused LUT	0	2	0%	
Number of fully used LUT-FF pairs	0	2	0%	
Number of slice register sites lost to control set restrictions	0	18,224	0%	
Number of bonded IOBs	15	232	6%	
Number of LOCed IOBs	15	15	100%	
Number of RAMB16BWERs	0	32	0%	

Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	0	16	0%	
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	1.78			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed May 21 11:04:28 2014	0	0	0
Translation Report	Current	Wed May 21 11:07:42 2014	0	0	0

Map Report	Current	Wed May 21 11:07:48 2014	0	0	6 Infos (0 new)
Place and Route Report	Current	Wed May 21 11:07:54 2014	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed May 21 11:07:58 2014	0	0	4 Infos (0 new)
Bitgen Report	Current	Wed May 21 11:11:28 2014	0	0	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Current	Wed May 21 11:05:28 2014
Post-Place and Route Simulation Model Report	Current	Wed May 21 11:09:08 2014
WebTalk Report	Current	Wed May 21 11:11:29 2014
WebTalk Log File	Current	Wed May 21 11:11:34 2014

Date Generated: 05/21/2014 - 12:35:25

Pinout Report - Wed May 21 12:35:52 2014

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank Number	Drive (mA)	Slew Rate	Termination	IOB Delay	Voltage	Constraint	IO Register	Signal Integrity
A1			GND											
A2		IOBS	IO_L2N_0	UNUSED		0								
A3		IOBS	IO_L4N_0	UNUSED		0								
A4		IOBS	IO_L5N_0	UNUSED		0								
A5		IOBS	IO_L6N_0	UNUSED		0								
A6		IOBS	IO_L8N_VREF_0	UNUSED		0								
A7		IOBS	IO_L10N_0	UNUSED		0								
A8		IOBS	IO_L33N_0	UNUSED		0								
A9		IOBS	IO_L35N_GCLK16_0	UNUSED		0								
A10		IOBS	IO_L37N_GCLK12_0	UNUSED		0								
A11		IOBS	IO_L39N_0	UNUSED		0								
A12		IOBS	IO_L41N_0	UNUSED		0								
A13		IOBS	IO_L50N_0	UNUSED		0								
A14		IOBS	IO_L62N_VREF_0	UNUSED		0								
A15		IOBS	IO_L64N_SCP4_0	UNUSED		0								
A16		IOBS	IO_L66N_SCP0_0	UNUSED		0								
A17			TCK											
A18			GND											
B1			VCCAUX								2.5			
B2		IOBM	IO_L2P_0	UNUSED		0								
B3		IOBM	IO_L4P_0	UNUSED		0								
B4		IOBM	IO_L5P_0	UNUSED		0								
B5			VCCO_0			0					any*****			
B6		IOBM	IO_L8P_0	UNUSED		0								
B7			GND											
B8		IOBM	IO_L33	UNUSE		0								

			P_0	D									
B9		IOBM	IO_L35P_GCLK17_0	UNUSED		0							
B10			VCCO_0			0					any*****		
B11		IOBM	IO_L39P_0	UNUSED		0							
B12		IOBM	IO_L41P_0	UNUSED		0							
B13			GND										
B14		IOBM	IO_L62P_0	UNUSED		0							
B15			VCCO_0			0					any*****		
B16		IOBM	IO_L66P_SCP1_0	UNUSED		0							
B17			VCCAUX								2.5		
B18			TMS										
C1		IOBS	IO_L83N_VREF_3	UNUSED		3							
C2		IOBM	IO_L83P_3	UNUSED		3							
C3			GND										
C4		IOBS	IO_L1N_VREF_0	UNUSED		0							
C5		IOBM	IO_L6P_0	UNUSED		0							
C6		IOBS	IO_L3N_0	UNUSED		0							
C7		IOBM	IO_L10P_0	UNUSED		0							
C8		IOBS	IO_L11N_0	UNUSED		0							
C9		IOBS	IO_L34N_GCLK18_0	UNUSED		0							
C10		IOBM	IO_L37P_GCLK13_0	UNUSED		0							
C11		IOBS	IO_L36N_GCLK14_0	UNUSED		0							
C12		IOBS	IO_L47N_0	UNUSED		0							
C13		IOBM	IO_L50P_0	UNUSED		0							
C14		IOBS	IO_L65N_SCP2_0	UNUSED		0							
C15		IOBM	IO_L64P_SCP5_0	UNUSED		0							
C16			GND										
C17		IOBM	IO_L29P_A23_M1A13_	UNUSED		1							

			1										
C18		IOBS	IO_L29N_A22_M1A14_1	UNUSED		1							
D1		IOBS	IO_L52N_M3A9_3	UNUSED		3							
D2		IOBM	IO_L52P_M3A8_3	UNUSED		3							
D3		IOBS	IO_L54N_M3A11_3	UNUSED		3							
D4		IOBM	IO_L1P_HSWAPEN_0	UNUSED		0							
D5			GND										
D6		IOBM	IO_L3P_0	UNUSED		0							
D7			VCCO_0			0					any*****		
D8		IOBM	IO_L11P_0	UNUSED		0							
D9		IOBM	IO_L34P_GCLK19_0	UNUSED		0							
D10			GND										
D11		IOBM	IO_L36P_GCLK15_0	UNUSED		0							
D12		IOBM	IO_L47P_0	UNUSED		0							
D13			VCCO_0			0					any*****		
D14		IOBM	IO_L65P_SCP3_0	UNUSED		0							
D15			TDI										
D16			TDO										
D17		IOBM	IO_L31P_A19_M1CKE_1	UNUSED		1							
D18		IOBS	IO_L31N_A18_M1A12_1	UNUSED		1							
E1		IOBS	IO_L50N_M3BA2_3	UNUSED		3							
E2			VCCO_3			3					any*****		
E3		IOBM	IO_L50P_M3WE_3	UNUSED		3							
E4		IOBM	IO_L54P_M3RESET_3	UNUSED		3							
E5			VCCAUX								2.5		

E6		IOBS	IO_L7N_0	UNUSED		0							
E7		IOBM	IO_L9P_0	UNUSED		0							
E8		IOBS	IO_L9N_0	UNUSED		0							
E9			VCCAUX							2.5			
E10			VCCO_0			0				any*****			
E11		IOBS	IO_L42N_0	UNUSED		0							
E12		IOBS	IO_L51N_0	UNUSED		0							
E13		IOBS	IO_L63N_SCP6_0	UNUSED		0							
E14			VCCAUX							2.5			
E15			GND										
E16		IOBM	IO_L33P_A15_M1A10_1	UNUSED		1							
E17			VCCO_1			1				any*****			
E18		IOBS	IO_L33N_A14_M1A4_1	UNUSED		1							
F1		IOBS	IO_L48N_M3BA1_3	UNUSED		3							
F2		IOBM	IO_L48P_M3BA0_3	UNUSED		3							
F3		IOBS	IO_L51N_M3A4_3	UNUSED		3							
F4		IOBM	IO_L51P_M3A10_3	UNUSED		3							
F5		IOBS	IO_L55N_M3A14_3	UNUSED		3							
F6		IOBM	IO_L55P_M3A13_3	UNUSED		3							
F7		IOBM	IO_L7P_0	UNUSED		0							
F8		IOBS	IO_L32N_0	UNUSED		0							
F9		IOBS	IO_L38N_VREF_0	UNUSED		0							
F10		IOBS	IO_L40N_0	UNUSED		0							
F11		IOBM	IO_L42P_0	UNUSED		0							
F12		IOBM	IO_L51P_0	UNUSED		0							
F13		IOBM	IO_L63P_SCP7	UNUSED		0							

			_0										
F14		IOBM	IO_L30P_A21_M1RESET_1	UNUSED		1							
F15		IOBM	IO_L1P_A25_1	UNUSED		1							
F16		IOBS	IO_L1N_A24_VREF_1	UNUSED		1							
F17		IOBM	IO_L35P_A11_M1A7_1	UNUSED		1							
F18		IOBS	IO_L35N_A10_M1A2_1	UNUSED		1							
G1		IOBS	IO_L46N_M3CLKN_3	UNUSED		3							
G2			GND										
G3		IOBM	IO_L46P_M3CLK_3	UNUSED		3							
G4			VCCO_3			3					any*****		
G5			GND										
G6		IOBS	IO_L53N_M3A12_3	UNUSED		3							
G7			VCCINT								1.2		
G8		IOBM	IO_L32P_0	UNUSED		0							
G9		IOBM	IO_L38P_0	UNUSED		0							
G10			VCCAUX								2.5		
G11		IOBM	IO_L40P_0	UNUSED		0							
G12			GND										
G13		IOBS	IO_L32N_A16_M1A9_1	UNUSED		1							
G14		IOBS	IO_L30N_A20_M1A11_1	UNUSED		1							
G15			VCCO_1			1					any*****		
G16		IOBM	IO_L38P_A5_M1CLK_1	UNUSED		1							
G17			GND										
G18		IOBS	IO_L38N_A4_M1CLKN_1	UNUSED		1							
H1		IOBS	IO_L41N_GCLK26_M3DQ5_3	UNUSED		3							
H2		IOBM	IO_L41	UNUSE		3							

			P_GCLK27_M3DQ4_3	D									
H3		IOBS	IO_L44N_GCLK20_M3A6_3	UNUSED		3							
H4		IOBM	IO_L44P_GCLK21_M3A5_3	UNUSED		3							
H5		IOBS	IO_L49N_M3A2_3	UNUSED		3							
H6		IOBM	IO_L49P_M3A7_3	UNUSED		3							
H7		IOBM	IO_L53P_M3CKE_3	UNUSED		3							
H8			GND										
H9			VCCINT								1.2		
H10			GND										
H11			VCCINT								1.2		
H12		IOBM	IO_L32P_A17_M1A8_1	UNUSED		1							
H13		IOBM	IO_L36P_A9_M1BA0_1	UNUSED		1							
H14		IOBS	IO_L36N_A8_M1BA1_1	UNUSED		1							
H15		IOBM	IO_L37P_A7_M1A0_1	UNUSED		1							
H16		IOBS	IO_L37N_A6_M1A1_1	UNUSED		1							
H17		IOBM	IO_L43P_GCLK5_M1DQ4_1	UNUSED		1							
H18		IOBS	IO_L43N_GCLK4_M1DQ5_1	UNUSED		1							
J1		IOBS	IO_L40N_M3DQ7_3	UNUSED		3							
J2			VCCO_3			3					any*****		
J3		IOBM	IO_L40P_M3DQ6_3	UNUSED		3							
J4			GND										
J5			VCCO_3			3					any*****		
J6		IOBS	IO_L47N_M3A13_3	UNUSED		3							

J7		IOBM	IO_L47P_M3A0_3	UNUSED		3							
J8			VCCINT								1.2		
J9			GND										
J10			VCCINT								1.2		
J11			GND										
J12			VCCAUX								2.5		
J13		IOBM	IO_L39P_M1A3_1	UNUSED		1							
J14			VCCO_1			1					any****		
J15			GND										
J16		IOBM	IO_L44P_A3_M1DQ6_1	UNUSED		1							
J17			VCCO_1			1					any****		
J18		IOBS	IO_L44N_A2_M1DQ7_1	UNUSED		1							
K1		IOBS	IO_L38N_M3DQ3_3	UNUSED		3							
K2		IOBM	IO_L38P_M3DQ2_3	UNUSED		3							
K3		IOBS	IO_L42N_GCLK24_M3LDM_3	UNUSED		3							
K4		IOBM	IO_L42P_GCLK25_TRDY2_M3UDM_3	UNUSED		3							
K5		IOBS	IO_L43N_GCLK22_IRDY2_M3CASN_3	UNUSED		3							
K6		IOBS	IO_L45N_M3ODT_3	UNUSED		3							
K7			VCCAUX								2.5		
K8			GND										
K9			VCCINT								1.2		
K10			GND										
K11			VCCINT								1.2		
K12		IOBM	IO_L34P_A13_M1WE_1	UNUSED		1							
K13		IOBS	IO_L34N_A12_M1BA2_1	UNUSED		1							
K14		IOBS	IO_L39N_M1O	UNUSED		1							

			DT_1											
K15		IOBM	IO_L41P_GCLK9_IRDY1_M1RASN_1	UNUSED		1								
K16		IOBS	IO_L41N_GCLK8_M1CASN_1	UNUSED		1								
K17		IOBM	IO_L45P_A1_M1LDQS_1	UNUSED		1								
K18		IOBS	IO_L45N_A0_M1LDQSN_1	UNUSED		1								
L1		IOBS	IO_L37N_M3DQ1_3	UNUSED		3								
L2		IOBM	IO_L37P_M3DQ0_3	UNUSED		3								
L3		IOBS	IO_L39N_M3LDQSN_3	UNUSED		3								
L4		IOBM	IO_L39P_M3LDQS_3	UNUSED		3								
L5		IOBM	IO_L43P_GCLK23_M3RASN_3	UNUSED		3								
L6		IOBM	IO_L31P_3	UNUSED		3								
L7		IOBM	IO_L45P_M3A3_3	UNUSED		3								
L8			VCCINT								1.2			
L9			GND											
L10			VCCINT								1.2			
L11			GND											
L12		IOBM	IO_L40P_GCLK11_M1A5_1	UNUSED		1								
L13		IOBS	IO_L40N_GCLK10_M1A6_1	UNUSED		1								
L14		IOBM	IO_L61P_1	UNUSED		1								
L15		IOBM	IO_L42P_GCLK7_M1UDM_1	UNUSED		1								
L16		IOBS	IO_L42N_GCLK6_TRDY1_M1LD	UNUSED		1								

			M_1											
L17		IOBM	IO_L46P_FCS_B_M1DQ2_1	UNUSED		1								
L18		IOBS	IO_L46N_FOE_B_M1DQ3_1	UNUSED		1								
M1		IOBS	IO_L36N_M3DQ9_3	UNUSED		3								
M2			GND											
M3		IOBM	IO_L36P_M3DQ8_3	UNUSED		3								
M4			VCCO_3			3					any***			
M5		IOBS	IO_L31N_VREF_3	UNUSED		3								
M6			GND											
M7			VCCINT								1.2			
M8	A<3>	IOB	IO_L40P_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
M9			VCCAUX								2.5			
M10		IOBM	IO_L22P_2	UNUSED		2								
M11	p<4>	IOB	IO_L15P_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
M12			VCCINT								1.2			
M13		IOBS	IO_L61N_1	UNUSED		1								
M14		IOBM	IO_L53P_1	UNUSED		1								
M15			VCCO_1			1					any***			
M16		IOBM	IO_L47P_FWE_B_M1DQ0_1	UNUSED		1								
M17			GND											
M18		IOBS	IO_L47N_LDC_M1DQ1_1	UNUSED		1								
N1		IOBS	IO_L35N_M3DQ11_3	UNUSED		3								
N2		IOBM	IO_L35P_M3DQ10_3	UNUSED		3								
N3		IOBS	IO_L1N_VREF_3	UNUSED		3								
N4		IOBM	IO_L1P_3	UNUSED		3								
N5		IOBM	IO_L64P_D8_2	UNUSED		2								
N6		IOBM	IO_L47	UNUSE		2								

			P_2	D									
N7		IOBM	IO_L44P_2	UNUSED		2							
N8	A<2>	IOB	IO_L40N_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
N9		IOBS	IO_L22N_2	UNUSED		2							
N10		IOBM	IO_L20P_2	UNUSED		2							
N11	p<5>	IOB	IO_L15N_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
N12		IOBM	IO_L13P_M1_2	UNUSED		2							
N13			GND										
N14		IOBS	IO_L53N_VREF_1	UNUSED		1							
N15		IOBM	IO_L50P_M1UDQS_1	UNUSED		1							
N16		IOBS	IO_L50N_M1UDQSN_1	UNUSED		1							
N17		IOBM	IO_L48P_HDC_M1DQ8_1	UNUSED		1							
N18		IOBS	IO_L48N_M1DQ9_1	UNUSED		1							
P1		IOBS	IO_L34N_M3UDQSN_3	UNUSED		3							
P2		IOBM	IO_L34P_M3UDQS_3	UNUSED		3							
P3		IOBS	IO_L2N_3	UNUSED		3							
P4		IOBM	IO_L2P_3	UNUSED		3							
P5			VCCAUX								2.5		
P6		IOBS	IO_L64N_D9_2	UNUSED		2							
P7		IOBS	IO_L47N_2	UNUSED		2							
P8		IOBS	IO_L44N_2	UNUSED		2							
P9			VCCO_2			2					3.30		
P10			VCCAUX								2.5		
P11		IOBS	IO_L20N_2	UNUSED		2							
P12		IOBS	IO_L13N_D10_2	UNUSED		2							
P13			CMPCS_B_2										
P14			VCCAUX								2.5		
P15		IOBM	IO_L74P_AWAKE_1	UNUSED		1							

P16		IOBS	IO_L74N_DOUT_BUSY_1	UNUSED		1							
P17		IOBM	IO_L49P_M1DQ10_1	UNUSED		1							
P18		IOBS	IO_L49N_M1DQ11_1	UNUSED		1							
R1			GND										
R2			VCCO_3			3					any*****			
R3		IOBM	IO_L62P_D5_2	UNUSED		2							
R4			GND										
R5		IOBM	IO_L48P_D7_2	UNUSED		2							
R6			VCCO_2			2					3.30			
R7		IOBM	IO_L46P_2	UNUSED		2							
R8		IOBM	IO_L31P_GCLK31_D14_2	UNUSED		2							
R9			GND										
R10		IOBM	IO_L29P_GCLK3_2	UNUSED		2							
R11	p<6>	IOB	IO_L16P_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
R12			VCCO_2			2					3.30			
R13		IOBM	IO_L3P_D0_DIN_MISO_MISO1_2	UNUSED		2							
R14			GND										
R15		IOBM	IO_L1P_CCLK_2	UNUSED		2							
R16			SUSPEND										
R17			VCCO_1			1					any*****			
R18			GND										
T1		IOBS	IO_L33N_M3DQ13_3	UNUSED		3							
T2		IOBM	IO_L33P_M3DQ12_3	UNUSED		3							
T3		IOBS	IO_L62N_D6_2	UNUSED		2							
T4		IOBM	IO_L63P_2	UNUSED		2							
T5		IOBS	IO_L48N_RDWR_B_VREF_2	UNUSED		2							

T6		IOBM	IO_L45P_2	UNUSED		2							
T7		IOBS	IO_L46N_2	UNUSED		2							
T8		IOBS	IO_L31N_GCLK30_D15_2	UNUSED		2							
T9	A<5>	IOB	IO_L32P_GCLK29_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
T10	A<6>	IOB	IO_L29N_GCLK2_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
T11	p<7>	IOB	IO_L16N_VREF_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
T12		IOBM	IO_L19P_2	UNUSED		2								
T13		IOBS	IO_L3N_MOSI_CSI_B_MISO0_2	UNUSED		2								
T14		IOBM	IO_L12P_D1_MISO2_2	UNUSED		2								
T15		IOBS	IO_L1N_M0_CMPMISO_2	UNUSED		2								
T16			GND											
T17		IOBM	IO_L51P_M1DQ12_1	UNUSED		1								
T18		IOBS	IO_L51N_M1DQ13_1	UNUSED		1								
U1		IOBS	IO_L32N_M3DQ15_3	UNUSED		3								
U2		IOBM	IO_L32P_M3DQ14_3	UNUSED		3								
U3		IOBM	IO_L65P_INIT_B_2	UNUSED		2								
U4			VCCO_2			2					3.30			
U5		IOBM	IO_L49P_D3_2	UNUSED		2								
U6			GND											
U7		IOBM	IO_L43P_2	UNUSED		2								
U8	A<1>	IOB	IO_L41P_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
U9			VCCO_2			2					3.30			
U10		IOBM	IO_L30P_GCLK1_D13_2	UNUSED		2								
U11		IOBM	IO_L23	UNUSE		2								

			P_2	D										
U12			GND											
U13		IOBM	IO_L14P_D11_2	UNUSED		2								
U14			VCCO_2			2					3.30			
U15	p<2>	IOB	IO_L5P_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
U16	p<0>	IOB	IO_L2P_CMPCLK_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
U17		IOBM	IO_L52P_M1DQ14_1	UNUSED		1								
U18		IOBS	IO_L52N_M1DQ15_1	UNUSED		1								
V1			GND											
V2			PROGRAM_B_2											
V3		IOBS	IO_L65N_CSO_B_2	UNUSED		2								
V4		IOBS	IO_L63N_2	UNUSED		2								
V5		IOBS	IO_L49N_D4_2	UNUSED		2								
V6		IOBS	IO_L45N_2	UNUSED		2								
V7		IOBS	IO_L43N_2	UNUSED		2								
V8	A<0>	IOB	IO_L41N_VREF_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
V9	A<4>	IOB	IO_L32N_GCLK28_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
V10		IOBS	IO_L30N_GCLK0_USERCCLK_2	UNUSED		2								
V11		IOBS	IO_L23N_2	UNUSED		2								
V12		IOBS	IO_L19N_2	UNUSED		2								
V13		IOBS	IO_L14N_D12_2	UNUSED		2								
V14		IOBS	IO_L12N_D2_MISO3_2	UNUSED		2								
V15	p<3>	IOB	IO_L5N_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
V16	p<1>	IOB	IO_L2N_CMPMOSI_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	NO	NONE
V17			DONE_2											
V18			GND											

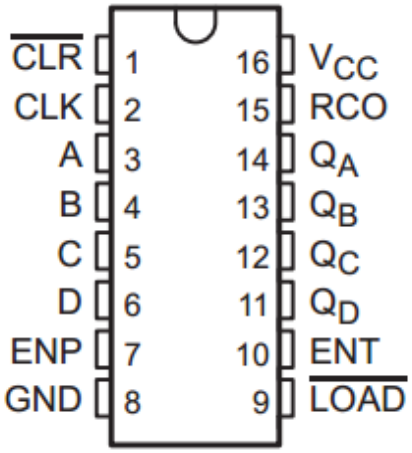
WESTERN MICHIGAN UNIVERSITY
ECE 5510 APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN
Homework Assignment #2

Task 2:

Download the Data Sheets of the **SN74ALS163 Synchronous 4-Bit Binary Counter** from Texas Instruments' Web site. Use the available **CAD tools to design, simulate and compile a functionally** equivalent circuit on your **Xilinx Spartan-6 chip**. However, downloading the bit file to your Nexys 3 Board is **NOT** required.

Algorithm of SN74ALS163 Synchronous 4-Bit Binary Counter

The task elaborates the functionally equivalent circuit of SN74ALS163 Synchronous 4-Bit Binary Counter. To execute this task, we have some inputs and outputs. Look the figure below.



SN74ALS163

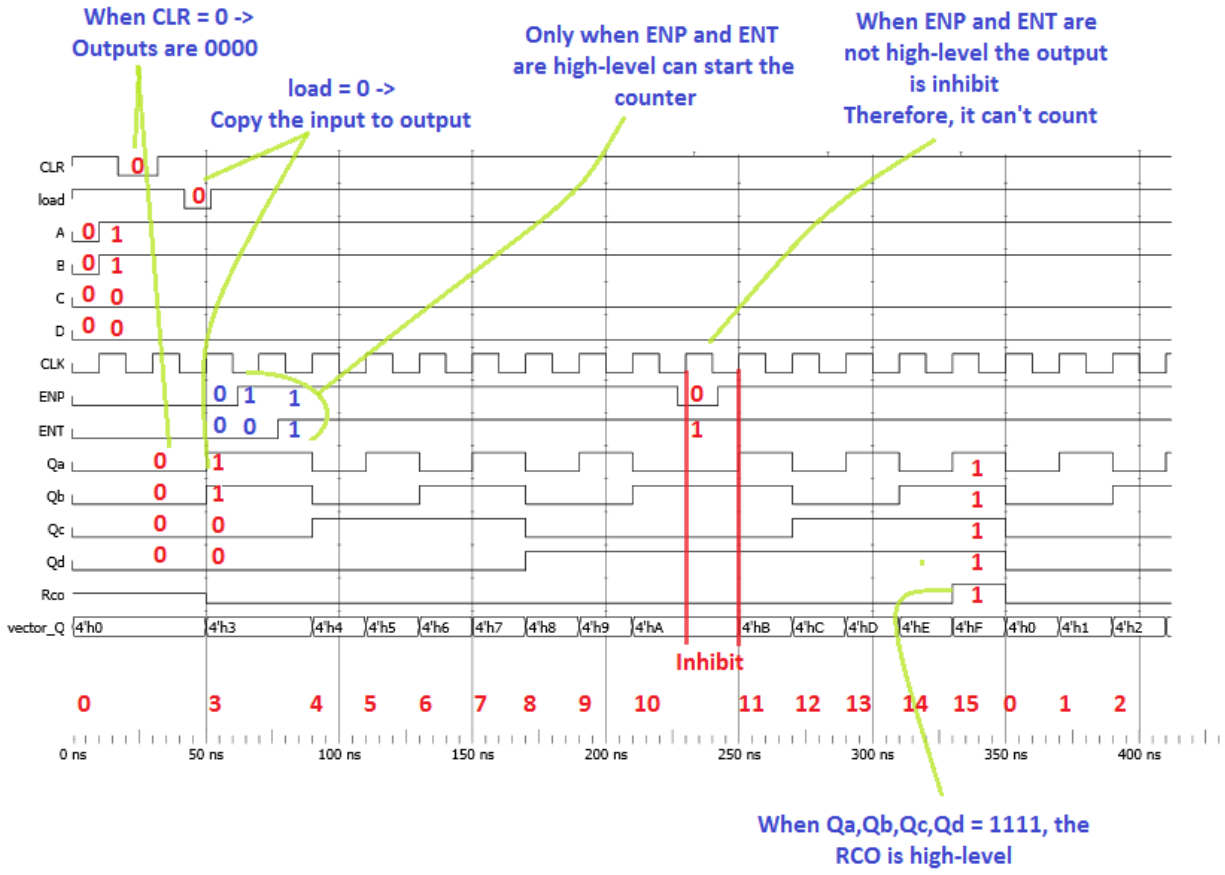
The counter can be present to any number between 0 and 15. Furthermore, it can start with any number between these numbers. It is possible because we can set up a low level at the load (LOAD). Consequently, the initial count will be the value in the input A, B, C, D. The CLR input when active in low can clear the count to 0000. Also, we have the inputs ENP and ENT that are conditional to count because both must be high to count and ENT is a conditional to enable RCO. RCO, always produces a high-level pulse while the count is 15.

I developed a finite state machine to reproduce the functionally equivalent circuit of SN74ALS163. To test the operation, I created a file .do to test the correct operation.

- I checked the CLR. When it is the low-level, the output must be 0000;
- I checked the LOAD. When the load is in the low-level, the input: A, B, C, and D is copied to the output: Qa, Qb, Qc, and Qd.
- I checked the RCO because it should be high-level when the output is 1111 = "15".
- I checked the inputs: ENP and ENT because the counter just can work when the ENP and ENT if high-level. In case it doesn't happen, the output cannot change.
- Finally, checked the all counter states.

Simulation - Wave

Look the wave below:



WESTERN MICHIGAN UNIVERSITY
ECE 5510 APPLICATION SPECIFIC INTEGRATED CIRCUIT DESIGN
Homework Assignment #2

File .vhd

Counter_vhdl.vhd

```
1
2   library IEEE;
3   use IEEE.STD_LOGIC_1164.ALL;
4
5   entity Counter_vhdl is
6      port( A, B, C, D  : in std_logic;
7            ENP         : in std_logic;
8            ENT         : in std_logic;
9            CLR         : in std_logic;
10           CLK         : in std_logic;
11           load        : in std_logic;
12           Rco         : out std_logic;
13           Qa, Qb, Qc, Qd : out std_logic);
14  end Counter_vhdl;
15
16  architecture Behavioral of Counter_vhdl is
17     type state_type is (start, load_in, clear, s0, s1, s2, s3, s4, s5, s6, s7, s8,
    s9, s10, s11, s12, s13, s14, s15);
18     signal present_state, next_state: state_type := start; --initial state idle
19     signal vector   : std_logic_vector( 3 downto 0 );
20     signal vector_Q : std_logic_vector( 3 downto 0 );
21  begin
22
23  Load_abcd: process(A, B, C, D)
24  begin
25     vector(0)<=A;
26     vector(1)<=B;
27     vector(2)<=C;
28     vector(3)<=D;
29  end process Load_abcd;
30
31  count_process: process(present_state, load, ENP, ENT, CLR, vector)
32  begin
33     case present_state is
34     when start =>
35        if (load = '0' and CLR = '1') then
36           if (vector = "0000") then     -- 0
37              next_state <= s0;
38           elsif (vector = "0001") then  -- 1
39              next_state <= s1;
40           elsif (vector = "0010") then  -- 2
41              next_state <= s2;
42           elsif (vector = "0011") then  -- 3
43              next_state <= s3;
44           elsif (vector = "0100") then  -- 4
45              next_state <= s4;
46           elsif (vector = "0101") then  -- 5
47              next_state <= s5;
48           elsif (vector = "0110") then  -- 6
49              next_state <= s6;
50           elsif (vector = "0111") then  -- 7
51              next_state <= s7;
52           elsif (vector = "1000") then  -- 8
53              next_state <= s8;
54           elsif (vector = "1001") then  -- 9
```

Counter_vhdl.vhd

```
55                next_state <= s9;
56             elsif (vector = "1010") then  -- 10
57                next_state <= s10;
58             elsif (vector = "1011") then  -- 11
59                next_state <= s11;
60             elsif (vector = "1100") then  -- 12
61                next_state <= s12;
62             elsif (vector = "1101") then  -- 13
63                next_state <= s13;
64             elsif (vector = "1110") then  -- 14
65                next_state <= s14;
66             elsif (vector = "1111") then  -- 15
67                next_state <= s15;
68             end if;
69          else
70             vector_Q <= "0000";
71          end if;
72       when load_in =>
73       when clear =>
74       when s0 =>
75          vector_Q <= "0000";
76          Rco <= '0';
77          if (ENP = '1' and ENT = '1' ) then
78             next_state <= s1;
79          else
80             next_state <= s0;
81          end if;
82       when s1 =>
83          vector_Q <= "0001";
84          Rco <= '0';
85          if (ENP = '1' and ENT = '1') then
86             next_state <= s2;
87          else
88             next_state <= s1;
89          end if;
90       when s2 =>
91          vector_Q <= "0010";
92          Rco <= '0';
93          if (ENP = '1' and ENT = '1') then
94             next_state <= s3;
95          else
96             next_state <= s2;
97          end if;
98       when s3 =>
99          vector_Q <= "0011";
100         Rco <= '0';
101         if (ENP = '1' and ENT = '1') then
102            next_state <= s4;
103         else
104            next_state <= s3;
105         end if;
106      when s4 =>
107         vector_Q <= "0100";
108         Rco <= '0';
109         if (ENP = '1' and ENT = '1') then
```

Counter_vhdl.vhd

```
110             next_state <= s5;
111          else
112             next_state <= s4;
113          end if;
114       when s5 =>
115          vector_Q <= "0101";
116          Rco <= '0';
117          if (ENP = '1' and ENT = '1') then
118             next_state <= s6;
119          else
120             next_state <= s5;
121          end if;
122       when s6 =>
123          vector_Q <= "0110";
124          Rco <= '0';
125          if (ENP = '1' and ENT = '1') then
126             next_state <= s7;
127          else
128             next_state <= s6;
129          end if;
130       when s7 =>
131          vector_Q <= "0111";
132          Rco <= '0';
133          if (ENP = '1' and ENT = '1') then
134             next_state <= s8;
135          else
136             next_state <= s7;
137          end if;
138       when s8 =>
139          vector_Q <= "1000";
140          Rco <= '0';
141          if (ENP = '1' and ENT = '1') then
142             next_state <= s9;
143          else
144             next_state <= s8;
145          end if;
146       when s9 =>
147          vector_Q <= "1001";
148          Rco <= '0';
149          if (ENP = '1' and ENT = '1') then
150             next_state <= s10;
151          else
152             next_state <= s9;
153          end if;
154       when s10 =>
155          vector_Q <= "1010";
156          Rco <= '0';
157          if (ENP = '1' and ENT = '1') then
158             next_state <= s11;
159          else
160             next_state <= s10;
161          end if;
162       when s11 =>
163          vector_Q <= "1011";
164          Rco <= '0';
```

Counter_vhdl.vhd

```
165         if (ENP = '1' and ENT = '1') then
166            next_state <= s12;
167         else
168            next_state <= s11;
169         end if;
170      when s12 =>
171         vector_Q <= "1100";
172         Rco <= '0';
173         if (ENP = '1' and ENT = '1') then
174            next_state <= s13;
175         else
176            next_state <= s12;
177         end if;
178      when s13 =>
179         vector_Q <= "1101";
180         Rco <= '0';
181         if (ENP = '1' and ENT = '1') then
182            next_state <= s14;
183         else
184            next_state <= s13;
185         end if;
186      when s14 =>
187         vector_Q <= "1110";
188         Rco <= '0';
189         if (ENP = '1' and ENT = '1') then
190            next_state <= s15;
191         else
192            next_state <= s14;
193         end if;
194      when s15 =>
195         vector_Q <= "1111";
196         Rco <= '1';
197         if (ENP = '1' and ENT = '1') then
198            next_state <= s0;
199         else
200            next_state <= s15;
201         end if;
202      end case;
203   end process count_process;
204
205   Q_process: process(vector_Q)
206   begin
207      Qa <= vector_Q(0);
208      Qb <= vector_Q(1);
209      Qc <= vector_Q(2);
210      Qd <= vector_Q(3);
211   end process Q_process;
212
213   clk_process: process(CLK)
214   begin
215      --wait until (CLK'event and CLK = '1'); --wait until the rising edge
216      if (CLK'event and CLK = '1') then
217         if (CLR = '0') then
218            present_state <= start;
219         else
```

Counter_vhdl.vhd

```
220             present_state <= next_state;
221           end if;
222         end if;
223     end process clk_process;
224
225     end Behavioral;
226
227
```

Simulation: File .do

```
#####################################
#          Macro for the SN7ALS163          #
#####################################
restart
# Generates de clock with T = 20ns
force CLK 0 0, 1 10ns -r 20ns

# Initial Information
force A 0
force B 0
force C 0
force D 0
force ENP 0
force ENT 0
force load 1
force CLR 1
# Initial condition for A, B, C, D
run 10ns
force A 1
force B 1
force C 0
force D 0
# Clear test
run 7ns
force CLR 0
run 15ns
force CLR 1

# Load of the initial condition
run 10ns
force load 0
run 10ns
force load 1
# Test of the inputs ENP and ENT
run 10ns
force ENP 1
run 15ns
force ENT 1
```

 # Maintain the count

run 150ns

Test the Inhibit

force ENP 0

run 15ns

force ENP 1

run 170ns

File .ucf

```
# PlanAhead Generated physical constraints

NET "A" LOC = T10;

# PlanAhead Generated IO constraints

NET "A" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "B" LOC = T9;

# PlanAhead Generated IO constraints

NET "B" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "C" LOC = V9;

# PlanAhead Generated IO constraints

NET "C" IOSTANDARD = LVCMOS33;
NET "CLK" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "CLR" LOC = M8;
NET "D" LOC = N8;
NET "ENP" LOC = U8;
NET "ENT" LOC = V8;
```

```
NET "load" LOC = T5;

# PlanAhead Generated IO constraints

NET "load" IOSTANDARD = LVCMOS33;
NET "ENP" IOSTANDARD = LVCMOS33;
NET "ENT" IOSTANDARD = LVCMOS33;
NET "D" IOSTANDARD = LVCMOS33;
NET "CLR" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "Qa" LOC = U16;
NET "Qb" LOC = V16;

# PlanAhead Generated IO constraints

NET "Qa" IOSTANDARD = LVCMOS33;
NET "Qb" IOSTANDARD = LVCMOS33;
NET "Qc" IOSTANDARD = LVCMOS33;
NET "Qd" IOSTANDARD = LVCMOS33;
NET "Rco" IOSTANDARD = LVCMOS33;

# PlanAhead Generated physical constraints

NET "Qc" LOC = U15;
NET "Qd" LOC = V15;
NET "Rco" LOC = M11;
NET "CLK" LOC = C9;
```

Counter_vhdl Project Status (05/21/2014 - 12:56:47)			
Project File:	SN74ALS163.xise	**Parser Errors:**	No Errors
Module Name:	Counter_vhdl	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.3	• **Warnings:**	13 Warnings (13 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	10	18,224	1%	
Number used as Flip Flops	5			
Number used as Latches	5			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	19	9,112	1%	
Number used as logic	18	9,112	1%	
Number using O6 output only	12			
Number using O5 output only	0			
Number using O5 and O6	6			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	1			
Number with same-slice carry load	0			
Number with other load	0			
Number of occupied Slices	8	2,278	1%	
Nummber of MUXCYs used	0	4,556	0%	

Number of LUT Flip Flop pairs used	22			
Number with an unused Flip Flop	13	22	59%	
Number with an unused LUT	3	22	13%	
Number of fully used LUT-FF pairs	6	22	27%	
Number of unique control sets	2			
Number of slice register sites lost to control set restrictions	6	18,224	1%	
Number of bonded IOBs	14	232	6%	
Number of LOCed IOBs	14	14	100%	
IOB Latches	5			
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	5	248	2%	
Number used as OLOGIC2s	5			
Number used as OSERDES2s	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	

Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.80			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed May 21 12:47:52 2014	0	10 Warnings (10 new)	2 Infos (2 new)
Translation Report	Current	Wed May 21 12:56:29 2014	0	0	0
Map Report	Current	Wed May 21 12:56:35 2014	0	3 Warnings (3 new)	6 Infos (6 new)
Place and Route Report	Current	Wed May 21 12:56:41 2014	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed May 21 12:56:46 2014	0	0	4 Infos (4 new)
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Current	Wed May 21 12:47:54 2014

Date Generated: 05/21/2014 - 12:56:47

Pinout Report - Wed May 21 12:57:21 2014

Pin Number	Signal Name	Pin Usage	Pin Name	Direction	IO Standard	IO Bank Number	Drive (mA)	Slew Rate	Termination	IOB Delay	Voltage	Constraint	IO Register	Signal Integrity
A1			GND											
A2		IOBS	IO_L2N_0	UNUSED		0								
A3		IOBS	IO_L4N_0	UNUSED		0								
A4		IOBS	IO_L5N_0	UNUSED		0								
A5		IOBS	IO_L6N_0	UNUSED		0								
A6		IOBS	IO_L8N_VREF_0	UNUSED		0								
A7		IOBS	IO_L10N_0	UNUSED		0								
A8		IOBS	IO_L33N_0	UNUSED		0								
A9		IOBS	IO_L35N_GCLK16_0	UNUSED		0								
A10		IOBS	IO_L37N_GCLK12_0	UNUSED		0								
A11		IOBS	IO_L39N_0	UNUSED		0								
A12		IOBS	IO_L41N_0	UNUSED		0								
A13		IOBS	IO_L50N_0	UNUSED		0								
A14		IOBS	IO_L62N_VREF_0	UNUSED		0								
A15		IOBS	IO_L64N_SCP4_0	UNUSED		0								
A16		IOBS	IO_L66N_SCP0_0	UNUSED		0								
A17			TCK											
A18			GND											
B1			VCCAUX								2.5			
B2		IOBM	IO_L2P_0	UNUSED		0								
B3		IOBM	IO_L4P_0	UNUSED		0								
B4		IOBM	IO_L5P_0	UNUSED		0								
B5			VCCO_0			0					any*****			
B6		IOBM	IO_L8P_0	UNUSED		0								
B7			GND											
B8		IOBM	IO_L33	UNUSE		0								

			P_0	D										
B9		IOBM	IO_L35P_GCLK17_0	UNUSED		0								
B10			VCCO_0			0					any*****			
B11		IOBM	IO_L39P_0	UNUSED		0								
B12		IOBM	IO_L41P_0	UNUSED		0								
B13			GND											
B14		IOBM	IO_L62P_0	UNUSED		0								
B15			VCCO_0			0					any*****			
B16		IOBM	IO_L66P_SCP1_0	UNUSED		0								
B17			VCCAUX								2.5			
B18			TMS											
C1		IOBS	IO_L83N_VREF_3	UNUSED		3								
C2		IOBM	IO_L83P_3	UNUSED		3								
C3			GND											
C4		IOBS	IO_L1N_VREF_0	UNUSED		0								
C5		IOBM	IO_L6P_0	UNUSED		0								
C6		IOBS	IO_L3N_0	UNUSED		0								
C7		IOBM	IO_L10P_0	UNUSED		0								
C8		IOBS	IO_L11N_0	UNUSED		0								
C9	CLK	IOB	IO_L34N_GCLK18_0	INPUT	LVCMOS33	0				NONE		LOCATED	NO	NONE
C10		IOBM	IO_L37P_GCLK13_0	UNUSED		0								
C11		IOBS	IO_L36N_GCLK14_0	UNUSED		0								
C12		IOBS	IO_L47N_0	UNUSED		0								
C13		IOBM	IO_L50P_0	UNUSED		0								
C14		IOBS	IO_L65N_SCP2_0	UNUSED		0								
C15		IOBM	IO_L64P_SCP5_0	UNUSED		0								
C16			GND											
C17		IOBM	IO_L29P_A23_M1A13_	UNUSED		1								

			1										
C18		IOBS	IO_L29N_A22_M1A14_1	UNUSED		1							
D1		IOBS	IO_L52N_M3A9_3	UNUSED		3							
D2		IOBM	IO_L52P_M3A8_3	UNUSED		3							
D3		IOBS	IO_L54N_M3A11_3	UNUSED		3							
D4		IOBM	IO_L1P_HSWAPEN_0	UNUSED		0							
D5			GND										
D6		IOBM	IO_L3P_0	UNUSED		0							
D7			VCCO_0			0					any*****		
D8		IOBM	IO_L11P_0	UNUSED		0							
D9		IOBM	IO_L34P_GCLK19_0	UNUSED		0							
D10			GND										
D11		IOBM	IO_L36P_GCLK15_0	UNUSED		0							
D12		IOBM	IO_L47P_0	UNUSED		0							
D13			VCCO_0			0					any*****		
D14		IOBM	IO_L65P_SCP3_0	UNUSED		0							
D15			TDI										
D16			TDO										
D17		IOBM	IO_L31P_A19_M1CKE_1	UNUSED		1							
D18		IOBS	IO_L31N_A18_M1A12_1	UNUSED		1							
E1		IOBS	IO_L50N_M3BA2_3	UNUSED		3							
E2			VCCO_3			3					any*****		
E3		IOBM	IO_L50P_M3WE_3	UNUSED		3							
E4		IOBM	IO_L54P_M3RESET_3	UNUSED		3							
E5			VCCAUX								2.5		

E6		IOBS	IO_L7N_0	UNUSED		0							
E7		IOBM	IO_L9P_0	UNUSED		0							
E8		IOBS	IO_L9N_0	UNUSED		0							
E9			VCCAUX							2.5			
E10			VCCO_0			0				any*****			
E11		IOBS	IO_L42N_0	UNUSED		0							
E12		IOBS	IO_L51N_0	UNUSED		0							
E13		IOBS	IO_L63N_SCP6_0	UNUSED		0							
E14			VCCAUX							2.5			
E15			GND										
E16		IOBM	IO_L33P_A15_M1A10_1	UNUSED		1							
E17			VCCO_1			1				any*****			
E18		IOBS	IO_L33N_A14_M1A4_1	UNUSED		1							
F1		IOBS	IO_L48N_M3BA1_3	UNUSED		3							
F2		IOBM	IO_L48P_M3BA0_3	UNUSED		3							
F3		IOBS	IO_L51N_M3A4_3	UNUSED		3							
F4		IOBM	IO_L51P_M3A10_3	UNUSED		3							
F5		IOBS	IO_L55N_M3A14_3	UNUSED		3							
F6		IOBM	IO_L55P_M3A13_3	UNUSED		3							
F7		IOBM	IO_L7P_0	UNUSED		0							
F8		IOBS	IO_L32N_0	UNUSED		0							
F9		IOBS	IO_L38N_VREF_0	UNUSED		0							
F10		IOBS	IO_L40N_0	UNUSED		0							
F11		IOBM	IO_L42P_0	UNUSED		0							
F12		IOBM	IO_L51P_0	UNUSED		0							
F13		IOBM	IO_L63P_SCP7	UNUSED		0							

			_0										
F14		IOBM	IO_L30P_A21_M1RESET_1	UNUSED		1							
F15		IOBM	IO_L1P_A25_1	UNUSED		1							
F16		IOBS	IO_L1N_A24_VREF_1	UNUSED		1							
F17		IOBM	IO_L35P_A11_M1A7_1	UNUSED		1							
F18		IOBS	IO_L35N_A10_M1A2_1	UNUSED		1							
G1		IOBS	IO_L46N_M3CLKN_3	UNUSED		3							
G2			GND										
G3		IOBM	IO_L46P_M3CLK_3	UNUSED		3							
G4			VCCO_3			3					any*****		
G5			GND										
G6		IOBS	IO_L53N_M3A12_3	UNUSED		3							
G7			VCCINT								1.2		
G8		IOBM	IO_L32P_0	UNUSED		0							
G9		IOBM	IO_L38P_0	UNUSED		0							
G10			VCCAUX								2.5		
G11		IOBM	IO_L40P_0	UNUSED		0							
G12			GND										
G13		IOBS	IO_L32N_A16_M1A9_1	UNUSED		1							
G14		IOBS	IO_L30N_A20_M1A11_1	UNUSED		1							
G15			VCCO_1			1					any*****		
G16		IOBM	IO_L38P_A5_M1CLK_1	UNUSED		1							
G17			GND										
G18		IOBS	IO_L38N_A4_M1CLKN_1	UNUSED		1							
H1		IOBS	IO_L41N_GCLK26_M3DQ5_3	UNUSED		3							
H2		IOBM	IO_L41	UNUSE		3							

			P_GCLK27_M3DQ4_3	D									
H3		IOBS	IO_L44N_GCLK20_M3A6_3	UNUSED		3							
H4		IOBM	IO_L44P_GCLK21_M3A5_3	UNUSED		3							
H5		IOBS	IO_L49N_M3A2_3	UNUSED		3							
H6		IOBM	IO_L49P_M3A7_3	UNUSED		3							
H7		IOBM	IO_L53P_M3CKE_3	UNUSED		3							
H8			GND										
H9			VCCINT								1.2		
H10			GND										
H11			VCCINT								1.2		
H12		IOBM	IO_L32P_A17_M1A8_1	UNUSED		1							
H13		IOBM	IO_L36P_A9_M1BA0_1	UNUSED		1							
H14		IOBS	IO_L36N_A8_M1BA1_1	UNUSED		1							
H15		IOBM	IO_L37P_A7_M1A0_1	UNUSED		1							
H16		IOBS	IO_L37N_A6_M1A1_1	UNUSED		1							
H17		IOBM	IO_L43P_GCLK5_M1DQ4_1	UNUSED		1							
H18		IOBS	IO_L43N_GCLK4_M1DQ5_1	UNUSED		1							
J1		IOBS	IO_L40N_M3DQ7_3	UNUSED		3							
J2			VCCO_3			3					any*****		
J3		IOBM	IO_L40P_M3DQ6_3	UNUSED		3							
J4			GND										
J5			VCCO_3			3					any*****		
J6		IOBS	IO_L47N_M3A13_3	UNUSED		3							

J7		IOBM	IO_L47P_M3A0_3	UNUSED		3							
J8			VCCINT								1.2		
J9			GND										
J10			VCCINT								1.2		
J11			GND										
J12			VCCAUX								2.5		
J13		IOBM	IO_L39P_M1A3_1	UNUSED		1							
J14			VCCO_1			1					any****		
J15			GND										
J16		IOBM	IO_L44P_A3_M1DQ6_1	UNUSED		1							
J17			VCCO_1			1					any****		
J18		IOBS	IO_L44N_A2_M1DQ7_1	UNUSED		1							
K1		IOBS	IO_L38N_M3DQ3_3	UNUSED		3							
K2		IOBM	IO_L38P_M3DQ2_3	UNUSED		3							
K3		IOBS	IO_L42N_GCLK24_M3LDM_3	UNUSED		3							
K4		IOBM	IO_L42P_GCLK25_TRDY2_M3UDM_3	UNUSED		3							
K5		IOBS	IO_L43N_GCLK22_IRDY2_M3CASN_3	UNUSED		3							
K6		IOBS	IO_L45N_M3ODT_3	UNUSED		3							
K7			VCCAUX								2.5		
K8			GND										
K9			VCCINT								1.2		
K10			GND										
K11			VCCINT								1.2		
K12		IOBM	IO_L34P_A13_M1WE_1	UNUSED		1							
K13		IOBS	IO_L34N_A12_M1BA2_1	UNUSED		1							
K14		IOBS	IO_L39N_M1O	UNUSED		1							

			DT_1											
K15		IOBM	IO_L41P_GCLK9_IRDY1_M1RASN_1	UNUSED		1								
K16		IOBS	IO_L41N_GCLK8_M1CASN_1	UNUSED		1								
K17		IOBM	IO_L45P_A1_M1LDQS_1	UNUSED		1								
K18		IOBS	IO_L45N_A0_M1LDQSN_1	UNUSED		1								
L1		IOBS	IO_L37N_M3DQ1_3	UNUSED		3								
L2		IOBM	IO_L37P_M3DQ0_3	UNUSED		3								
L3		IOBS	IO_L39N_M3LDQSN_3	UNUSED		3								
L4		IOBM	IO_L39P_M3LDQS_3	UNUSED		3								
L5		IOBM	IO_L43P_GCLK23_M3RASN_3	UNUSED		3								
L6		IOBM	IO_L31P_3	UNUSED		3								
L7		IOBM	IO_L45P_M3A3_3	UNUSED		3								
L8			VCCINT								1.2			
L9			GND											
L10			VCCINT								1.2			
L11			GND											
L12		IOBM	IO_L40P_GCLK11_M1A5_1	UNUSED		1								
L13		IOBS	IO_L40N_GCLK10_M1A6_1	UNUSED		1								
L14		IOBM	IO_L61P_1	UNUSED		1								
L15		IOBM	IO_L42P_GCLK7_M1UDM_1	UNUSED		1								
L16		IOBS	IO_L42N_GCLK6_TRDY1_M1LD	UNUSED		1								

			M_1											
L17		IOBM	IO_L46P_FCS_B_M1DQ2_1	UNUSED		1								
L18		IOBS	IO_L46N_FOE_B_M1DQ3_1	UNUSED		1								
M1		IOBS	IO_L36N_M3DQ9_3	UNUSED		3								
M2			GND											
M3		IOBM	IO_L36P_M3DQ8_3	UNUSED		3								
M4			VCCO_3			3					any***			
M5		IOBS	IO_L31N_VREF_3	UNUSED		3								
M6			GND											
M7			VCCINT								1.2			
M8	CLR	IOB	IO_L40P_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
M9			VCCAUX								2.5			
M10		IOBM	IO_L22P_2	UNUSED		2								
M11	Rco	IOB	IO_L15P_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	YES	NONE
M12			VCCINT								1.2			
M13		IOBS	IO_L61N_1	UNUSED		1								
M14		IOBM	IO_L53P_1	UNUSED		1								
M15			VCCO_1			1					any***			
M16		IOBM	IO_L47P_FWE_B_M1DQ0_1	UNUSED		1								
M17			GND											
M18		IOBS	IO_L47N_LDC_M1DQ1_1	UNUSED		1								
N1		IOBS	IO_L35N_M3DQ11_3	UNUSED		3								
N2		IOBM	IO_L35P_M3DQ10_3	UNUSED		3								
N3		IOBS	IO_L1N_VREF_3	UNUSED		3								
N4		IOBM	IO_L1P_3	UNUSED		3								
N5		IOBM	IO_L64P_D8_2	UNUSED		2								
N6		IOBM	IO_L47	UNUSE		2								

			P_2	D										
N7		IOBM	IO_L44P_2	UNUSED		2								
N8	D	IOB	IO_L40N_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
N9		IOBS	IO_L22N_2	UNUSED		2								
N10		IOBM	IO_L20P_2	UNUSED		2								
N11		IOBS	IO_L15N_2	UNUSED		2								
N12		IOBM	IO_L13P_M1_2	UNUSED		2								
N13			GND											
N14		IOBS	IO_L53N_VREF_1	UNUSED		1								
N15		IOBM	IO_L50P_M1UDQS_1	UNUSED		1								
N16		IOBS	IO_L50N_M1UDQSN_1	UNUSED		1								
N17		IOBM	IO_L48P_HDC_M1DQ8_1	UNUSED		1								
N18		IOBS	IO_L48N_M1DQ9_1	UNUSED		1								
P1		IOBS	IO_L34N_M3UDQSN_3	UNUSED		3								
P2		IOBM	IO_L34P_M3UDQS_3	UNUSED		3								
P3		IOBS	IO_L2N_3	UNUSED		3								
P4		IOBM	IO_L2P_3	UNUSED		3								
P5			VCCAUX								2.5			
P6		IOBS	IO_L64N_D9_2	UNUSED		2								
P7		IOBS	IO_L47N_2	UNUSED		2								
P8		IOBS	IO_L44N_2	UNUSED		2								
P9			VCCO_2			2					3.30			
P10			VCCAUX								2.5			
P11		IOBS	IO_L20N_2	UNUSED		2								
P12		IOBS	IO_L13N_D10_2	UNUSED		2								
P13			CMPCS_B_2											
P14			VCCAUX								2.5			
P15		IOBM	IO_L74P_AWAKE_1	UNUSED		1								

P16		IOBS	IO_L74N_DOUT_BUSY_1	UNUSED		1								
P17		IOBM	IO_L49P_M1DQ10_1	UNUSED		1								
P18		IOBS	IO_L49N_M1DQ11_1	UNUSED		1								
R1			GND											
R2			VCCO_3			3					any*****			
R3		IOBM	IO_L62P_D5_2	UNUSED		2								
R4			GND											
R5		IOBM	IO_L48P_D7_2	UNUSED		2								
R6			VCCO_2			2					3.30			
R7		IOBM	IO_L46P_2	UNUSED		2								
R8		IOBM	IO_L31P_GCLK31_D14_2	UNUSED		2								
R9			GND											
R10		IOBM	IO_L29P_GCLK3_2	UNUSED		2								
R11		IOBM	IO_L16P_2	UNUSED		2								
R12			VCCO_2			2					3.30			
R13		IOBM	IO_L3P_D0_DIN_MISO_MISO1_2	UNUSED		2								
R14			GND											
R15		IOBM	IO_L1P_CCLK_2	UNUSED		2								
R16			SUSPEND											
R17			VCCO_1			1					any*****			
R18			GND											
T1		IOBS	IO_L33N_M3DQ13_3	UNUSED		3								
T2		IOBM	IO_L33P_M3DQ12_3	UNUSED		3								
T3		IOBS	IO_L62N_D6_2	UNUSED		2								
T4		IOBM	IO_L63P_2	UNUSED		2								
T5	load	IOB	IO_L48N_RDWR_B_VREF_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE

T6		IOBM	IO_L45P_2	UNUSED		2							
T7		IOBS	IO_L46N_2	UNUSED		2							
T8		IOBS	IO_L31N_GCLK30_D15_2	UNUSED		2							
T9	B	IOB	IO_L32P_GCLK29_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
T10	A	IOB	IO_L29N_GCLK2_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
T11		IOBS	IO_L16N_VREF_2	UNUSED		2							
T12		IOBM	IO_L19P_2	UNUSED		2							
T13		IOBS	IO_L3N_MOSI_CSI_B_MISO0_2	UNUSED		2							
T14		IOBM	IO_L12P_D1_MISO2_2	UNUSED		2							
T15		IOBS	IO_L1N_M0_CMPMISO_2	UNUSED		2							
T16			GND										
T17		IOBM	IO_L51P_M1DQ12_1	UNUSED		1							
T18		IOBS	IO_L51N_M1DQ13_1	UNUSED		1							
U1		IOBS	IO_L32N_M3DQ15_3	UNUSED		3							
U2		IOBM	IO_L32P_M3DQ14_3	UNUSED		3							
U3		IOBM	IO_L65P_INIT_B_2	UNUSED		2							
U4			VCCO_2			2					3.30		
U5		IOBM	IO_L49P_D3_2	UNUSED		2							
U6			GND										
U7		IOBM	IO_L43P_2	UNUSED		2							
U8	ENP	IOB	IO_L41P_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
U9			VCCO_2			2					3.30		
U10		IOBM	IO_L30P_GCLK1_D13_2	UNUSED		2							
U11		IOBM	IO_L23	UNUSE		2							

			P_2	D										
U12			GND											
U13		IOBM	IO_L14P_D11_2	UNUSED		2								
U14			VCCO_2			2					3.30			
U15	Qc	IOB	IO_L5P_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	YES	NONE
U16	Qa	IOB	IO_L2P_CMPCLK_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	YES	NONE
U17		IOBM	IO_L52P_M1DQ14_1	UNUSED		1								
U18		IOBS	IO_L52N_M1DQ15_1	UNUSED		1								
V1			GND											
V2			PROGRAM_B_2											
V3		IOBS	IO_L65N_CSO_B_2	UNUSED		2								
V4		IOBS	IO_L63N_2	UNUSED		2								
V5		IOBS	IO_L49N_D4_2	UNUSED		2								
V6		IOBS	IO_L45N_2	UNUSED		2								
V7		IOBS	IO_L43N_2	UNUSED		2								
V8	ENT	IOB	IO_L41N_VREF_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
V9	C	IOB	IO_L32N_GCLK28_2	INPUT	LVCMOS33	2				NONE		LOCATED	NO	NONE
V10		IOBS	IO_L30N_GCLK0_USERCCLK_2	UNUSED		2								
V11		IOBS	IO_L23N_2	UNUSED		2								
V12		IOBS	IO_L19N_2	UNUSED		2								
V13		IOBS	IO_L14N_D12_2	UNUSED		2								
V14		IOBS	IO_L12N_D2_MISO3_2	UNUSED		2								
V15	Qd	IOB	IO_L5N_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	YES	NONE
V16	Qb	IOB	IO_L2N_CMPMOSI_2	OUTPUT	LVCMOS33	2	12	SLOW				LOCATED	YES	NONE
V17			DONE_2											
V18			GND											