Counter_vhdl Project Status (05/21/2014 - 12:56:47)			
Project File:	SN74ALS163.xise	**Parser Errors:**	No Errors
Module Name:	Counter_vhdl	**Implementation State:**	Placed and Routed
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.3	• **Warnings:**	13 Warnings (13 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	10	18,224	1%	
Number used as Flip Flops	5			
Number used as Latches	5			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	19	9,112	1%	
Number used as logic	18	9,112	1%	
Number using O6 output only	12			
Number using O5 output only	0			
Number using O5 and O6	6			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number used exclusively as route-thrus	1			
Number with same-slice register load	1			
Number with same-slice carry load	0			
Number with other load	0			
Number of occupied Slices	8	2,278	1%	
Nummber of MUXCYs used	0	4,556	0%	

Number of LUT Flip Flop pairs used	22			
Number with an unused Flip Flop	13	22	59%	
Number with an unused LUT	3	22	13%	
Number of fully used LUT-FF pairs	6	22	27%	
Number of unique control sets	2			
Number of slice register sites lost to control set restrictions	6	18,224	1%	
Number of bonded IOBs	14	232	6%	
Number of LOCed IOBs	14	14	100%	
IOB Latches	5			
Number of RAMB16BWERs	0	32	0%	
Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	1	16	6%	
Number used as BUFGs	1			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	5	248	2%	
Number used as OLOGIC2s	5			
Number used as OSERDES2s	0			
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	

Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.80			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed May 21 12:47:52 2014	0	10 Warnings (10 new)	2 Infos (2 new)
Translation Report	Current	Wed May 21 12:56:29 2014	0	0	0
Map Report	Current	Wed May 21 12:56:35 2014	0	3 Warnings (3 new)	6 Infos (6 new)
Place and Route Report	Current	Wed May 21 12:56:41 2014	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed May 21 12:56:46 2014	0	0	4 Infos (4 new)
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Current	Wed May 21 12:47:54 2014

Date Generated: 05/21/2014 - 12:56:47