parity_vhdl Project Status (05/21/2014 - 11:11:34)			
Project File:	parity.xise	**Parser Errors:**	No Errors
Module Name:	parity_vhdl	**Implementation State:**	Programming File Generated
Target Device:	xc6slx16-3csg324	• **Errors:**	No Errors
Product Version:	ISE 14.3	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				[-]
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	0	18,224	0%	
Number of Slice LUTs	2	9,112	1%	
Number used as logic	2	9,112	1%	
Number using O6 output only	2			
Number using O5 output only	0			
Number using O5 and O6	0			
Number used as ROM	0			
Number used as Memory	0	2,176	0%	
Number of occupied Slices	1	2,278	1%	
Nummber of MUXCYs used	0	4,556	0%	
Number of LUT Flip Flop pairs used	2			
Number with an unused Flip Flop	2	2	100%	
Number with an unused LUT	0	2	0%	
Number of fully used LUT-FF pairs	0	2	0%	
Number of slice register sites lost to control set restrictions	0	18,224	0%	
Number of bonded IOBs	15	232	6%	
Number of LOCed IOBs	15	15	100%	
Number of RAMB16BWERs	0	32	0%	

Number of RAMB8BWERs	0	64	0%	
Number of BUFIO2/BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	0	16	0%	
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	248	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	248	0%	
Number of OLOGIC2/OSERDES2s	0	248	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	32	0%	
Number of ICAPs	0	1	0%	
Number of MCBs	0	2	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	1.78			

Performance Summary			[-]
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:			

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Wed May 21 11:04:28 2014	0	0	0
Translation Report	Current	Wed May 21 11:07:42 2014	0	0	0

Map Report	Current	Wed May 21 11:07:48 2014	0	0	6 Infos (0 new)
Place and Route Report	Current	Wed May 21 11:07:54 2014	0	0	2 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	Wed May 21 11:07:58 2014	0	0	4 Infos (0 new)
Bitgen Report	Current	Wed May 21 11:11:28 2014	0	0	0

Secondary Reports		[-]
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Current	Wed May 21 11:05:28 2014
Post-Place and Route Simulation Model Report	Current	Wed May 21 11:09:08 2014
WebTalk Report	Current	Wed May 21 11:11:29 2014
WebTalk Log File	Current	Wed May 21 11:11:34 2014

Date Generated: 05/21/2014 - 12:35:25