CS224
Lab No: 6
Section No: 5
Erkin Aydın
ID: 22002956
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Part 1)

No.	Cache Size KB	N way cache	Word Size (no. of bits)	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	64	1	32	4	4,096	16	12	2	2	No
2	64	2	32	4	2,048	17	11	2	2	Yes
3	64	4	32	8	512	18	9	3	2	Yes
4	64	Full	32	8	1	27	0	3	2	Yes
5	128	1	16	4	16,384	14	14	2	1	No
6	128	2	16	4	8,192	15	13	2	1	Yes
7	128	4	16	16	1,024	16	10	4	1	Yes
8	128	Full	16	16	1	26	0	4	1	Yes

Part 2)

a.

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x24($0)	Compulsory	Conflict	Conflict	Conflict	Conflict
lw $t2, 0xAC($0)	Compulsory	Conflict	Conflict	Conflict	Conflict
lw $t3, 0xC8($0)	Conflict	Conflict	Conflict	Conflict	Conflict

b. In this part, it is assumed that no block replacement policy is implemented, thus, for example, no U-bit exists.

Number of Words(There are 2-ways, 2 sets in each, and each set contains 4 words): 16
A Word Size: 32-bits
Total Word Bits: 32 x 16 = 512-bits

Number of Tags(There are 2-ways, 2 sets in each, and each set contains 1 tag): 4
A Tag Size: 27-bits
Total Tag Bits: 27 x 4 = 108-bits

Total V Bits: 4

Total Bits = Total V Bits + Total Tag Bits + Total Word Bits = 624-bits.

c.

Number of AND Gates: 2
Number of OR Gates: 1
Number of EQUALITY COMPARATORs: 2
Number of MULTIPLEXERs: 3

Part 3)

a.

Instruction	Iteration No.				
	1	**2**	**3**	**4**	**5**
lw $t1, 0x24($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xAC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xC8($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b.

Each word is 32-bits, and we have 2 blocks in total, where the block size is 1 word. Thus,
Total Word Bits: 32 x 2 = 64-bits

Our Tag size is 30-bits, and since we have 2-ways in this cache,
Total Tag Bits: 30 x 2 = 60-bits

Our valid bit, V, size is 1-bit, and since we have 2-ways in this cache,
Total Valid Bits: 2 x 1 = 2-bits

We need only one bit for LRU policy, that is, U-bit.
Total U Bits : 1-bit

Total Bit Number: Total Word Bits + Total Tag Bits + Total Valid Bits + Total U Bits = 127-bits

c.

Number of AND Gates: 2
Number of OR Gates: 1
Number of EQUALITY COMPARATORs: 2
Number of MULTIPLEXERs: 1

Part 4)
AMAT Calculation:
2 + 0.1(4 + 0.05 x 20) = 2 + 0.4 + 0.05 x 2 = 2.5 clock cycles.

CPU Time Calculation:
CPU Time: I * CPI * T
I: 10^{10}
CPI: 2.5 clock cycles
T: 2GHz = $2x10^{-9}s$
CPU Time = $10^{10}x2.5x2x10^{-9}s = 50\,seconds$