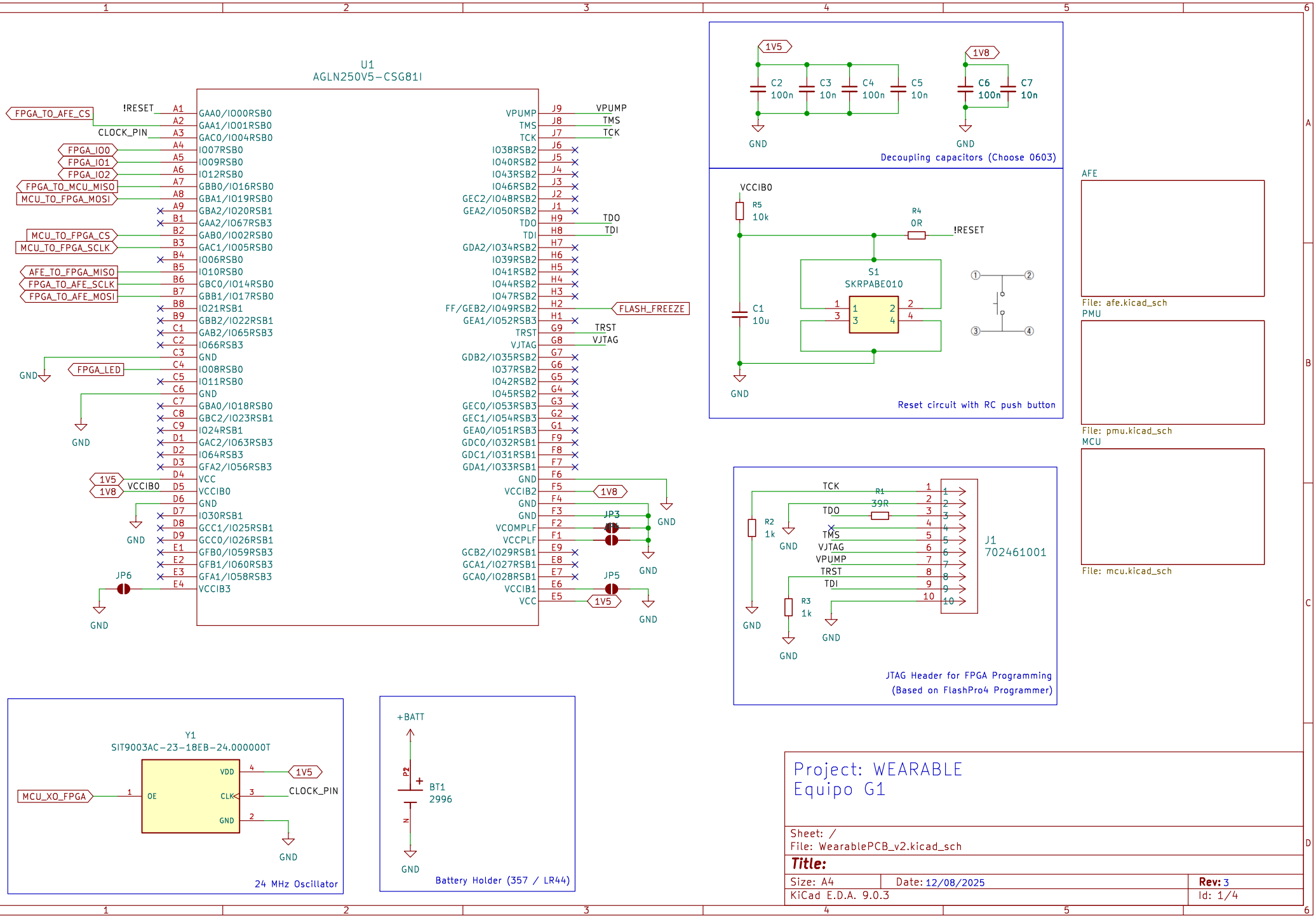
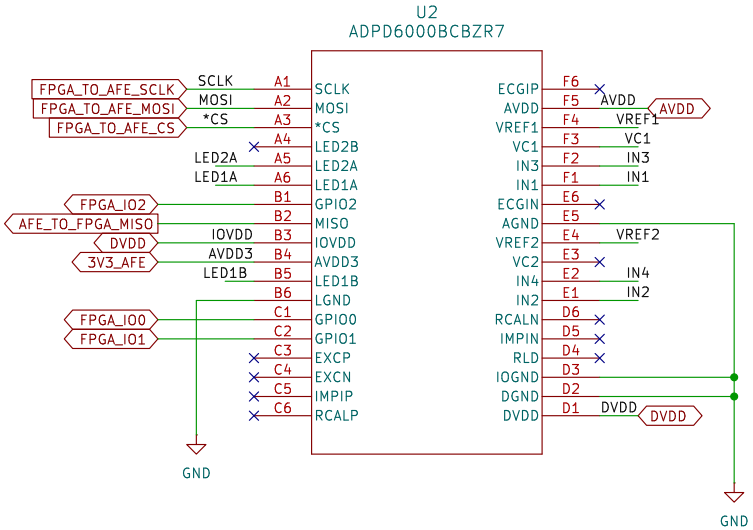
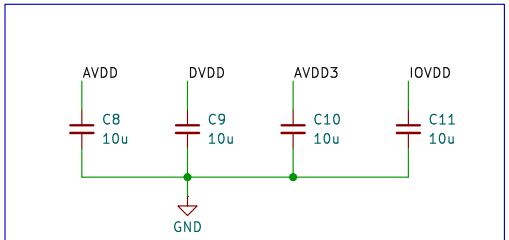

U1
AGLN250V5-CSG81I
FPGA_TO_AFE_CS
!RESET
CLOCK_PIN
FPGA_IO0
FPGA_IO1
FPGA_IO2
FPGA_TO_MCU_MISO
MCU_TO_FPGA_MOSI
MCU_TO_FPGA_CS
MCU_TO_FPGA_SCLK
AFE_TO_FPGA_MISO
FPGA_TO_AFE_SCLK
FPGA_TO_AFE_MOSI
FPGA_LED
GND
1V5
1V8
VCCIB0
JP6
VPUMP
TMS
TCK
TDO
TDI
FLASH_FREEZE
TRST
VJTAG
JP3
JP5
1V5
1V8
GND
Decoupling capacitors (Choose 0603)
C2 100n
C3 10n
C4 100n
C5 10n
C6 100n
C7 10n
VCCIB0
R5 10k
R4 0R
!RESET
S1
SKRPABE010
C1 10u
Reset circuit with RC push button
AFE
File: afe.kicad_sch
PMU
File: pmu.kicad_sch
MCU
File: mcu.kicad_sch
TCK
TDO
TMS
VJTAG
VPUMP
TRST
TDI
R1 39R
R2 1k
R3 1k
J1
702461001
JTAG Header for FPGA Programming
(Based on FlashPro4 Programmer)
Y1
SIT9003AC-23-18EB-24.000000T
MCU_XO_FPGA
OE
VDD
CLK
CLOCK_PIN
24 MHz Oscillator
+BATT
BT1
2996
Battery Holder (357 / LR44)
Project: WEARABLE
Equipo G1
Sheet: /
File: WearablePCB_v2.kicad_sch
Title:
Size: A4
Date: 12/08/2025
Rev: 3
KiCad E.D.A. 9.0.3
Id: 1/4

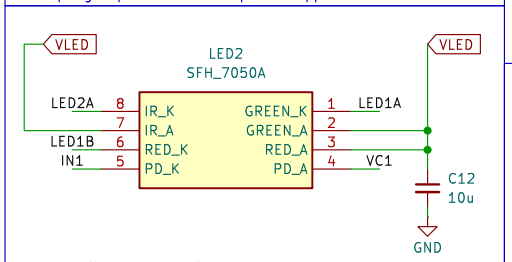
LEDxA and LEDxB are the LEDs cathodes pin. We can drive up to 2 LEDs simultaneously (one for each driver pair).



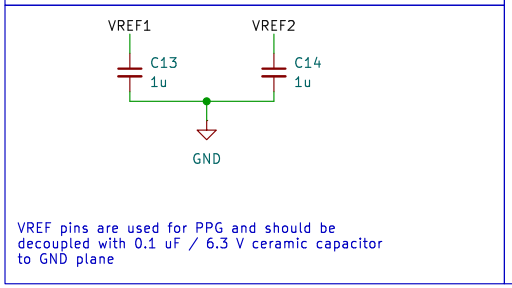
The critical part of the PCB design for the AFE is how to handle IN1–IN4 nodes. This is where the photodiode output is going to enter the AFE. Therefore, the traces have to be carefully placed and also shortened, since parasitic coupling is going to add noise. Also, keep everything away from digital signals. Guard using ground plan



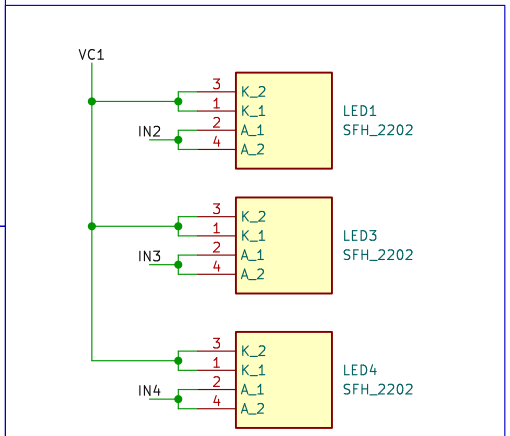
Decoupling capacitors for the power supplies



LED Hub (IR, Green, Red) + 1 Photodiode



VREF pins are used for PPG and should be decoupled with 0.1 uF / 6.3 V ceramic capacitor to GND plane



3 Photodiodes

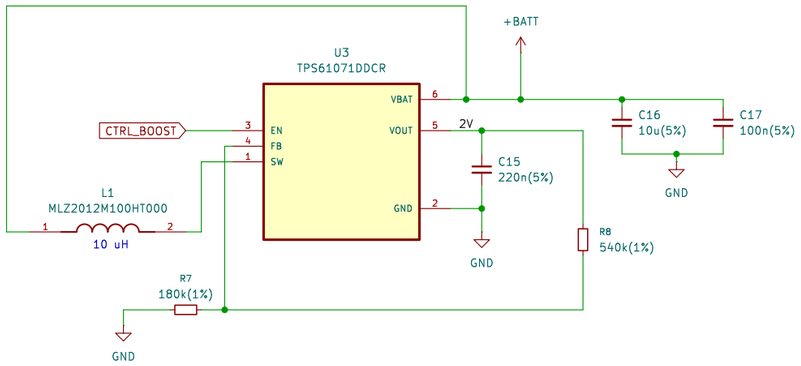
VC1 and VC2 are output voltage sources for photodiode common cathode bias.

Project: WEARABLE
Equipo G1 – AFE Schematic

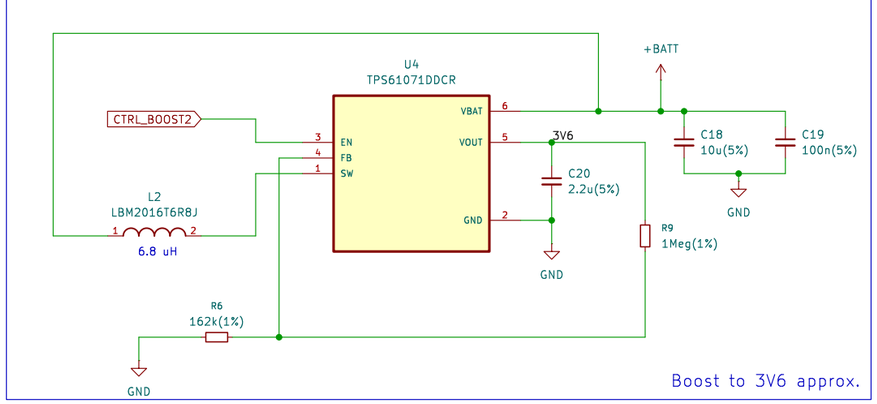
Sheet: /AFE/
File: afe.kicad_sch

Title:

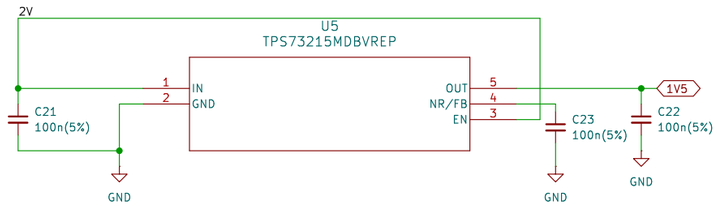
Size: A4	Date: 12/08/2025	**Rev:** 3
KiCad E.D.A. 9.0.3		Id: 2/4



Boost to 2V approx.

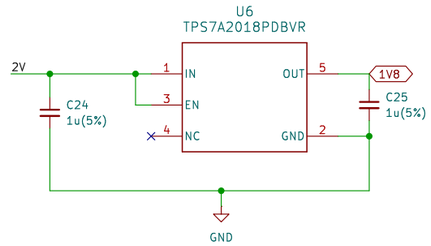


Boost to 3V6 approx.



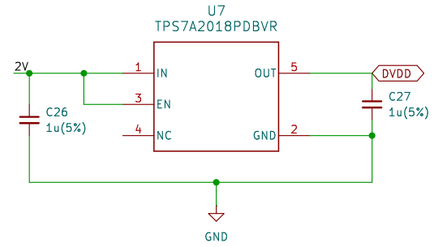
Regulation to 1.5 V (FPGA Core)
Use Low ESR Capacitors

The regulator has an internal pull-down resistor that will drive low the enable signal when the potential on the EN pin is lower than 0.9 V



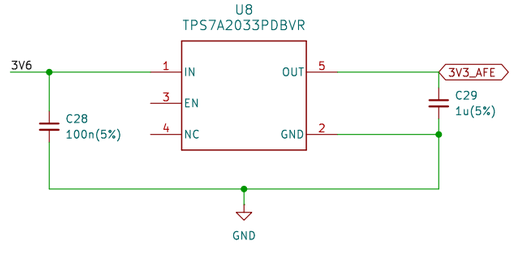
Goes to I/Os and MCU
Regulation to 1.8 V (FPGA Banks -> I/Os and MCU core)

The regulator has an internal pull-down resistor that will drive low the enable signal when the potential on the EN pin is lower than 0.9 V

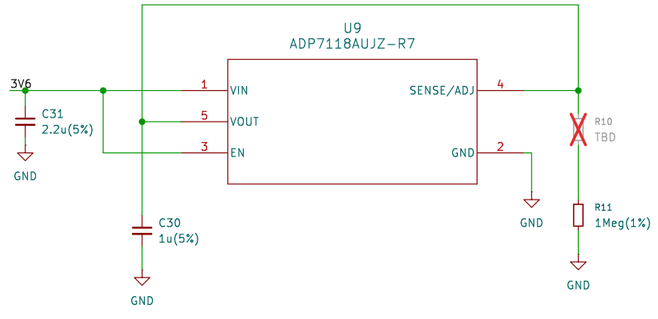


Regulation to 1.8 V (I/Os and digital supply for AFE)

The regulator has an internal pull-down resistor that will drive low the enable signal when the potential on the EN pin is lower than 0.9 V



Regulation to 3.3 V (AFE 3V3 Supply)



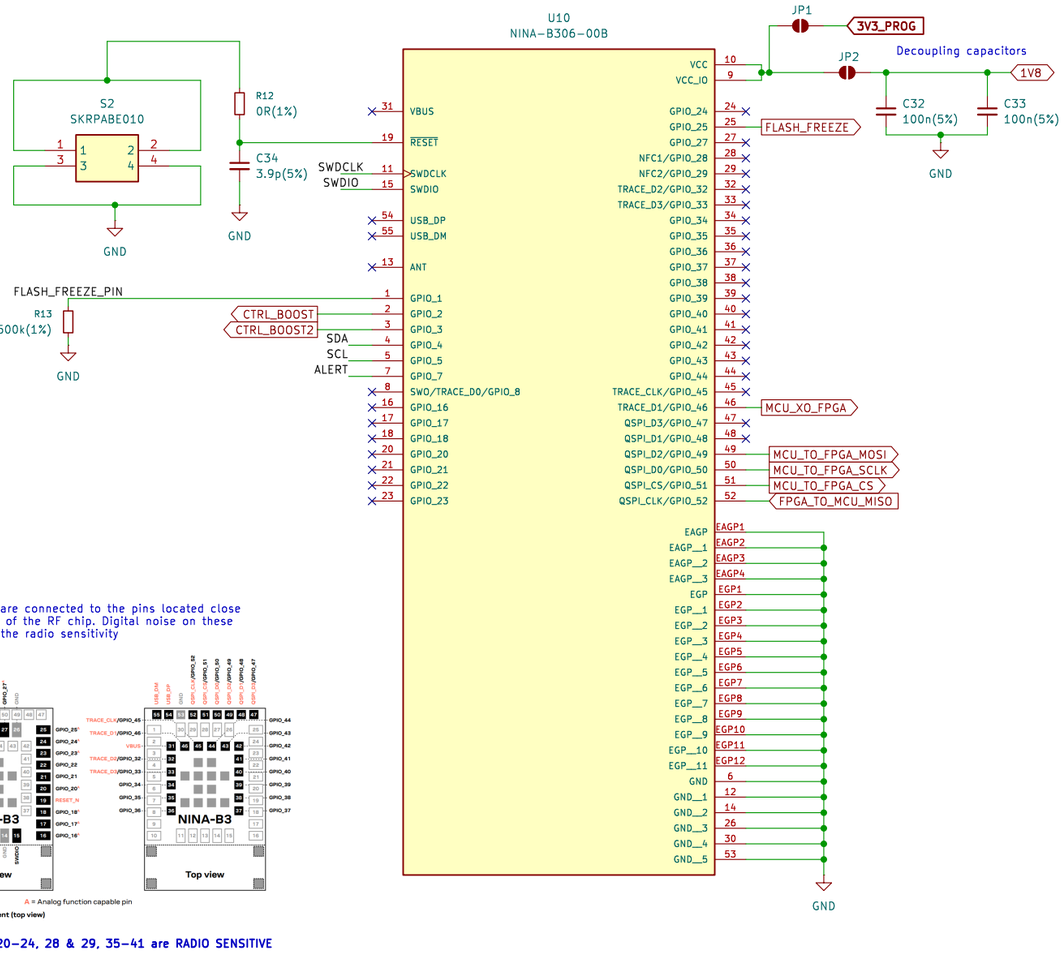
Analog LDO for LED Driving

Project: WEARABLE
Equipo G1 – PMU Schematic

Sheet: /PMU/
File: pmu.kicad_sch

Title:

Size: A3	Date: 12/08/2025	**Rev:** 3
KiCad E.D.A. 9.0.3		Id: 3/4

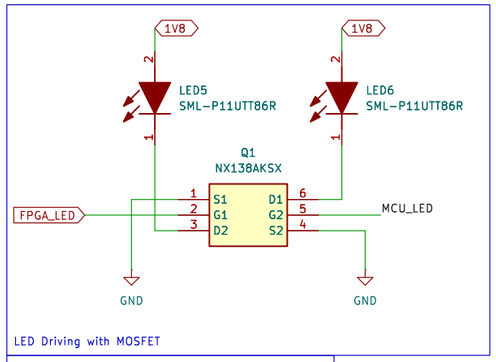


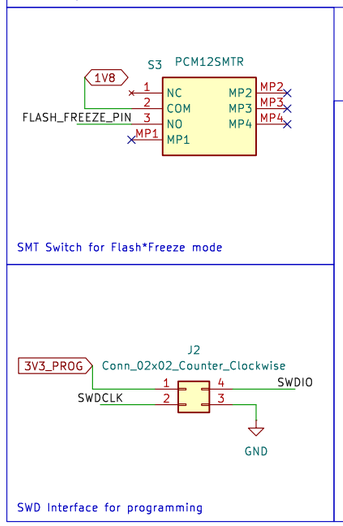
Some GPIO pins are connected to the pins located close to the radio part of the RF chip. Digital noise on these pins can reduce the radio sensitivity

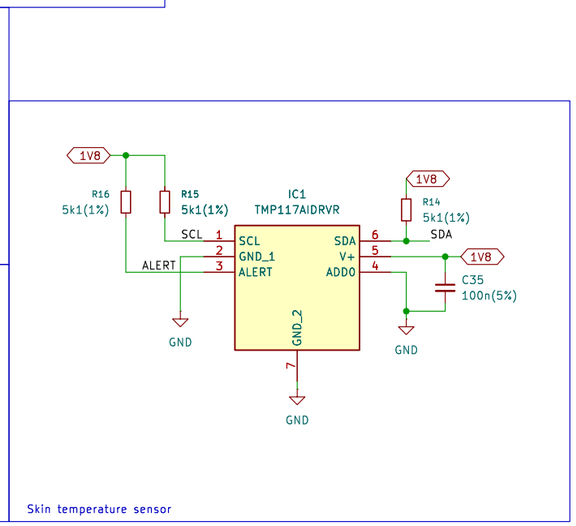
A = Analog function capable pin

Figure 4: NINA-B30 series pin assignment (top view)

GPIO 16–18, 20–24, 28 & 29, 35–41 are RADIO SENSITIVE







Project: WEARABLE
Equipo G1 – MCU Schematic

Sheet: /MCU/
File: mcu.kicad_sch

Title:

Size: A3 | Date: 13/08/2025 | **Rev:** 3
KiCad E.D.A. 9.0.3 | Id: 4/4