SHIV NADAR
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Shiv Nadar Institute of Eminence Greater Noida
Department of Computer Science Engineering

Computer Organisation and Architecture
(CSD-211)

Mid Term, Date: Oct 4, 2023

Timing: 3:00 to 5:00 PM | III Semester | Max mark: 80

Instructions

- All the questions are compulsory. However there are some choices in question no. 1,2,4,5,6,7, and 9.
- Write question number clearly and visible. Avoid mixing of parts with different question.
- You are not supposed to carry any electronic devices(pen drive, hard disk, smart-watch, cellphones, headphones, and earphones.) except calculators.
- Unexpectedly writing extra will not help you in gaining more marks, so try to write in points.

1. Short answer type questions(attempt any 5 only):
   (a) Why we wait for memory function completed step needed for reading from or writing to the main memory? **(2)**
   (b) What is little endian and big endian? **(2)**
   (c) The range of representable normalized number in the floating point binary fractional representation in a 32bit word in 1 bit sign , 8 bit excess 128 biased exponent, and the 32 bit mantissa is..... **(2)**
   (d) Define advantages of RISC over CISC. **(2)**
   (e) Give all the fields of the R-Type and I-type instructions in MIPS. **(2)**
   (f) How many values of X and Y are possible for **(2)**

$$(42)_9 = (X3)_Y$$

2. Write a short note (not more than 100 words)on following:(any 3) **(12)**
   (a) Instruction Decoder
   (b) Step Decoder

(c) Role of Multiplexer in ALU

(d) Disadvantage of Single bus organization

(e) Fetch, Decode, Execute cycle

3. A portion of an assembly language program written for an 8-bit microprocessor is given below along with explanations. The code is intended to introduce a software time delay. The processor is driven by a 5 MHz clock. The time delay (in microsec) introduced by the program is **(5)**

```
        MVI B, 64H ; Move immediate the given byte into register B. Takes 7 clock
      periods.
LOOP : DCR B ; Decrement register B. Affects Flags. Takes 4 clock periods.
        JNZ LOOP ; Jump to address with Label LOOP if zero flag is not set.
```

Takes 10 clock periods when jump is performed and 7 clock periods when jump is not performed

4. Attempt any one: **(4)**

(a) We are considering an enhancement to the high performance processor of a web server. The enhanced version of CPU is 25 times faster on search queries than the old processor. The Old processor is busy with search queries 70% of the time, what is the speedup gained by integrating the enchanced CPU?

(b) Intel added a new floating point unit to the power CPU. After modification in the circuit new CPU became 10 times faster. Limitation of the power is the I/O bound server which consumes 60% time for I/O. What will be the overall speed up of the system.

5. Design any one: **(4)**

(a) Design a combinational circuit of 4X4 binary multiplier.

(b) Design a combinational circuit of a bus system orientation for 4-register each of size 4 bit.

6. Attempt any two from the following: **(10)**

(a) A company is releasing 2 latest versions (beta and gamma) of its basic processor architeture named alpha. Beta and gamma are designed by making modifications on three major components (X,Y,and Z) of the alpha. It was observed that for a program A the fraction of the total execution time on these three components, X, Y, and Z are 40%, 30% and 20%, respectively. Beta speeds up X and Z by 2 times but slows down Y by 1.3 times, where as gamma speeds up X, Y, and Z by 1.2,1.3, and 1.4 times, respectively.

i) How much faster is gamma over alpha for running A?

ii) Whether beta or gamma is faster for running A? Find the speed up factor.

(b) A common transformation required in graphics processor is square root. Implementations of floating point (FP) square root vary significantly in performance, especially among processors designed for graphics. Suppose FP square root (FPSQR) is responsible for 20% of the execution time of a critical graphics benchmark. One proposal is to enhance the FPSQR hardware and speed up this operation by a factor of 10. The other alternative is just to try to make all FP instructions in the graphics processor run faster by a factor of 1.6; FP instructions are responsible for half of the execution time for the application. Compare these two design alternatives using Amdahl's law.

(c) Consider two programs A and B that solves a given problem. A is scheduled to run on a processor P1 operating at 1GHz and B is scheduled to run on a processor P2 running at 1.4GHz.A has total 10000 instructions, Out of which 20% are branch instructions, 40% load store instructions and rest are ALU instructions. B is composed of 25% branch instructions. The number of load store instructions in B is twice the count of ALU instructions. Total instruction count of B is 12000. In both P1 and P2 branch instructions have an average CPI of 5 and ALU instructions has an average CPI of 1.5. Both the architectures differ in the CPI of load-store instruction. They are 2 and 3 for P1 and P2, respectively. Which mapping (A on P1 or B on P2)solves the problem faster, and by how much?

7. Attempt any one: **(10)**

(a) Construct a 8-bit ALU design for a simple processor. You can take neccessary assumptions if required and mention it clearly in your answer.

(b) Registers R1 and R2 of a computer contains the decimal values 2900 and 3300. What is the effective address of the memory operand in each of the following instructions?

a) LOAD R1, 55(R2)

b) MOV 2000, R7

c) STORE 95(R1,R2), R5

d) ADD (R1)+,R5

e) SUB -(R2),R5

8. Draw a labeled diagram for a single bus organization of a CPU. Mention all the basic units clearly in your diagram. (Consider Address size of 16 bits and data size of 8 bits.) **(10)**

9. Attempt any one from the following: **(15)**

   (a) Write control signal steps for the following instructions:
   2000: LDA 1100
   2001: MOV B, A
   2002: DCR B

   (b) Write all the steps in order to fetch a word from memory requested by processor and storing a word into memory from the processor. Consider single bus organization of the CPU organisation.

Best wishes