Q16.(3 marks) a) What are different types of misses in cache memory? Briefly explain.

*b)***(3 marks)** It is a usual convention to use higher order bits of the address as tag bits and middle bits are used for indexing (<Tag, Index, offset>) in the set-associative mapping of cache. What problem will arise if higher order bits are used for indexing?

c) **(3 marks)** For a 32KB direct mapped cache with 128 byte cache block, calculate the number of sets. Find the address of the starting byte of the first word in the block that contains the address 0xA21967EF.

Q17.(5 marks) The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write-back (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards. What is the number of cycles required to complete the execution sequence?

or

Q18.(5 marks) Consider a processor with a delayed branch that has three delay slots. Two compilers -- compiler A and compiler B, could run on this processor. Compiler A can fill the first delay slot 60% of the time and the second delay slot 40% of the time and the third delay slot 20 % of the time. Compiler B can fully fill all three delay slots. Assuming that branches account for 20% of all instructions and arithmetic/logic operations for the remaining 80% of the instructions for any program, what is the improvement of CPI with compiler B compared to CPI with compiler A?

Q19.(4 marks each) Differentiate between followings(logical points only):

(a) RISC vs CISC

(b) Loosely coupled and Tightly coupled Multiprocessor.

(c) I/O mapped I/O and Memory Mapped I/O

Q20.(6 marks) Explain the principle of pipelining with the help of space time diagram. Derive an expression for speed up. Explain types of hazards with proper example.

Q21.(4 marks)(a) Consider a system, that uses Interrupt Driven I/O for a particular device which has a data transfer rate of 10 KBPS . The processing of the interrupt takes 250 microseconds . What percentage of CPU time is consumed by I/O device, if I/O device interrupts for every 2 bytes of data transfer?

(b)**(3 marks)** Enumerate the steps that are undertaken on arrival and acknowledgement of an interrupt?

(c)**(3 marks)** Why is Stack data structure so important for processing of interrupts?

(d)**(3 marks)** In what way does an interrupt differ from a function call?

(e)**(3 marks)** What role does the CPU play in a DMA based data transfer system?

Q22. (4 marks each) Consider a CPU that is connected to a pressure sensing system of an oil bath, and a temperature sensing system for the same bath. How would you design the system so that if the temperature or pressure goes beyond the respective specified ranges, a corresponding alarm will be activated. Otherwise, the processor will continually record the log of the temperatures and pressures, every 5 msec.

i) Can you provide a block diagram for your solution?

ii) Can you provide a high level description (pseudo-code) of the program that the CPU will execute?

Shiv Nadar Institute of Eminance
CSD211:Computer Organization and Architecture
End-Term Examination

Set No. A

Duration: 3 Hour   **M.M.: 100**
Instructions:
- The question paper contains three parts. Answer all questions in Part–A , Part–B and Part–C .
- Part-A and Part-B need to be filled in the question paper only.
- Attempt carefully, cutting and erasing are not allowed in Part-A and Part-B.
- Written sheets will be provided for Part-C only. Unnecesaary lengthy answers will be penlized
- Use of scientific calculators is permitted.
*- **Q7 to Q9** are MCQs having only one correct answer. Mark correct answer only.*
*- Options are provided between: **Q12 vs Q13, and Q17 vs Q18.***
- All the answers should be brief and to the point. Unnecesaary lengthy answers will be penlized.
- No clarification will be entertained during the examination. You may mention the assumptions while answering the questions, if required.

Part-A(each of 2 marks X 10= 20 Marks)

Q1. Consider a 5 stage instruction pipeline with latencies (in ns) 1,2,3,4, and 5 respectively. Find the average CPI of Non-pipeline CPU when speed up achieved with respect to pipeline is 4 (assume ideal case for peipelining). **Ans**_____

Q2. 4-way set associative cache memory with a capacity of 16KB is built using a block size of 8 words. The word length is 32-bits. The size of the physical address space is 4GB. Find the number of bits for the tag field. Consider memory word-addressable.

Ans_____

Q3. A given application written in java runs in 15 sec on a desktop processor. A new java compiler is released that requires only 0.6 as many instructions as the old compiler. Unfortunately, it increases the CPI by 1.1. How fast can we expect the application to run using this new compiler?

Ans_____

Q4. True/ False (0.5 x 4 =2 marks)

a. High associativity in a cache reduces compulsory misses.   (   )
b. Both DRAM and SRAM must be refreshed periodically.   (   )
c. Forwarding can present all data depending pipeline hazard.   (   )
d. The performance of a pipelined processor or suffers of the pipeline stages share hardware resources.   (   )

Q5. Three processor making companies C1, C2 and C3 release modifications to the three major components (X,Y and Z) of their processors to improve the execution time. The fraction of the total execution time utilized by a running application on X, Y and Z are 25%, 55% and20%, respectively. The speedup gained for the components X, Y and Z corresponding the individual companies are outlined below. Calculate the speedup obtained for the processors belonging to each individual companies. Rank the companies in terms of the speedup of their processors.

Proccesor	X	Y	Z
C1	1.2	0.3	1.6
C2	0.8	1.5	2.1
C3	1.8	0.6	1.2

Ans.

Q6. The following bit pattern represents a floating point number in IEEE 754 single precision format 1 10000011 101 0000 0000 0000 0000 0000. What is the value of the number in decimal form?

Ans_____

 Consider the following floating point format mantissa is a pure fraction in sign magnitude form.

Sign Bit(15th bit)	Excess of 64 Exponent (14th bit-8th bit)	Mantissa(7th bit-0th bit)

Q7. The decimal number 0.239 x 2^{13} has the following hexadecimal representation (without normalization) and rounding off.   ( ) OD24   ( ) OD4D   ( )4DOD   ( ) 4D3D.

Q8. The normalised representation for the above format is specified as follows. The mantisa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field. The normalised representation of the above number 0.239 x 2 ^{13} is
( ) 0A20   ( ) 1134   ( ) 49D0   ( ) 4AE8

Q9. The main memory of a computer has 2 cm blocks while the cache has 2C blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block K The main memory maps to the set.
(   ) (Kmod m) of the cache   (   ) (Kmod c) of the cache
(   ) (K mod 2c) of the cache   (   ) (K mod 2cm) of the cache

Q10. A memory system has a cache, a main memory and a disk. If the hit rate in the cache is 98% and the hit rate in the main memory in 99% .What in the average memory access time if it takes 2 cycles to access the cache, 150 cycles to fetch a line from main memory and 100,000 cycle to access the secondary memory.

Ans:_____

Part-B(20 Marks)

Q11.(8 marks) Assume that we have three scenario : A fully associative cache, A two way set associative cache, and A direct mapped cache The cache size in 256 bytes The cache line size is 8 bytes. All variables are 4 bytes. Assume that we have separate instruction and data caches . Assume that a(1024) is assigned to memory location byte 0 through 4095. b→4096 – 4099 , q→4104 – 4107, c→4100 – 4103 , r→4108 – 4111, i→4112 – 4115. Assume cold cache & LRU replacement

```
(A). for(i=0:i<16:i++)                    (B). for(i=0:i<16:i++)
       {                                         {
              b+ = q*a[i] ;                              b+ = q*a[64*i] ;
       }                                         }
     for(i=0:i<16:i++)                        for(i=0:i<16:i++)
       {                                         {
              c+ = r*a[i] ;                              c+ = r*a[64*i] ;
       }                                         }
```
a. How many data cache read, compulsory misses, capacity misses and conflict misses will occur in fully associative cache in scenario (A).
Ans:_____
b. How many data cache read misses will occur in fully associative cache in scenario (B).
Ans:_____
c. How many data cache read misses will occur in direct mapping cache in scenario (B).
Ans:_____
d. How many data cache read misses will occur in 2 way set associative cache in scenario (B).
Ans:_____

Q12. (8 marks) Consider the following sequences of branch outcomes. T means the branch is taken; N means the branch is not taken.
          Sequence 1: T, T, T, N   **Sequence 2: T, N, T, T, N**

a) What is the accuracy of the always-taken branch predictor for each sequence?(.......................)

b) What is the accuracy of the always-not-taken branch predictor for each sequence?(.................)

c) What is the accuracy of the 2-bit branch predictor for each sequence? Assume the predictor starts in the "weak" not taken state (lower-right).(...)

d) What is the accuracy of the 2-bit branch predictor for each sequence, if the sequence repeats thousands of times?(..)

or

Q13.(8 marks) We have a program core consisting of five conditional branches. The program core will be executed thousands of times. Below are the outcomes of each branch for one execution of the program core (T for taken, N for not taken).
Branch 1: T-T-T-T   **Branch 2: N-N-N-N**   **Branch 3: N-T-N-T-N-T**
          Branch 4: T-N-T-N-T-N   **Branch 5: T-T-N-T-T-N-T-T**
Assume the behavior of each branch remains the same for each program core execution. For the dynamic branch prediction schemes below, assume that each branch maps to a unique entry in the branch history table. Further assume that each BHT entry is initialized to the same stage before each execution: (a) Always taken (b) Always not taken (c) 1-bit predictor, initialized to predict taken (d) 2-bit predictor, initialized to weakly predict taken
What is the branch prediction accuracy for branch 1 to 5 with prediction scheme (a) through (d)? Use the following table to fill out your final answer.

Branches	Prediction schemes			
	(a)	(b)	(c)	(d)
1				
2				
3				
4				
5				

Q14.(4 marks) Consider a processor with 64 registers and an instruction set of 12 instructions. Each instruction has 5 distinct fields namely opcode , two source register identifier, one destination register identifier and a 12 bit immediate value. Each instructor must be stored in memory in byte aligned fashion. If the program has 100 instructions, the amount of memory (in bytes) consumed by the program text is what?

Ans:_____

Part-C(need to be written on answer sheet)(60 Marks)

Q15.(4 marks) Consider the unpipelined processor. Assume that it has a 1 nsec clock cycle and that it uses 4 cycles for ALU operations and branches, and 5 cycles for memory operations. Assume that the relative frequencies of these operations are 40%, 20% and 40 % respectively. Suppose that due to clock skew and setup, pipelining the processor adds 0.2 nsec of overhead in clock . How much speedup, we will gain from pipeline?.