CSD211: Computer organization and architecture
Quiz-2

(Cache mapping)

Ques1 A computer has a 1MB, 8-way set associative write back data cache with a block size of 8 words. The word length is 32-bits. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to the address tag, 2 valid bits, 1 modified bit, and 1 replacement bit. Calculate-

a. The number of bits in the tag field ……

b. The size of the cache tag directory ……

c. Number of bits in block offset……..

d. Number of lines and sets in cache…….

(Memory hierarchy)

Ques2 Consider a memory hierarchy with a level system cache with L1, L2, and L3 cache levels. Cache levels have the following properties:

Level	Hit-Ratio	Access Time	Search time
L1	70%	1 ns	0.2 ns
L2	80%	10 ns	0.4 ns
L3	100%	50 ns	0.5 ns

The transfer time to move a word block from L3 to L2 and L2 to L1 is 2 ns and 1.5 ns per word, respectively. Calculate the average access time of cache hierarchy.

…….

Ques3 Consider a two-level cache hierarchy with L1 and L2 caches. An application incurs 1.4 memory accesses per instruction on average. For this

application, the miss rate of the L1 cache is 0.1; the L2 cache experiences, on average, 7 misses per 1000 instructions. The miss rate of L2 expressed correctly to two decimal places is

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Ques4 Consider a cache of size 128 Byte Direct mapped cache and 16 bit address and each block of 32 Bytes. CPU generates address streams of 0x1070, 0x2080, 0x1068, 0x0190, 0x1084, 0x6178, 0x008C, 0x0F00, 0x1064. How many of them are MISS and How many of them are HIT?

(Pipeline Questions)
Ques5 Consider a 5 stage instruction pipeline with latencies (in ns) 1, 2, 3, 4, and 5, respectively. Find the average CPI of non-pipeline CPU when speed up achieved with respect to pipeline is 4 (assume ideal case for pipelining)

(I/O interrupts)
Ques6: The following are some events that occur after a device controller issues an interrupt while process L is under execution?

(P) The processor pushes the process status onto the control stack.
(Q) The processor finishes the execution of the current instruction.
(R) The processor executes the interrupt service routine.
(S) The processor pops the process status from the control stack.
(T) The processor loads the new PC value based on the interrupt.
Write the correct order of events regarding interrupts.
