**CSD 211 Computer organization and architecture**

**Extra Quiz**

**1st Dec 2023**

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**Ques1** A cache memory that has a hit rate of 0.8 has an access latency 10ns and miss penalty 100ns. An optimization is done on the cache to reduce the miss rate. However, the optimization results in an increase of cache access latency to 15ns, whereas the miss penalty is not affected. The minimum hit rate *(rounded off to two decimal places)* needed after the optimization such that it should not increase the average memory access time is _____. **(2 Marks)**

**Ques2** A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____ . **(1 Mark)**

**Ques3** Consider a 5 stage instruction pipeline with latencies (in ns) 1, 2, 3, 4, and 5, respectively. Find the average CPI of non-pipeline CPU when speed up achieved with respect to pipeline is 4 (assume ideal case for pipelining). **(3 Marks)**

**Ques4** 4-way set associative cache memory with a capacity of 16 KB is built using a block size of 8 words. The word length is 32-bits. The size of the physical address space is 4GB. Find the number of bits for the tag field. **(3 Marks)**

**Ques5** The following are some events that occur after a device controller issues an interrupt while process L is under execution? **(1 Mark)**

(P) The processor pushes the process status onto the control stack.
(Q) The processor finishes the execution of the current instruction.
(R) The processor executes the interrupt service routine.
(S) The processor pops the process status from the control stack.
(T) The processor loads the new PC value based on the interrupt.
Write the correct order of events regarding interrupts.