CSD211

Computer organization and architecture

Cache memory worksheet

Ques1 Consider a system with two levels of caches. The access times of level-1 cache, level-2 cache, and the main memory are 1 ns, 10 ns, and 500 ns, respectively. The hit rates of level-1 caches and level-2 caches are 0.8 and 0.9. What is the average access time of the system, ignoring the search time within the cache?

Ques2 What is the average memory access time for a machine with a cache hit rate of 80%, a cache access time of 5 ns and main memory access time of 100 ns when-

1. Simultaneous access memory organization is used.
2. Hierarchical access memory organization is used.

Ques3 Assume a memory access to main memory on a cache "miss" takes 30 ns and a memory access to the cache on a cache "hit" takes 3 ns. If 80% of the processor's memory requests result in a cache "hit", what is the average memory access time?

Ques4 The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	Read access time (in nanoseconds)	Hit ratio
I-Cache	2	0.8
D-Cache	2	0.9

L2-Cache	8	0.9

The read access time of main memory is 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the writeback policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In the execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

Ques5 Consider a 3 Level Memory System with the following specifications

- $(H_1,H_2,H_3) = (0.8,0.9,1)$
- $(T_1,T_2,T_3) = (2,100,500)$ nanosec / word
- If there is miss at L_1 and a hit atL2, a 2-Word block must be transferred from L_2 to L_1
- IF there is miss at both levels, then 4-Word block must be bought from L_3 to L2, and concerned block must be moved from L_2 to L_1

The referred word must always be given from L_1 only to the processor.

1. Average Access Time Taken Given that the data width between L_1 to L_2 and L_2 to L_3 is 1 Word block is T_{avg-1}
2. Average Access Time Taken Given that the data width between L_1 to L_2 and L_2 to L_3 is 4 Word block is T_{avg-2}

What is the ratio of T_{avg-1} to T_{avg-2}

Ques6 The following cache represents a 2-way set associative cache, i.e., there are two lines per set. Notice that the set ID values start at 011011012 and increment every other row. This is meant to imply that you are looking at a group of lines/sets toward the middle of the cache and not the entire cache.

There are 14 bits for the tag, 8 bits for the set id, and 2 bits for the word id. Answer the following 3 questions based on this cache.

Tag (binary values)	Set ID (binary values)	Word within block			
		00	01	10	11
10100001001001	01101101	00_{16}	61_{16}	$C2_{16}$	23_{16}
11100001100100	01101101	10_{16}	71_{16}	$D2_{16}$	33_{16}
11001011010110	01101110	20_{16}	81_{16}	$E2_{16}$	43_{16}
11100101101011	01101110	30_{16}	91_{16}	$F2_{16}$	53_{16}
11110110110100	01101111	40_{16}	$A1_{16}$	02_{16}	63_{16}
10100111010101	01101111	50_{16}	$B1_{16}$	12_{16}	73_{16}
10101010111110	01110000	84_{16}	$E5_{16}$	46_{16}	$A7_{16}$
10101010010011	01110000	94_{16}	$F5_{16}$	56_{16}	$B7_{16}$
01110001001000	01110001	$A4_{16}$	$A5_{16}$	66_{16}	$C7_{16}$
00001101101101	01110001	$B4_{16}$	15_{16}	76_{16}	$D7_{16}$
01011010010010	01110010	$C4_{16}$	25_{16}	86_{16}	$E7_{16}$
10101111001011	01110010	$D4_{16}$	35_{16}	96_{16}	$F7_{16}$

(i) A copy of the data from memory address 7121C5 (hex) is contained in the portion of the cache shown above. Enter the value that was retrieved from that address as a two-digit hexadecimal number with no base identification, e.g., 0x4F (hexadecimal 4F) should be entered as 4F. _____

Note: Convert the given hec memory address into binary and then check all types of bits to reach the right point.

(ii) How many lines are contained in this cache?

(iii) How many blocks are contained in the memory space (not the cache, but the memory) of the cache system defined above?

Ques7 Consider a direct mapped cache of size 32KB with a block size of 32 bytes. The CPU generates 32-bit addresses. Find the number of bits required for cache indexing and tag bits.

Ques8 4-way set associative cache memory with a capacity of 16KB is built using a block size of 8 words. The word length is 32-bits. The size of the physical address space is 4GB. Find the number of bits for the tag field.

Ques9 In a **k-way** set associative cache, the cache is divided into **v sets**, each of which consists of **k lines**. The lines of a set are placed in sequence, one after another. The lines in **set s** are sequenced before the lines in **set (s+1)**. The main memory blocks are numbered **0** onwards. The main memory block numbered **'j'** must be mapped to any one of the cache lines from- (any 1 option is correct)

1. (j mod v) x k to (j mod v) x k + (k – 1)
2. (j mod v) to (j mod v) + (k – 1)
3. (j mod k) to (j mod k) + (v – 1)
4. (j mod k) x v to (j mod k) x v + (v – 1)

Ques10 A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks, and each block contains 256 8-bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the tag, set, and word fields?

Ques11 A computer has a 256 KB, 4-way set associative write back data cache with a block size of 32 bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to the address tag, 2 valid bits, 1 modified bit, and 1 replacement bit. calculate-

a. The number of bits in tag field
b. The size of the cache tag directory
c. Number of bits in block offset
d. Number of lines and sets in cache