CSE 436 Digital Integrated Circuits

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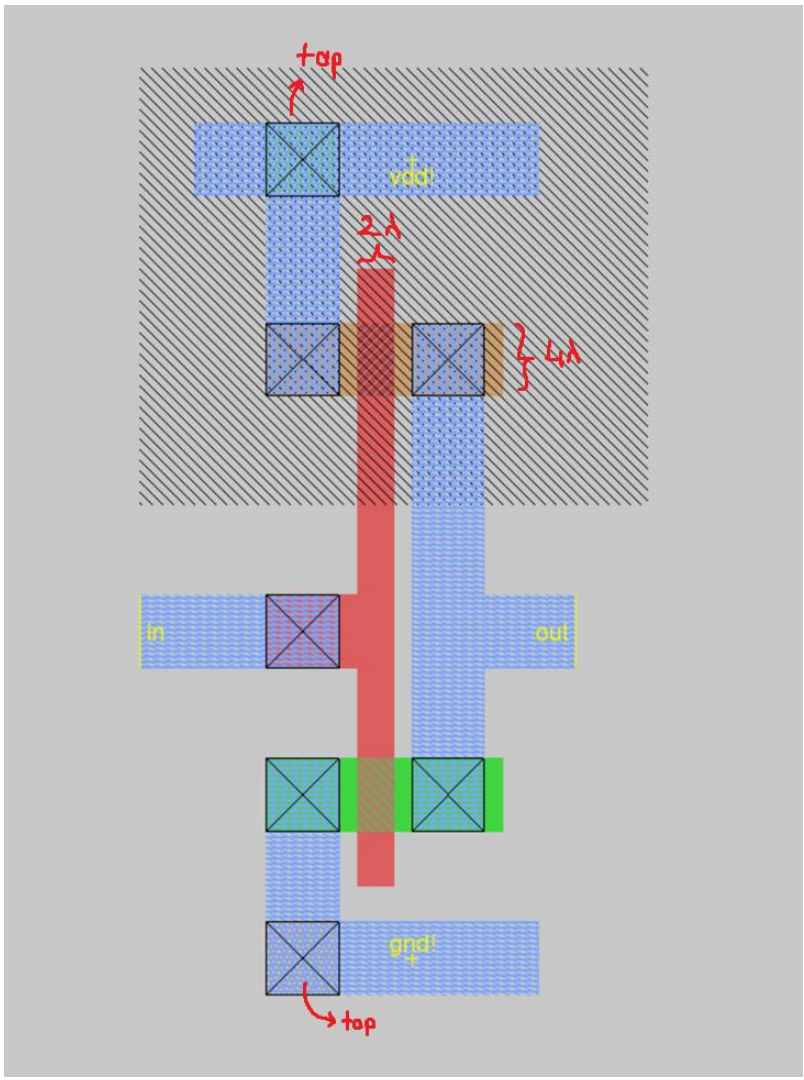
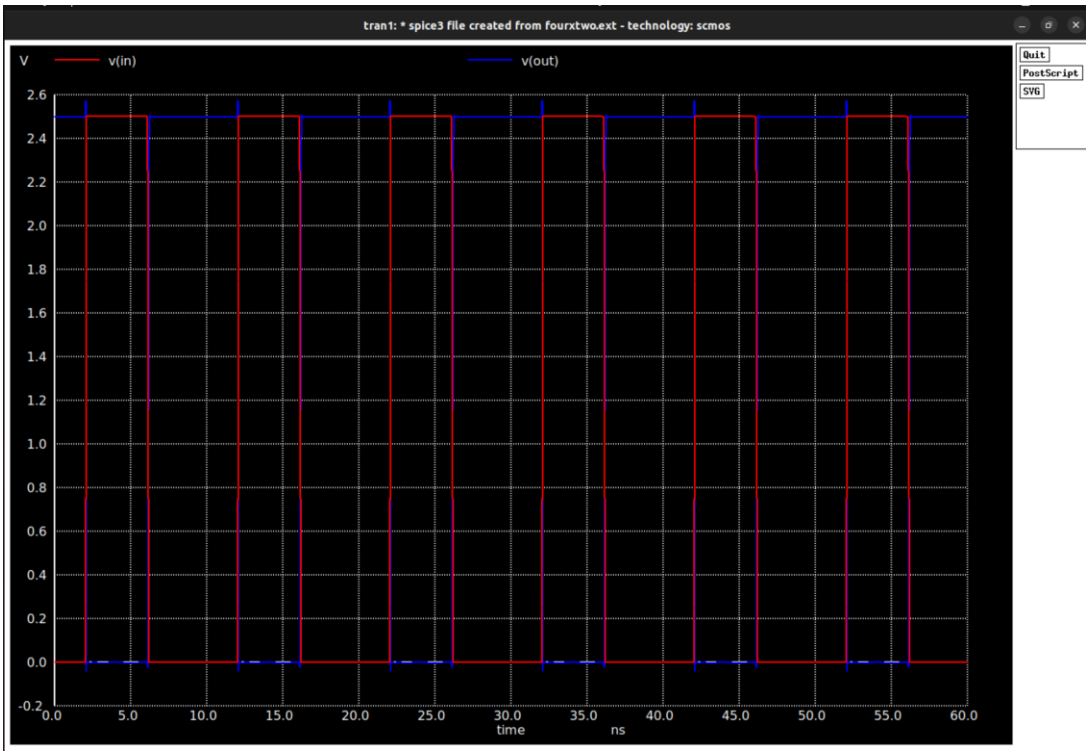
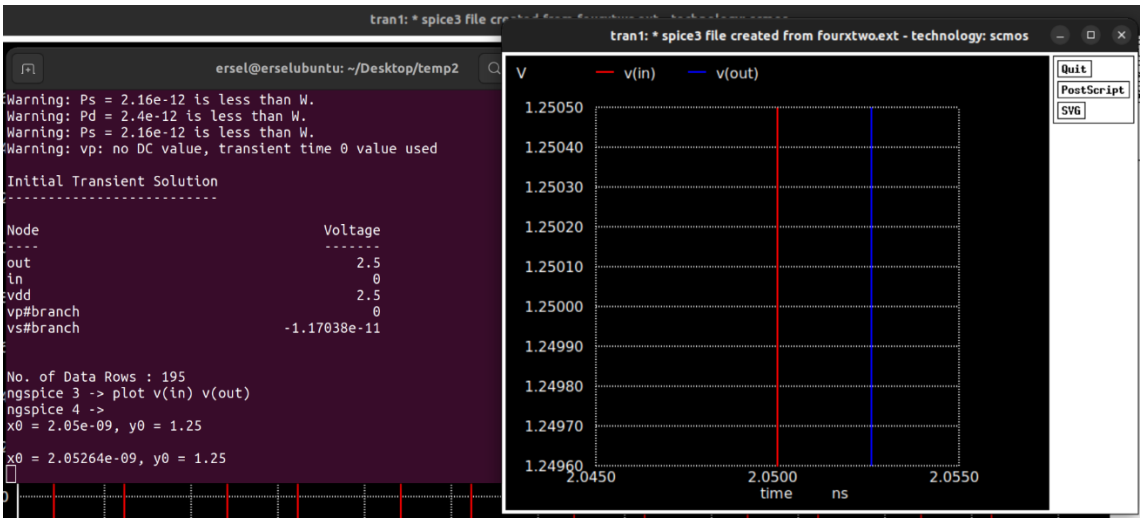
HW1 Report

This is the Magic Layout screenshot of inverter with 4λ/2λ PMOS and NMOS transistors and tap.

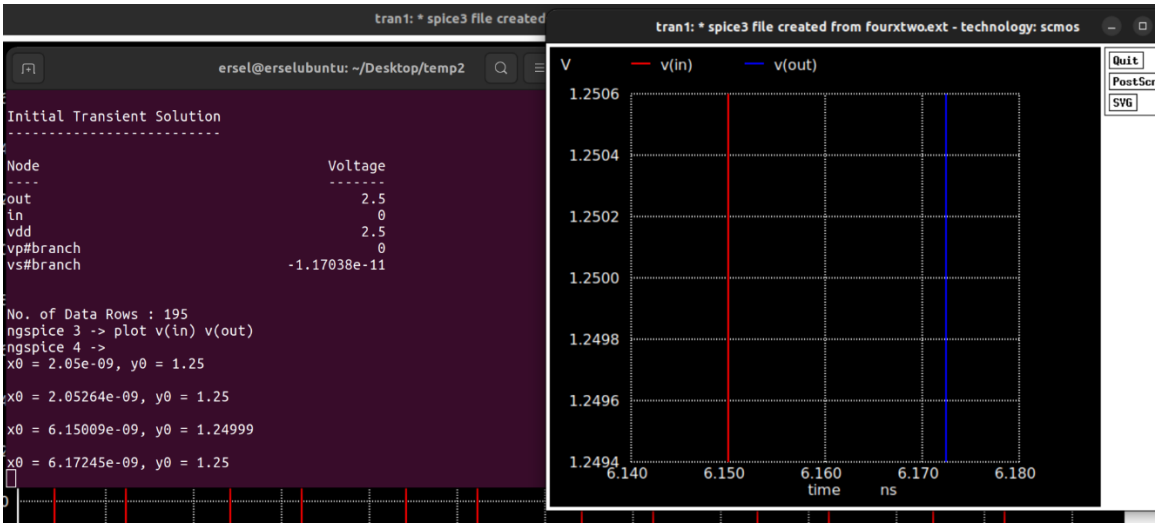




This is the plotting of v(in) and v(out) for 4λ/2λ inverter.

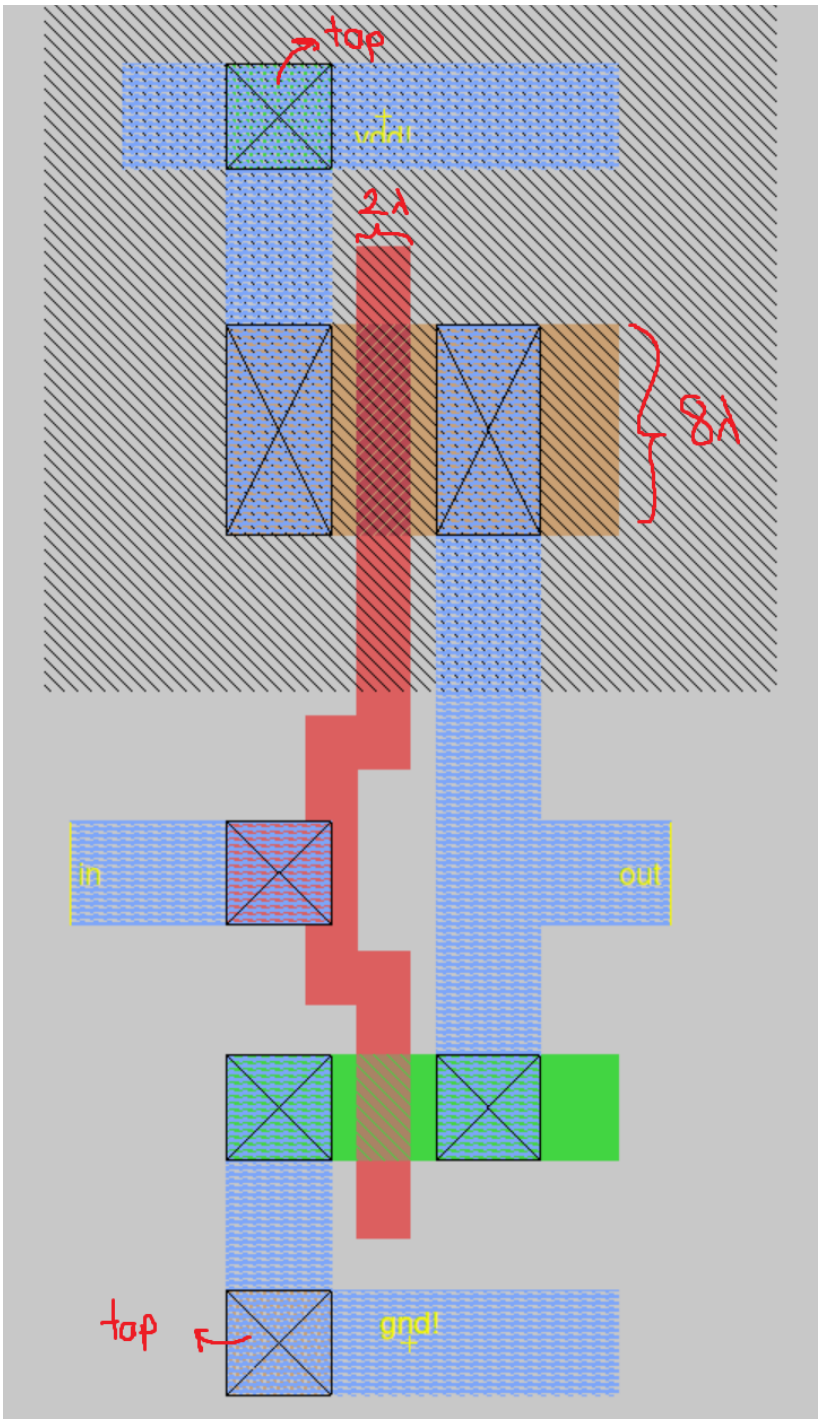


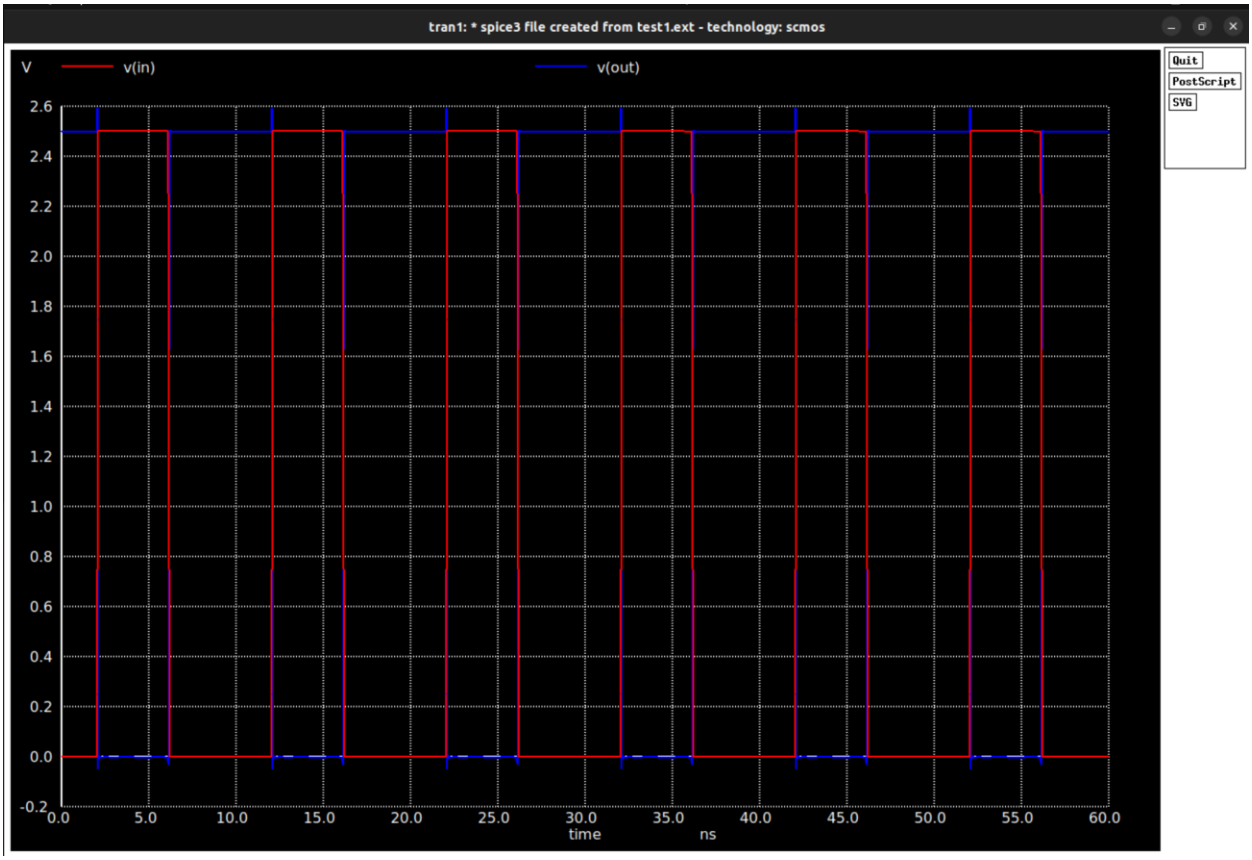
For the 4λ/2λ inverter, High-to-low delay, at 1.25 V(in) is 2.05e-09, at 1.25 V(out) is 2.05264e-09. So, the result is 2.64e-12, which is 2.64 picoseconds.



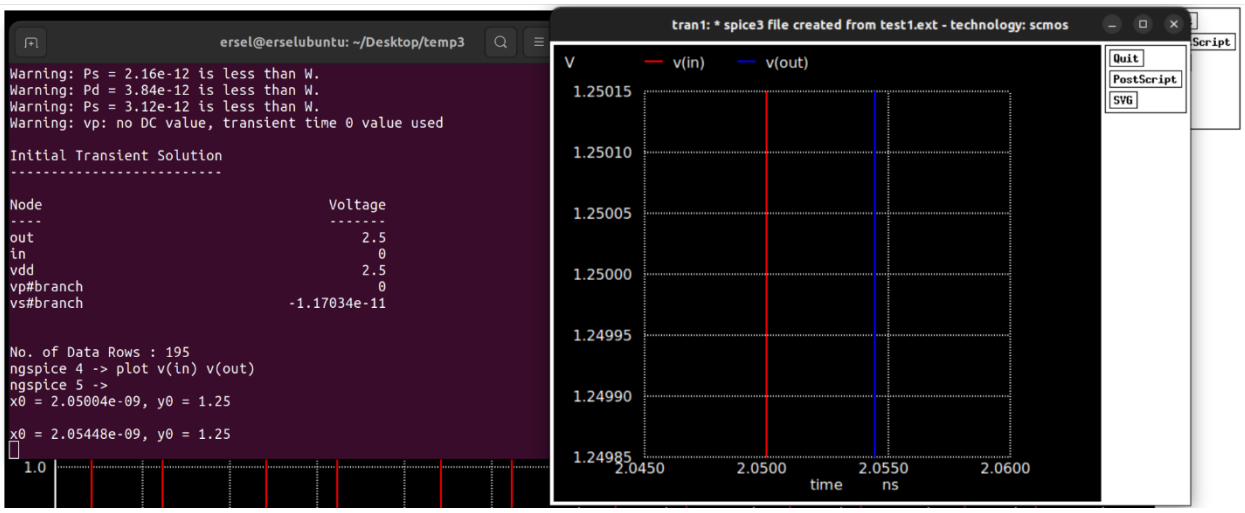
For the 4λ/2λ inverter, Low-to-high delay, at 1.25 V(in) is 6.15009e-09, at 1.25 V(out) is 6.17245e-09. So, the result is 2.236e-08 seconds, which is 22.36 picoseconds.

This is the Magic Layout screenshot of inverter with 8λ/2λ PMOS and 4λ/2λ NMOS transistors and tap.

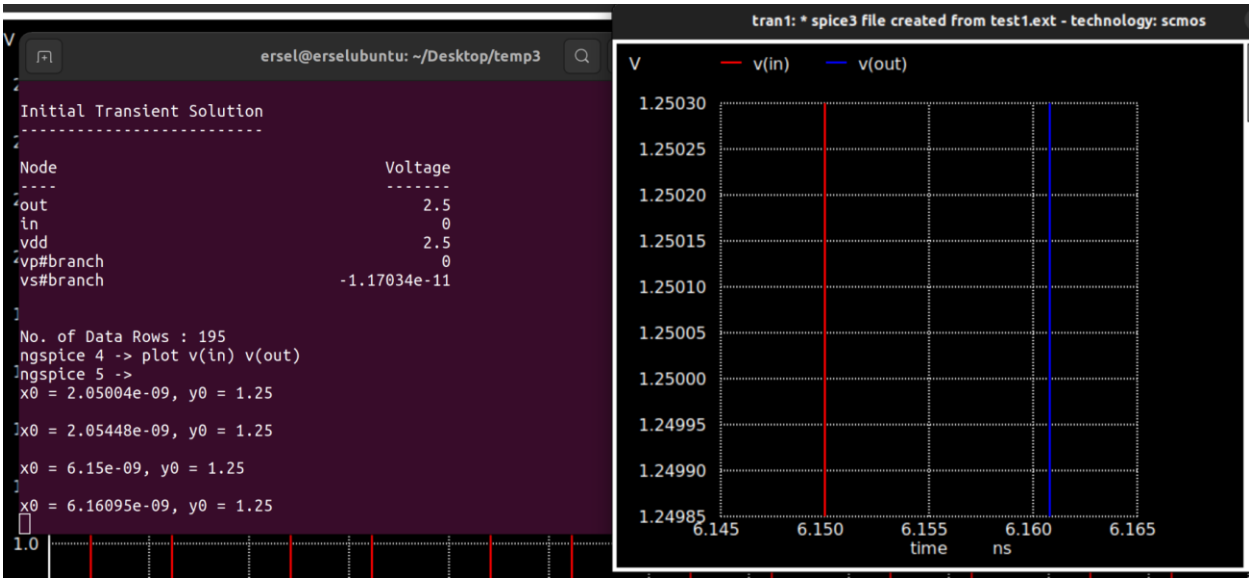




This is the plotting of v(in) and v(out) for 8λ/2λ inverter.



For the 8λ/2λ inverter, High-to-low delay, at 1.25 V(in) is 2.05004e-09, at 1.25 V(out) is 2.05448e-09. So, the result is 4.44 picoseconds.



For the 8λ/2λ inverter, low-to-high delay, at 1.25 V(in) is 6.15e-09, at 1.25 V(out) is 6.16095e-09. So, the result is 10.95 picoseconds.

In low-to-high delay we can see that delay of 8λ/2λ inverter is smaller and in high-to-low delay is little bit bigger then 4λ/2λ inverter.