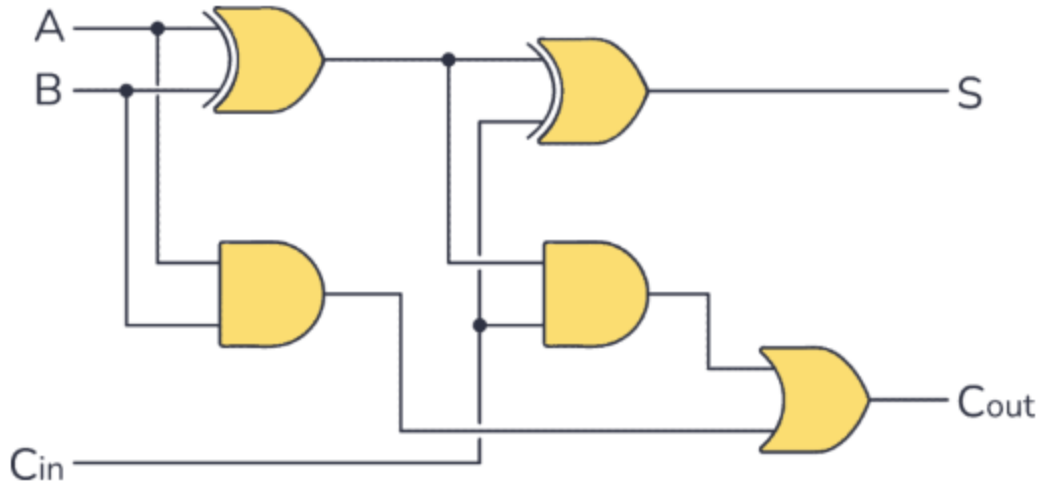
Digital Integrated Circuits

HW2 (Late Submission Report) - 15.12.2030

ERSEL CELAL EREN

In the project, I needed 4 Full Adders for the Carry Ripple Adder and 2 Half Adders for each Full Adder. I had to find the smallest components needed for designing at the transistor level. To design a Half Adder, 1 XOR gate and 1 AND gate were required.



A Full Adder Circuit

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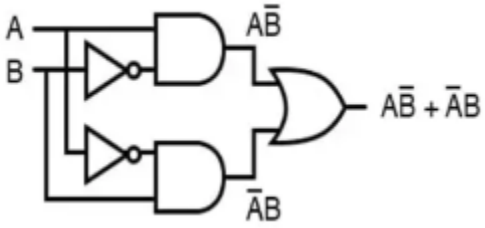
For the XOR design, I followed the schematic below. I designed the XOR using 2 Inverters, 2 AND gates, and 1 OR gate. To create an AND gate, I combined a NAND and an Inverter. For the OR gate, I combined a NOR and an Inverter.



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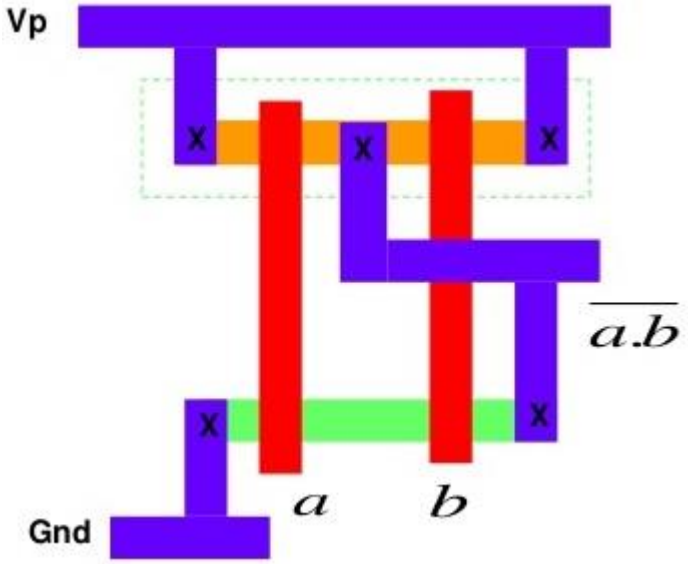
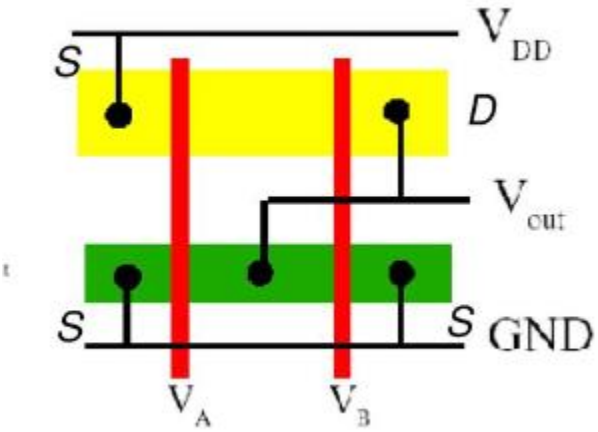
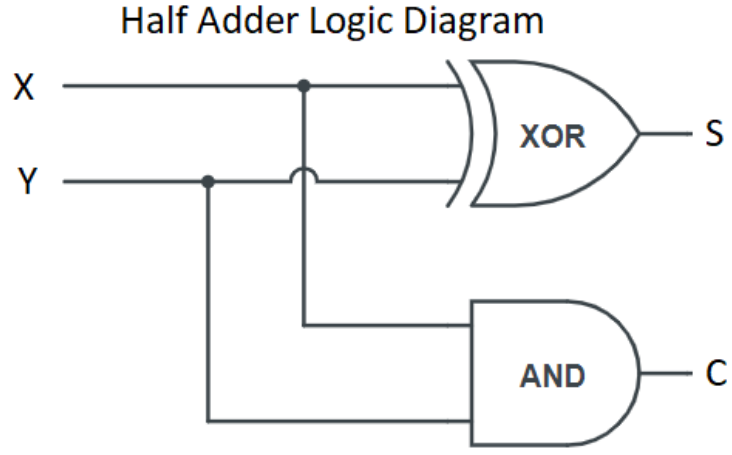
I considered following drawing for the NAND gate.



I considered following diagram for the NOR gate.



After combining all of these, I obtained the following Half Adder.



S = X'Y + XY' and C = XY

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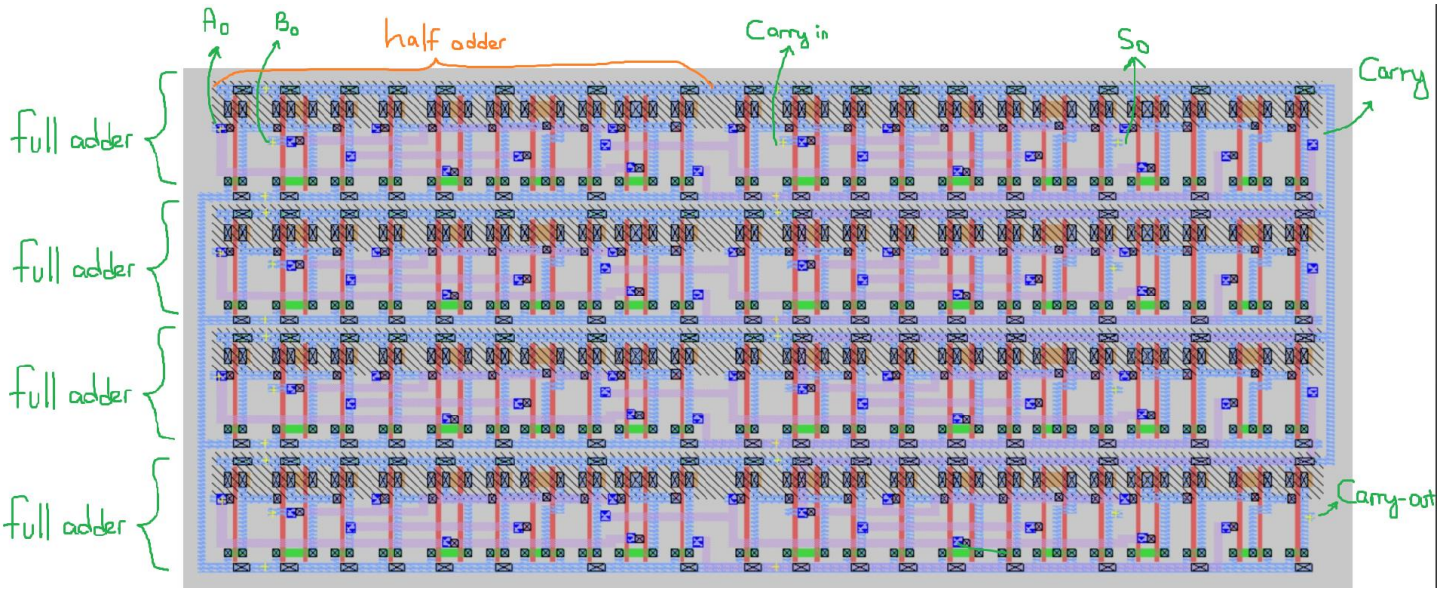
This is the full layout of 4-bit Carry Ripple Adder.



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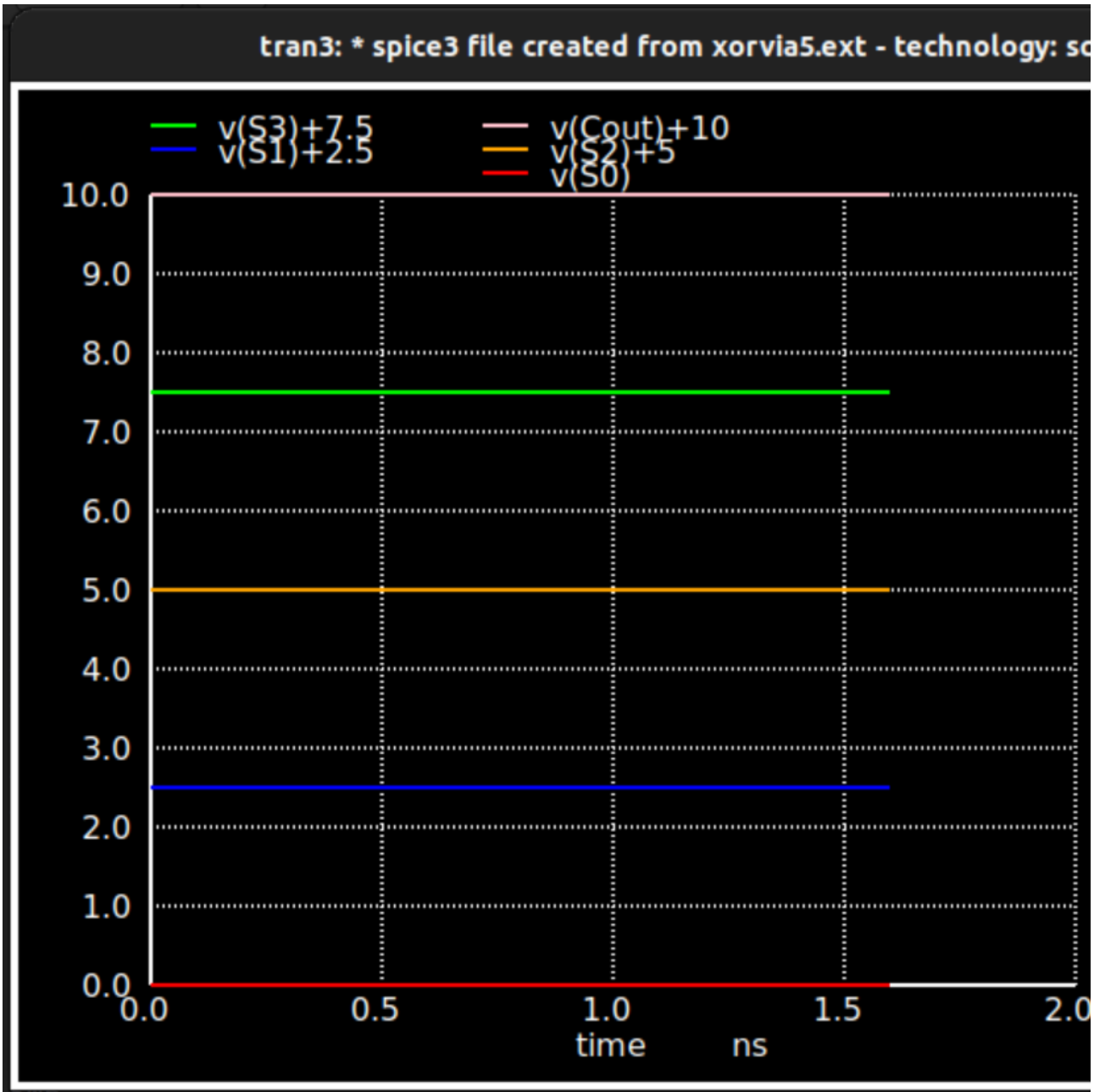
TEST CASES :

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508 Vin4 A1 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
509 Vin6 A2 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
510 Vin8 A3 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
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512 Vin3 Cin gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
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514 Vin2 B0 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
515 Vin5 B1 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
516 Vin7 B2 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
517 Vin9 B3 gnd PULSE(0, 0, 200p, 400p, 400p, 800p, 1600p)
518
519 .TRAN 1p 1600p
520 .OPTIONS
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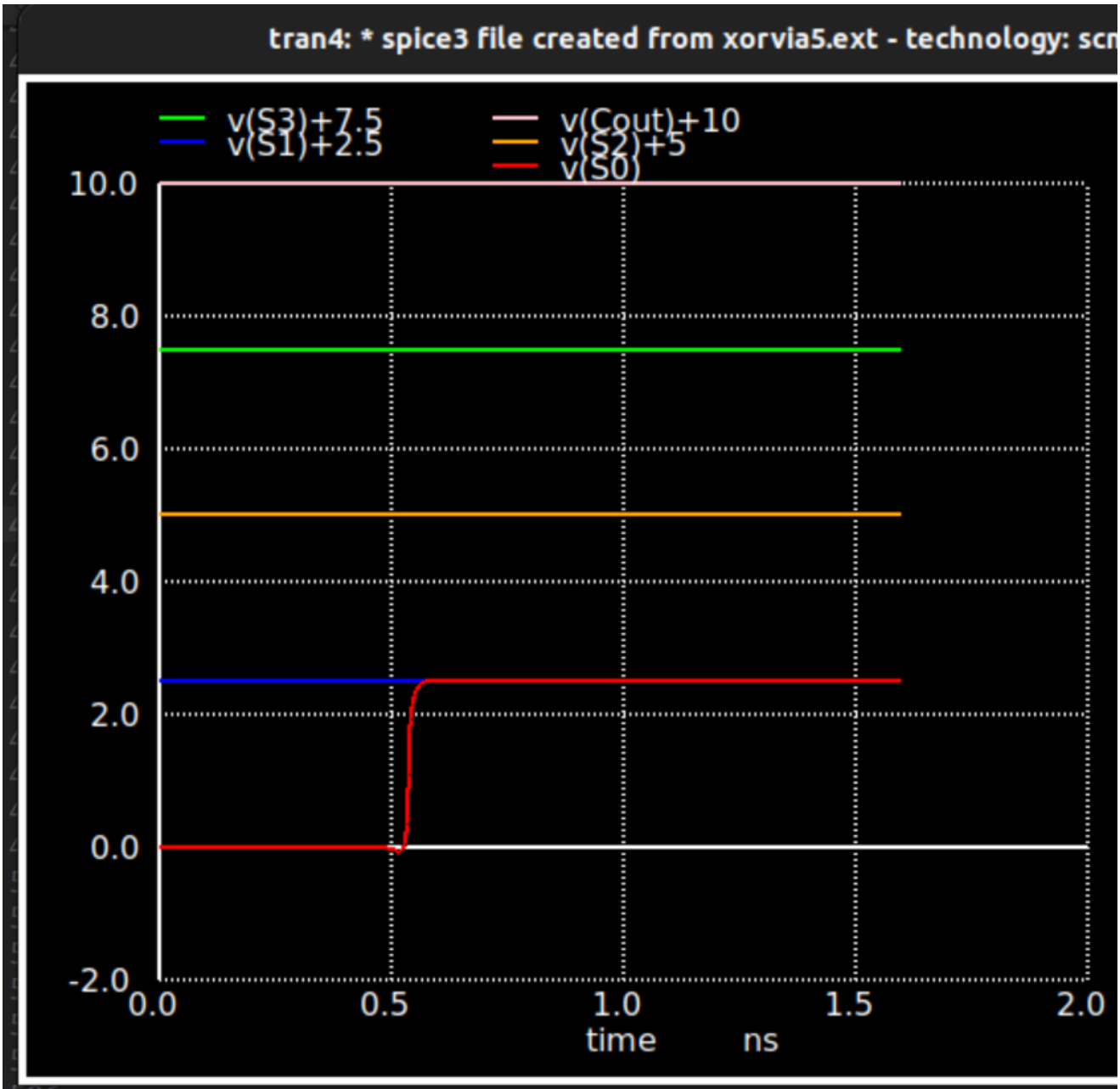


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512 Vin3 Cin gnd PULSE(0, 2.5, 200p, 400p, 400p, 800p, 1600p)
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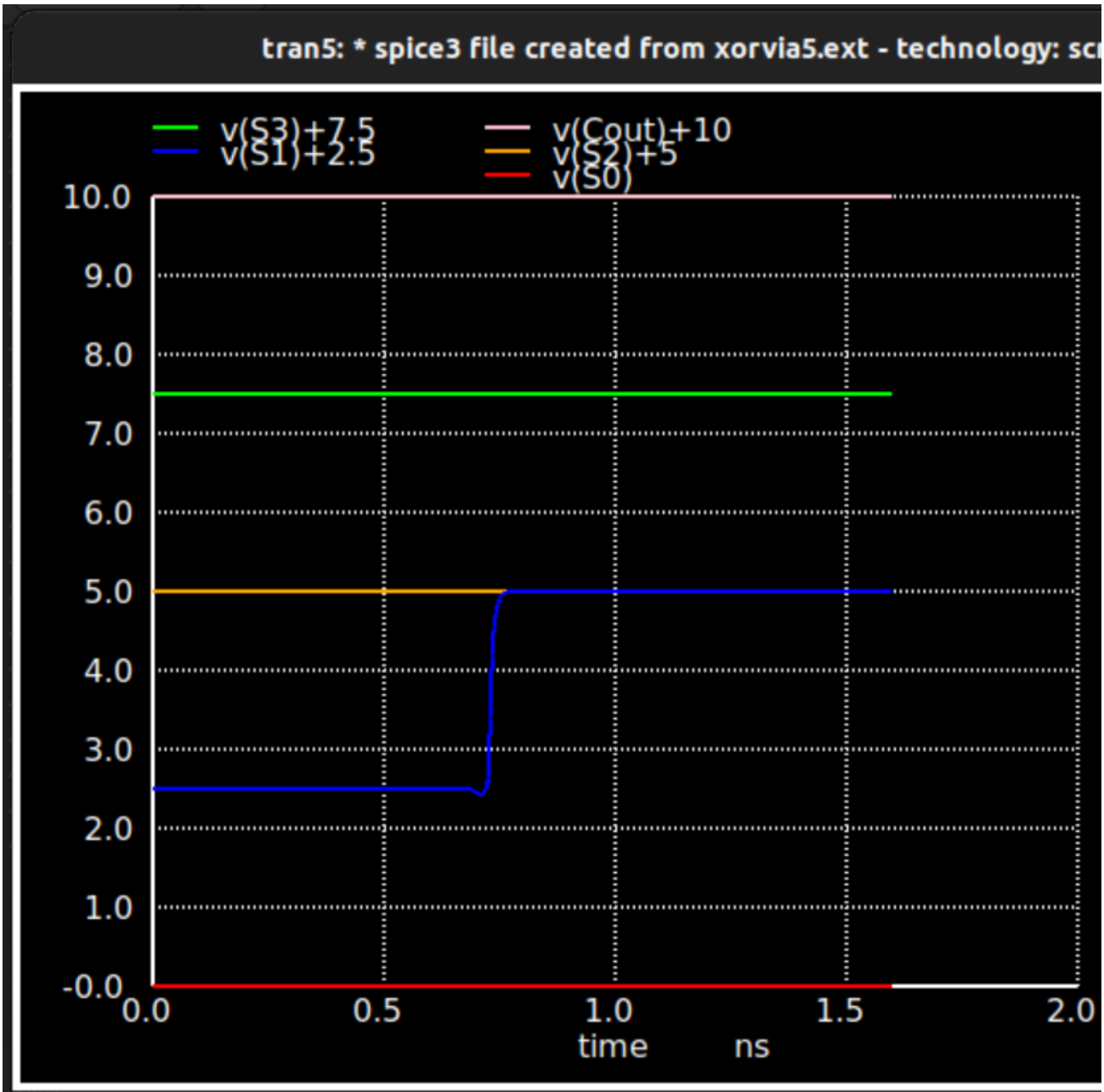


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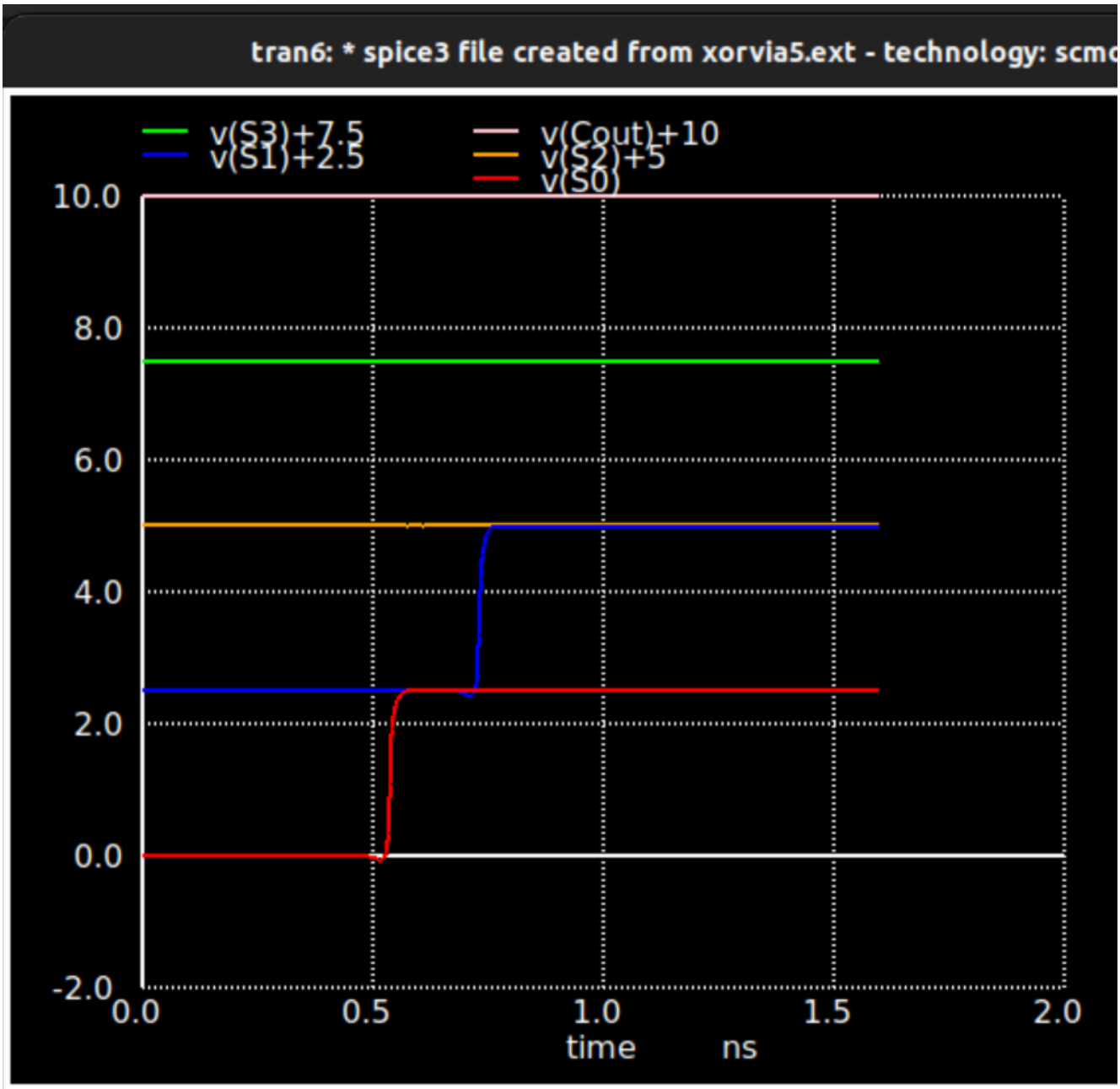


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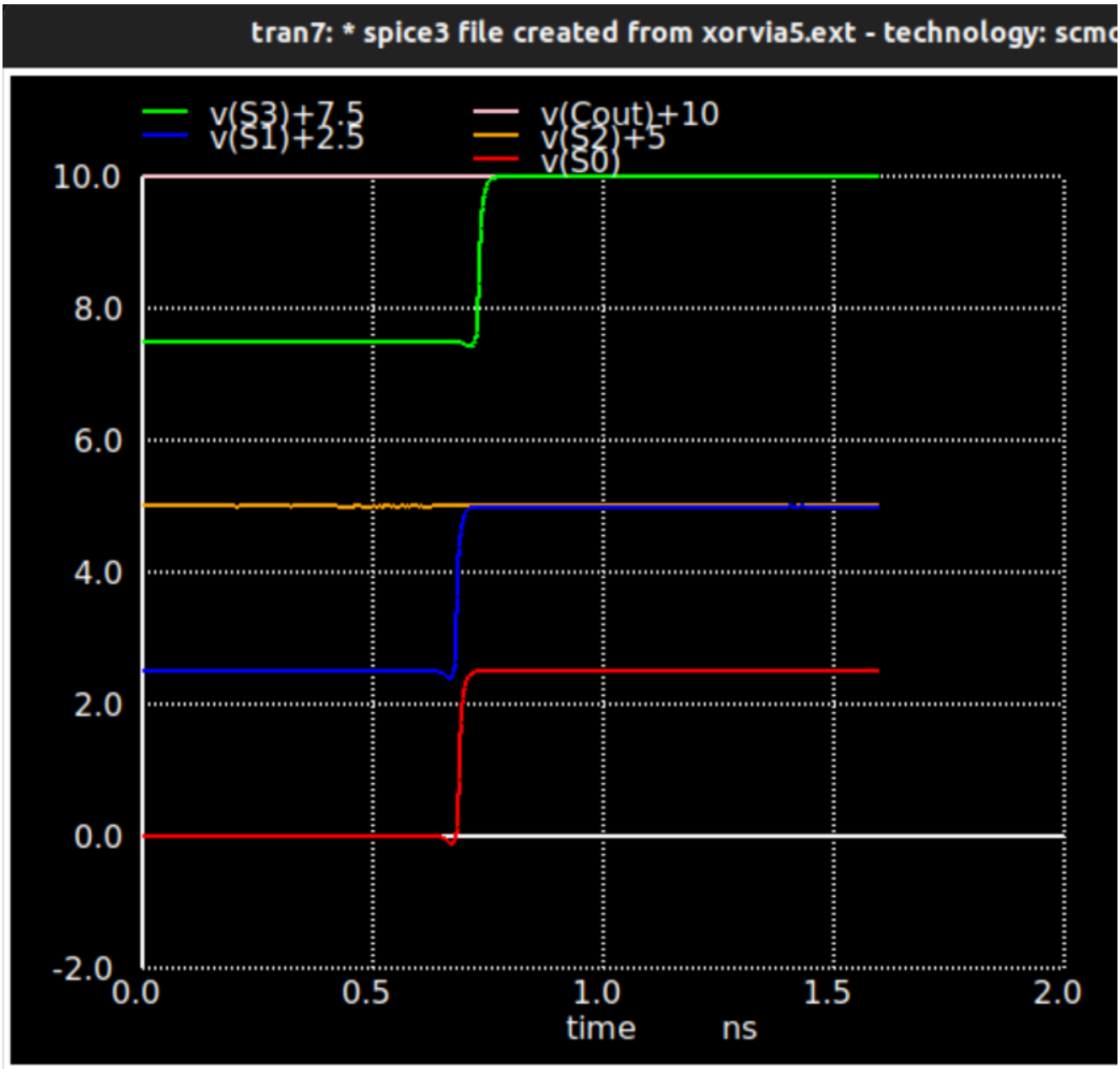


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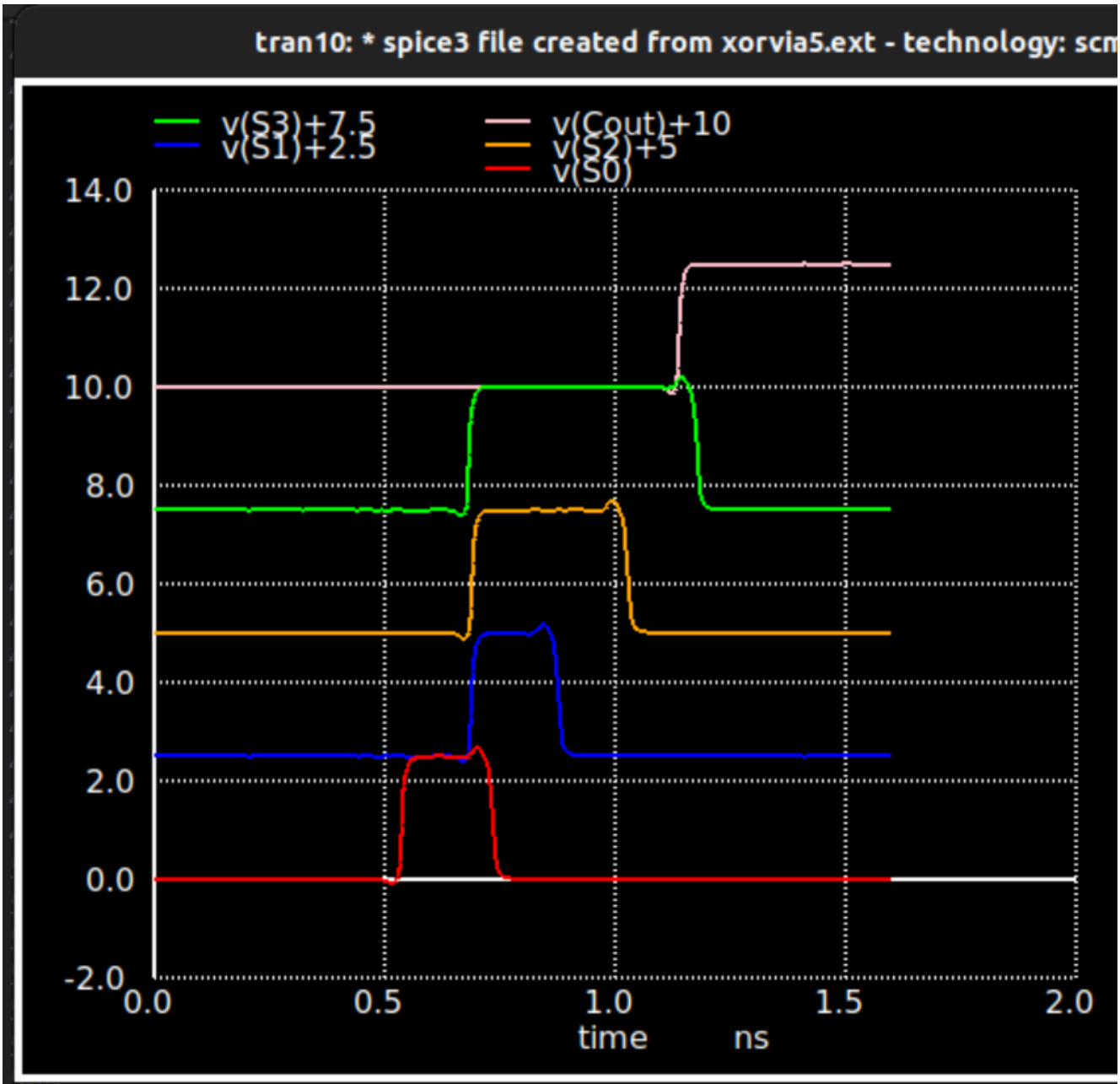


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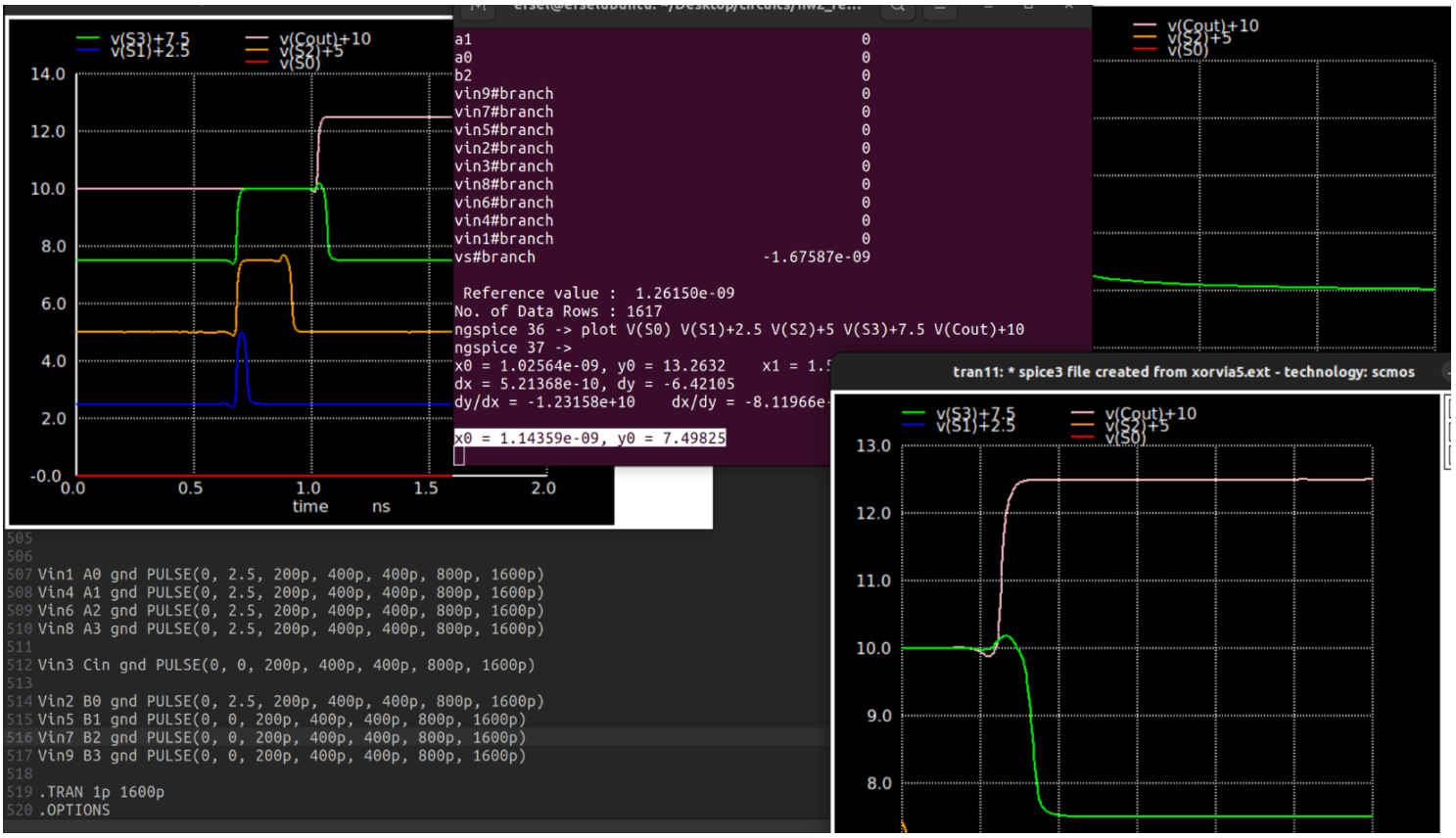
Critical Path Plot : 1111 and 0001 addition.



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Size of the layout

- Width = 73.8 micron
- Height = 31.92 micron