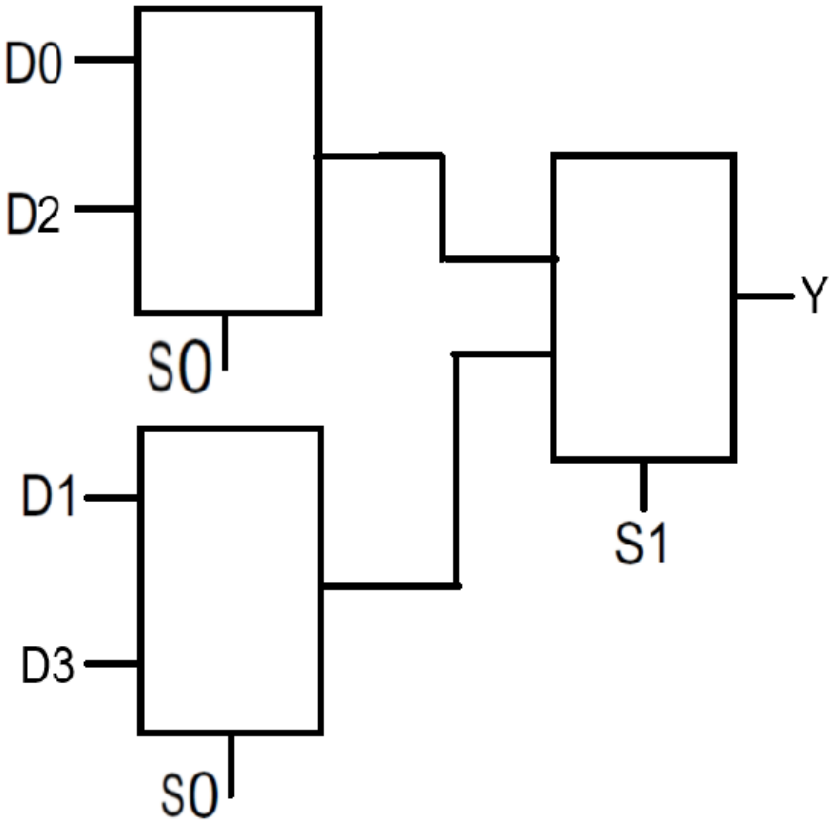
CSE436 Digital Integrated Circuits

Assignment 3 – Report

Ersel Celal Eren

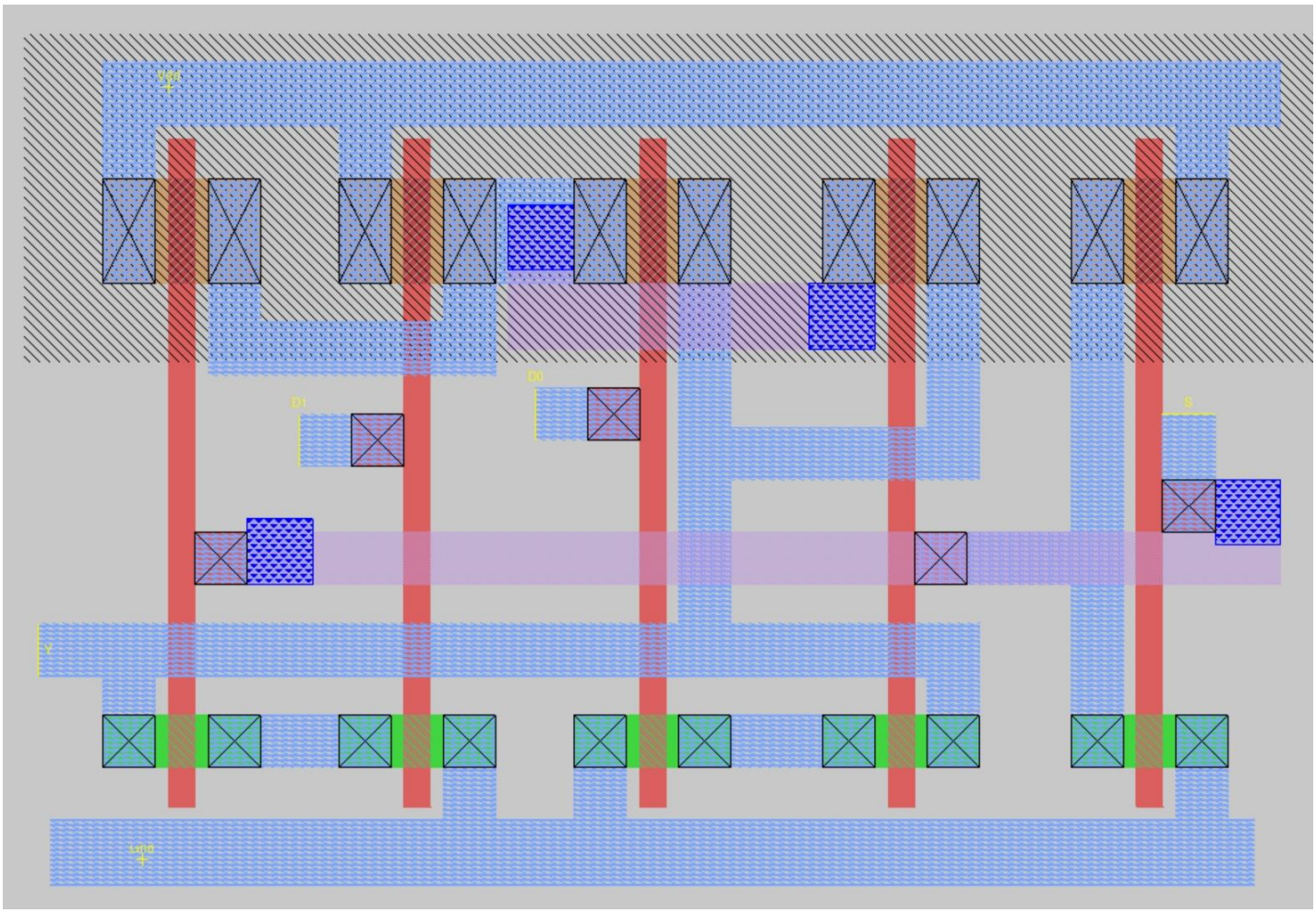
1901042673

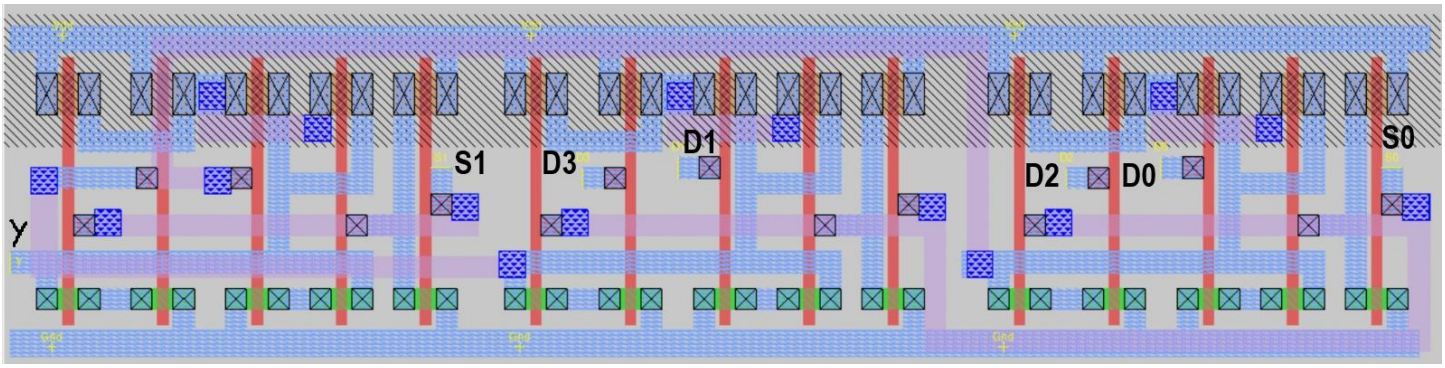
I have designed 2x1 inverting mux and then combined 3 of them to get 4x1 Mux. After designed the layout, I realized that at 1st version of my design when S0 = 0 and S1 = 1, mux selects D2 instead of D1 and when S0 = 1 and S1 = 0, mux selects D1 instead of D2. Then I replaced the labels of D2 and D1 in Magic layout and I get the following structure. Now this design is correctly working as it should.



==========

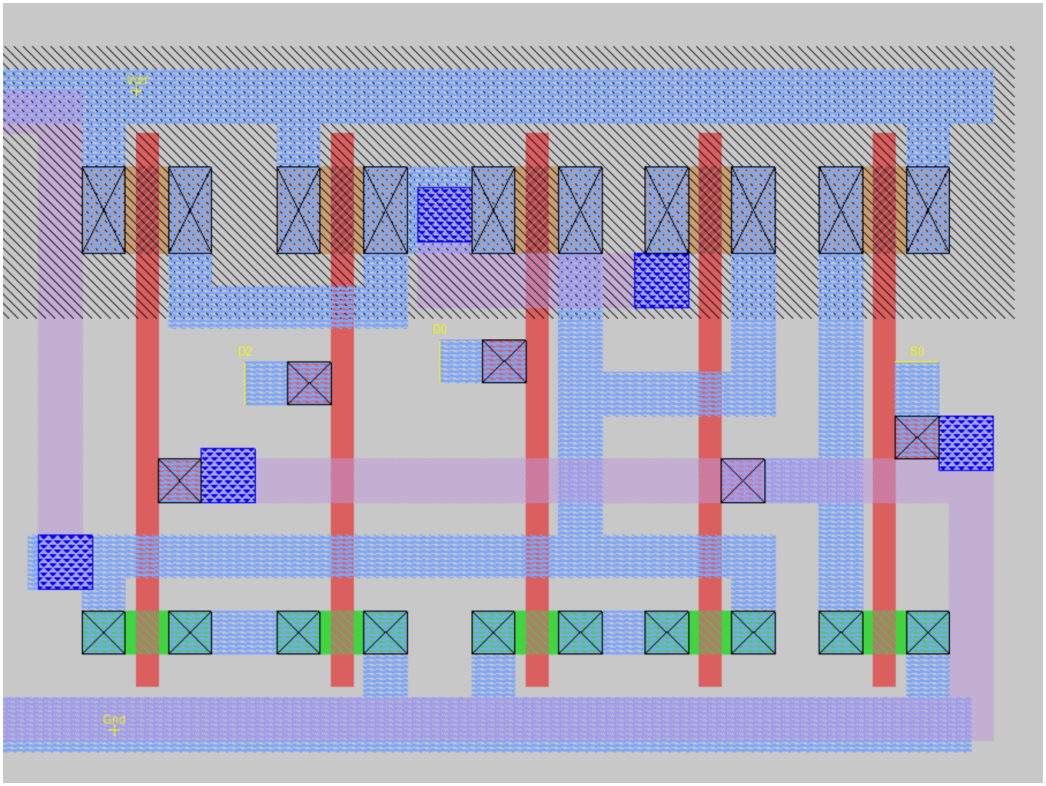
Here the following is Magic layout of 4x1 Mux using 3 2x1 Mux.





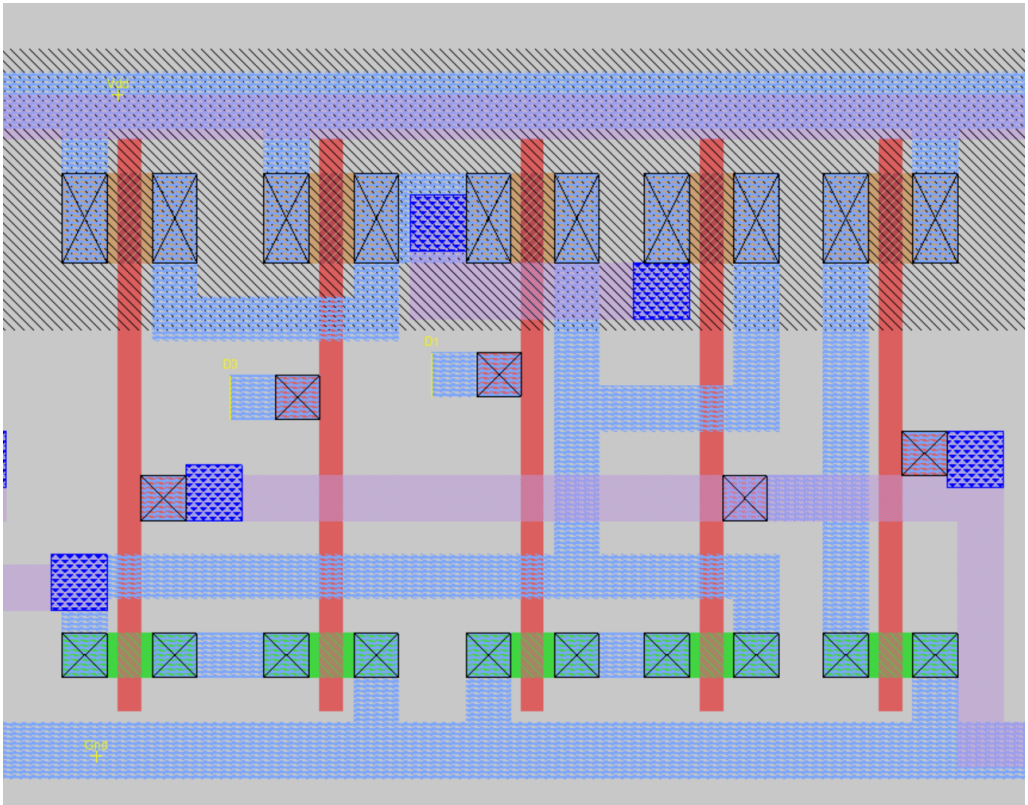
==========

First 2x1 Mux



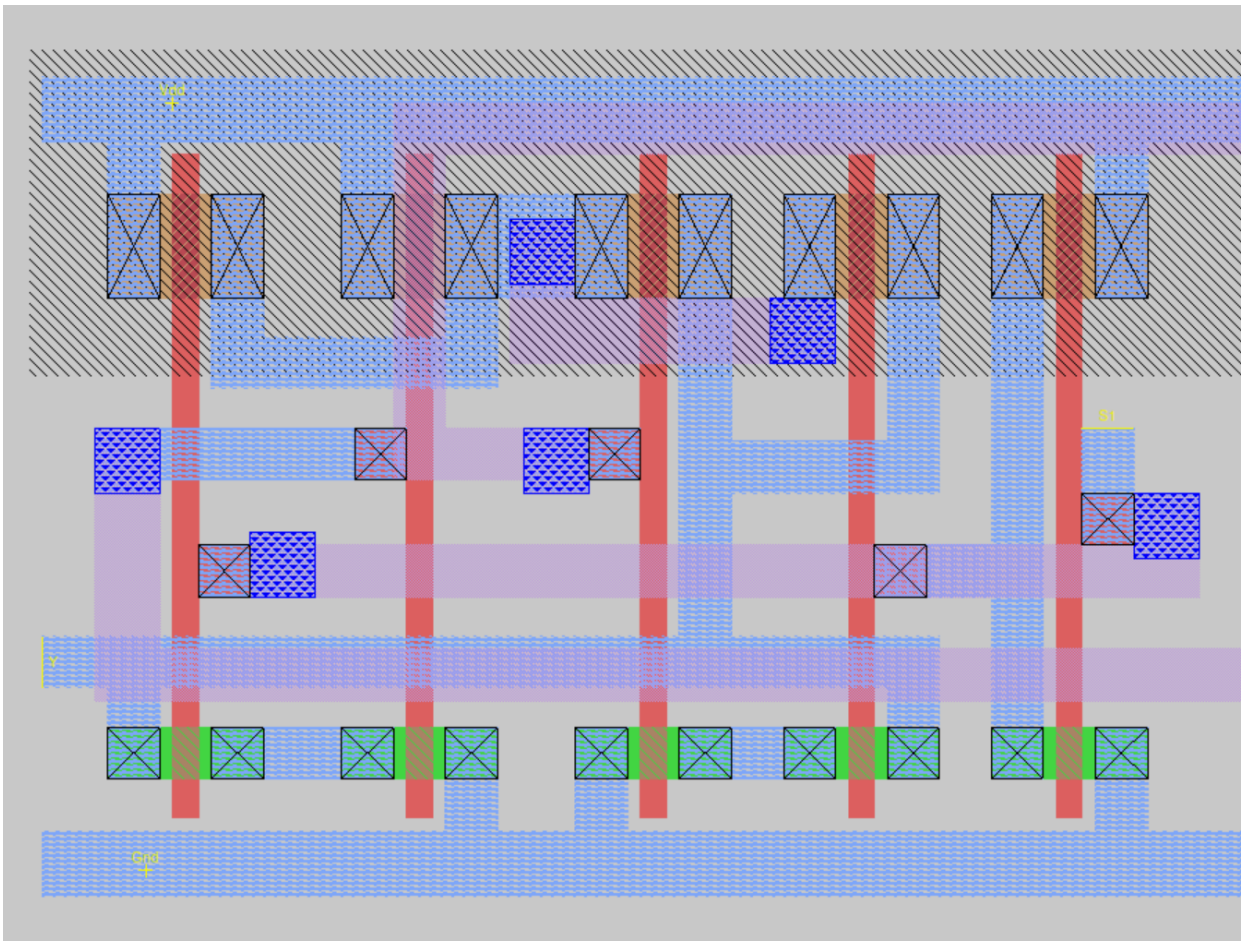
==========

Second 2x1 Mux



==========

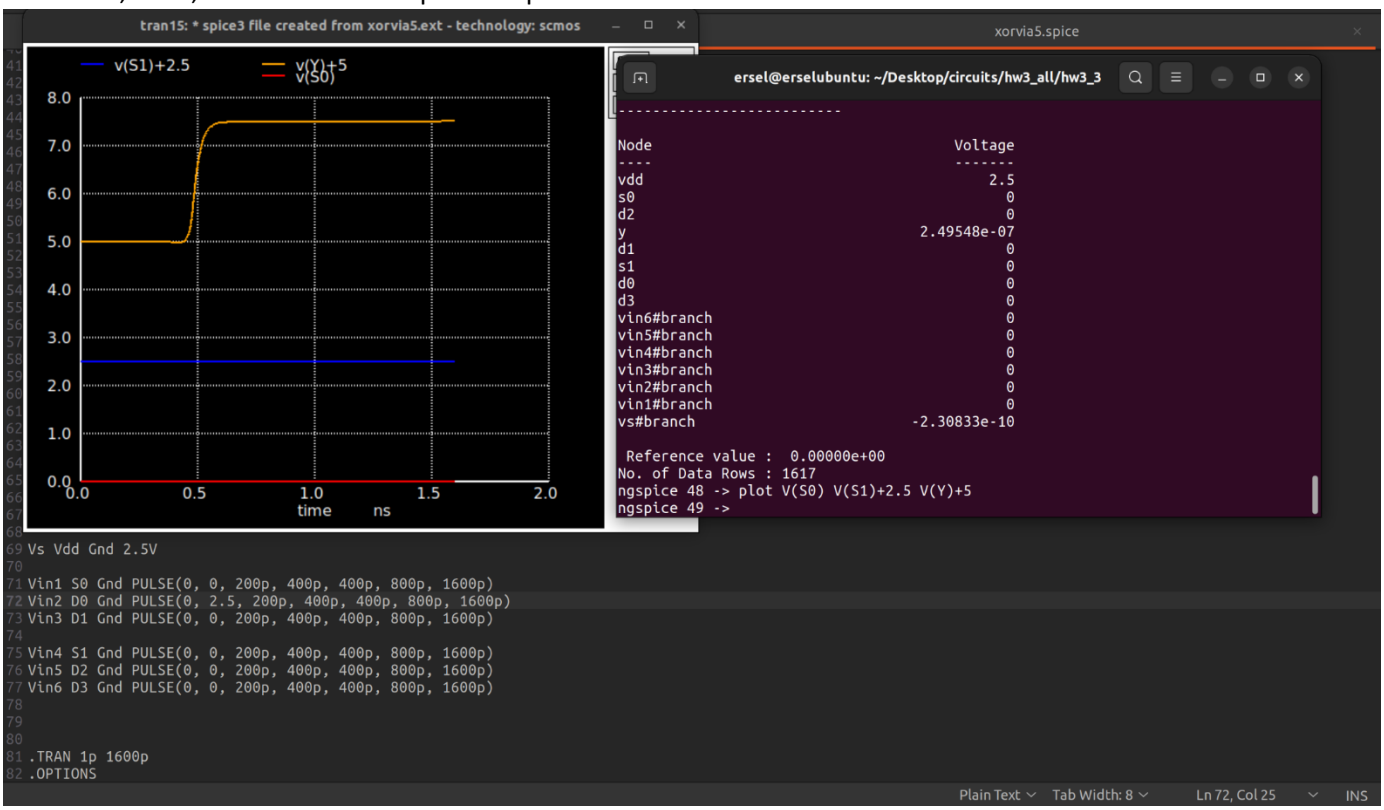
Third 2x1 Mux



Functionality Tests

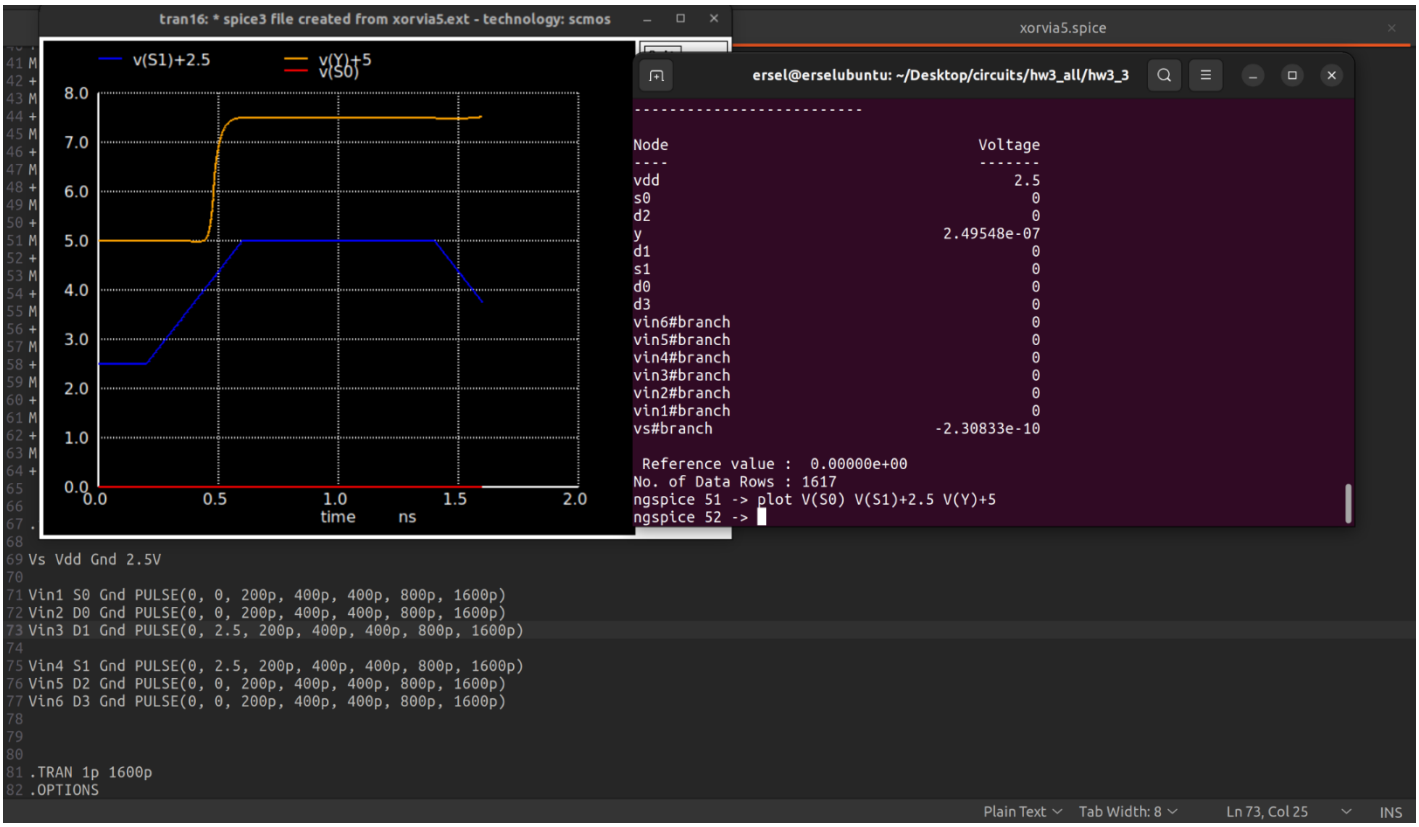
==========

For S0 = 0, S1=0, mux selects D0 input as expected.



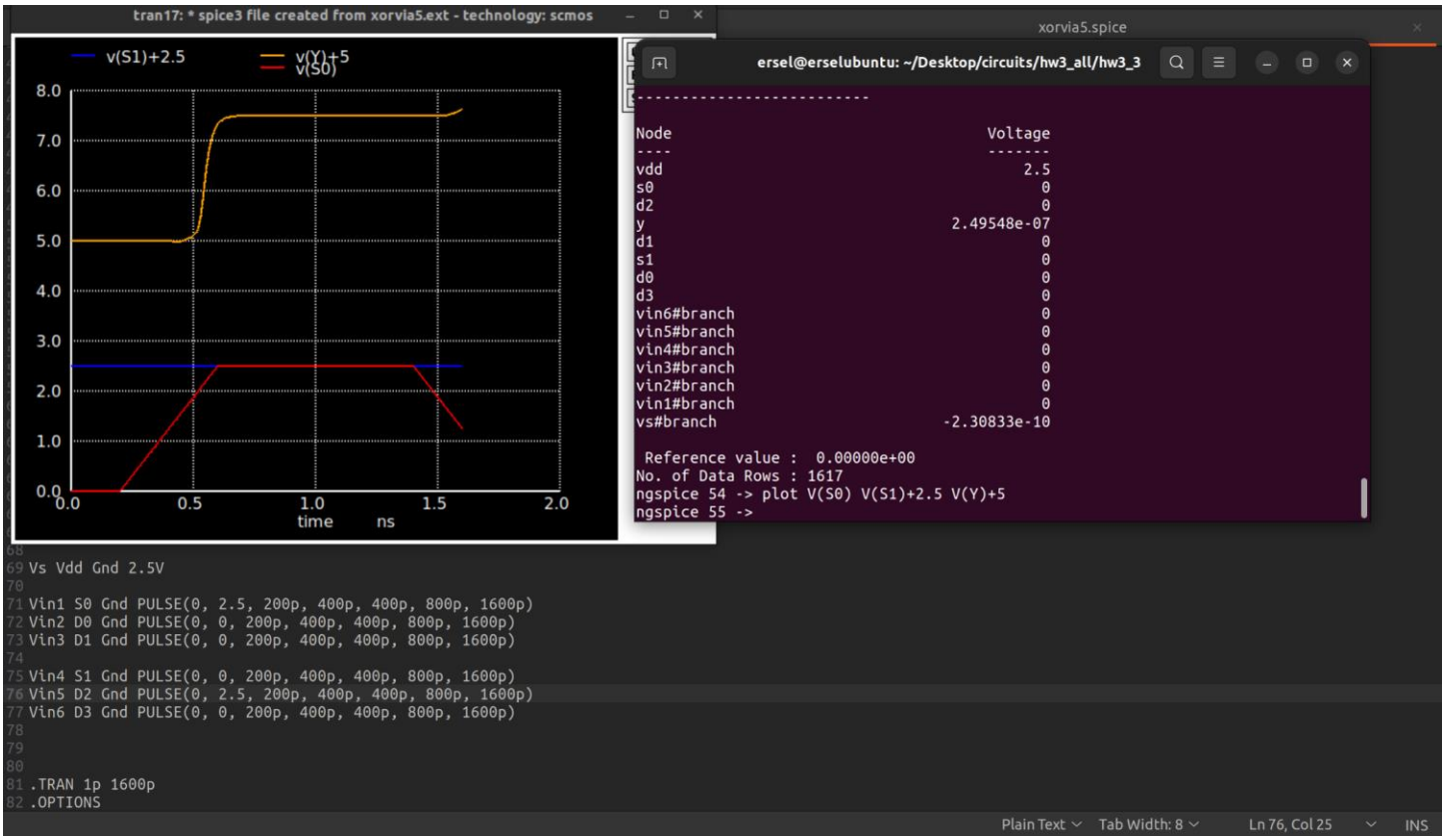
==========

For S0=0 and S1=1, mux selects D1 input as expected.



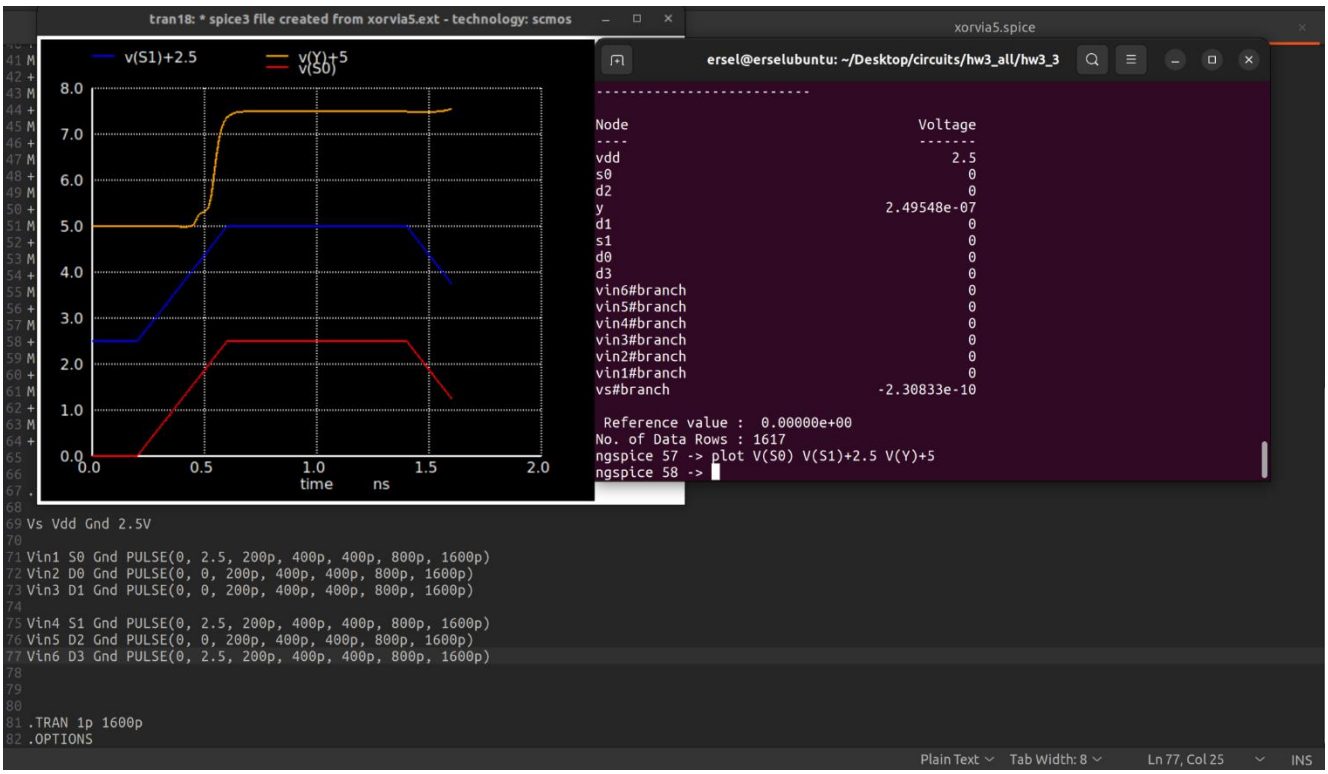
==========

For S0 = 1 and S1 = 0, mux selects D2 input as expected.



==========

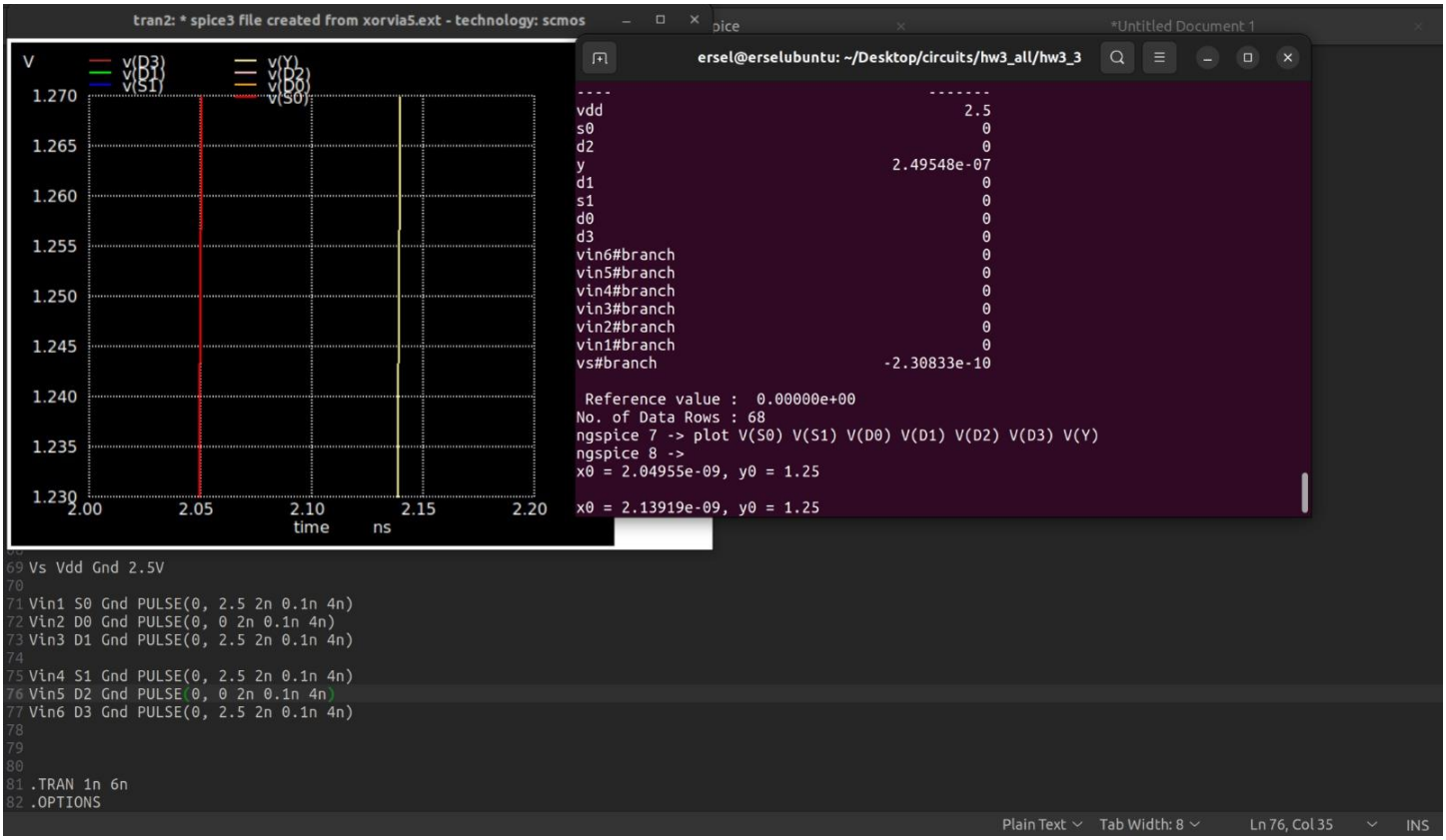
For S0 = 1 and S1 = 1, mux selects D3 input as expected.



==========

Critical Path Delay

I though occurs when
S0 = 1 | S1 = 1
D0 = 0 | D1 = 1 | D2 = 0 | D3 = 1
Since in my design places of D1 and D2 are reversed, you may consider D1 = 0 and D2 = 1 in worst case.



Delay is 0.08964 nanoseconds.