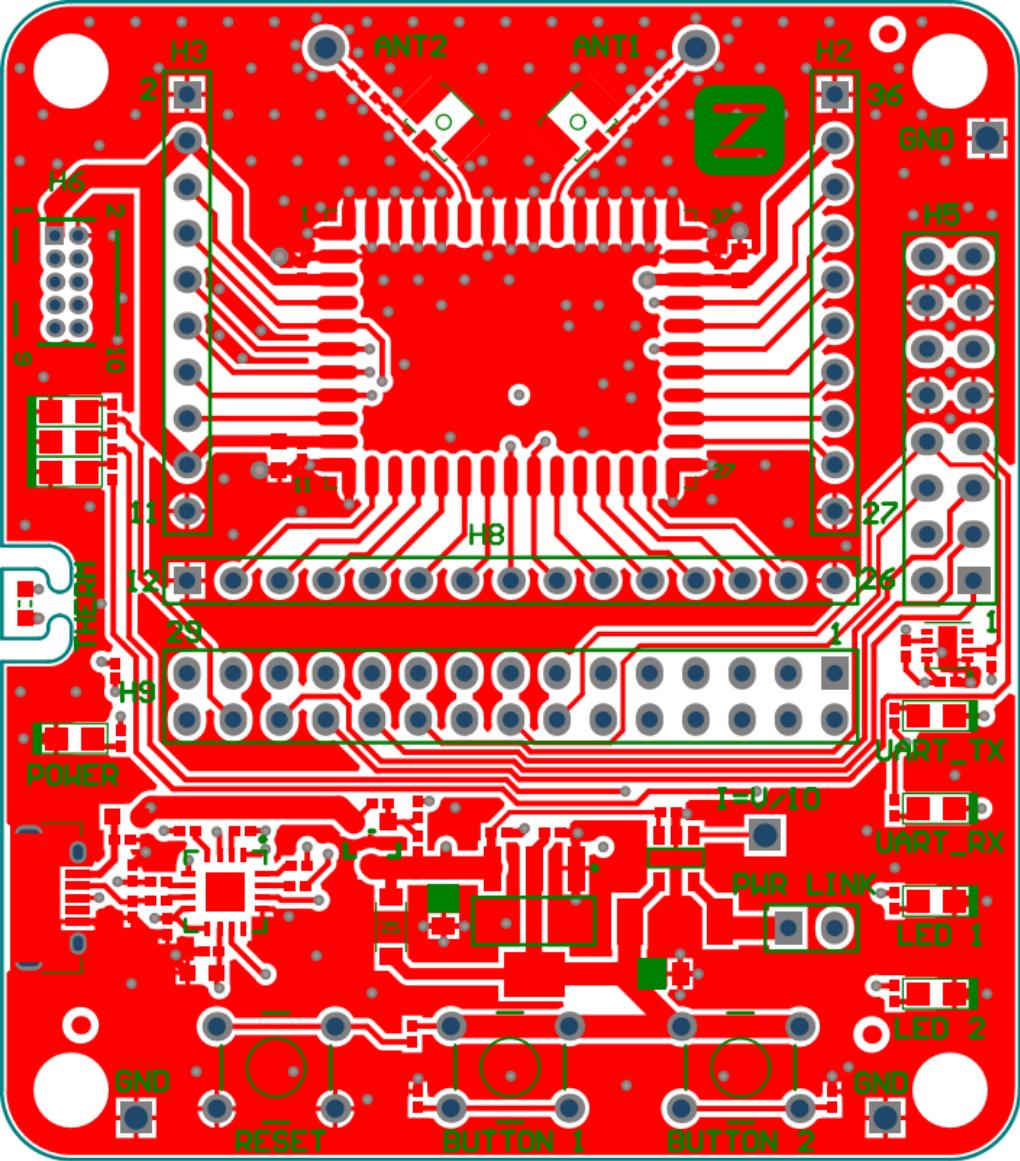
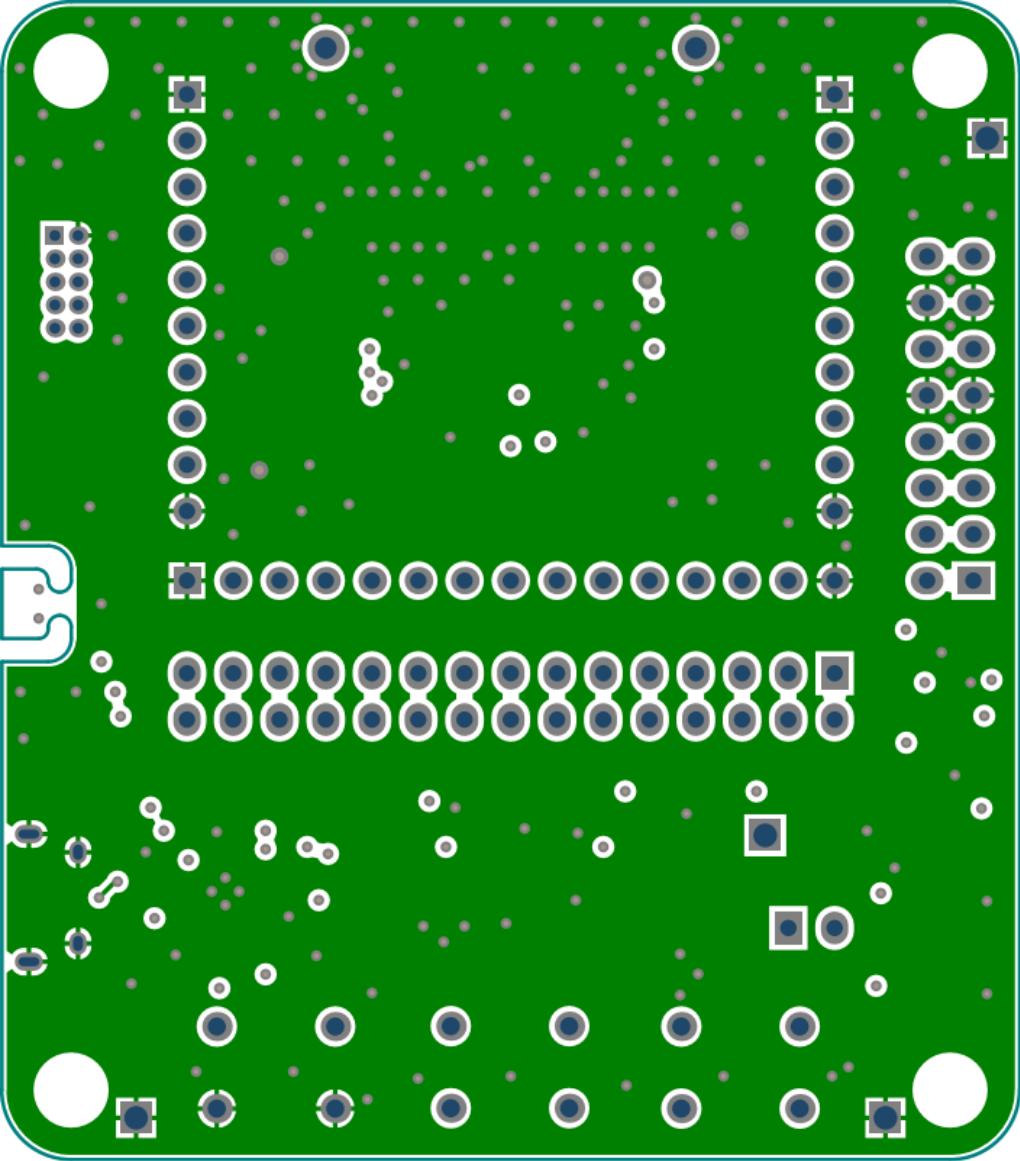


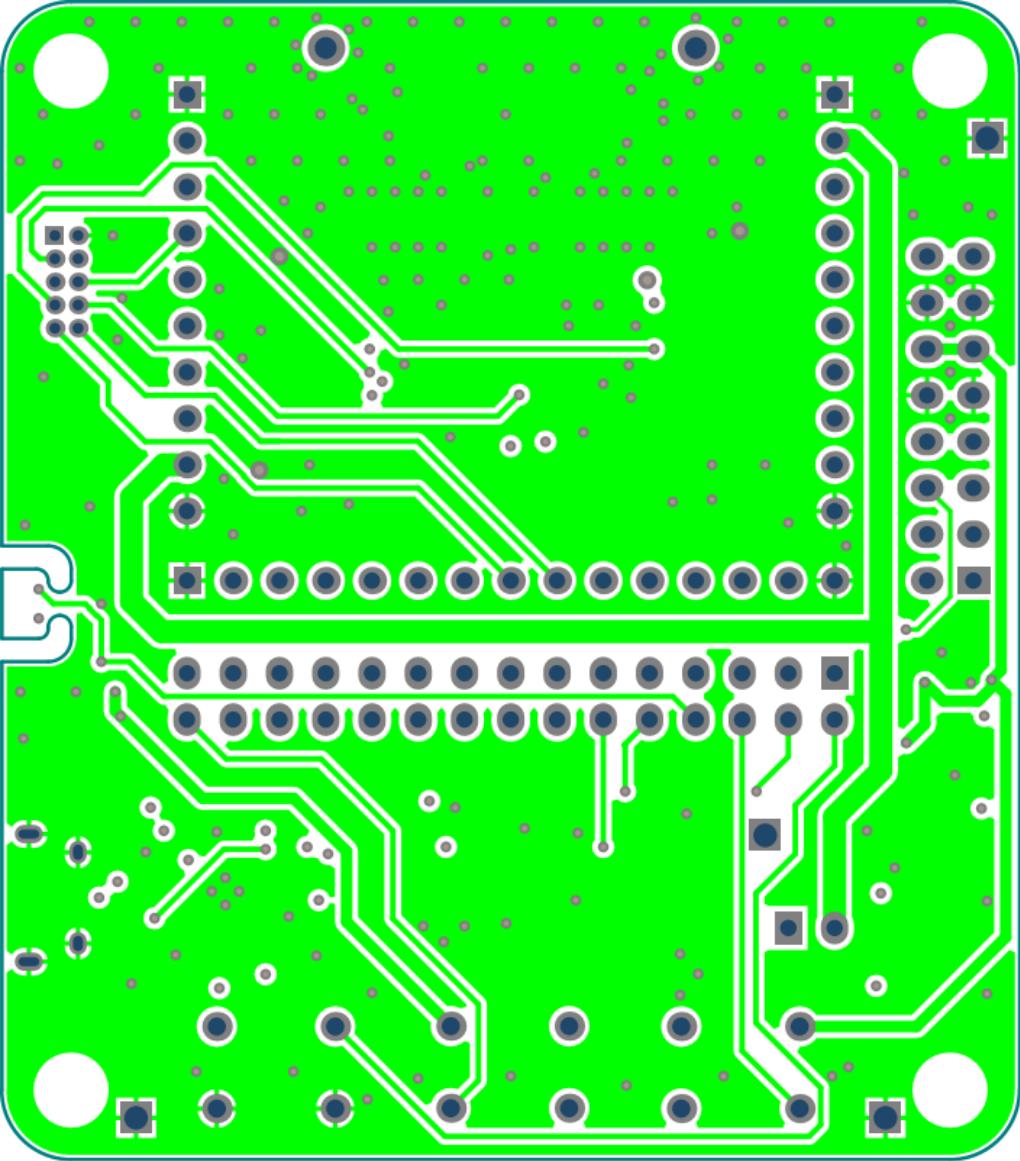
Top Overlay



Top Overlay



GND1



GND2

1ЯТИЕ

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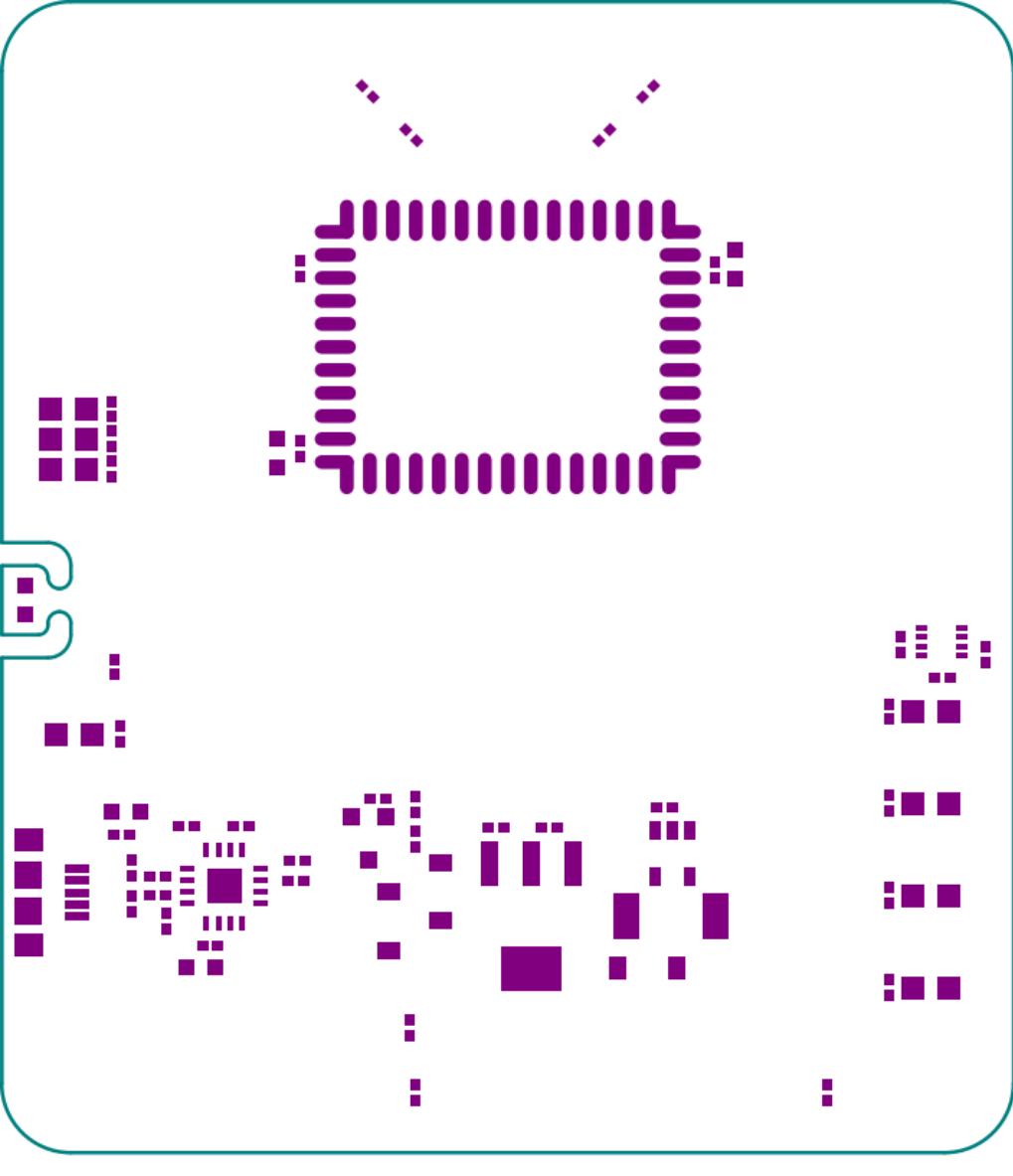
NAME: **MARYA**
#ART: **WMAx06-E03**

I

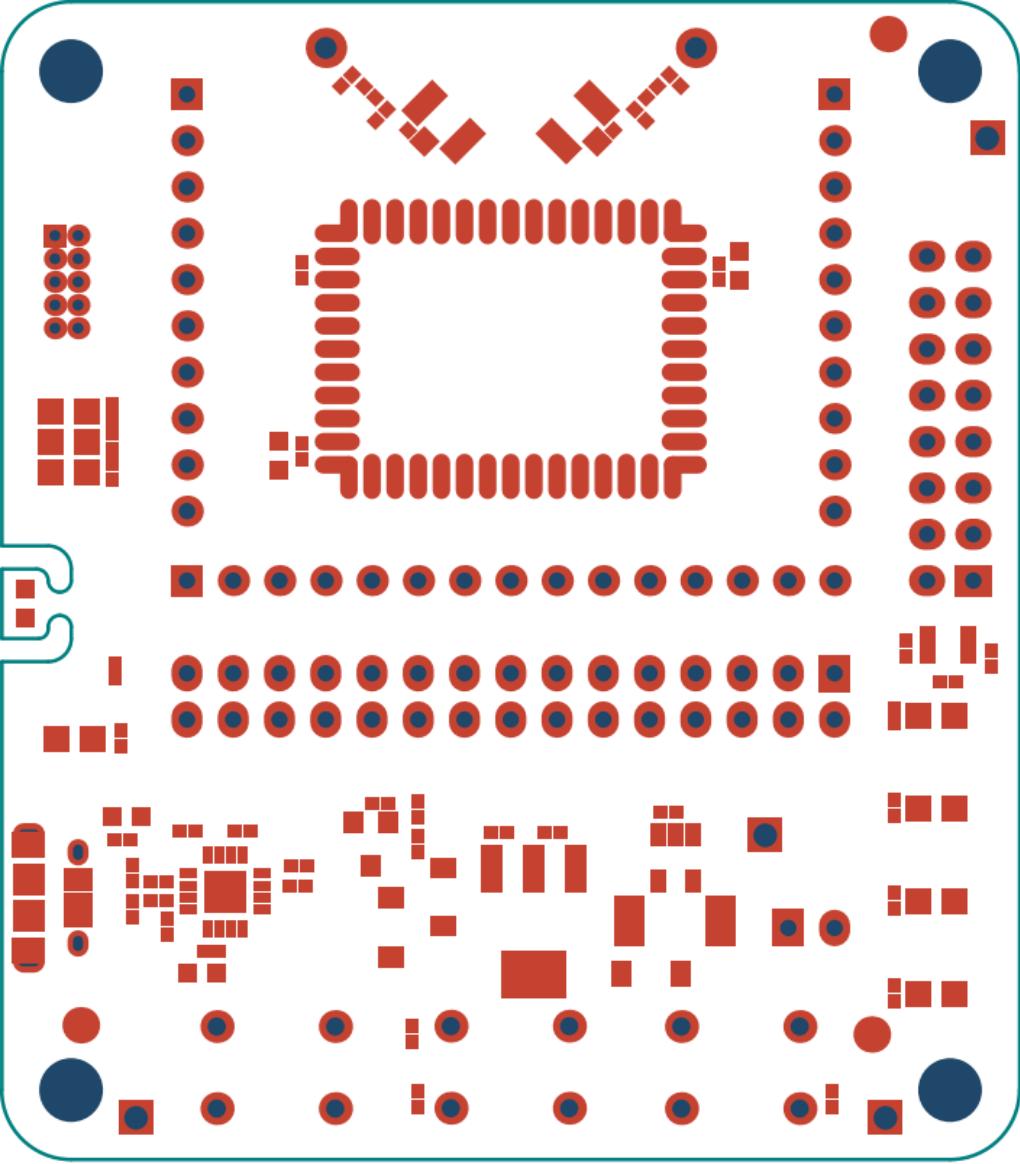
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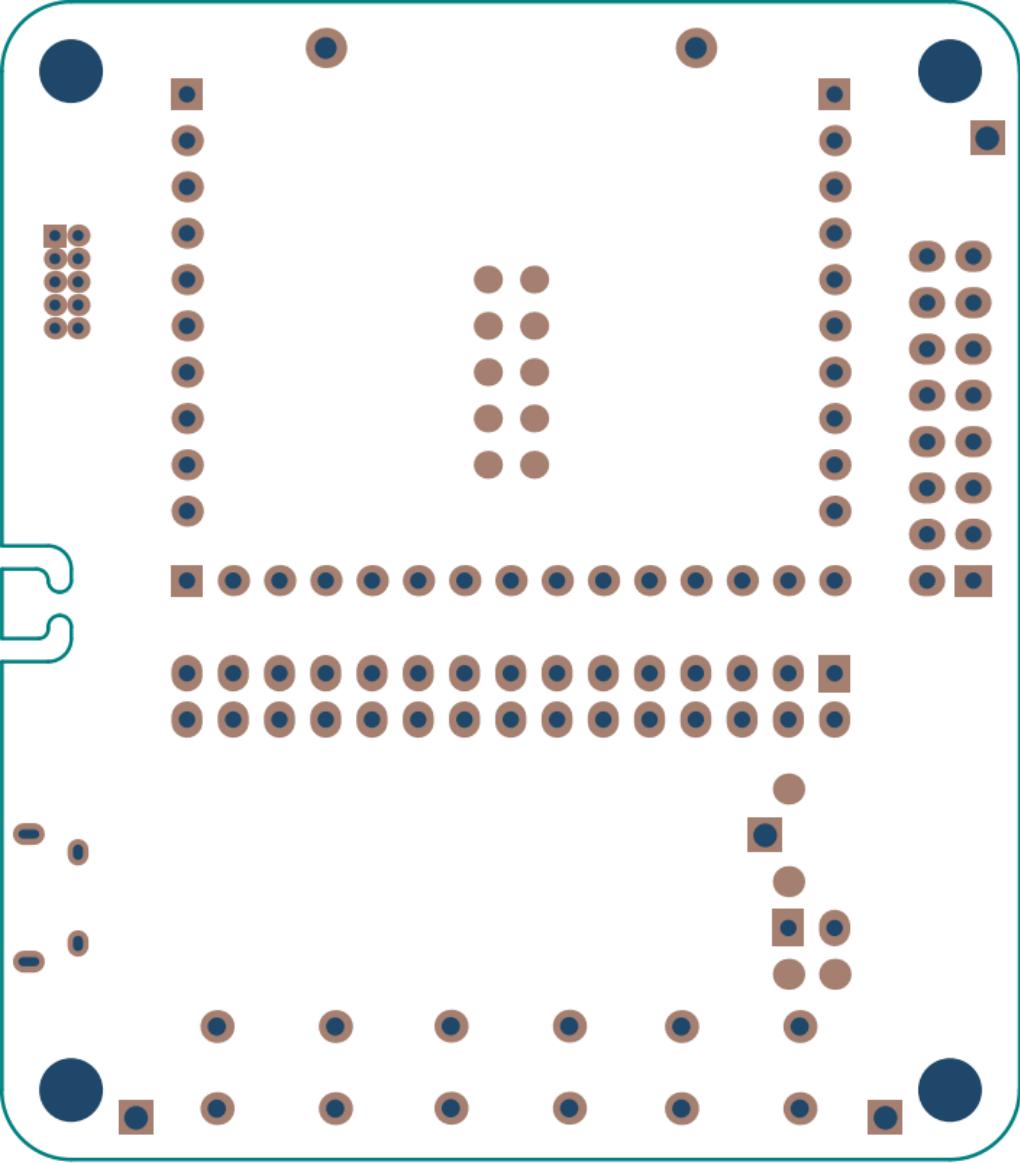


Top Paste



Top Solder

Bottom Paste



Bottom Solder

NOTES: UNLESS OTHERWISE SPECIFIED

1. SPECIFICATIONS/TOLERANCES:

- A. FABRICATE PER IPC-6012, CLASS 2, USING PROVIDED DATA FILES Moray_Rev4.ZIP
- B. ALL SPECIFICATIONS USED SHALL BE PER THEIR LATEST REVISIONS.
- C. THE DIMENSIONS OF CIRCUIT FEATURES IN THE PROVIDED DATA MAY BE ADJUSTED ONLY TO COMPENSATE FOR PROCESS TOLERANCES; ADDING, REMOVING OR RELOCATING CIRCUIT FEATURES IS NOT ALLOWED
- D. REMOVE ALL BURRS AND BREAK SHARP EDGES, .381 [.015] MAX RADIUS.
- E. PARENTHETICAL INFORMATION IS FOR REFERENCE ONLY.
- F. REPAIR OF PCB DEFECTS IS NOT PERMITTED.

2. DIELECTRIC MATERIAL:

- A. DIELECTRIC MATERIAL SHALL BE PER IPC-4101/99, /124, /126 OR /129 (RoHS COMPLIANT EPOXY-GLASS)
- B. MINIMUM DIELECTRIC THICKNESS SHALL BE .051 [.002] FOR REFERENCED STACK-UP DIMENSIONS OF .076 [.003] OR GREATER; IPC-6012 REQUIREMENTS SHALL OTHERWISE APPLY. SINGLE-PLY CONSTRUCTION IS ALLOWED.
- C. SEE LAYER STACK-UP FOR REQUIRED COPPER WEIGHTS AND THE FINISHED PCB THICKNESS, IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.
- D. FINISHED PCB THICKNESS SHALL BE MEASURED OVER LANDS AND/OR CONDUCTORS NOT COVERED BY SOLDER MASK. IF SPECIFIED, 1/3 OZ. STARTING FOIL MAY BE ACHIEVED BY 1/2 OZ. FOIL REDUCTION.

3. DRILLING:

- A. VIA DIAMETERS SHALL BE VERIFIED BEFORE PLATING; ALL OTHER HOLE DIAMETERS ARE FINISHED DIMENSIONS.
- B. LAYER-TO-LAYER MISREGISTRATION SHALL BE .127 [.005] MAXIMUM.

4. SOLDER MASK:

- A. APPLY LPI SOLDER MASK OVER BARE COPPER USING PROVIDED DATA.
- B. SOLDER MASK SHALL BE PER IPC-SM-840, CLASS T, COLOR ORANGE
- C. THE DIMENSIONS OF SOLDER MASK-DEFINED PADS ON PLANES AND/OR WIDE CONDUCTORS SHALL NOT BE MODIFIED.

5. SILKSCREEN/MARKING:

- A. SILKSCREEN PCB PER PROVIDED DATA USING PERMANENT, NON-CONDUCTIVE INK, COLOR WHITE.
- B. SUPPLIER ID AND TRACEABILITY INFORMATION SHALL NOT BE APPLIED ON ANY LAYER OF THE PCB
- C. INK SHALL NOT BE APPLIED TO ANY SOLDERABLE SURFACE OR TOP LAYER. USING PROVIDED DATA.

6. ELECTRICAL TEST:

- A. DESIGN VERIFICATION SHALL BE DONE PRIOR TO PCB FABRICATION USING GERBER DATA AND AN IPC-D-356 NETLIST.
- B. ALL PCB'S SHALL BE 100% ELECTRICALLY TESTED FOR OPENS AND SHORTS
- C. APPLY TEST STAMP IN NON-LEGEND AREA ON BOTTOM SIDE OF PCB.

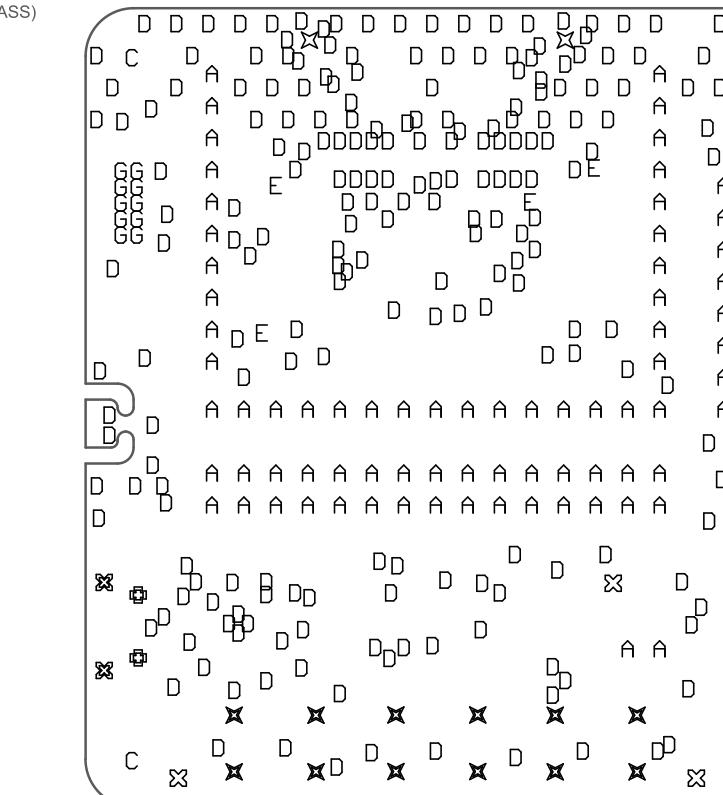
7. FINAL FINISH:

- 7A. FINAL FINISH SHALL BE ELECTROLESS NICKEL/IMMERSION GOLD (ENIG) PER IPC-4552.

8. IMPEDANCE:

- A. IMPEDANCE TOLERANCE SHALL BE +/- 10%.
- B. SEE LAYER STACK-UP FOR IMPEDANCE REQUIREMENTS.

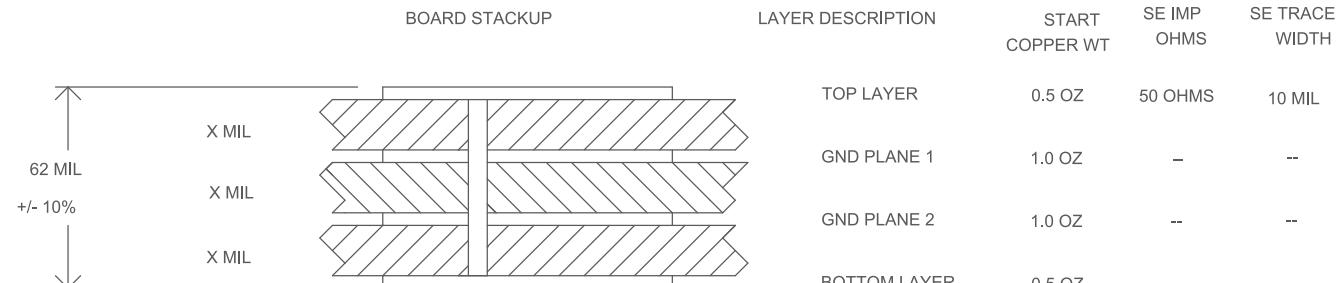
- 9. IF PANELIZATION SPECIFICATIONS ARE PROVIDED, THE PCB'S SHALL BE DELIVERED IN PANEL FORM. HOWEVER, THESE SPECIFICATIONS MAY BE REPLACED BY SUPPLIER PREFERRED (SPECIFICATIONS AS APPROVED).



Drill Drawing

Symbol	Hole Count	Finished Hole Size	Plated	Hole Type
X	2	19.69mil <0.500mm>	PTH	Slot
+	2	21.65mil <0.550mm>	PTH	Slot
X	2	47.24mil <1.200mm>	PTH	Round
E	4	19.69mil <0.500mm>	PTH	Round
X	4	51.18mil <1.300mm>	PTH	Round
C	4	137.80mil <3.500mm>	NPTH	Round
G	10	23.62mil <0.600mm>	PTH	Round
X	12	39.37mil <1.000mm>	PTH	Round
A	83	35.43mil <0.900mm>	PTH	Round
D	232	11.81mil <0.300mm>	PTH	Round
355 Total				

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



FILE EXTENSIONS:

- *.GTO - Top Overlay (Silkscreen)
- *.GTS - Top Solder Mask
- *.GTP - Top Solder Paste
- *.GBS - Bottom Solder Mask
- *.GD1 - Drill Drawing
- *.GG1 - Drill Guide
- *.GKO - Keep Out
- *.TXT - NC Drill Top-Bottom

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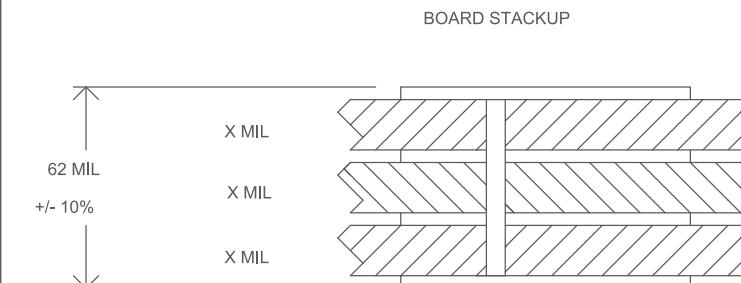
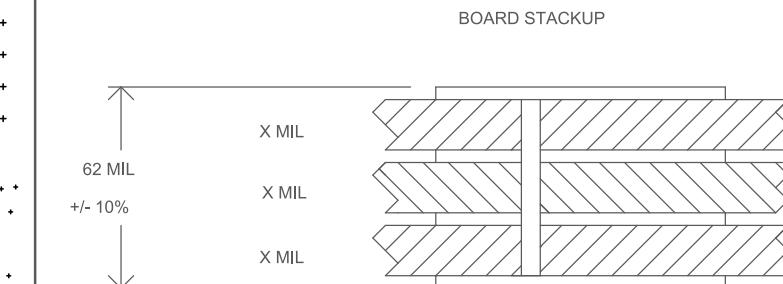
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Drill Guide

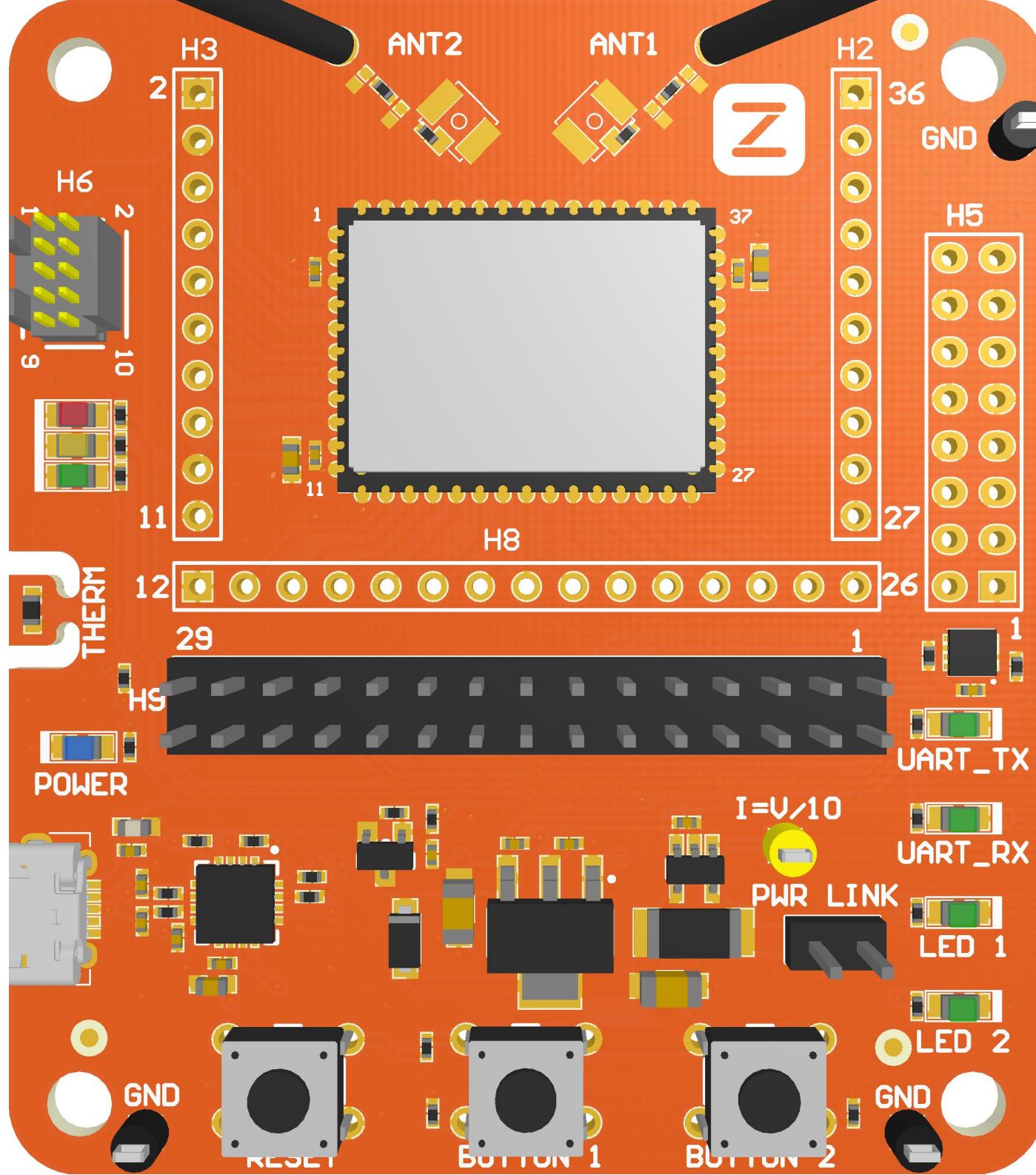


Project:	Moray (AMW006-E03)
Company:	Zentri
Drawn By:	Chad O'Neill
PCB Num:	90-002-0025-040
Date:	8/12/2015 Rev: 4



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I
GND
VDD GND

NAME	MORAY
PART#	AMWx06-E03.4