TPS20xxC and TPS20xxC-2 Current Limited, Power-Distribution Switches

1 Features

- Single Power Switch Family
- Pin-for-Pin With Existing TI Switch Portfolio
- Rated Currents of 0.5 A, 1 A, 1.5 A, 2 A
- ±20% Accurate, Fixed, Constant Current Limit
- Fast Overcurrent Response: 2 µs
- Deglitched Fault Reporting
- Selected Parts With (TPS20xxC) and Without (TPS20xxC-2) Output Discharge
- Reverse Current Blocking
- Built-In Soft Start
- Ambient Temperature Range: –40°C to 85°C
- UL Listed and CB-File No. E169910

2 Applications

- USB Ports and Hubs, Laptops, and Desktops
- High-Definition Digital TVs
- Set-Top Boxes
- Short-Circuit Protection

3 Description

The TPS20xxC and TPS20xxC-2 power-distribution switch family is intended for applications, such as USB, where heavy capacitive loads and short circuits are likely to be encountered. This family offers multiple devices with fixed current-limit thresholds for applications from 0.5 A to 2 A.

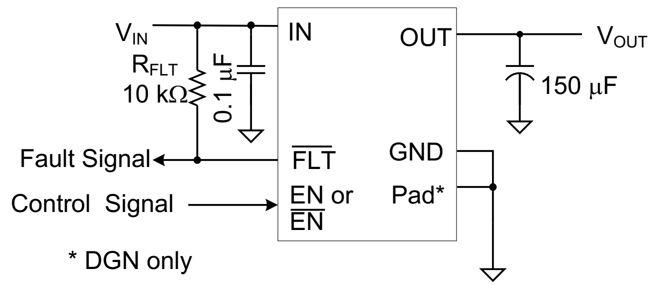
The TPS20xxC and TPS20xxC-2 family limits the output current to a safe level by operating in a constant-current mode when the output load exceeds the current limit threshold. This provides a predictable fault current under all conditions. The fast overload response time eases the burden on the main 5-V supply to provide regulated power when the output is shorted. The power-switch rise and fall times are controlled to minimize current surges during turnon and turnoff.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS20xxC, TPS20xxC-2	SOT-23 (5)	2.90 mm × 1.60 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (July 2013) to Revision H — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Deleted *Devices* table (previously Table 1) 4

Changes from Revision F (August 2012) to Revision G — **Page**

- Deleted (See Table 1) from Feature: UL Listed and CB-File No. E169910 1
- Changed From: PXKI To: PYKI in the DEVICE INFORMATION table SOT23-5 (DBV) column (TPS2069C) 4
- Deleted Note 2 from : "UL listed and CB complete" 4

Changes from Revision E (April 2012) to Revision F — **Page**

- Added device TPS20xxC-2 1
- Changed Feature From: Ouput Discharge When TPS20XXC is Disabled To: Selected parts with (TPS20xxC) and without (TPS20xxC-2) Output Discharge 1
- Added devices TPS2041C, TPS2061C, TPS2065C-2, TPS2068C, and TPS2069C-2 to the Device Information table 4
- Added the TPS2069C-2 Device 4
- Added PXKI in the DEVICE INFORMATION table SOT23-5 (DBV) column (TPS2069C) 4
- Added devices TPS2041C, TPS2061C, TPS2065C-2, TPS2068C, and TPS2069C-2 to and removed Product Preview.... 4
- Added Note 1 to the RECOMMENDED OPERATING CONDITIONS table 6
- Added TPS2041C, TPS2061C, TPS2068C, TPS2065C-2 and TPS2069C-2 devices to I_{OUT} in the RECOMMENDED OPERATING CONDITIONS table 6
- Added the DBV option to Power Switch $R_{DS(on)}$ 1.5 A rated output, 25°C mΩ 7
- Added the DBV option to Power Switch $R_{DS(on)}$ 1.5 A rated output 7
- Changed I_{SO} Current Limit 7

- Added Leakage Current 7
- Added the DBV option to Power Switch $R_{DS(on)}$ 1.5 A rated output 8
- Changed I_{SO} Current Limit 8
- Added Leakage Current 8
- Changed the second para graph of the ENABLE section 15
- Added sentence to end of paragraph in the OUTPUT DISCHARGE section 16

Changes from Revision D (February 2012) to Revision E — **Page**

- Changed the POWER DISSIPATION AND JUNCTION TEMPERATURE section. Replaced paragraph " While it is recommended..." 22

Changes from Revision C (October 2011) to Revision D — **Page**

- Added Feature UL Listed and CB-File No. E169910 (See) 1
- Added table Note 2, UL listed and CB complete. 4
- Added V_{IH} and V_{IL} information to the ROC Table 6

Changes from Revision B (September 2011) to Revision C — **Page**

- Changed From: PXF1 To: PXFI and From: PSG1 To: PXGI in the DEVICE INFORMATION table MOSP-8 (DGK) column 4
- Changed TPS2000C (MSOP-8) status From: Preview To: Active in Table 1 4
- Changed the θJACustom 2 A Rated DGK value from N/A to 110.3 7
- Added Figure 45 - DGK Package PCB Layout Example 23

Changes from Revision A (July 2011) to Revision B — **Page**

- Added the DGK Package Information throughout the data sheet 4
- Changed title of Figure 30 From: NEW FIG To: TPS2065C 50 Ω Short Circuit 19

Changes from Original (June 2011) to Revision A — **Page**

- Changed the TPS2051C, TPS2065C, and TPS2069C Devices Status From: Preview To: Active 4
- Corrected pinout numbers for the 5-PIN PACKAGE 5

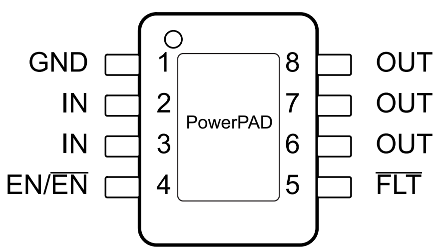
5 Device Comparison Table

MAXIMUM OPERATING CURRENT	OUTPUT DISCHARGE	ENABLE	BASE PART NUMBER	PACKAGED DEVICE AND MARKING[1]		
				MSOP-8 (DGN) PowerPAD™	SOT23-5 (DBV)	VSSOP-8 (DGK)
0.5	Y	Low	TPS2041C	—[2]	PYJI	—
0.5	Y	High	TPS2051C	—	VBYQ	—
1	Y	Low	TPS2061C	PXMI	PXLI	—
1	Y	High	TPS2065C	VCAQ	VCAQ	—
1	N	High	TPS2065C-2	PYRI	PYQI	—
1.5	Y	Low	TPS2068C	PXNI	—	—
1.5	Y	High	TPS2069C	VBUQ	PYKI	—
1.5	N	High	TPS2069C-2	PYSI	—	—
2	Y	Low	TPS2000C	BCMS	—	PXFI
2	Y	High	TPS2001C	VBWQ	–	PXGI

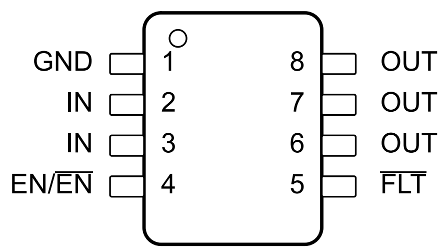
(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) "–" indicates the device is not available in this package.

6 Pin Configuration and Functions

DGN Package
8-Pin MSOP-PowerPAD
Top View



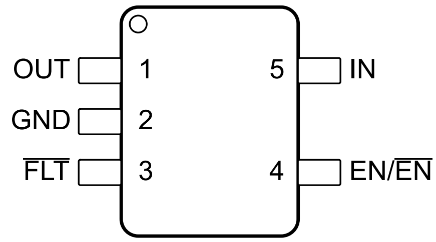
DGK Package
8-Pin VSSOP
Top View



Pin Functions - 8 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/$\overline{EN}$	4	I	Enable input, logic high turns on power switch
$\overline{FLT}$	5	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	1	—	Ground connection
IN	2, 3	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	6, 7, 8	PWR	Power-switch output, connect to load
PowerPAD (DGN Only)	PowerPAD	—	Internally connected to GND. Connect PAD to GND plane as a heatsink for the best thermal performance. PAD may be left floating if desired. See *Power Dissipation and Junction Temperature* for guidance.

DBV Package
5-Pin SOT-23
Top View



Pin Functions - 5 Pins

PIN		I/O	DESCRIPTION
NAME	NO.		
EN/$\overline{\text{EN}}$	4	I	Enable input, logic high turns on power switch
$\overline{\text{FLT}}$	3	O	Active-low open-drain output, asserted during overcurrent, or overtemperature conditions
GND	2	—	Ground connection
IN	5	PWR	Input voltage and power-switch drain; connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	1	PWR	Power-switch output, connect to load.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)(3)]

	MIN	MAX	UNIT
Voltage on IN, OUT, EN or $\overline{\text{EN}}$, $\overline{\text{FLT}}$ [(4)]	–0.3	6	V
Voltage from IN to OUT	–6	6	V
Maximum junction temperature, T_J	Internally Limited		
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Absolute maximum ratings apply over recommended junction temperature range.
(3) Voltages are with respect to GND unless otherwise noted.
(4) See *Input and Output Capacitance*.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	
		IEC 61000-4-2 contact discharge	±8000	
		IEC 61000-4-2 air-gap discharge[(3)]	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) V_{OUT} was surged on a PCB with input and output bypassing per the *Typical Application Diagram* on the first page (except input capacitor was 22 µF) with no device failures.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, IN		4.5		5.5	V
V_{EN}	Input voltage, EN or $\overline{EN}$		0		5.5	V
V_{IH}	High-level input voltage, EN or $\overline{EN}$		2			V
V_{IL}	Low-level input voltage, EN or $\overline{EN}$				0.7	V
I_{OUT}	Continuous output current, OUT[1]	TPS2041C and TPS2051C			0.5	A
		TPS2061C, TPS2065C and TPS2065C-2			1	
		TPS2068C, TPS2069C and TPS2069C-2			1.5	
		TPS2000C and TPS2001C			2	
T_J	Operating junction temperature		–40		125	°C
$I_{\overline{FLT}}$	Sink current into $\overline{FLT}$		0		5	mA

(1) Some package and current rating may request an ambient temperature derating of 85°C.

7.4 Thermal Information: SOT-23

THERMAL METRIC[1]		TPS20xxC, TPS20xxC-2		UNIT
		DBV (SOT-23)[2]	DBV (SOT-23)[3]	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	224.9	220.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	95.2	89.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.4	46.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.6	5.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.3	46.2	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W
$R_{\theta JA}$Custom	See *Power DIssipation and Junction Temperature*	139.3	134.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Rated at 0.5 A or 1 A.
(3) Rated at 1.5 A or 2 A.

7.5 Thermal Information: MSOP-PowerPAD

THERMAL METRIC[1]		TPS20xxC, TPS20xxC-2			UNIT
		DGN (MSOP-PowerPAD)[2]	DGN (MSOP-PowerPAD)[3]	DGK (VSSOP)[4]	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.1	67.1	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.3	80.8	94.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	37.2	126.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.3	5.6	24.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42	36.9	125.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	39.2	32.1	—	°C/W
$R_{\theta JA}$Custom	See *Power DIssipation and Junction Temperature*	66.5	61.3	110.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Rated at 0.5 A or 1 A.
(3) Rated at 1.5 A or 2 A.
(4) Rated at 2 A.

7.6 Electrical Characteristics: $T_J = T_A = 25°C$

Unless otherwise noted: V_{IN} = 5 V, V_{EN} = V_{IN} or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A. See *Device Comparison Table* for the rated current of each part number. Parametrics over a wider operational range are shown in *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*(1).

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(on)}$	Input – output resistance	0.5-A rated output, 25°C	DBV		97	110	mΩ
		0.5-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		96	130	mΩ
		1-A rated output, 25°C	DBV		96	110	mΩ
			DGN		86	100	
		1-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		96	130	mΩ
			DGN		86	120	
		1.5-A rated output, 25°C	DBV		76	91	mΩ
			DGN		69	84	mΩ
		1.5-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DBV		76	106	mΩ
			DGN		69	98	mΩ
		2-A rated output, 25°C	DGN, DGK		72	84	mΩ
		2-A rated output, –40°C ≤ (T_J , T_A) ≤ 85°C	DGN, DGK		72	98	mΩ
CURRENT LIMIT							
I_{OS}(2)	Current limit, See Figure 6	0.5-A rated output	TPS20xxC	0.67	0.85	1.01	A
		1-A rated output	TPS20xxC	1.3	1.55	1.8	
			TPS20xxC-2	1.18	1.53	1.88	
		1.5-A rated output	TPS20xxC	1.7	2.15	2.5	
			TPS20xxC-2	1.71	2.23	2.75	
		2-A rated output	TPS20xxC	2.35	2.9	3.4	
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A			0.01	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A				2	
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A			60	70	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A				85	
I_{lkg}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}	TPS20xxC-2		0.05	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}				2	
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}			0.1	1	µA
		–40°C ≤ (T_J , T_A) ≤ 85°C, V_{OUT} = 5 V, V_{IN} = 0 V, measure I_{VOUT}				5	
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance(3)	V_{IN} = V_{OUT} = 5 V, disabled	TPS20xxC	400	470	600	Ω

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See *Current Limit* section for explanation of this parameter.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.7 Electrical Characteristics: –40°C ≤ T_J ≤ 125°C

Unless otherwise noted:4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN} or $V_{\overline{EN}}$ = GND, I_{OUT} = 0 A, typical values are at 5 V and 25°C. See *Device Comparison Table* for the rated current of each part number.

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
POWER SWITCH							
$R_{DS(ON)}$	Input – output resistance	0.5-A rated output	DBV		97	154	mΩ
		1-A rated output	DBV		96	154	mΩ
			DGN		86	140	
		1.5-A rated output	DBV		76	121	mΩ
			DGN		69	112	mΩ
		2-A rated output	DGN, DGK		72	112	mΩ
ENABLE INPUT (EN or $\overline{EN}$)							
	Threshold	Input rising		1	1.45	2	V
	Hysteresis			0.07	0.13	0.2	V
	Leakage current	(V_{EN} or $V_{\overline{EN}}$) = 0 V or 5.5 V		–1	0	1	µA
CURRENT LIMIT							
I_{OS}(2)	Current limit, See Figure 23	0.5-A rated output	TPS20xxC	0.65	0.85	1.05	A
		1-A rated output	TPS20xxC	1.2	1.55	1.9	
			TPS20xxC-2	1.1	1.53	1.96	
		1.5-A rated output	TPS20xxC	1.6	2.15	2.7	
			TPS20xxC-2	1.6	2.23	2.86	
		2-A rated output	TPS20xxC	2.3	2.9	3.6	
t_{IOS}	Short-circuit response time(3)	V_{IN} = 5 V (see Figure 6), One-half full load → R_{SHORT} = 50 mΩ, Measure from application to when current falls below 120% of final value			2		µs
SUPPLY CURRENT							
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A			0.01	10	µA
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A			65	90	µA
I_{lkg}	Leakage current	V_{OUT} = 0 V, V_{IN} = 5 V, disabled, measure I_{VIN}	TPS20XXC-2		0.05		µA
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, measure I_{VOUT}			0.2	20	µA
UNDERVOLTAGE LOCKOUT							
V_{UVLO}	Rising threshold	V_{IN}↑		3.5	3.75	4	V
	Hysteresis(3)	V_{IN}↓			0.14		V
$\overline{FLT}$							
	Output low voltage, $\overline{FLT}$	$I_{\overline{FLT}}$ = 1 mA				0.2	V
	OFF-state leakage	$V_{\overline{FLT}}$ = 5.5 V				1	µA
$t_{\overline{FLT}}$	$\overline{FLT}$ deglitch	$\overline{FLT}$ assertion or deassertion deglitch		6	9	12	ms
OUTPUT DISCHARGE							
R_{PD}	Output pulldown resistance	V_{IN} = 4 V, V_{OUT} = 5 V, disabled	TPS20XXC	350	560	1200	Ω
		V_{IN} = 5 V, V_{OUT} = 5 V, disabled	TPS20XXC	300	470	800	
THERMAL SHUTDOWN							
	Rising threshold (T_J)	In current limit		135			°C
		Not in current limit		155			
	Hysteresis (3)				20		

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See *Current Limit* for explanation of this parameter.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

7.8 Timing Requirements: $T_J = T_A = 25°C$

				MIN	NOM	MAX	UNIT
ENABLE INPUT (EN or $\overline{EN}$)							
t_{ON}	Turnon time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↑ or $\overline{EN}$ ↓. See Figure 1, Figure 3, and Figure 4	0.5-A and 1-A Rated	1	1.4	1.8	ms
			1.5-A and 2-A Rated	1.2	1.7	2.2	
t_{OFF}	Turnoff time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↓ or $\overline{EN}$ ↑. See Figure 1, Figure 3, and Figure 4	0.5-A and 1-A Rated	1.3	1.65	2	ms
			1.5-A and 2-A Rated	1.7	2.1	2.5	
t_R	Rise time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 2	0.5-A and 1-A Rated	0.4	0.55	0.7	ms
			1.5-A and 2-A Rated	0.5	0.7	1	
t_F	Fall time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V. See Figure 2	0.5-A and 1-A Rated	0.25	0.35	0.45	ms
			1.-5A and 2-A Rated	0.3	0.43	0.55	

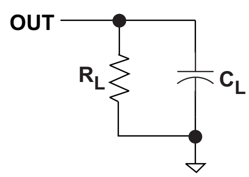


Figure 1. Output Rise and Fall Test Load

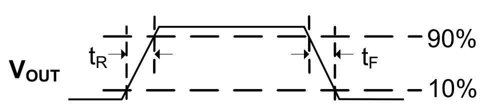


Figure 2. Power-On and Power-Off Timing

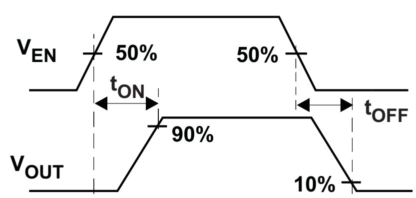


Figure 3. Enable Timing, Active High Enable

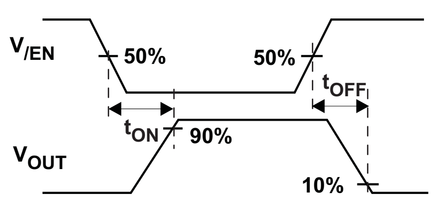


Figure 4. Enable Timing, Active Low Enable

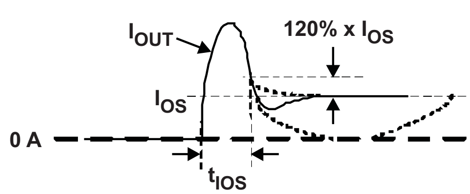


Figure 5. Output Short-Circuit Parameters

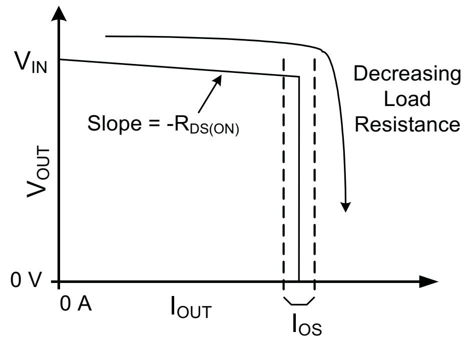


Figure 6. Output Characteristic Showing Current Limit

7.9 Typical Characteristics

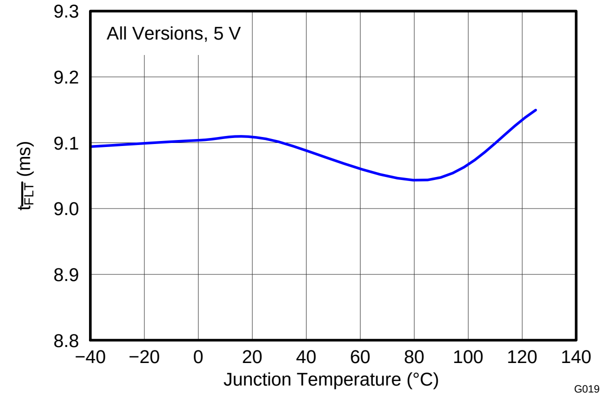


Figure 7. Deglitch Period ($T_{\overline{FLT}}$) vs Temperature

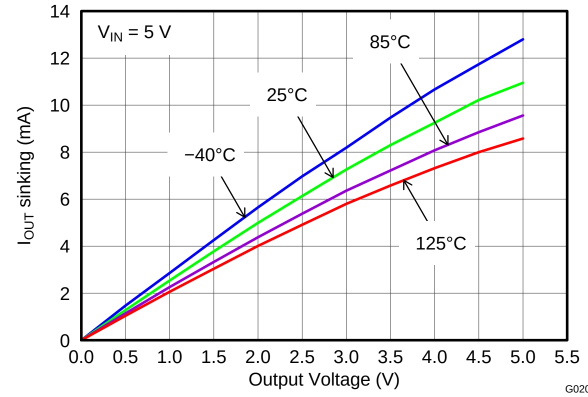


Figure 8. Output Discharge Current vs Output Voltage

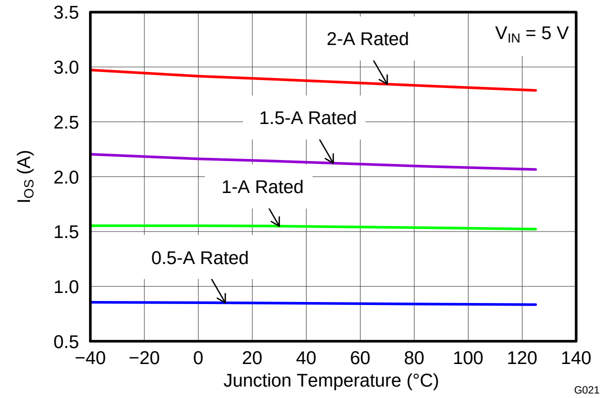


Figure 9. Short Circuit Current (I_{OS}) vs Temperature

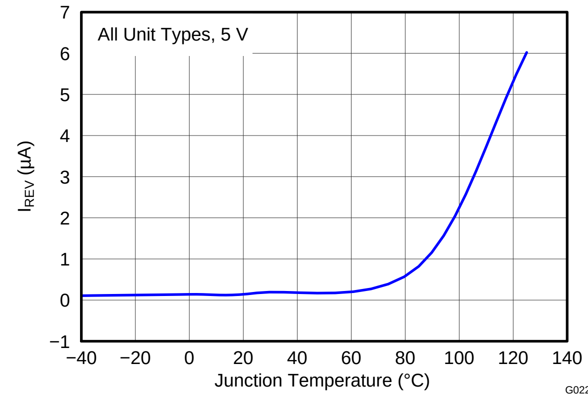


Figure 10. Reverse Leakage Current (I_{REV}) vs Temperature

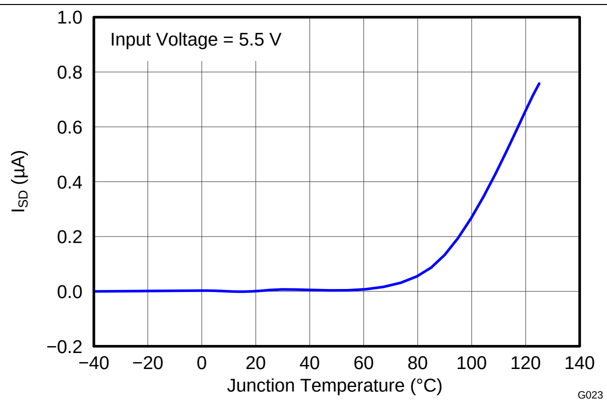


Figure 11. Disabled Supply Current (I_{SD}) vs Temperature

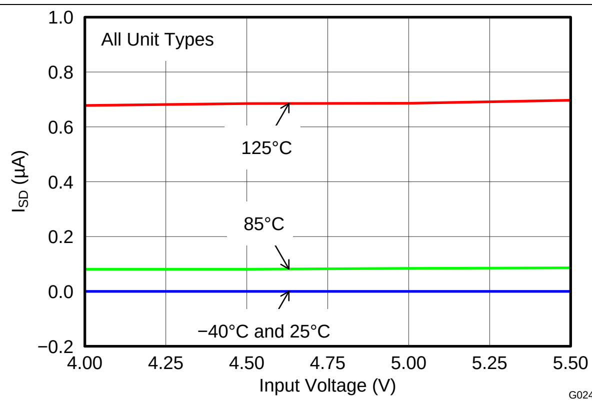


Figure 12. Disabled Supply Current (I_{SD}) vs Input Voltage

Typical Characteristics (continued)

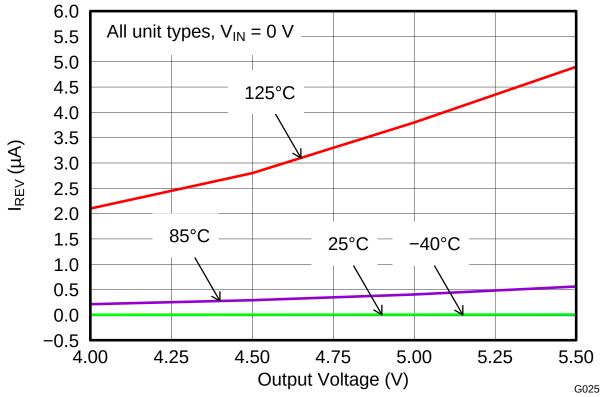


Figure 13. Reverse Leakage Current (I_{REV}) vs Output Voltage

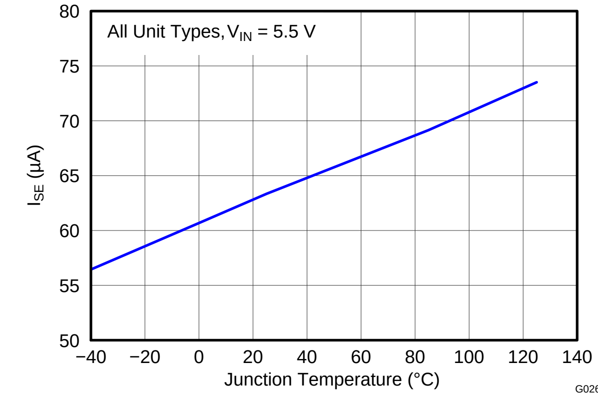


Figure 14. Enabled Supply Current (I_{SE}) vs Temperature

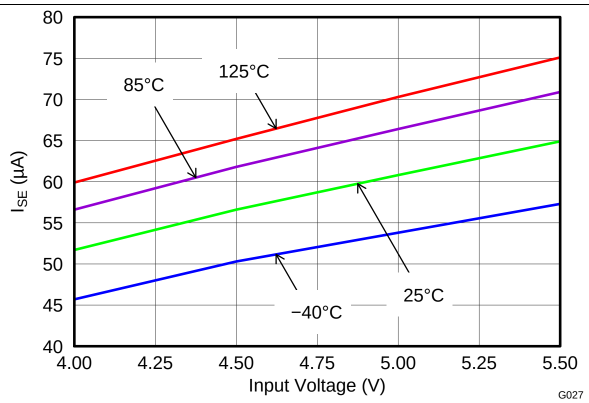


Figure 15. Enabled Supply Current (I_{SE}) vs Input Voltage

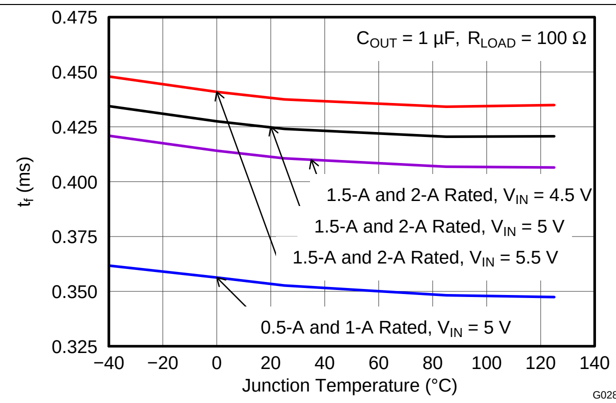


Figure 16. Output Fall Time (T_F) vs Temperature

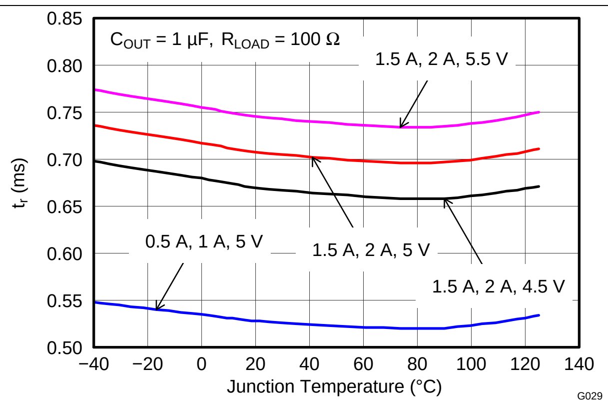


Figure 17. Output Rise Time (T_R) vs Temperature

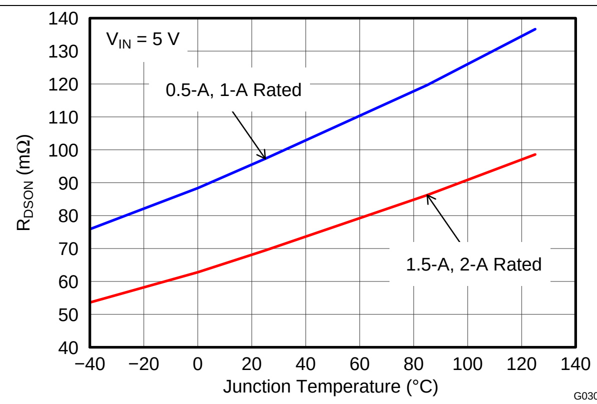


Figure 18. Input-Output Resistance ($R_{DS(ON)}$) vs Temperature

Typical Characteristics (continued)

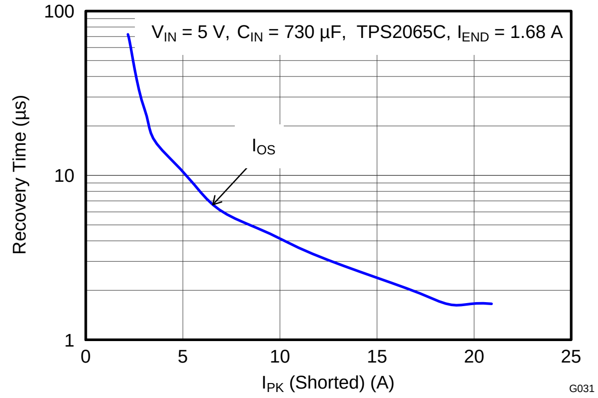


Figure 19. Recovery vs Current Peak

8 Detailed Description

8.1 Overview

The TPS20xxC and TPS20xxC-2 are current-limited, power-distribution switches providing a range from 0.5 A and 2 A of continuous load current in 5-V circuits. These parts use N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. They are designed for applications where short circuits or heavy capacitive loads are encountered. Device features include enable, reverse blocking when disabled, output discharge pulldown, overcurrent protection, overtemperature protection, and deglitched fault reporting.

8.2 Functional Block Diagram

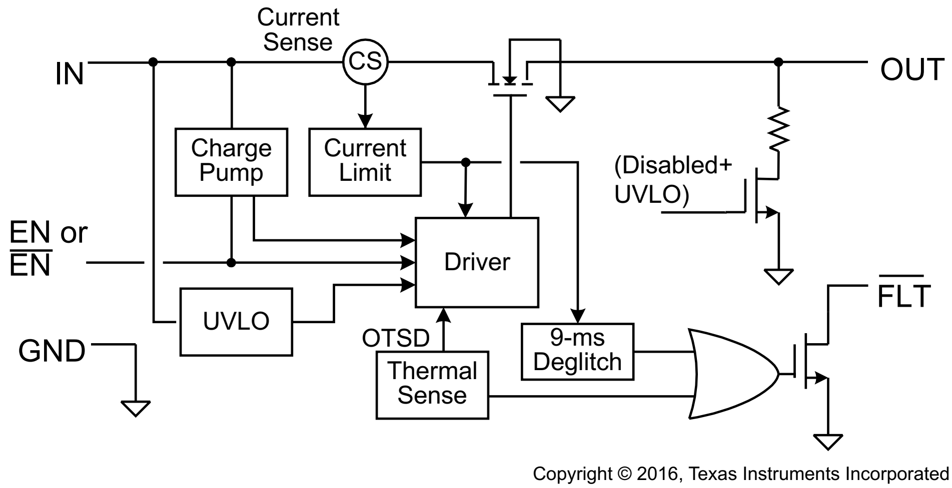


Figure 20. TPS20xxC Block Diagram

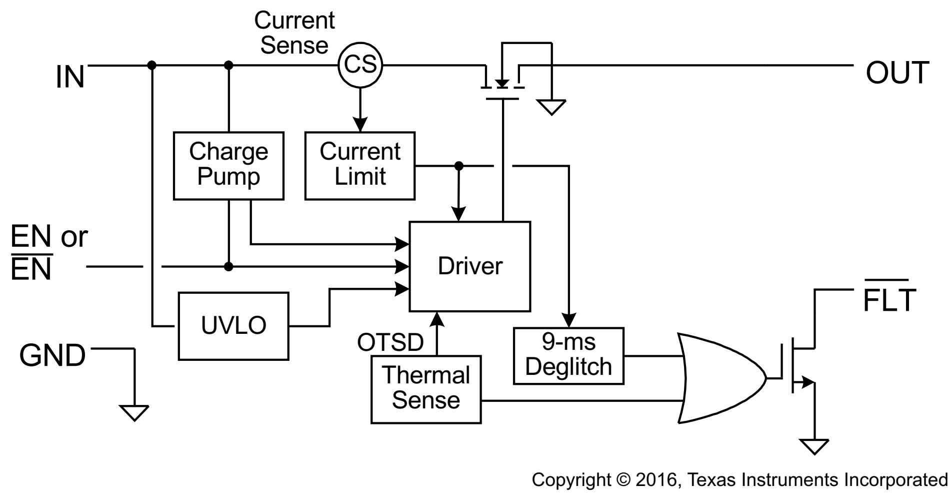


Figure 21. TPS20xxC-2 Block Diagram

8.3 Feature Description

8.3.1 Undervoltage Lockout

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted ON/OFF cycling due to input voltage drop from large current surges. FLT is high impedance when the TPS20xxC and TPS20xxC-2 are in UVLO.

Feature Description (continued)

8.3.2 Enable

The logic enable input (EN, or $\overline{EN}$), controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPS20xxC and TPS20xxC-2 are disabled. Disabling the TPS20xxC and TPS20xxC-2 immediately clears an active $\overline{FLT}$ indication. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPS20xxC and TPS20xxC-2 and the external loading (especially capacitance). TPS20xxC fall time is controlled by the loading (R and C), and the output discharge (R_{PD}). TPS20xxC-2 does not have the output discharge (R_{PD}), fall time is controlled by the loading (R and C). An output load consisting of only a resistor experiences a fall time set by the TPS20xxC and TPS20xxC-2. An output load with parallel R and C elements experiences a fall time determined by the (R × C) time constant if it is longer than the t_F TPS20xxC and TPS20xxC-2.

The enable must not be left open, and may be tied to VIN or GND depending on the device.

8.3.3 Internal Charge Pump

The device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

8.3.4 Current Limit

The TPS20xxC and TPS20xxC-2 responds to overloads by limiting output current to the static I_{OS} levels shown in *Electrical Characteristics: T_J = T_A = 25°C*. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} × R_{LOAD}). Two possible overload conditions can occur. The first overload condition occurs when either:

1. input voltage is first applied, enable is true, and a short circuit is present (load which draws I_{OUT} > I_{OS})
2. input voltage is present and the TPS20xxC and TPS20xxC-2 are enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPS20xxC and TPS20xxC-2 ramps the output current to I_{OS}. The TPS20xxC and TPS20xxC-2 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated in Figure 26 where the device was enabled into a short, and subsequently cycles current OFF and ON as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} (Figure 5 and Figure 6) when the specified overload (see *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*) is applied. The response speed and shape varies with the overload level, input circuit, and rate of application. The current limit response will vary between simply settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPS20xxC and TPS20xxC-2 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle. This is demonstrated by Figure 27, Figure 28, and Figure 29.

The TPS20xxC and TPS20xxC-2 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. This is due to the relatively large power dissipation [(V_{IN} – V_{OUT}) × I_{OS}] driving the junction temperature up. The device turns off when the junction temperature exceeds 135°C (minimum) while in current limit. The device remains off until the junction temperature cools 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products that are similar to the TPS20xxC and TPS20xxC-2. Many older designs have an output I vs V characteristic similar to the plot labeled *Current Limit with Peaking* in Figure 22. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPS20xxC and TPS20xxC-2 family of parts does not present noticeable peaking in the current limit, corresponding to the characteristic labeled *Flat Current Limit* in Figure 22. This is why the I_{OC} parameter is not present in *Electrical Characteristics: –40°C ≤ T_J ≤ 125°C*.

Feature Description (continued)

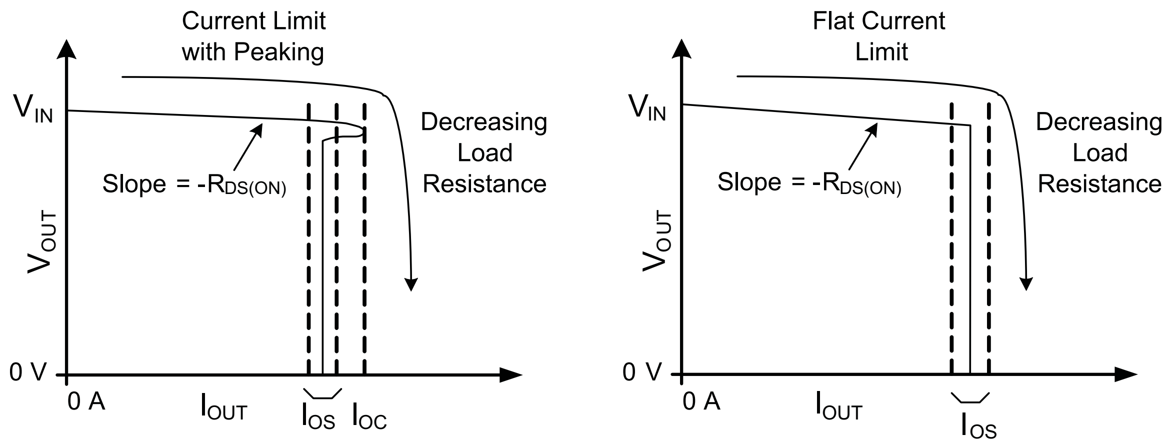


Figure 22. Current Limit Profiles

8.3.5 $\overline{\text{FLT}}$

The $\overline{\text{FLT}}$ open-drain output is asserted (active low) during an overload or overtemperature condition. A 9-ms deglitch on both the rising and falling edges avoids false reporting at start-up and during transients. A current limit condition shorter than the deglitch period clears the internal timer upon termination. The deglitch timer does not integrate multiple short overloads and declare a fault. This is also true for exiting from a faulted state. An input voltage with excessive ripple and large output capacitance may interfere with operation of $\overline{\text{FLT}}$ around I_{OS} as the ripple drives the TPS20xxC and TPS20xxC-2 in and out of current limit.

If the TPS20xxC and TPS20xxC-2 are in current limit and the overtemperature circuit goes active, $\overline{\text{FLT}}$ goes true immediately (see Figure 27); however, the exiting this condition is deglitched (see Figure 29). $\overline{\text{FLT}}$ is tripped just as the knee of the constant-current limiting is entered. Disabling the TPS20xxC and TPS20xxC-2 clears an active $\overline{\text{FLT}}$ as soon as the switch turns off (see Figure 26). $\overline{\text{FLT}}$ is high impedance when the TPS20xxC and TPS20xxC-2 are disabled or in undervoltage lockout (UVLO).

8.3.6 Output Discharge

A 470-Ω (typical) output discharge dissipates stored charge and leakage current on OUT when the TPS20xxC is in UVLO or disabled. The pulldown circuit loses bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V. The TPS20xxC-2 does not have this function. The output is be controlled by an external loadings when the device is in ULVO or disabled.

8.4 Device Functional Modes

There are no other functional modes.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS20xxC and TPS20xxC-2 current-limited power switch uses N-channel MOSFETs in applications requiring continuous load current. The device enters constant-current mode when the load exceeds the current limit threshold.

9.2 Typical Application

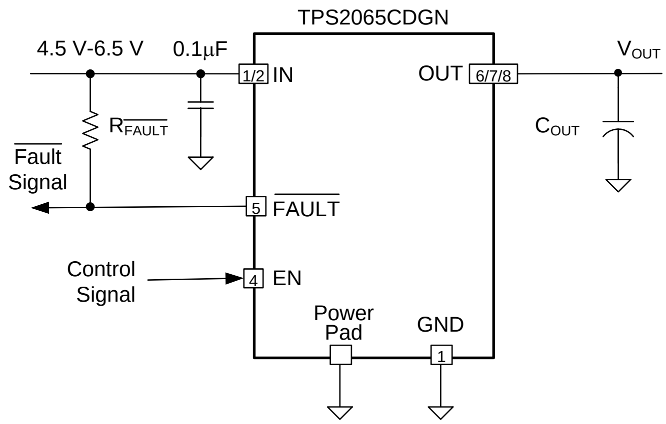


Figure 23. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following input parameters:

1. The TPS2065CDGN operates from a 5-V to ±0.5-V input rail.
2. What is the normal operation current, for example, the maximum allowable current drawn by portable equipment for USB 3.0 port is 900 mA, so the normal operation current is 900 mA, and the minimum current limit of power switch must exceed 900 mA to avoid false trigger during normal operation. For the TPS2065C device, target 1-A continuous output current application.
3. What is the maximum allowable current provided by up-stream power, the maximum current limit of power switch that must lower it to ensure power switch can protect the up-stream power when overload is encountered at the output of power switch. For the TPS2065C device, the maximum I_{OS} is 1.8 A.

9.2.2 Detailed Design Procedure

To begin the design process a few parameters must be decided upon. The designer must know the following:

1. Normal input operation voltage
2. Output continuous current
3. Maximum up-stream power supply output current

9.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, TI recommends placing a 0.1-µF or greater ceramic bypass capacitor between IN and GND, as close to the device as possible for local noise decoupling.

Typical Application (continued)

All protection circuits such as the TPS20xxC and TPS20xxC-2 has the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2× the applied. The second cause is due to the abrupt reduction of output short-circuit current when the TPS20xxC and TPS20xxC-2 turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPS20xxC and TPS20xxC-2 output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current limit speed of the TPS20xxC and TPS20xxC-2 to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the TPS20xxC and TPS20xxC-2 input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPS20xxC and TPS20xxC-2 has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120-µF minimum output capacitance is required. Typically a 150-µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, then TI recommends a minimum of 10-µF ceramic capacitance on the output. The voltage undershoot must be controlled to less than 1.5 V for 10 µs.

9.2.3 Application Curves

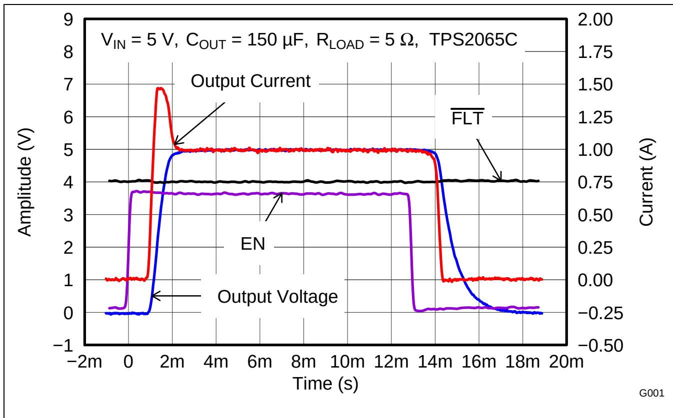


Figure 24. TPS2065C Output Rise / Fall 5 Ω

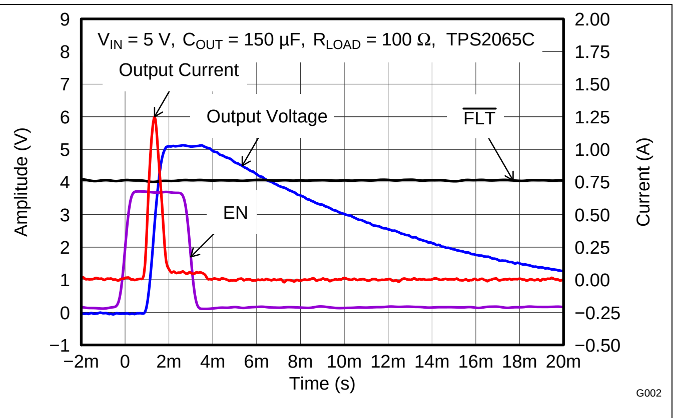


Figure 25. TPS2065C Output Rise / Fall 100 Ω

Typical Application (continued)

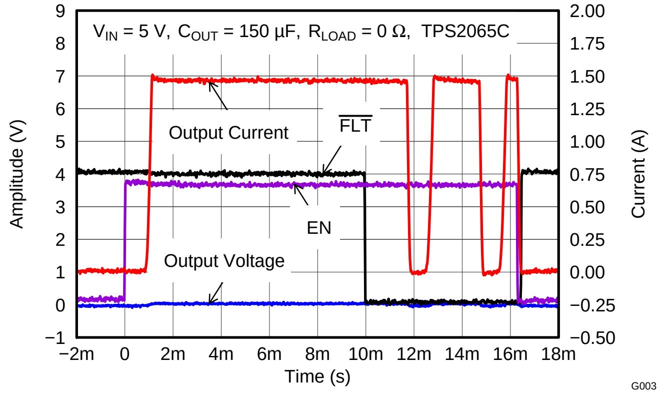


Figure 26. TPS2065C Enable into Output Short

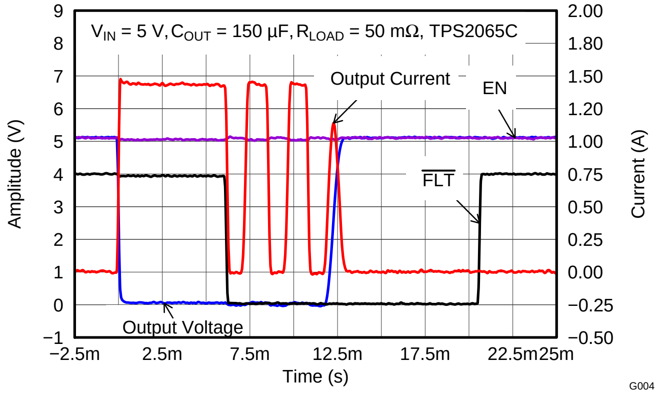


Figure 27. TPS2065C Pulsed Short Applied

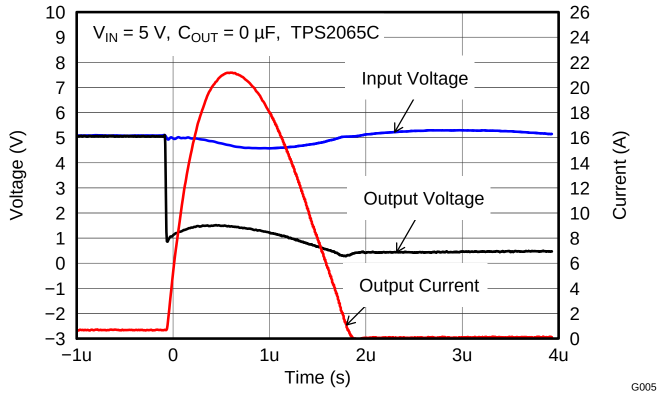


Figure 28. TPS2065C Short Applied

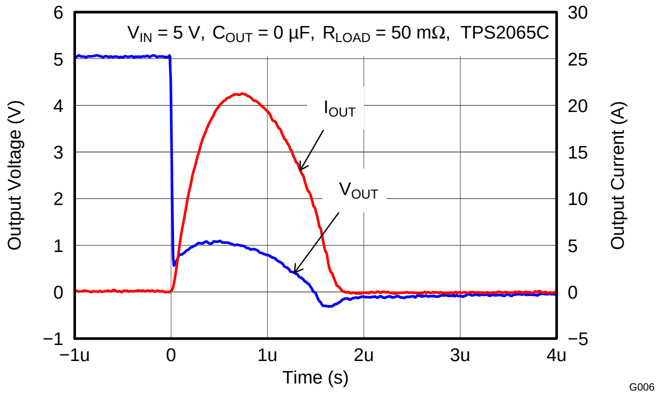


Figure 29. TPS2065C Pulsed 1.45-A Load

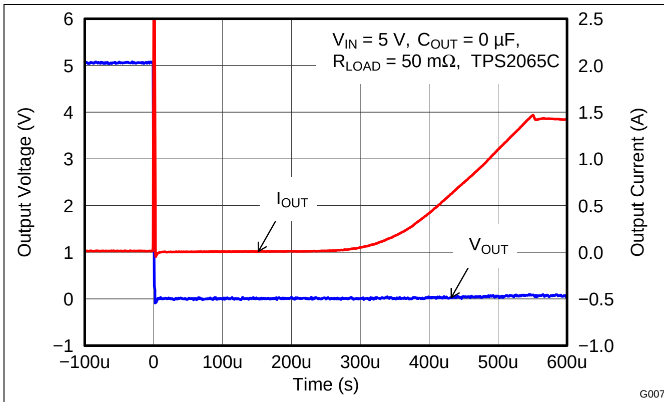


Figure 30. TPS2065C 50-mΩ Short Circuit

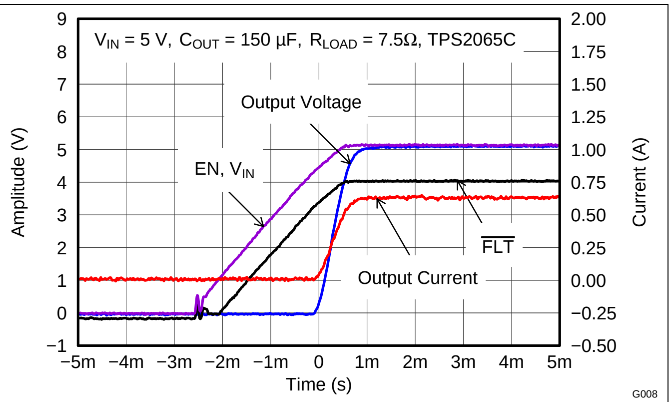


Figure 31. TPS2065C Power Up – Enabled

Typical Application (continued)

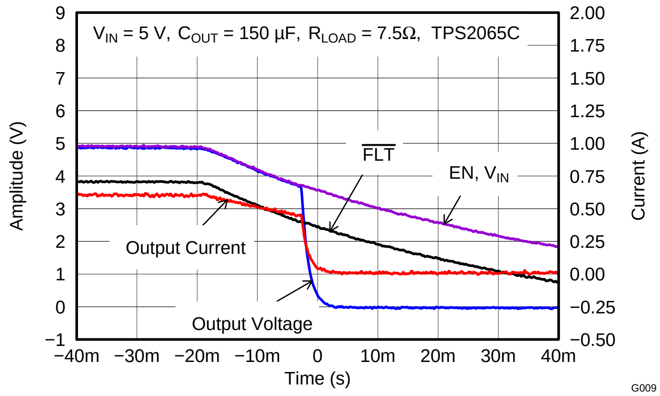


Figure 32. TPS2065C Power Down – Enabled

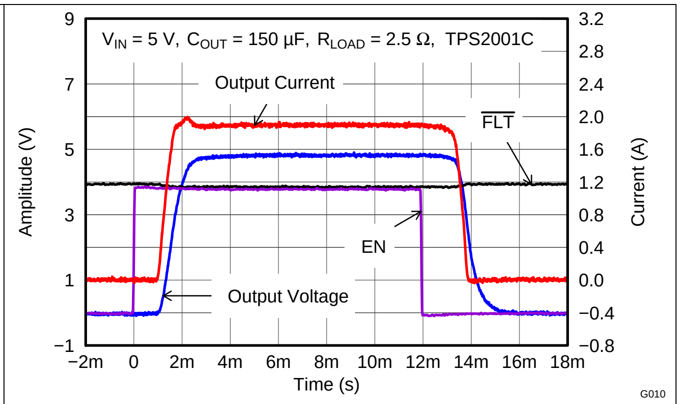


Figure 33. TPS2001C Turnon into 2.5 Ω

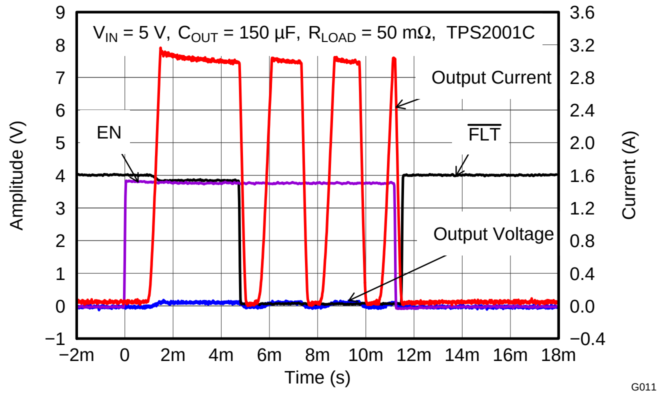


Figure 34. TPS2001C Enable into Short

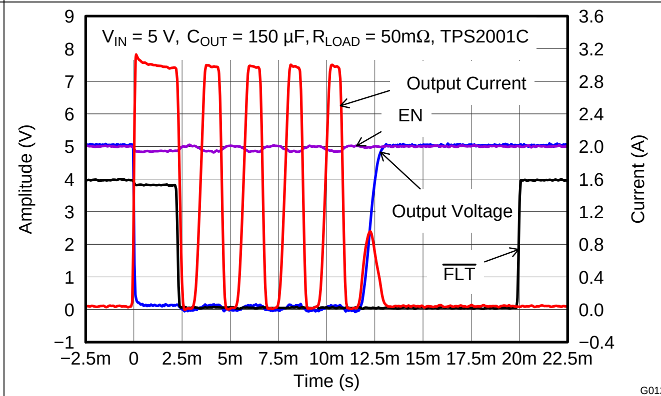


Figure 35. TPS2001C Pulsed Output Short

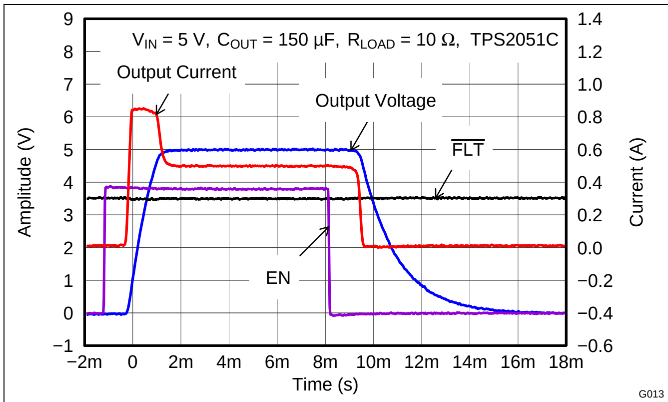


Figure 36. TPS2051C Turnon into 10 Ω

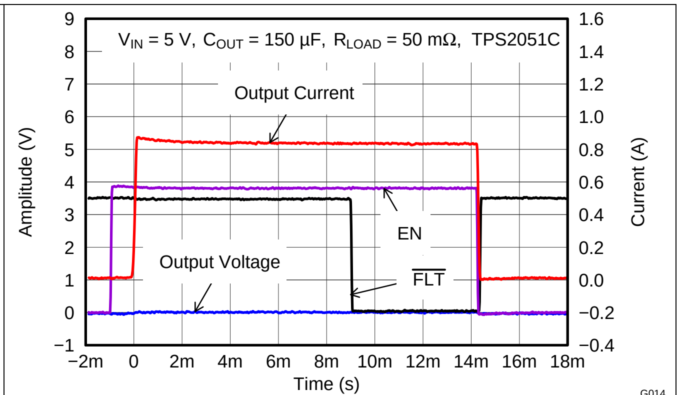


Figure 37. TPS2051C Enable into Short

Typical Application (continued)

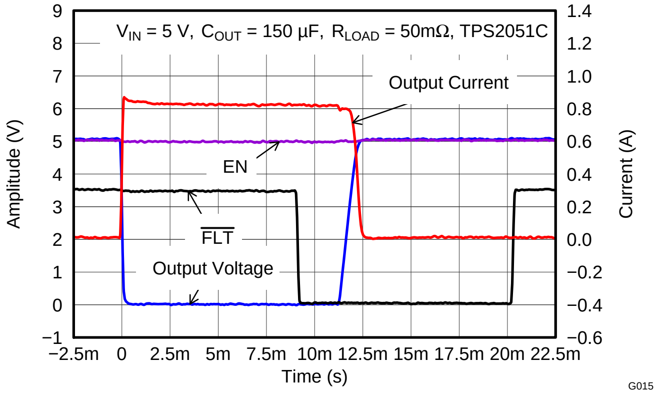


Figure 38. TPS2051C Pulsed Output Short

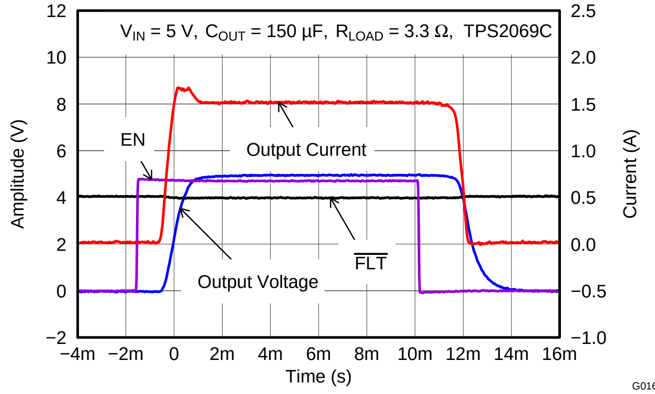


Figure 39. TPS2069C Turnon into 3.3 Ω

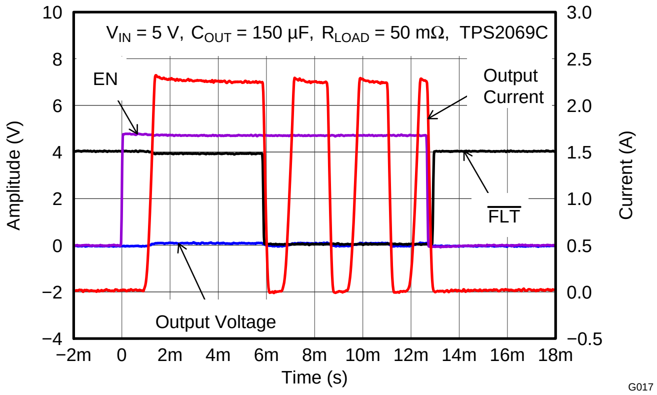


Figure 40. TPS2069C Enable into Short

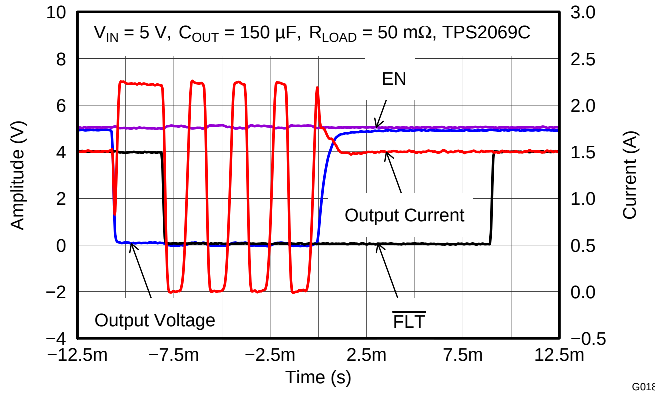


Figure 41. TPS2069C Pulsed Output Short

10 Power Supply Recommendations

Design of the devices is for operation from an input voltage supply range of 4.5 V to 5.5 V. The current capability of the power supply should exceed the maximum current limit of the power switch.

11 Layout

11.1 Layout Guidelines

1. Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low inductance trace.
2. Place at least 10-µF low ESR ceramic capacitor near the OUT and GND pins, and make the connections using a low inductance trace.
3. The PowerPAD must be directly connected to PCB ground plane using wide and short copper trace.

11.2 Layout Example

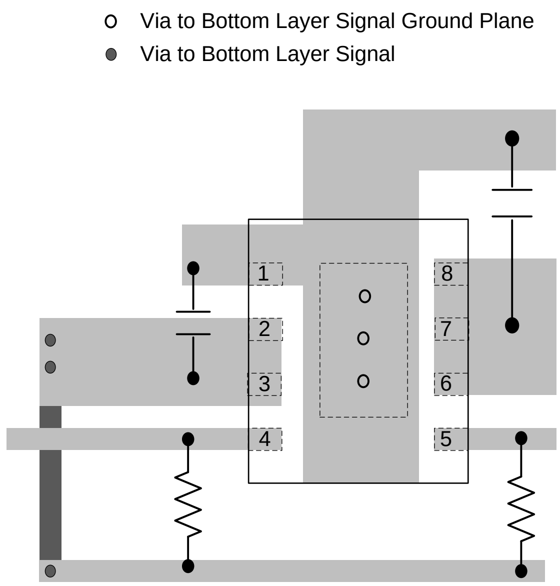


Figure 42. Recommended Layout

11.3 Power Dissipation and Junction Temperature

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPS20xxC and TPS20xxC-2. The system designer can control choices of package, proximity to other power dissipating devices, and printed-circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow.

Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. The lower junction temperatures achieved by soldering the pad improve the efficiency and reliability of both TPS20xxC and TPS20xxC-2 parts and the system. The following examples were used to determine the θ_{JA}Custom thermal impedances noted in *Thermal Information: SOT-23* and *Thermal Information: MSOP-PowerPAD*. They were based on use of the JEDEC high-k circuit board construction (2 signal and 2 plane) with 4, 1-oz. copper weight, layers.

While TI recommends that the DGN package PAD be soldered to circuit board copper fill and vias for low thermal impedance, there may be cases where this is not desired. For example, use of routing area under the IC. Some devices are available in packages without the PowerPad (DGK) specifically for this purpose. The θ_{JA} for the DGN package with the pad not soldered and no extra copper, is approximately 141°C/W for 0.5-A and 1-A rated parts, and 139°C/W for the 1.5-A and 2-A rated parts. The θ_{JA} for the DGK mounted per Figure 45 is 110.3°C/W. These values may be used in Equation 1 to determine the maximum junction temperature.

Power Dissipation and Junction Temperature (continued)

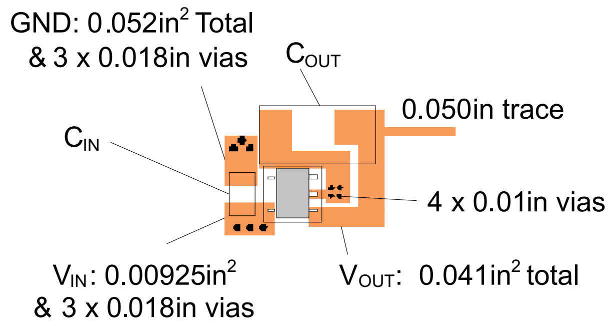


Figure 43. DBV Package PCB Layout Example

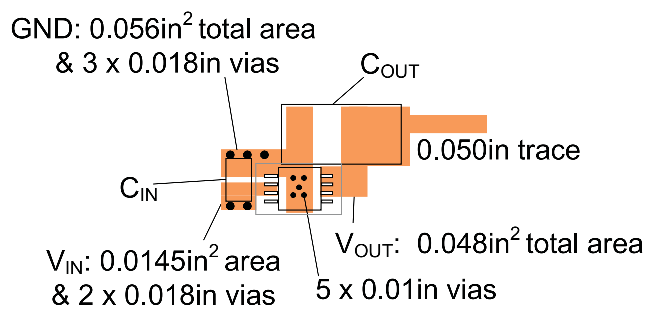


Figure 44. DGN Package PCB Layout Example

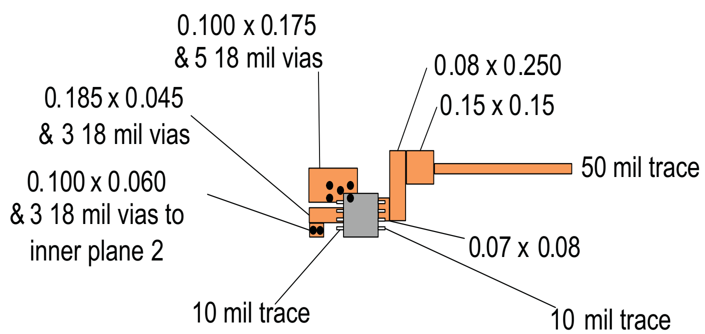


Figure 45. DGK Package PCB Layout Example

As shown in Equation 1, the following procedure requires iteration because power loss is due to the internal MOSFET $I^2 \times R_{DS(ON)}$, and $R_{DS(ON)}$ is a function of the junction temperature. As an initial estimate, use the $R_{DS(ON)}$ at 125°C from the *Typical Characteristics*, and the preferred package thermal resistance for the preferred board construction from the *Thermal Information: SOT-23* table.

Power Dissipation and Junction Temperature (continued)

$$T_J = T_A + ((I_{OUT}^2 \times R_{DS(ON)}) \times \theta_{JA}) \tag{1}$$

where

- I_{OUT} = rated OUT pin current (A)
- $R_{DS(ON)}$ = Power switch ON-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)
- θ_{JA} = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, estimate a new value of $R_{DS(ON)}$ using the typical characteristic plot and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction or a package with lower θ_{JA}.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS2000C	Click here	Click here	Click here	Click here	Click here
TPS2001C	Click here	Click here	Click here	Click here	Click here
TPS2041C	Click here	Click here	Click here	Click here	Click here
TPS2051C	Click here	Click here	Click here	Click here	Click here
TPS2061C	Click here	Click here	Click here	Click here	Click here
TPS2065C	Click here	Click here	Click here	Click here	Click here
TPS2065C-2	Click here	Click here	Click here	Click here	Click here
TPS2068C	Click here	Click here	Click here	Click here	Click here
TPS2069C	Click here	Click here	Click here	Click here	Click here
TPS2069C-2	Click here	Click here	Click here	Click here	Click here

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
905X0205100	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VBYQ	Samples
TPS2000CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXFI	Samples
TPS2000CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXFI	Samples
TPS2000CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BCMS	Samples
TPS2000CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BCMS	Samples
TPS2001CDGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXGI	Samples
TPS2001CDGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXGI	Samples
TPS2001CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	VBWQ	Samples
TPS2001CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	VBWQ	Samples
TPS2041CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PYJI	Samples
TPS2041CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PYJI	Samples
TPS2051CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VBYQ	Samples
TPS2051CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VBYQ	Samples
TPS2061CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PXLI	Samples
TPS2061CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PXLI	Samples
TPS2061CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXMI	Samples
TPS2061CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXMI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2065CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCAQ	Samples
TPS2065CDBVR-2	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PYQI	Samples
TPS2065CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	VCAQ	Samples
TPS2065CDBVT-2	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PYQI	Samples
TPS2065CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	VCAQ	Samples
TPS2065CDGN-2	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PYRI	Samples
TPS2065CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	VCAQ	Samples
TPS2065CDGNR-2	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PYRI	Samples
TPS2068CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXNI	Samples
TPS2068CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PXNI	Samples
TPS2069CDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PYKI	Samples
TPS2069CDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PYKI	Samples
TPS2069CDGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	VBUQ	Samples
TPS2069CDGN-2	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PYSI	Samples
TPS2069CDGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	VBUQ	Samples
TPS2069CDGNR-2	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	PYSI	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

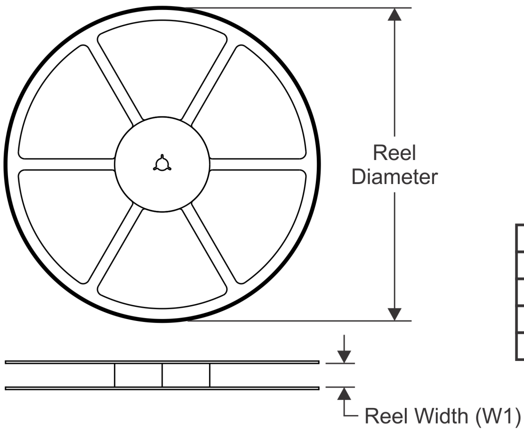
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

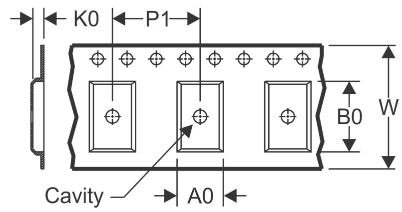
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

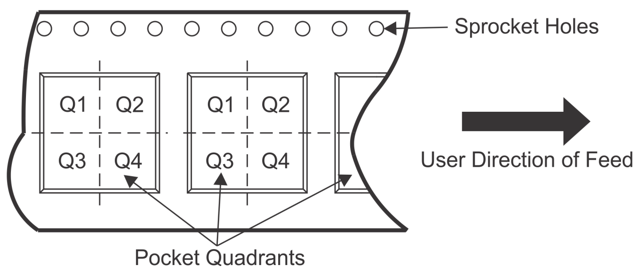


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

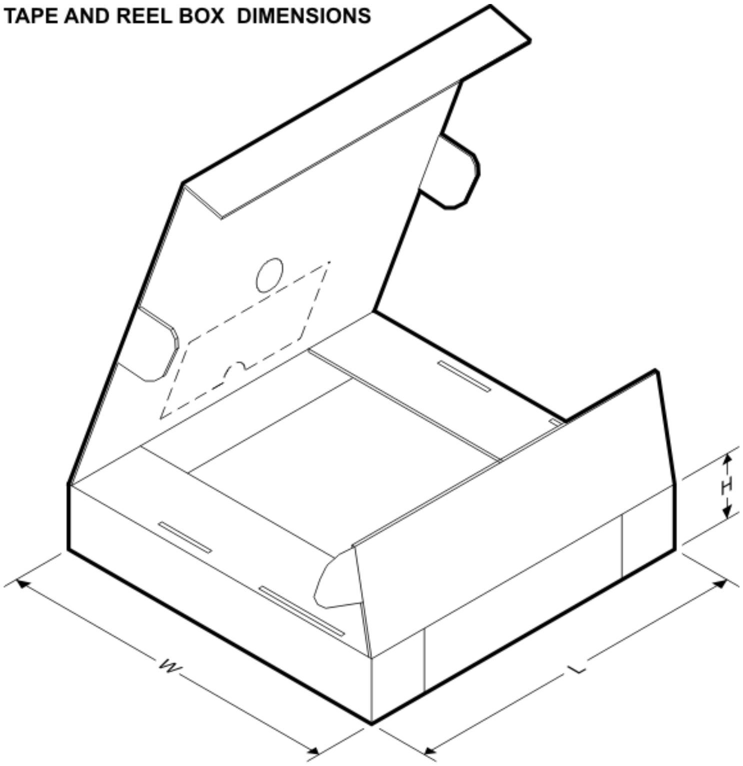


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2000CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2000CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001CDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2001CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2041CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2041CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2041CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2041CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2051CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2051CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2061CDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2061CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2061CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2061CDBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2061CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVR-2	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDBVT-2	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2065CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2065CDGNR-2	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2068CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2069CDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS2069CDBVT	SOT-23	DBV	5	250	178.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TPS2069CDGNR	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS2069CDGNR-2	MSOP-PowerPAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

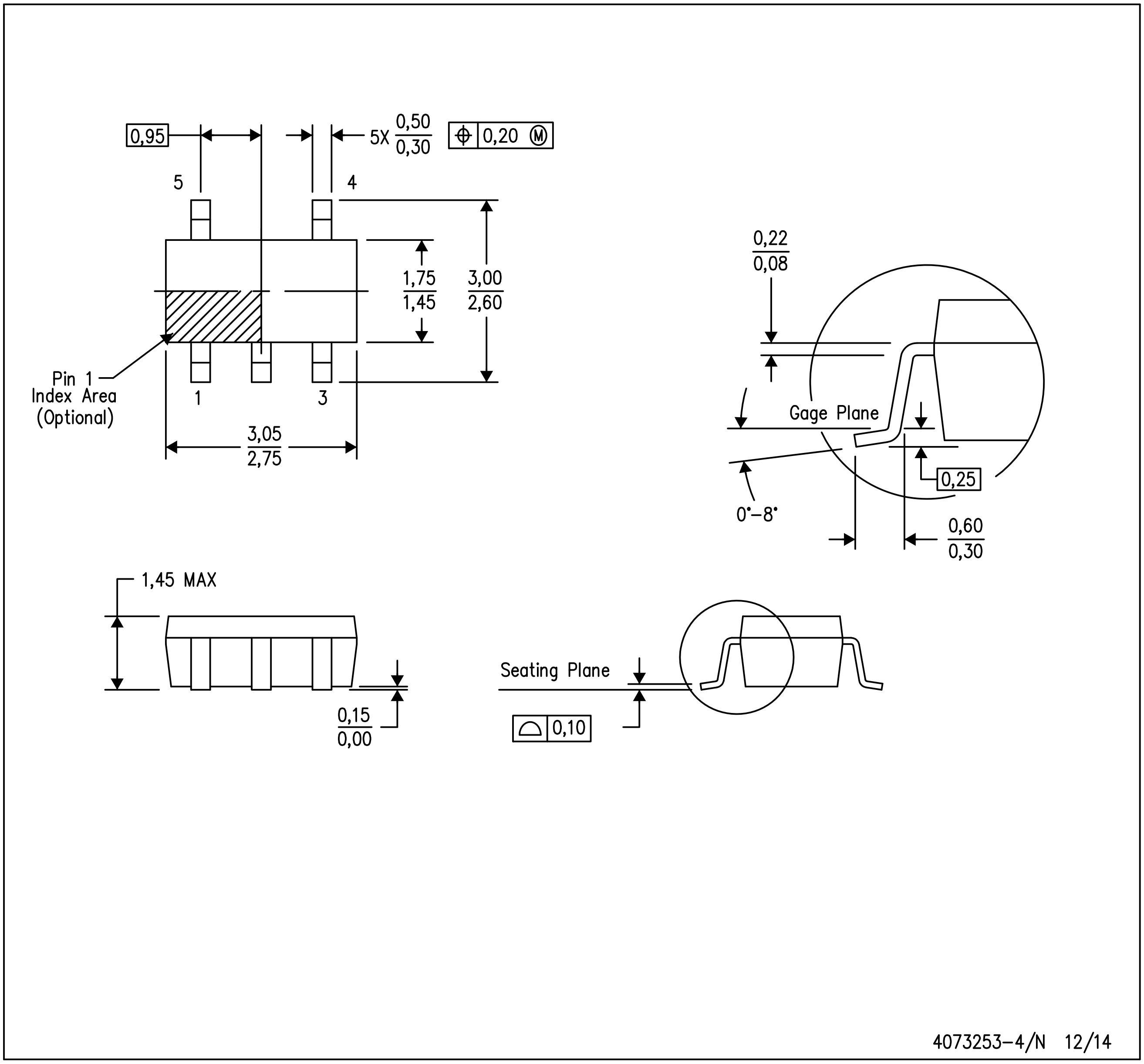


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2000CDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TPS2000CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2001CDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TPS2001CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2041CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2041CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2041CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2041CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2051CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2051CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2051CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2061CDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS2061CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2061CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2061CDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
TPS2061CDGNR	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS2065CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065CDBVR-2	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2065CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2065CDBVT-2	SOT-23	DBV	5	250	180.0	180.0	18.0

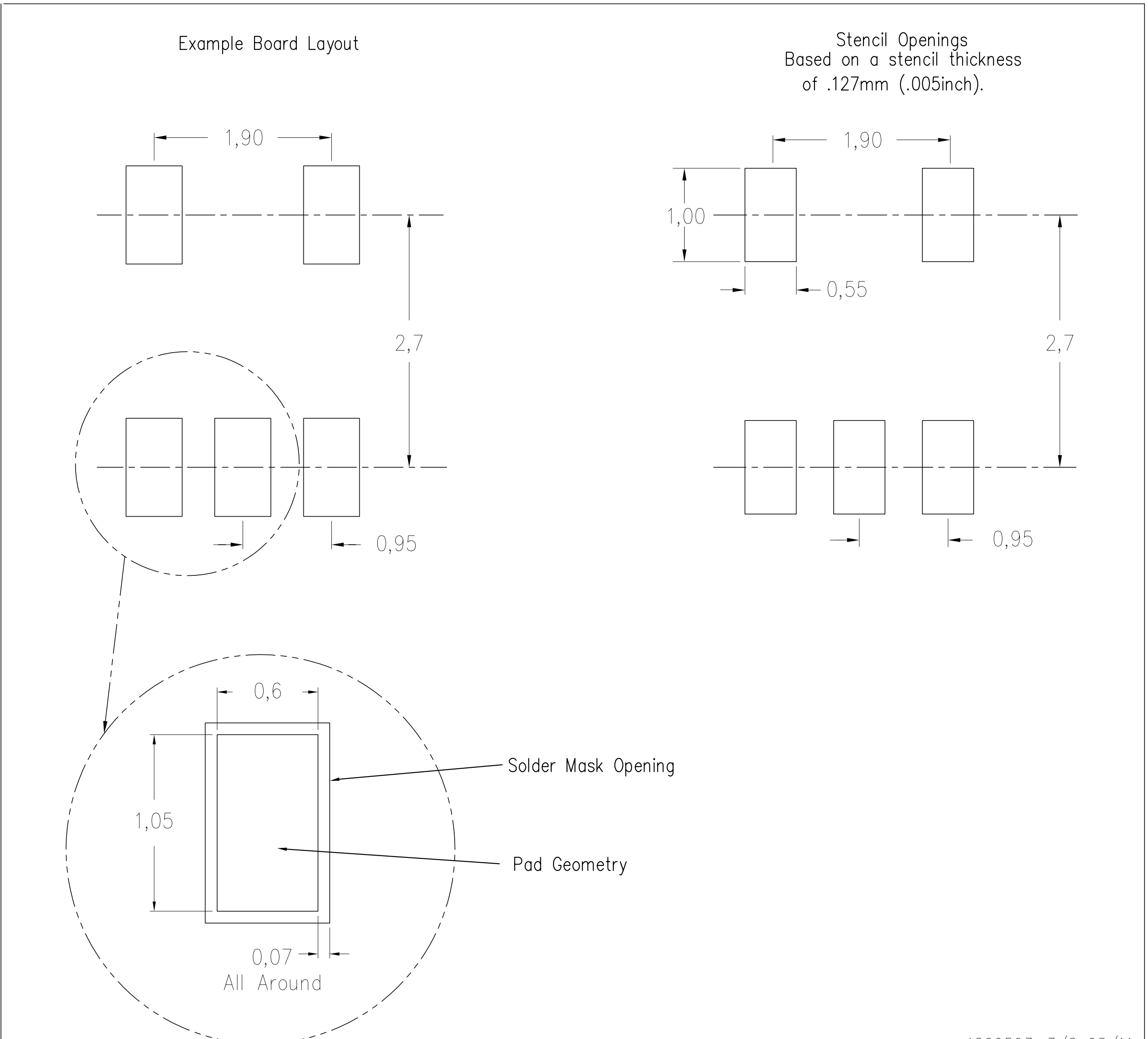
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2065CDGNR	MSOP-PowerPAD	DGN	8	2500	360.0	162.0	98.0
TPS2065CDGNR-2	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS2068CDGNR	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS2069CDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS2069CDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS2069CDGNR	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0
TPS2069CDGNR-2	MSOP-PowerPAD	DGN	8	2500	366.0	364.0	50.0

DBV (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO-178 Variation AA.

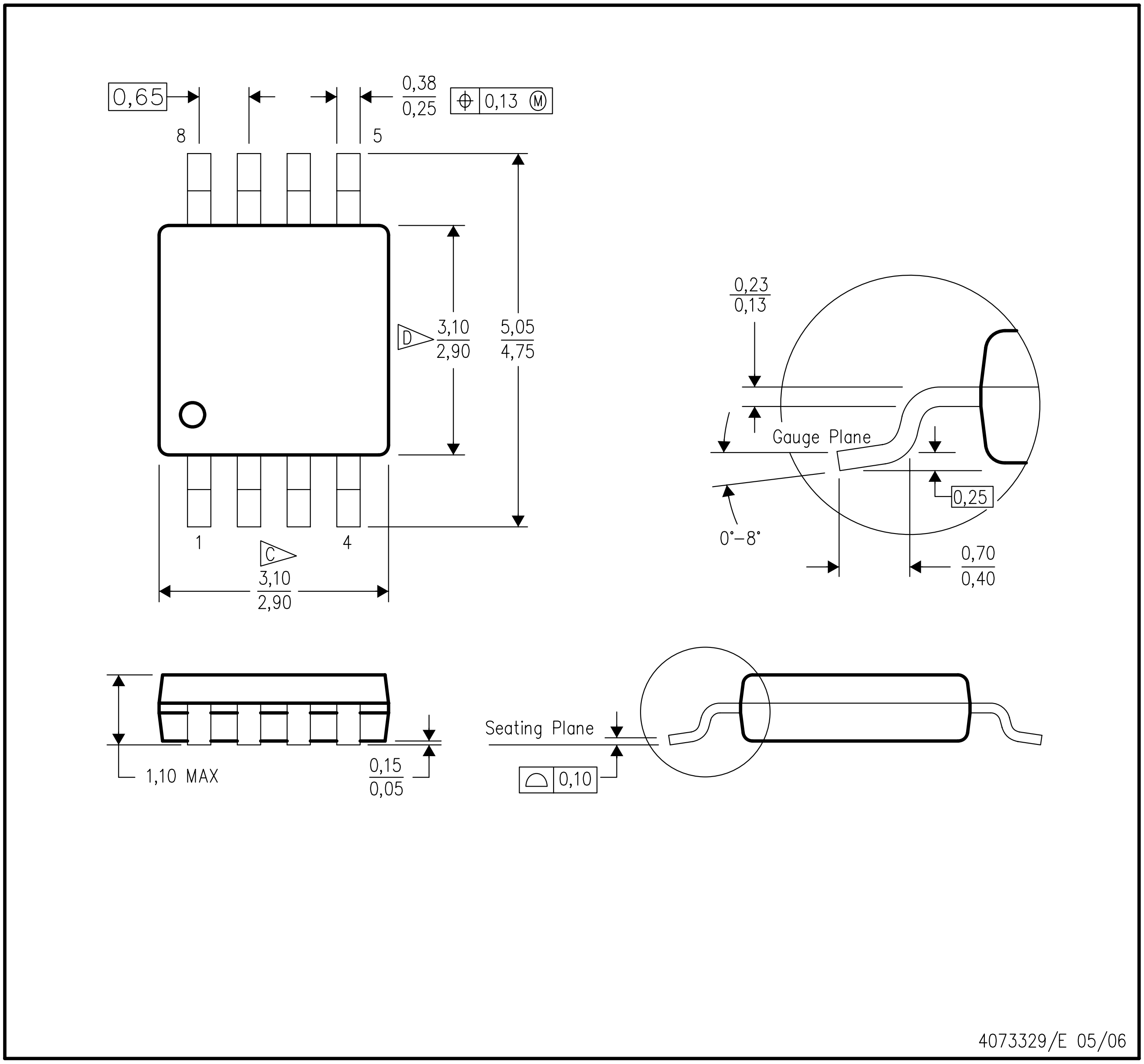
DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



4209593–3/C 08/11

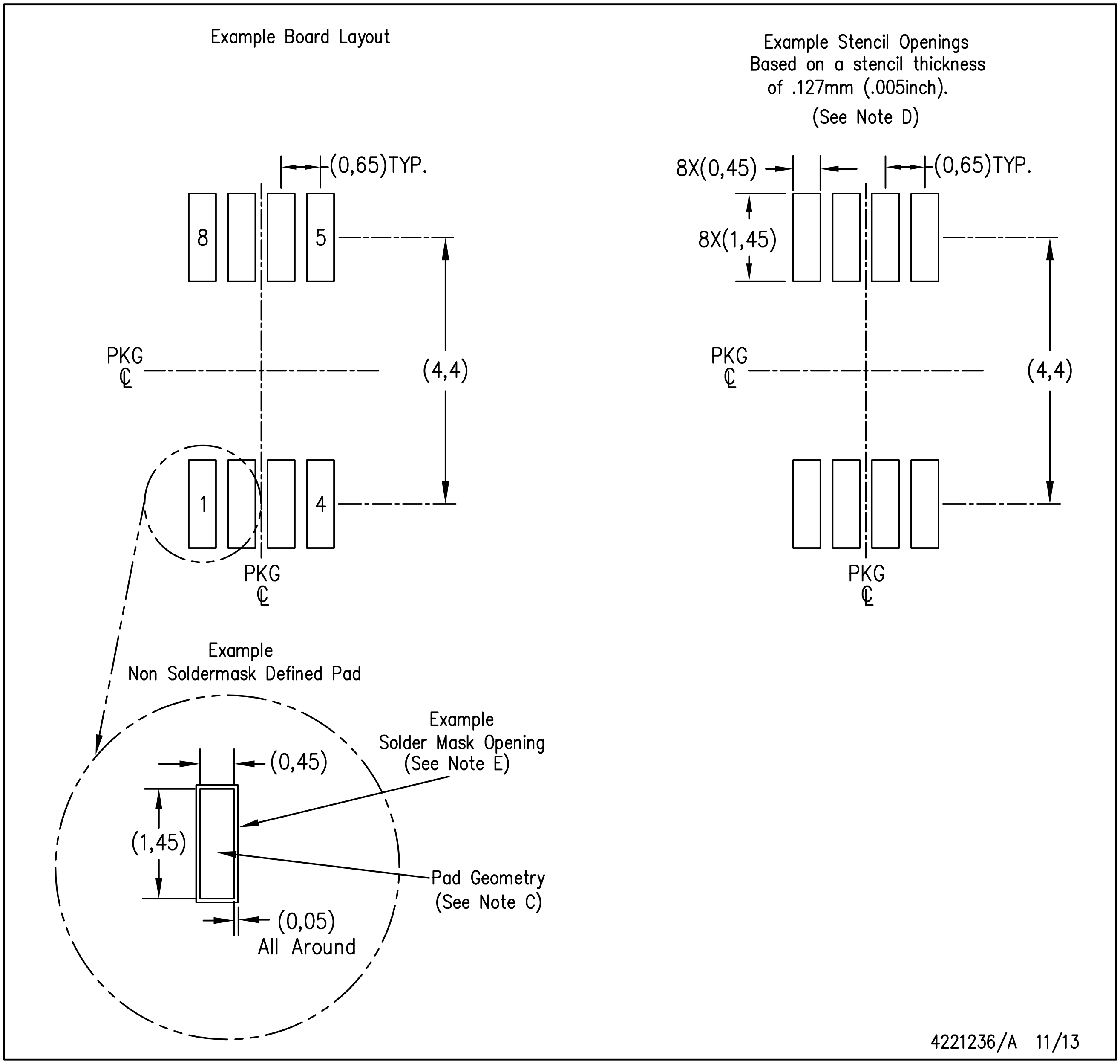
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



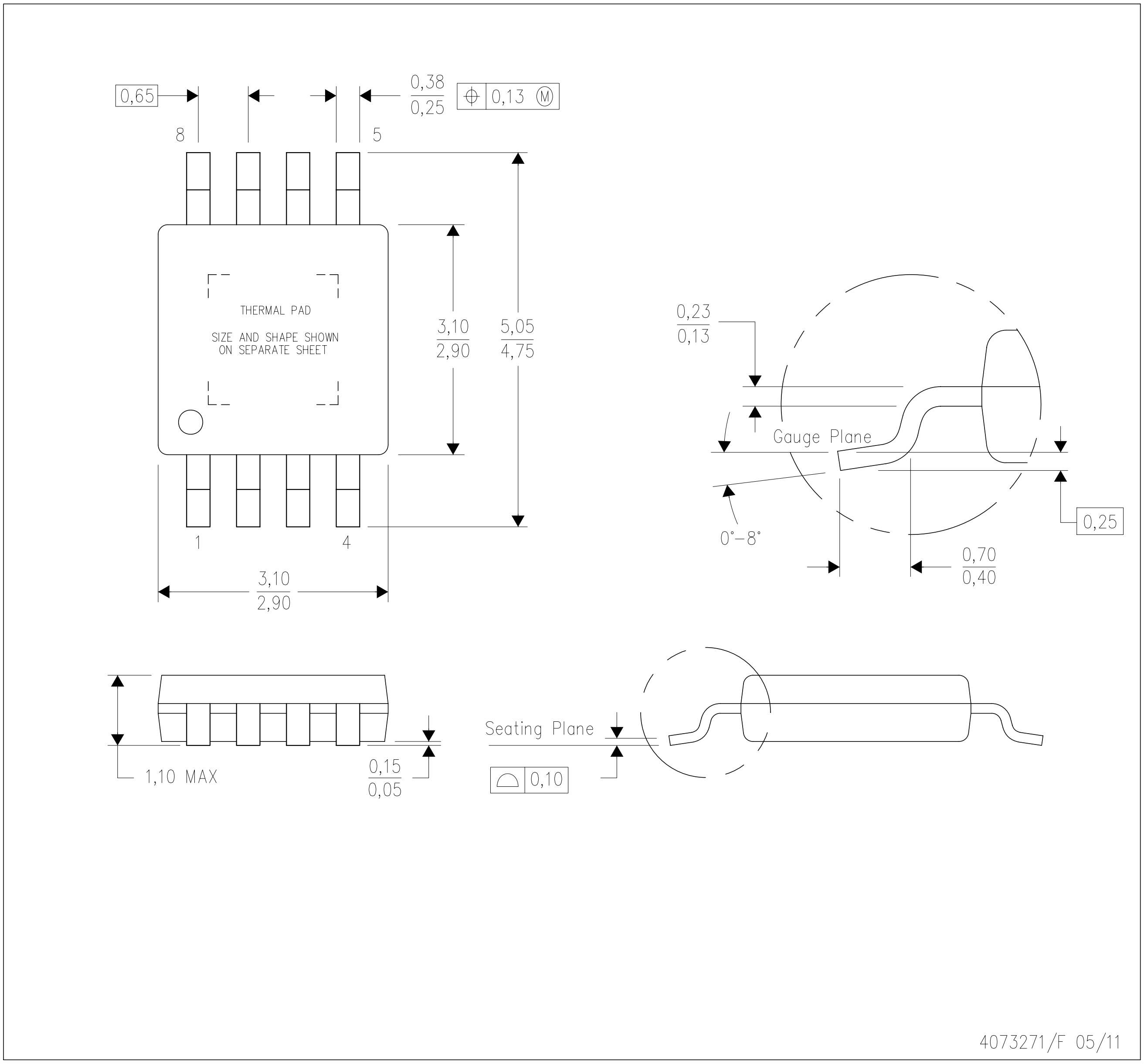
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S-PDSO-G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

PowerPAD is a trademark of Texas Instruments.

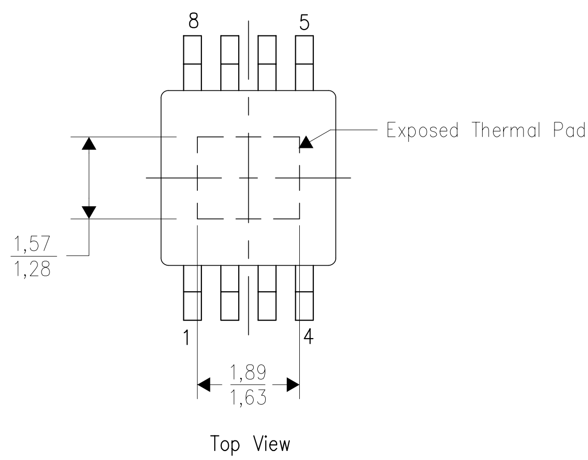
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

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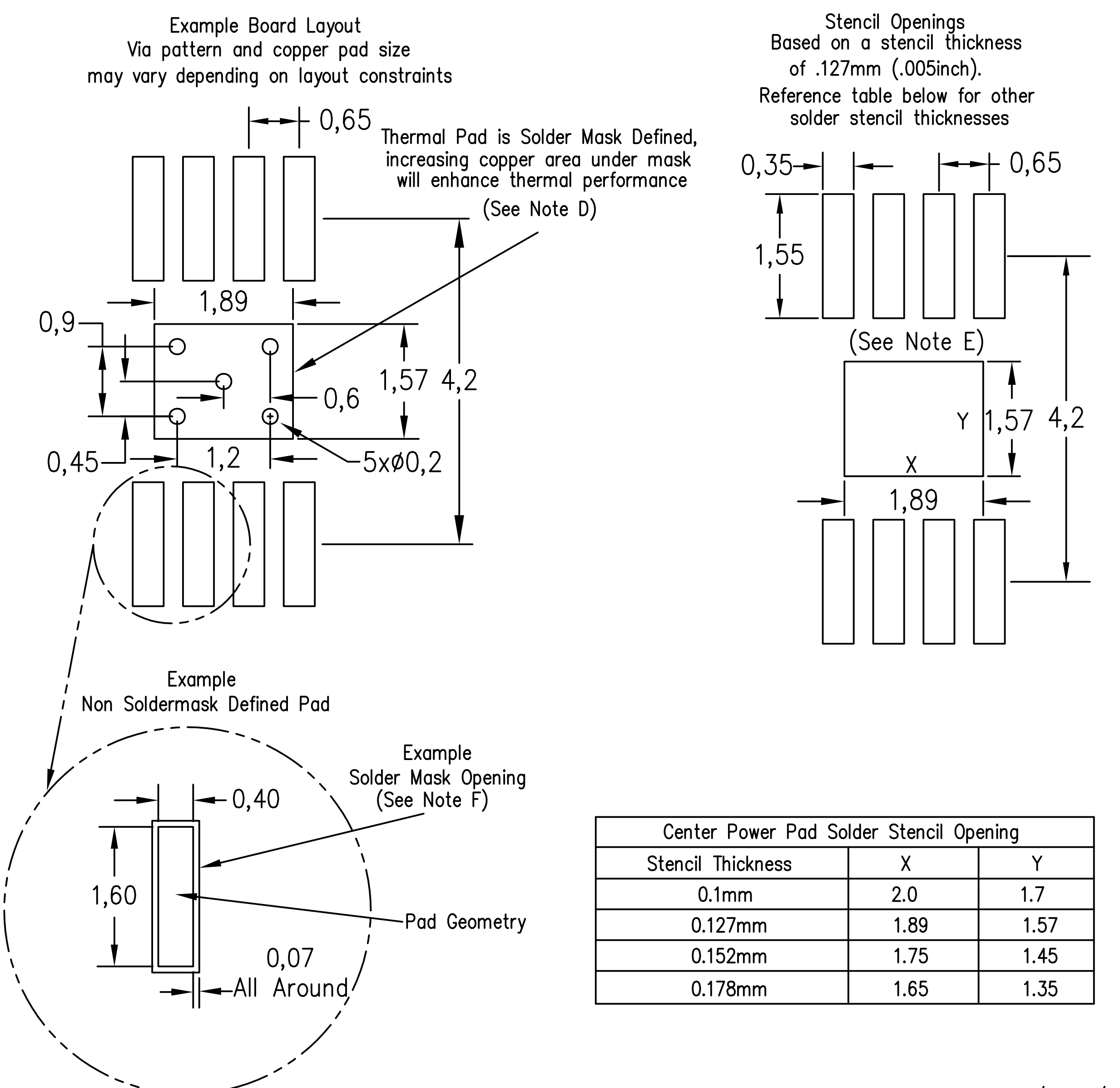
DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

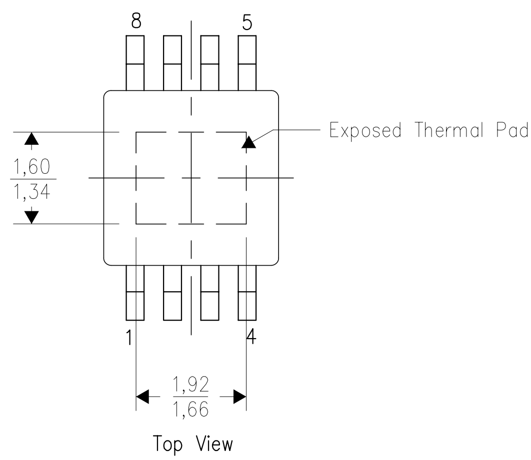
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206323-4/I 12/11

NOTE: All linear dimensions are in millimeters

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