

Sega Game Gear on a Chip

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Agenda

- Introduction / Problem Description
- The Sega Game Gear
- Prototyping Platform
- Design Strategy & Process
- Component Descriptions
- Testing Strategy / Assessment Metrics
- Issues of Concern

Underlying Goal

Reimplement all the digital components of
a legacy computer system in a FPGA

Purpose

Why?

- **Maintainability** - You can no longer buy parts to service legacy computer systems
- **Upgradability** - Reimplementation gives an opportunity to add additional features
- **Portability** - Do not need all the original big clunky hardware. Reimplementation can be embedded in new designs



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Sega Game Gear

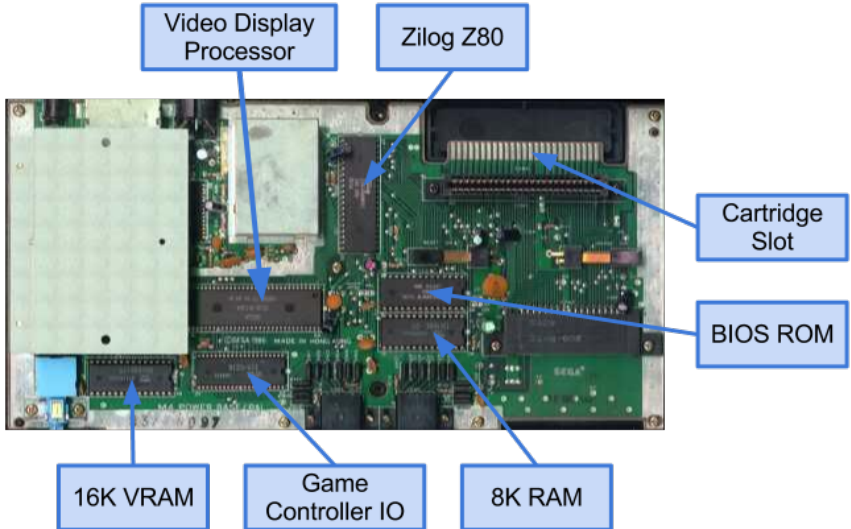


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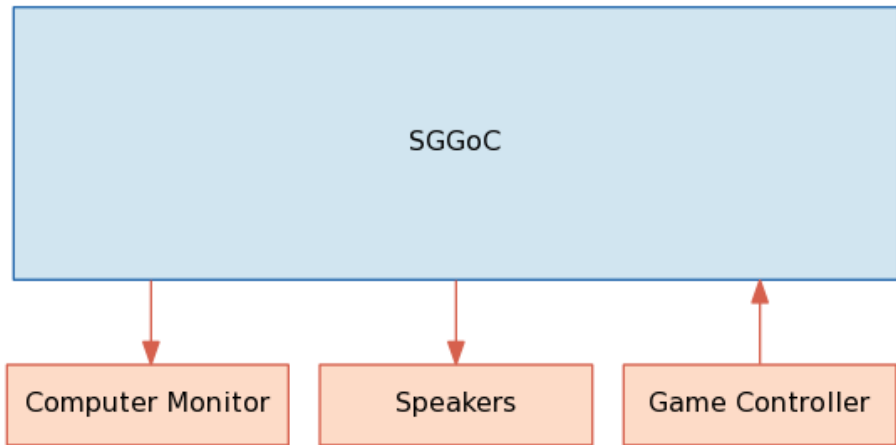
- Released April 1990
- Mobile version of the Sega Master System (functionally identical)
- Standard system architecture for the time (Z80 CPU, tri-state buses, etc...)



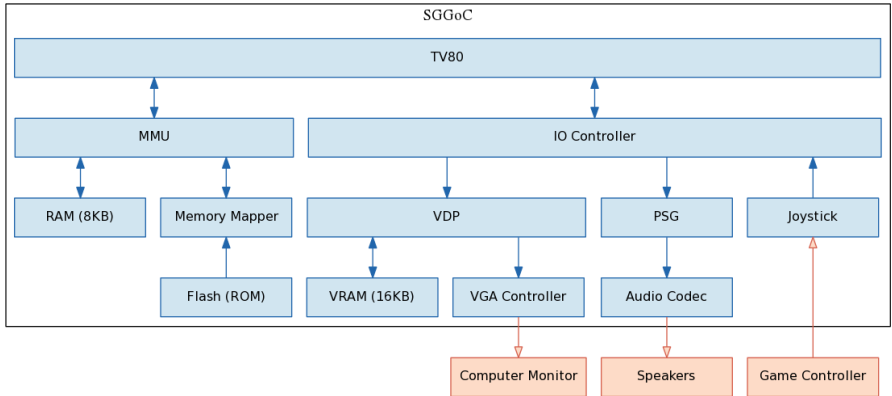
Sega Master System PCB



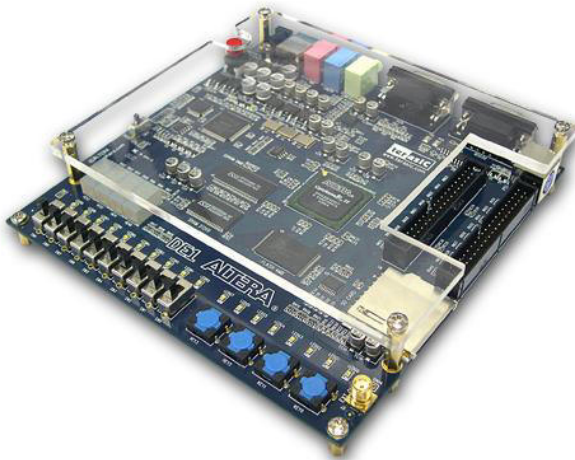
Black Box Diagram



Transparent Box Diagram

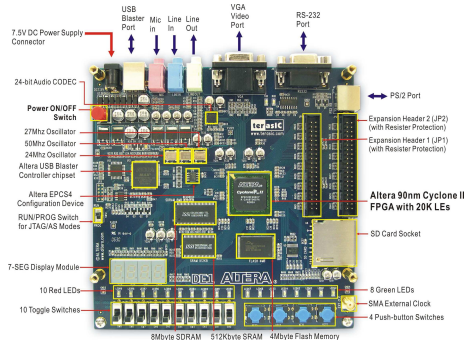


FPGA Development Board



Altera DE1

- Cyclone II EP2C20F484C7
- VGA, Audio, SD Card, 4 MB Flash
- Supports a familiar command line development environment
- Extremely good documentation



Design Strategy

1. Break down system components according to the original system architecture
2. Implement each component to match the original functionality described by official and non official documents
3. Test each components functionality against the actual hardware (in our case an emulator)
4. Tie components together in a way that is better suited toward FPGA technology (*E.g.* avoid tri-state buses)

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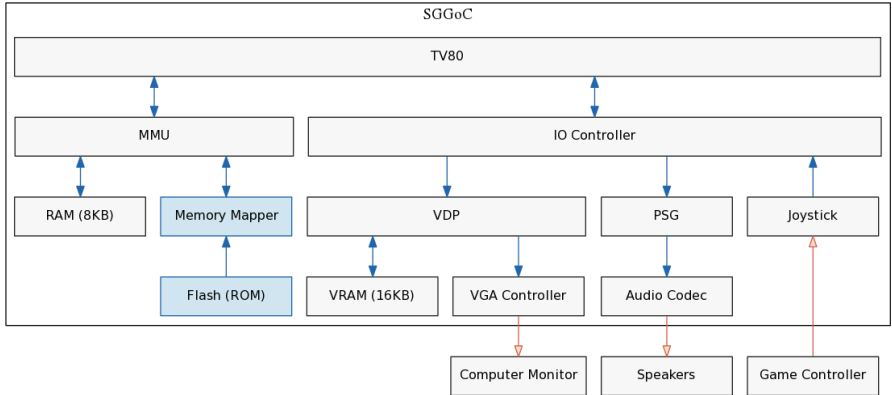
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Game Cartridge



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Each game cartridge made up of at least two components:

- Game data ROM
- Memory Mapper



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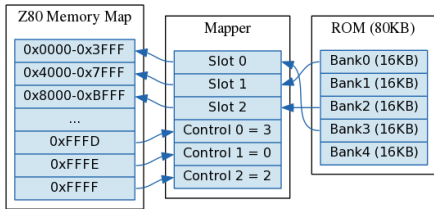


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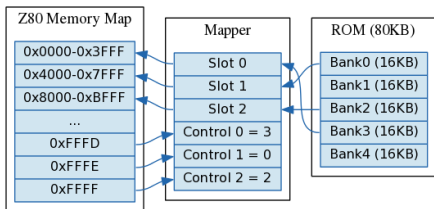
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Storing Game ROMs

A few options to store game ROMs:

1. Hookup the actual cartridge

- Straight forward
- Don't have to re-implement the memory mappers
- Defeats most of the point of the project

2. Store them on a SD card

- Extremely portable / convenient
- Complicated interface

3. Store them on the 4MB flash chip on the DE1

- Fairly straightforward
- Extremely non-portable
- Flash chip looks just like original ROM chips

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Need a tool to load a ROM file into the flash chip from the PC

1. Load RS232-to-Flash bridge into the FPGA
2. PC waits for FPGA to request a byte
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4. FPGA writes byte to flash
5. Go back to 2

Can also do the reverse to read back and verify the flash contents against the ROM file

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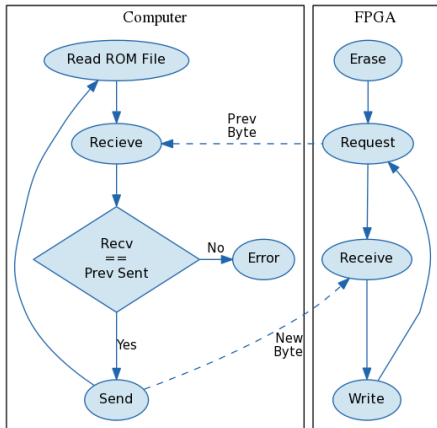
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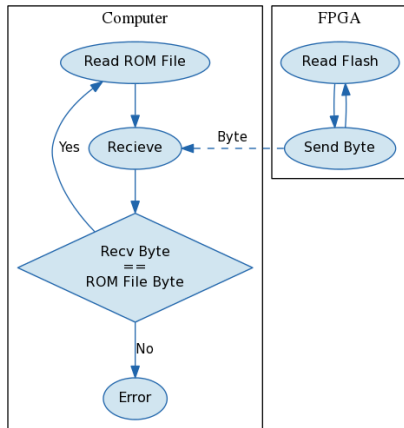
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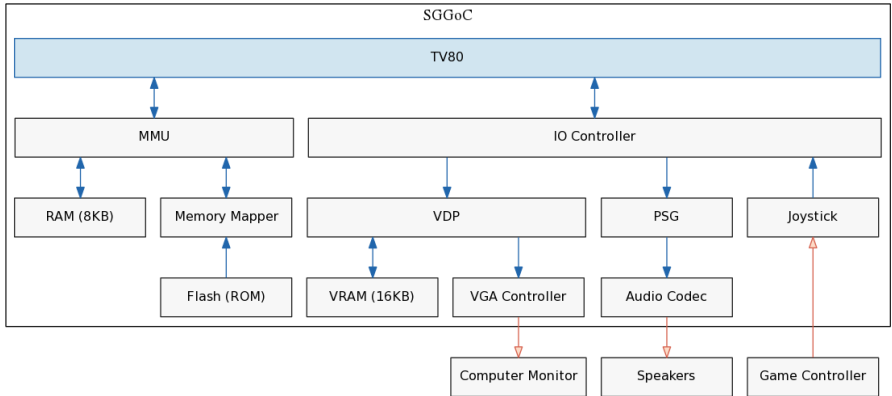
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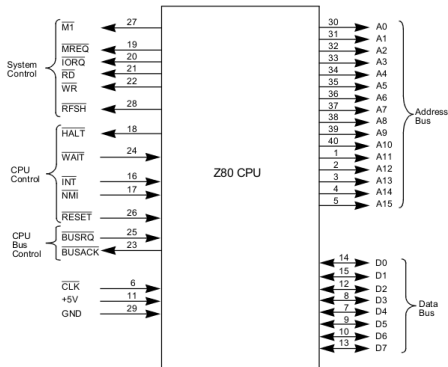


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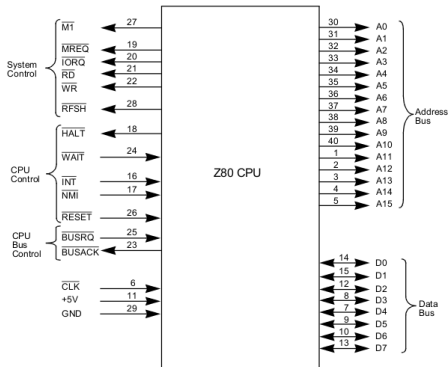
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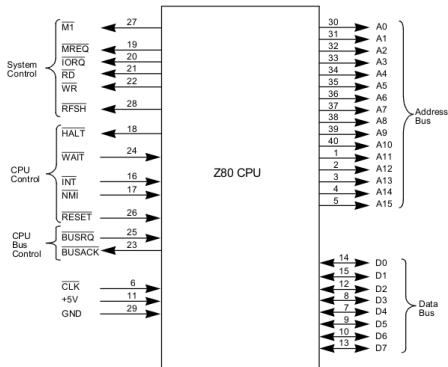
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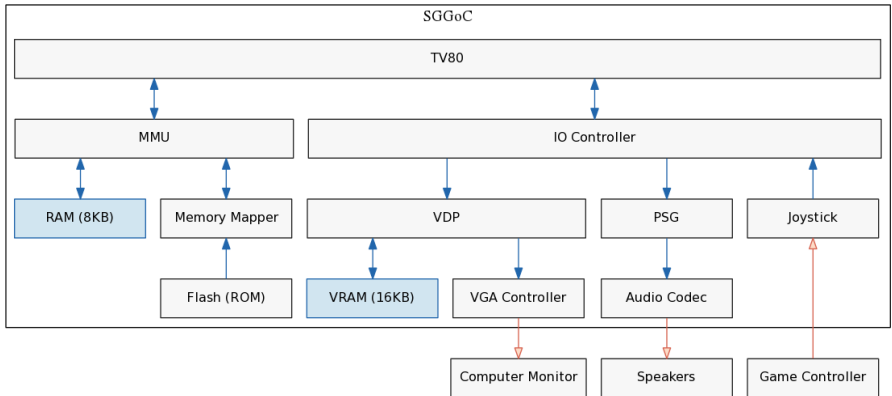
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System and Video RAM



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- Cyclon II has enough internal block RAM (30KB) to fit both system and video RAM
- *Design Strategy:* Write code that implies generic block RAM as opposed to device specific primitives to increase portability of codebase

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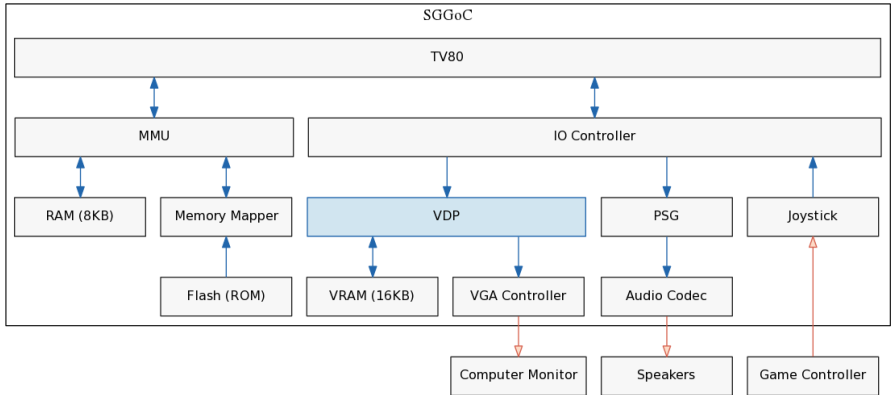
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- Used in a number of legacy systems but no good HDL implementation exists online
- Meant to drive CRTs so functionality maps perfectly to the VGA interface on the DE1
- Communicates with the Z80 as an IO device

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Testing Strategy

Game Gear is hard to test/verify

- Its only output is video (no UART, JTAG, etc..)
- Most documentation is 3rd party

Our strategy:

1. Use an emulator to watch memory fetches and get memory dumps
2. Initialize our RAMs with these dumps and verify we achieve the same visual output
3. Watch instruction fetches with a logic analyzer and see if they match the emulator

Could replace emulator with a logic/bus analyzer connected to the original hardware

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Issues of Concern

- Each component is tightly dependant on each other. Need to implement each one correctly for whole system to function.
- If something doesn't work we cannot simply change the design spec. We are working against an established spec that cannot be changed.

Questions?