GOWIN
PROGRAMMING FOR THE FUTURE

GW2AR series of FPGA Products

Data Sheet

DS226-2.5E, 2025-05-23

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Revision History

Date	Version	Description
05/11/2018	1.1E	Initial release.
08/01/2018	1.2E	● PLL Structure diagram updated. ● The description of the SystemIO status for blank chips updated.
09/10/2018	1.3E	$V_{CCO2/6/7}$ and V_{CCX} of GW2AR-18 QN88 with SDRAM embedded are internal short circuited.
11/12/2018	1.4E	● PSRAM added. ● GW2AR-18 QN88P and EQ144P with PSRAM added. ● Part Name updated.
01/09/2019	1.5E	Reference manuals for memories updated.
04/01/2019	1.6E	● Changed the operating temperature (Industrial) to junction temperature. ● The package of EQ176 added.
11/12/2019	1.7E	● Number of Max. I/O updated. ● The package size of LQ144/EQL144/LQ176/EQ176 fixed. ● IODELAY description updated.
03/10/2020	1.8E	Bit width and capacity of GW2AR-18 added.
06/19/2020	1.8.1E	● Package name optimized. Figures of part name optimized.
08/07/2020	1.9E	QN88PF and EQ144PF added.
05/28/2021	1.9.1E	PG256S added.
05/25/2022	1.9.2E	● Recommended I/O operating conditions updated. ● Power supply ramp rates updated.
09/06/2022	2.0E	● The maximum value of the differential input threshold V_{THD} updated. ● Note about DC current limit added. ● “Table 3-3 Power Supply Ramp Rates” updated. ● “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” updated. ● “Figure 2-1 Architecture Overview” updated.
09/29/2022	2.1E	● The PG256S package removed. ● “2.3Configurable Function Units” added.
11/18/2022	2.1.1E	● “Figure 2-1 Output I/O Standards and Configuration Options” updated. ● “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” updated. ● Section 3.5.4 Byte-enable removed.
01/12/2023	2.1.2E	● “Table 3-1 Absolute Max. Ratings” updated. ● “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” updated. ● “Table 3-9 Static Current” updated.
02/27/2023	2.2E	● GW2AR-18 LQ144 and LQ176 removed. ● Information on Slew Rate removed.
10/10/2023	2.3E	● Editorial updates. ● Note about the default state of GPIOs modified. ● “2.5.2Memory Configuration Modes” added. ● The I/O logic output diagram and the I/O logic input diagram combined into “Figure 2-5 I/O Logic Input and Output”. ● “2.5.6 Power up Conditions” removed.

Date	Version	Description
		● “Table 3-3 Power Supply Ramp Rates” updated. ● Note for “Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions” modified. ● “Table 3-18 External Switching Characteristics” updated. ● “Figure 4-3 Package Marking Examples” updated.
03/14/2025	2.4E	● “Table 1-1 Product Resources” updated. ● Description of IODELAY module updated. ● Description of DES module optimized. ● Note about ripples added to“Table 3-2 Recommended Operating Conditions”. ● “Table 3-13 CFU Timing Parameters” updated. ● “Table 3-14 BSRAM Timing Parameters” updated. ● “Table 3-15 DSP Timing Parameters” updated. ● “Table 3-16 DSP Max Frequency Specifications” added. ● “Table 3-17 Gearbox Timing Parameters” added. ● Note on functional description of dual port BSRAM and semi-dual port BSRAM modified.
05/23/2025	2.5E	● Features of DDR SDRAM updated. ● “Figure 2-1 Output I/O Standards and Configuration Options” updated: correcting drive strength values for some I/O types. ● “Table 2-2 Input I/O Standards and Configuration Options” updated: modifying V_{CCIO} values for some I/O types. ● “3.4.7 PLL Switching Characteristics” updated. ● Note for “Figure 4-3 Package Marking Examples” updated.

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1 General Description

The GW2AR FPGAs are members of the 2 series of the Arora family. The GW2AR devices are system-in-package chips with memory chips integrated into them based on the GW2A devices, featuring high-performance DSP resources, high-speed LVDS interfaces, and abundant BSRAM memory resources. These embedded resources combined with a streamlined FPGA architecture and 55nm process make the GW2AR series of FPGA products suitable for high-speed and low-cost applications.

Gowin provides an advanced FPGA hardware development environment that supports FPGA synthesis, placement & routing, bitstream generation and download, etc.

1.1 Features

- Lower power consumption
  - 55nm SRAM process
  - Core voltage: 1.0V
  - Supports dynamically turning on/off the clock
- System-in-package chips integrating SDRAMs/PSRAMs
- Multiple I/O standards
  - LVCMOS33/25/18/15/12；LVTTL33,SSTL33/25/18 I, II, SSTL15；HSTL18 I, II, HSTL15 I；PCI, LVDS25, RSDS, LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis options
  - Drive strength options
  - Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
  - Hot socketing
- MIPI D-PHY RX/TX Implemented by Using GPIOs
  - Supports MIPI CSI-2 and MIPI DSI RX/TX with a data rate of up to 1.2Gbps per lane
  - Two IO types are available: TLVDS, ELVDS
- High-performance DSP blocks
  - High-performance digital signal processing
  - Supports 9 x 9,18 x 18,36 x 36 bit multipliers and 54-bit accumulators
  - Supports cascading of multipliers

  - Supports pipeline mode and bypass mode
  - Pre-addition operation for the filter function
  - Supports barrel shifters
- Abundant basic logic cells
  - 4-input LUTs (LUT4s)
  - Supports shift registers and shadow SRAMs
- Block SRAMs with multiple modes
  - Supports Dual Port mode, Single Port mode, and Semi-Dual Port mode
- Flexible PLLs
  - Frequency adjustment (multiplication and division) and phase adjustment
  - Supports global clocks
- Configuration
  - JTAG configuration
  - Four GowinCONFIG configuration modes: SSPI, MSPI, CPU, SERIAL
  - Supports bitstream file encryption and security bit settings

1.2 Product Resources

Table 1-1 Product Resources

Device	GW2AR-18
LUT4s	20,736
Flip-Flops (FFs)	15,552
Shadow SRAM (SSRAM) Capacity (bits)	40K
Block SRAM (BSRAM) Capacity (bits)	828K
Number of BSRAMs	46
SDR / DDR SDRAM (bits)	64M / 128M
PSRAM (bits)	64M
Multipliers (18 x 18 Multipliers)	48
Maximum PLLs[1]	4
I/O Banks	8
Maximum GPIOs[2]	384
Core voltage	1.0V

Note!

- [1] Different packages support different numbers of PLLs. Up to four PLLs can be supported.
- [2] This is the maximum number of GPIOs the device can provide without package limitation. Please refer to Table 1-3 for the maximum number of user I/Os available for the specific packages.

Table1-2 Package-Memory Combinations

Package	Device	Memory Type	Width	Capacity	Available PLLs
EQ144[1]	GW2AR-18	SDR SDRAM	32 bits	64M bits	PLLL0/PLLL1/PLLR0/PLLR1
EQ144P[1] [2]	GW2AR-18	PSRAM	16 bits	64M bits	
EQ144PF[1] [2]	GW2AR-18	PSRAM	16 bits	64M bits	

Package	Device	Memory Type	Width	Capacity	Available PLLs
QN88	GW2AR-18	SDR SDRAM	32 bits	64M bits	PLLL1/ PLLR1
QN88P [2]	GW2AR-18	PSRAM	16 bits	64M bits	
QN88PF [2]	GW2AR-18	PSRAM	16 bits	64M bits	
EQ176	GW2AR-18	DDR SDRAM	16 bits	128M bits	PLLL1/PLLR0/PLLR1

Note!

- [1] $V_{CCPLLL1}$ and V_{CC} of the EQ144/EQ144P/EQ144PF packages are internally tied together. Please refer to Table 3-2 for details.
- [2] "P" indicates PSRAM; "F" indicates that some pins have been adjusted in QN88PF/EQ144PF compared with QN88P/EQ144P.

Table 1-3 Device-Package Combinations and Maximum User I/Os (True LVDS Pairs)

Package	Pitch (mm)	Size (mm)	E-pad Size (mm)	GW2AR-18
EQ144	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144P	0.5	20 x 20	9.74 x 9.74	120(35)
EQ144PF	0.5	20 x 20	9.74 x 9.74	120(35)
QN88	0.4	10 x 10	6.74 x 6.74	66(22)
QN88P	0.4	10 x 10	6.74 x 6.74	66(22)
QN88PF	0.4	10 x 10	6.74 x 6.74	66(22)
EQ176	0.4	20 x 20	6 x 6	140(45)

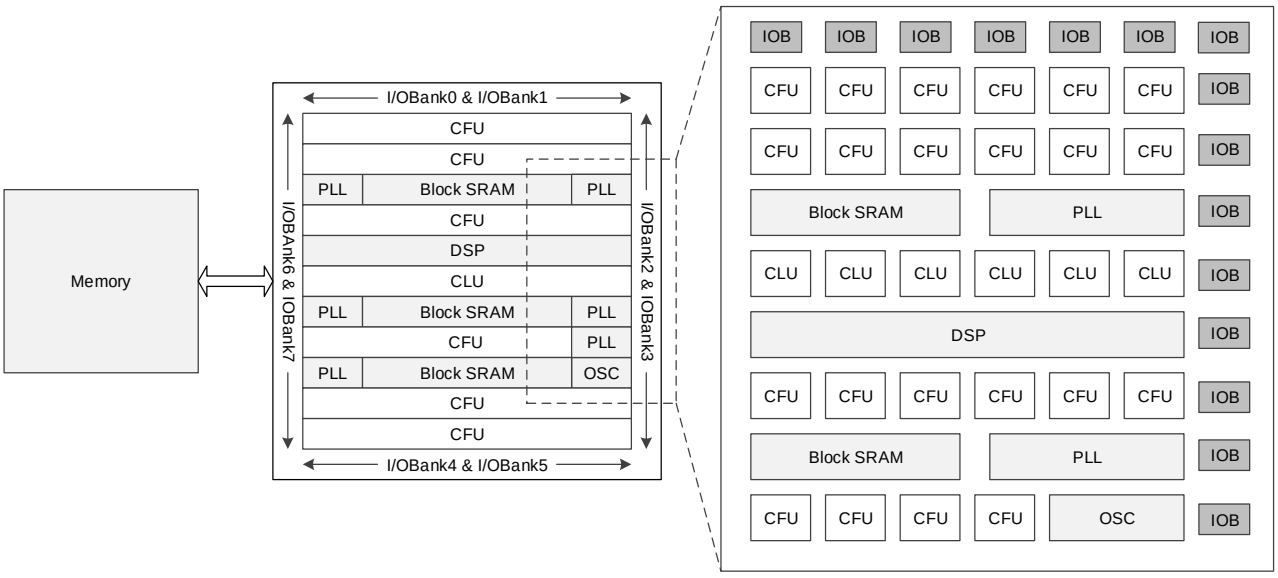
Note!

- The package types in this manual are referred to by acronyms, see 4.1 Part Naming for more information.
- JTAGSEL_N and JTAG pins cannot be used as GPIOs simultaneously. The number of maximum user I/Os noted in this table is referred to when the four JTAG pins (TCK, TDI, TDO, and TMS) are used as GPIOs. See UG229, GW2AR series of FPGA Products Package and Pinout for more details.

2 Architecture

2.1 Architecture Overview

Figure 2-1 Architecture Overview



As shown in Figure 2-1, the GW2AR device is a system-in-package(SIP) chip that combines the GW2A device and a memory chip. For the features of the memory chips, please refer to 2.2 Memory.

See Table 1-1 for more information on the resources provided. The core of the FPGA is an array of logic cells surrounded by IO blocks. Besides, BSRAMs, DSP blocks, PLLs, and an on-chip oscillator are provided.

The Configurable Function Unit (CFU) and the Configurable Logic Unit (CLU) are the two kinds of basic logic blocks that form the core of GW2AR FPGAs. Devices with different capacities have different numbers of rows and columns of CFUs/CLUs. For more information, see 2.3 Configurable Function Units.

The I/O resources in the GW2AR series of FPGA products are arranged around the periphery of the devices in groups referred to as

banks, which are divided into eight banks, including Bank0 - Bank7. The I/O resources support multiple I/O standards and can be used for regular mode, SDR mode, generic DDR mode, and DDR_MEM mode. For more information, see 2.4 Input/Output Blocks.

BSRAMs are arranged in row(s) inside the GW2AR series of FPGA products. Each BSRAM has a capacity of 18 Kbits and supports multiple configuration modes and operation modes. For more information, see 2.5 Block SRAM.

The GW2AR series of FPGA products provide DSP blocks. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU. For more information, see 2.6 Digital Signal Processing.

The GW2AR series of FPGA products have embedded PLL resources. The PLLs can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be realized by configuring the parameters. These FPGAs also have an embedded programmable on-chip clock oscillator that supports clock frequencies ranging from 2.5 MHz to 125MHz, providing clocking resources for the MSPI mode. It provides an MSPI clock source for the MSPI configuration mode with a tolerance of ±5%. For more information, see 2.7 Clocks and 2.11 On-chip Oscillator.

There are also abundant Configurable Routing Units (CRUs) that interconnect all the resources within the FPGA. For example, routing resources distributed in CFUs and IOBs interconnect resources in them. Routing resources can be automatically generated by the Gowin software. In addition, the GW2AR series of FPGA products also provide abundant dedicated clock resources, long wires (LWs), global set/reset (GSR) resources, programming options, etc. For more details, see 2.7 Clocks, 2.8 Long Wires, and 2.9 Global Set/Reset.

2.2 Memory

The GW2AR series of FPGA products in different packages have different capacities and types of memory. Please refer to 1.2 Product Resources for more information.

2.2.1 SDR SDRAM

Features

- Access time: 5.4ns/5.4ns
- Clock frequency: 166 MHz
- Data width: 32bits
- Capacity：64Mbits
- Synchronous Operation
- Internal pipelined architecture
- Four internal banks (512K x 32bits x 4 banks)
- Programmable mode
  - Column address strobe latency: 2 or 3
  - Burst lengths: 1, 2, 4, 8, or full page
  - Burst type: sequential mode or interleaved mode

  - Burst-Read-Single-Write
  - Burst stop function
- Byte masking function
- Auto refresh and self refresh
- 4,096 refresh cycles/64 ms
- 3.3V±0.3V power supply[1]
- LVTTL Interface

Note!

- [1] For more information about the power supply, please refer to Table 3-2.

Overview

The SDR SDRAM integrated in the GW2AR series of FPGA Products is a high-speed CMOS synchronous DRAM with a capacity of 64 Mbits. The SDR SDRAM consists of four banks with each bank containing 512K x 32 bits. Each bank is organized as 2048 rows x 256 columns x 32 bits. Burst accesses are supported. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The SDRAM provides read or write burst lengths of 1, 2, 4, 8, or full page, with a burst termination option. An auto pre-charge function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst sequence. Both the auto-refresh and self-refresh functions are easy to use. Besides, by using a programmable mode register, the system can choose the most suitable modes to maximize its performance.

The supply voltage for the SDR SDRAM interface is 3.3V, and the I/O Bank voltage that connects to the SDR SDRAM needs to be 3.3V. For more details, please refer to Table 3-2.

The IP Core Generator integrated in the Gowin Software supports a SDR SDRAM controller IP that can interface to both embedded and external SDRAMs. This controller IP can be used for the SDRAM power-up initialization, activation, auto-refresh, etc. For more information, please refer toIPUG279，Gowin SDRAM Controller User Guide.

2.2.2 DDR SDRAM

Features

- Clock frequency: 250MHz
- Data width: 16bits
- Capacity: 128 Mbits
- Differential clock input: CLK and ~CLK
- Bi-directional DQS
- Synchronous Operation
- Internal pipelined architecture
- Four internal banks, 2M x 16 bits for each bank
- Programmable Mode and Extended Mode registers
  - Column address strobe latency: 2, 2.5, 3
  - Burst lengths: 2, 4, 8
  - Burst type: sequential mode or interleaved mode

- Byte masking function
- DM Write Latency = 0
- Auto refresh and self refresh
- 4,096 refresh cycles/64 ms
- Pre-charge power down & active power down
- 2.5V±0.2V power supply[1]
- SSTL_2 interface

Note!

[1] For more information about the power supply, please refer to Table 3-2.

Overview

The DDR SDRAM integrated in the GW2AR series of FPGA products is a high-speed CMOS synchronous DRAM with a capacity of 128 Mbits. The DDR SDRAM consists of four banks with each bank containing 2M x16 bits. Data outputs occur at the rising edges of both CLK and ~CLK. Burst accesses are supported. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. Read or write burst lengths of 2, 4, or 8 are supported. An auto pre-charge function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst sequence. Both the auto-refresh and self-refresh functions are easy to use. Besides, by using a programmable mode register and extended mode register, the system can choose the most suitable modes to maximize its performance.

The supply voltage for the DDR SDRAM interface is 2.5V, and the I/O Bank voltage that connects to the DDR SDRAM needs to be 2.5V. For more details, please refer to Table 3-2.

The IP Core Generator integrated in the Gowin Software supports a DDR controller IP that can interface to both embedded and external SDRAMs. This controller IP can be used for the DDR power-up initialization, read calibration, auto-refresh, etc. For more information, please refer to IPUG507，Gowin DDR Memory Interface IP User Guide.

2.2.3 PSRAM

Features

- Clock frequency: 166MHz, DDR332
- Double Data Rate
- Data width: 16bits
- Read-write data strobe (RWDS)
- Temperature compensated refresh
- Partial array self-refresh (PASR)
- Hybrid sleep mode
- Deep power down(DPD)
- Drive strengths: 35, 50, 100, and 200 Ohm
- Burst access
- Burst lengths: 16/32/64/128
- Status/control registers
- 1.8V power supply[1]

Note!

[1] For more information about the power supply, please refer to Table 3-2.

The supply voltage for the PSRAM interface is 1.8V, and the I/O Bank voltage that connects to the PSRAM needs to be 1.8V. For more details, please refer to Table 3-2.

The IP Core Generator integrated in the Gowin Software supports a PSRAM controller IP that can interface to both embedded and external PSRAMs. This controller IP can be used for the PSRAM power-up initialization, read calibration, etc. For more information, please refer to IPUG525, Gowin HyperRAM & PSRAM Memory Interface IP User Guide.

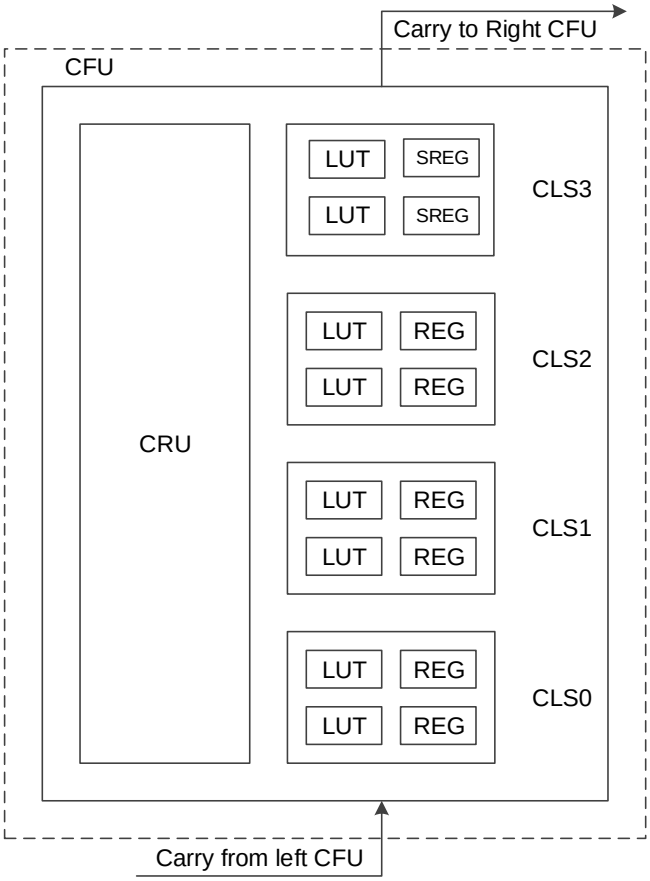
2.3 Configurable Function Units

Configurable Function Units (CFUs) and/or Configurable Logic Units (CLUs) are the basic cells that make up the core of Gowin FPGAs. Each basic cell consists of four Configurable Logic Sections (CLSs) and their routing resource Configurable Routing Units (CRUs), with three of the CLSs each containing two 4-input LUTs and two registers, and the remaining one only containing two 4-input LUTs, as shown in Figure 2-2.

The CLSs in the CLUs cannot be configured as SRAMs, but can be configured as basic LUTs, ALUs, and ROMs. The CLSs in the CFUs can be configured as basic LUTs, ALUs, SRAMs, and ROMs according to application scenarios.

For more information on the CFUs, see UG288, Gowin Configurable Function Unit (CFU) User Guide.

Figure 2-2 CFU Structure View



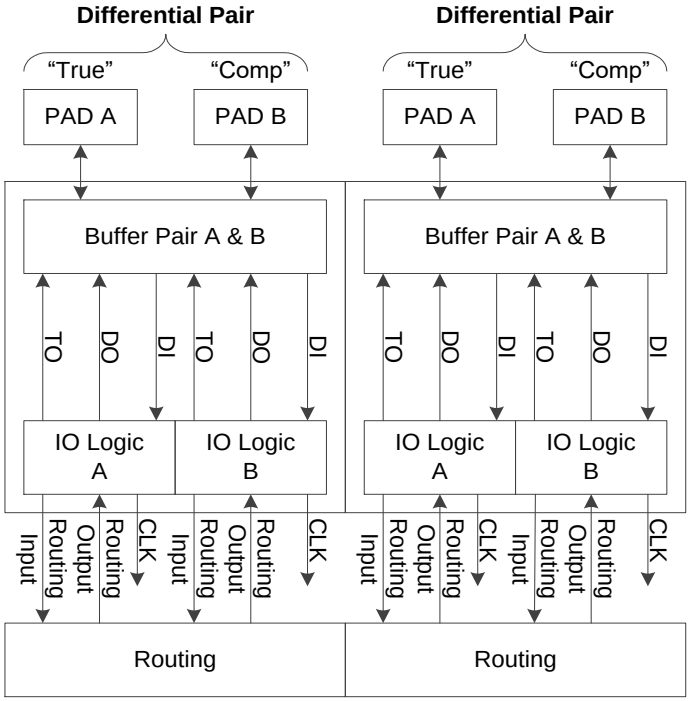
Note!

The SREGs need special patch support. Please contact Gowin’s technical support or local office for this patch.

2.4 Input/Output Blocks

The Input/Output Block (IOB) in the GW2AR series of FPGA products consists of a buffer pair, IO logic, and corresponding routing units. As shown below, each IOB connects to two pins (marked as A and B), which can be used as a differential pair or as two single-ended inputs/outputs.

Figure 2-3 IOB Structure View



The features of the IOB include:

- V_{CCIO} supplied to each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, HSTL, etc.
- Input hysteresis options
- Drive strength options
- Individual Bus Keeper, Pull-up/Pull-down, and Open Drain options
- Hot socketing
- IO logic supports basic mode, SDR mode, DDR mode, etc.

2.4.1 - 2.4.3 describe I/O standards, I/O logic, and I/O logic modes. For more information about the IOB, please refer to UG289,Gowin Programmable IO (GPIO) User Guide.

2.4.1 I/O Standards

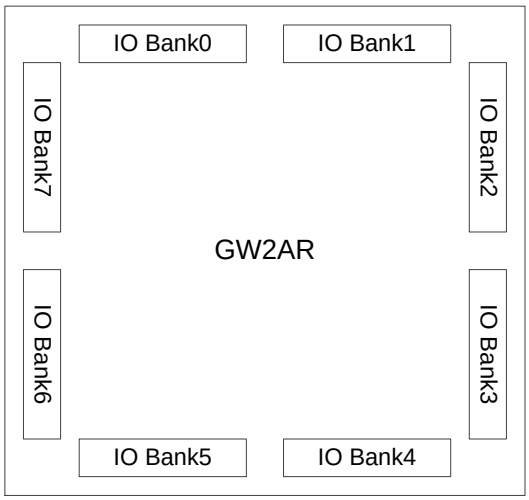
There are eight I/O Banks in the GW2AR series of FPGA products, as shown in Figure 2-4. Each bank has its own I/O power supply V_{CCIO}. V_{CCIO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V.

V_{CCX} and V_{CCIO} that power the SDR SDRAM need to be set to 3.3V, see 2.2.1 SDR SDRAM.

V_{CCX} and V_{CCIO} that power the DDR SDRAM need to be set to 2.5V, see 2.2.2 DDR SDRAM.

To support SSTL, HSTL, etc., Each bank also has one independent voltage source (V_{REF}) as the reference voltage. You can choose to use the internal V_{REF} (0.5 x V_{CCIO}) or the external V_{REF} input via any IO from the bank. V_{CCX} supports 2.5V and 3.3V.

Figure 2-4 I/O Bank Distribution View of GW2AR



Different banks in the GW2AR series of FPGA Products support different on-die termination settings, including single-ended resistors and differential resistors. Single-ended resistors are set for SSTL/HSTL input/output and are supported in Bank2/3/6/7. Differential resistors are set for LVDS input and are only supported in Bank 0/1, see UG289, Gowin Programmable IO User Guide for more details.

Note!

During configuration, all GPIOs of the device are high-impedance with internal weak pull-ups. After the configuration is complete, the I/O states are controlled by user programs and constraints. The states of configuration-related I/Os differ depending on the configuration mode.

For the V_{CCIO} requirements of different I/O standards, see Figure 2-1 and Table 2-2.

Figure 2-1 Output I/O Standards and Configuration Options

I/O Type (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVTTL33	Single-ended	3.3	4/8/12/16/24	Universal interface
LVCMOS33	Single-ended	3.3	4/8/12/16/24	Universal interface
LVCMOS25	Single-ended	2.5	4/8/12/16	Universal interface
LVCMOS18	Single-ended	1.8	4/8/12	Universal interface
LVCMOS15	Single-ended	1.5	4/8	Universal interface
LVCMOS12	Single-ended	1.2	4/8	Universal interface
SSTL25_I	Single-ended	2.5	8	Memory interface
SSTL25_II	Single-ended	2.5	8	Memory interface
SSTL33_I	Single-ended	3.3	8	Memory interface
SSTL33_II	Single-ended	3.3	8	Memory interface

I/O Type (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
SSTL18_I	Single-ended	1.8	8	Memory interface
SSTL18_II	Single-ended	1.8	8	Memory interface
SSTL15	Single-ended	1.5	8	Memory interface
HSTL18_I	Single-ended	1.8	8	Memory interface
HSTL18_II	Single-ended	1.8	8	Memory interface
HSTL15_I	Single-ended	1.5	8	Memory interface
PCI33	Single-ended	3.3	4/8	PC and embedded system
LVPECL33E	Differential	3.3	16	High-speed data transmission
MLVDS25E	Differential	2.5	16	LCD timing driver interface and column driver interface
BLVDS25E	Differential	2.5	16	Multi-point high-speed data transmission
RSDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25E	Differential	2.5	8	High-speed point-to-point data transmission
LVDS25	Differential(TLVDS)	2.5/3.3	1.25/2/2.5/3.5	High-speed point-to-point data transmission
RSDS	Differential(TLVDS)	2.5/3.3	1.25/2/2.5/3.5	High-speed point-to-point data transmission
MINILVDS	Differential(TLVDS)	2.5/3.3	1.25/2/2.5/3.5	LCD timing driver interface and column driver interface
PPLVDS	Differential(TLVDS)	2.5/3.3	1.25/2/2.5/3.5	LCD row/column driver
SSTL15D	Differential	1.5	8	Memory interface
SSTL25D_I	Differential	2.5	8	Memory interface
SSTL25D_II	Differential	2.5	8	Memory interface
SSTL33D_I	Differential	3.3	8	Memory interface
SSTL33D_II	Differential	3.3	8	Memory interface
SSTL18D_I	Differential	1.8	8	Memory interface
SSTL18D_II	Differential	1.8	8	Memory interface
HSTL18D_I	Differential	1.8	8	Memory interface
HSTL18D_II	Differential	1.8	8	Memory interface
HSTL15D_I	Differential	1.5	8	Memory interface
LVCMOS12D	Differential	1.2	4/8	Universal interface
LVCMOS15D	Differential	1.5	4/8	Universal interface

I/O Type (output)	Single-ended/Differential	Bank V_{CCIO}(V)	Drive Strength (mA)	Typical Applications
LVCMOS18D	Differential	1.8	4/8/12	Universal interface
LVCMOS25D	Differential	2.5	4/8/12/16	Universal interface
LVCMOS33D	Differential	3.3	4/8/12/16/24	Universal interface

Table 2-2 Input I/O Standards and Configuration Options

I/O Type (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
LVTTL33	Single-ended	3.3	Yes	No
LVCMOS33	Single-ended	3.3	Yes	No
LVCMOS25	Single-ended	2.5	Yes	No
LVCMOS18	Single-ended	1.8	Yes	No
LVCMOS15	Single-ended	1.5	Yes	No
LVCMOS12	Single-ended	1.2	Yes	No
SSTL15	Single-ended	1.5	No	Yes
SSTL25_I	Single-ended	2.5	No	Yes
SSTL25_II	Single-ended	2.5	No	Yes
SSTL33_I	Single-ended	3.3	No	Yes
SSTL33_II	Single-ended	3.3	No	Yes
SSTL18_I	Single-ended	1.8	No	Yes
SSTL18_II	Single-ended	1.8	No	Yes
HSTL18_I	Single-ended	1.8	No	Yes
HSTL18_II	Single-ended	1.8	No	Yes
HSTL15_I	Single-ended	1.5	No	Yes
PCI33	Single-ended	3.3	Yes	No
LVCMOS33OD25	Single-ended	2.5	No	No
LVCMOS33OD18	Single-ended	1.8	No	No
LVCMOS33OD15	Single-ended	1.5	No	No
LVCMOS25OD18	Single-ended	1.8	No	No
LVCMOS25OD15	Single-ended	1.5	No	No
LVCMOS18OD15	Single-ended	1.5	No	No
LVCMOS15OD12	Single-ended	1.2	No	No
LVCMOS25UD33	Single-ended	3.3	No	No
LVCMOS18UD25	Single-ended	2.5	No	No
LVCMOS18UD33	Single-ended	3.3	No	No

I/O Type (input)	Single-ended/Differential	Bank V_{CCIO}(V)	Hysteresis Options Supported?	V_{REF} Required?
LVCMOS15UD18	Single-ended	1.8	No	No
LVCMOS15UD25	Single-ended	2.5	No	No
LVCMOS15UD33	Single-ended	3.3	No	No
LVCMOS12UD15	Single-ended	1.5	No	No
LVCMOS12UD18	Single-ended	1.8	No	No
LVCMOS12UD25	Single-ended	2.5	No	No
LVCMOS12UD33	Single-ended	3.3	No	No
LVDS25	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33E	Differential	3.3	No	No
SSTL15D	Differential	1.5	No	No
SSTL25D_I	Differential	2.5	No	No
SSTL25D_II	Differential	2.5	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8	No	No
SSTL18D_II	Differential	1.8	No	No
HSTL18D_I	Differential	1.8	No	No
HSTL18D_II	Differential	1.8	No	No
HSTL15D_I	Differential	1.5	No	No
LVCMOS12D	Differential	1.2	No	No
LVCMOS15D	Differential	1.5	No	No
LVCMOS18D	Differential	1.8	No	No
LVCMOS25D	Differential	2.5	No	No
LVCMOS33D	Differential	3.3	No	No

2.4.2 I/O Logic

Figure 2-5 shows the I/O logic input and output of the GW2AR series

of FPGA products.

Figure 2-5 I/O Logic Input and Output

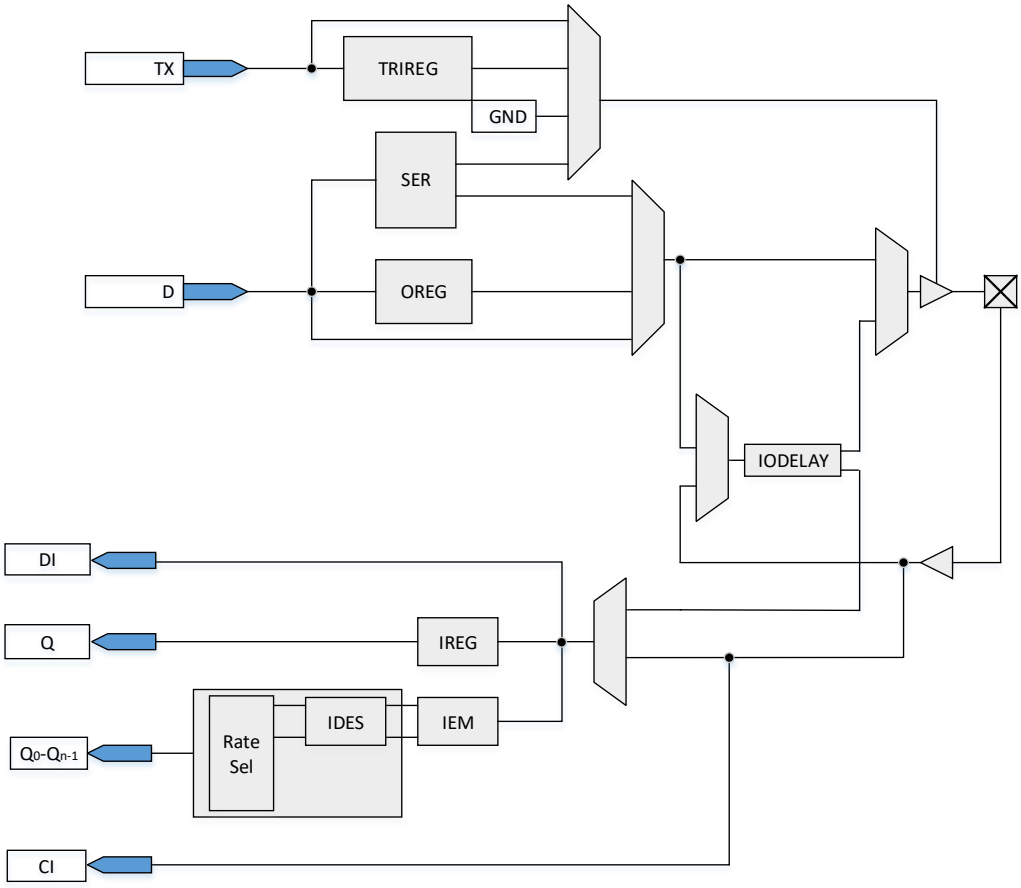


Table 2-3 Port Description

Port	I/O	Description
CI[1]	Input	GCLK input signal. For the number of GCLK input signals, please refer to UG115， GW2AR-18 Pinout.
DI	Input	IO port low-speed input signal input into the fabric directly.
Q	Output	IREG output signal in the SDR module.
Q_0-Q_{n-1}	Output	IDES output signal in the DDR module.

Note!

When CI is used as GCLK input, DI, Q, and Q_0-Q_{n-1} cannot be used as I/O input and output.

Descriptions of the I/O logic modules of the GW2AR series of FPGA products are presented below.

IODELAY

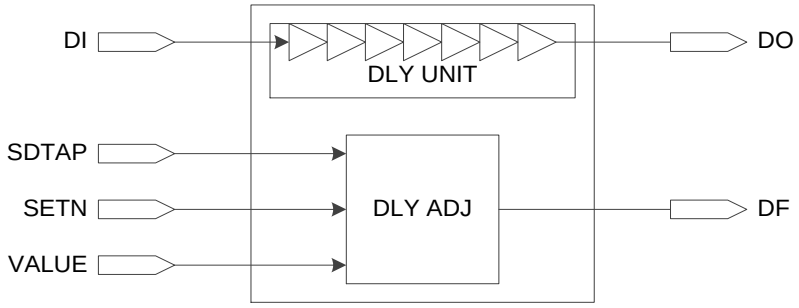
See Figure 2-6 for an overview of the IODELAY module. Each I/O of the GW2AR series of FPGA products contains the IODELAY module, through which you can add additional delays to the I/O to adjust the delay of the signal. The delay time of each step is $T_{dlyunit}$, and the number of steps is DLYSTEP. The total delay time of IODELAY can be calculated as

follows: $T_{totdly} = T_{dlyoffset} + T_{dlyunit} * DLYSTEP$. See Table 2-4 for the total delay time.

Table 2-4 Total Delay of IODELAY Module

	Min.	Typ.	Max.
$T_{dlyoffset}$	300ps	350ps	400ps
$T_{dlyunit}$	-	18ps	-
DLYSTEP	0	-	127

Figure 2-6 IODELAY Diagram



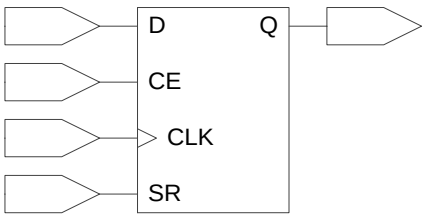
There are two ways to control the delay:

- Static control.
- Dynamic control: can be used with the IEM module to adjust the dynamic sampling window. The IODELAY module cannot be used for both input and output at the same time.

I/O Register

See Figure 2-7 for the I/O register in the GW2AR series of FPGA products. Each I/O provides one input register (IREG), one output register (OREG), and one tristate register (TRIREG).

Figure 2-7 I/O Register Diagram



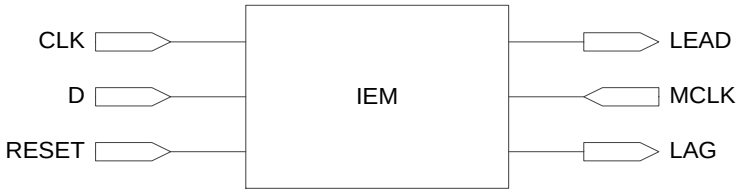
Note!

- CE can be programmed as either active low (0: enable) or active high (1: enable).
- CLK can be programmed as either rising edge triggering or falling edge triggering.
- SR can be programmed as either synchronous/asynchronous SET/RESET or disabled.
- The register can be programmed as a register or a latch.

IEM

The IEM(Input Edge Monitor) module is used to sample data edges and is used in generic DDR mode, as shown in Figure 2-8.

Figure 2-8 IEM Diagram



Deserializer(DES) and Clock Domain Transfer

This series of FPGA products provide a simple deserializer(DES) for input I/O logic to support advanced I/O protocols. The clock domain transfer module in DES provides the ability to safely switch the external sampling clock (strobe) domain to the internal continuously running clock domain. There are multiple registers used for data sampling.

The clock domain transfer module offers the following functions:

- Uses the internal continuous clock instead of the discontinuous DQS signal for data sampling. This feature applies to the DDR memory interface.
- For the DDR3 memory interface standard, aligns the DQS signal and data by read leveling.
- In generic DDR mode, when DQS.RCLK is used for sampling, the clock domain transfer module is also required.

Each DQS module provides WADDR and RADDR signals for the clock domain transfer modules in the same group.

SER

This series of FPGA products provide a simple serializer(SER) for output I/O logic to support advanced I/O protocols.

2.4.3 I/O Logic Modes

The I/O Logic of the GW2AR series of FPGA products supports several operation modes. In each operation mode, the I/O (or I/O differential pair) can be configured as output, input, INOUT or tristate output (output signal with tristate control).

2.5 Block SRAM

2.5.1 Introduction

The GW2AR series of FPGA products provide abundant block SRAM resources. These memory resources are distributed as blocks throughout the FPGA array in the form of rows. Therefore, they are called block static random access memories (BSRAMs). Each BSRAM block occupies 3 CFU locations. The capacity of each BSRAM can be up to 18,432 bits (18 Kbits). There are five configuration modes: Single Port mode, Dual Port mode, Semi-Dual Port mode, ROM mode, and FIFO mode.

The abundant BSRAM resources are available for implementing high-performance designs. The features of BSRAMs include:

- Up to 18,432 bits per BSRAM
- Clock frequency up to 380MHz (230MHz in Read-before-write mode)
- Supports Single Port mode
- Supports Dual Port mode
- Supports Semi-Dual Port mode
- Provides parity bits
- Supports ROM Mode
- Data widths from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Normal Read and Write
- Read-before-write
- Write-through

For more information on the BSRAMs, see UG285, Gowin BSRAM & SSRAM User Guide.

2.5.2 Memory Configuration Modes

BSRAMs in the GW2AR series of FPGA products support various data widths, see Table 2-5.

Table 2-5 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	ROM Mode
16K x 1	16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

Single Port Mode

The single port mode supports 2 read modes (bypass mode and pipeline mode) and 3 write modes (normal mode, write-through mode, and read-before-write mode). In single port mode, writing to or reading from one port is supported. During the write operation, the written data will be transferred to the output of the BSRAM. When the output register is bypassed, the new data will show up at the same write clock rising edge.

For more information on single port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Dual Port Mode

The Dual Port mode supports 2 read modes (Bypass mode and

Pipeline mode) and 2 write modes (Normal mode and Write-through mode). The applicable operations are as follows:

- Two independent read operations
- Two independent write operations
- An independent read operation and an independent write operation

Note!

Performing read and write operations to the same address at the same time is not allowed.

For more information on dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

Semi-Dual Port Mode

The semi-dual port mode supports 2 read modes (Bypass mode and Pipeline mode) and 1 write mode (Normal mode). Semi-dual port mode supports simultaneous read and write operations in the form of writing to port A and reading from port B.

Note!

Performing read and write operations to the same address at the same time is not allowed.

For more information on semi-dual port mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

ROM Mode

BSRAMs can be configured as ROMs. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization is completed during the device power-on process.

Each BSRAM can be configured as one 16Kbit ROM. For more information on ROM mode, please refer to UG285, Gowin BSRAM & SSRAM User Guide.

2.5.3 Mixed Data Width Configuration

The BSRAMs in the GW2AR series of FPGA products support mixed data width operations. In dual port mode and semi-dual port mode, the data widths for read and write can be different, see Table 2-6 and Table 2-7.

Table 2-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

- “*” denotes the modes supported.

Table 2-7 Semi-dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512x32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

- “*” denotes the modes supported.

2.5.4 Parity Bit

There are parity bits in BSRAMs. The 9th bit in each byte can be used as a parity bit to check the correctness of data transmission. It can also be used for data storage.

2.5.5 Synchronous Operation

- All the input registers of BSRAMs support synchronous write.
- The output registers can be used as pipeline registers to improve design performance.
- The output registers are bypass-able.

2.5.6 BSRAM Operation Modes

The BSRAM supports five different operations, including two read modes (Bypass mode and Pipeline mode) and three write modes (Normal mode, Write-through mode, and Read-before-write mode).

Read Mode

The following two read modes are supported.

PIPELINE MODE

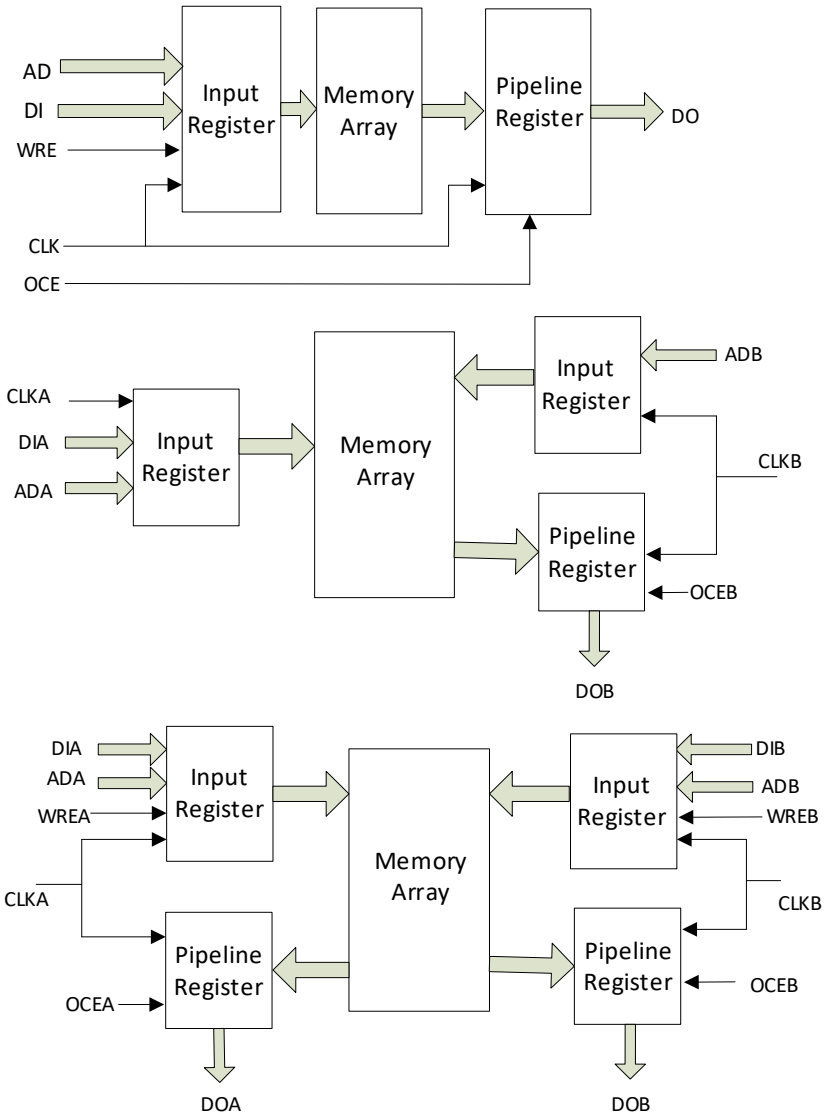
When a synchronous write cycles into a memory array with pipeline registers enabled, the data can be read from pipeline registers in the next clock cycle. The data bus can be up to 36 bits in this mode.

BYPASS MODE

When a synchronous write cycles into a memory array with pipeline registers bypassed, the outputs are registered at the memory array.

Figure 2-9 Pipeline Mode in Single Port Mode, Dual Port Mode, and Semi-dual

Port Mode



Write Mode

NORMAL MODE

In this mode, when you write data to one port, the output data of this port does not change. The written data will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when you write data to one port, the written data will appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when you write data to one port, the written data will be stored in the memory according to the address, and the original data in this address will appear at the output of this port.

2.5.7 Clock Mode

Table 2-8 lists the clock modes in different BSRAM modes:

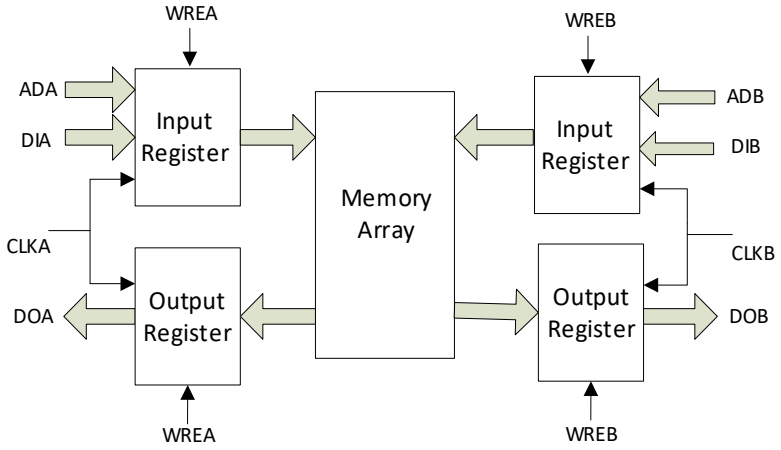
Table 2-8 Clock Modes in Different BSRAM Modes

Clock Mode	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 2-10 shows the independent clock operation in dual port mode with one clock at each port. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

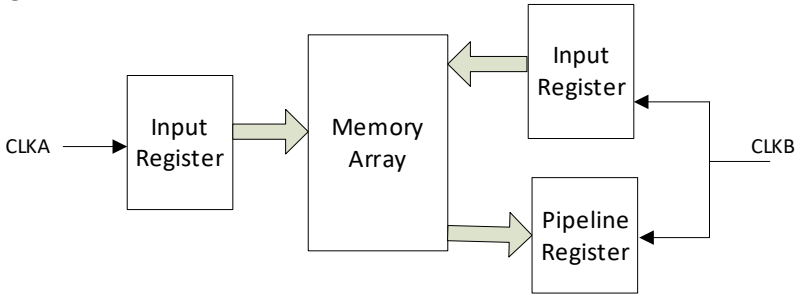
Figure 2-10 Independent Clock Mode



Read/Write Clock Mode

Figure 2-11 shows the read/write clock operation in semi-dual port mode with one clock at each port. The write clock (CLKA) controls data inputs, write addresses and read/write enable signals of Port A. The read clock (CLKB) controls data outputs, read addresses, and read enable signals of Port B.

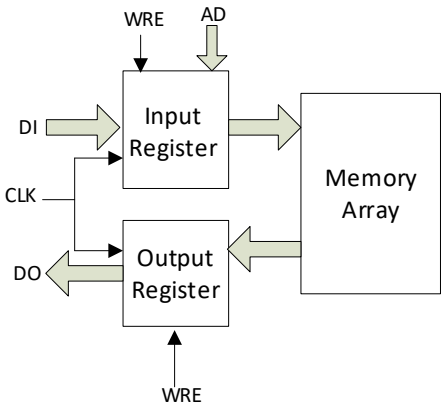
Figure 2-11 Read/Write Clock Mode



Single Port Clock Mode

Figure 2-12 shows the clock operation in single port mode.

Figure 2-12 Single Port Clock Mode



2.6 Digital Signal Processing

GW2AR devices provide abundant DSP resources. Gowin's DSP solutions can address high-performance digital signal processing needs such as FIR and FFT designs. The DSP resources have the advantages of stable timing performance, high resource utilization, and low power consumption.

The DSP resources offer the following functions:

- Multipliers with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data widths
- Barrel shifters
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number
- Supports pipeline mode and bypass mode.

2.6.1 Macro

The DSP blocks are distributed throughout the FPGA array in the form of rows. Each DSP block contains two macros, and each macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

Pre-adder

Each DSP macro contains two pre-adders for implementing pre-addition, pre-subtraction, and shifting.

The pre-adders are located at the first stage and have two input ports:

- Parallel 18-bit input B or SBI
- Parallel 18-bit input A or SIA

Note!

Each input port supports pipeline mode and bypass mode.

Gowin's pre-adders can be used independently as function blocks, which support 9-bit and 18-bit widths.

Multiplier

The multipliers are located after the pre-adders. The multipliers can be configured as 9 x 9, 18 x 18, 36 x 18, or 36 x 36. Register mode and bypass mode are supported in both input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Note!

Two macros can form one 36 x 36 multiplier.

Arithmetic Logic Unit

Each DSP macro contains one 54-bit ALU, which can further enhance multipliers' functions. Register mode and bypass mode are supported in both input and output ports. The functions include:

- Addition/subtraction operations of multiplier output data/0, data A, and data B
- Addition/subtraction operations of multiplier output data/0, data B, and carry C
- Addition/subtraction operations of data A, data B, and carry C

2.6.2 DSP Operation Modes

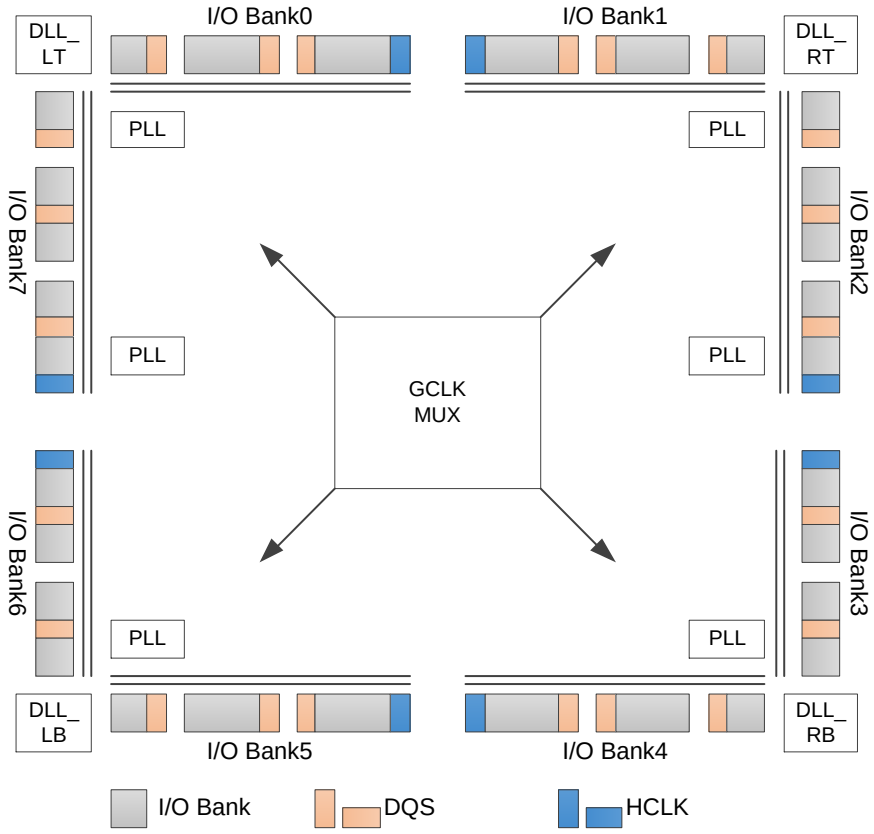
- Multiplier mode
- Multiply accumulator mode
- Multiply-add accumulator mode

For more information on the DSP resources, see *UG287, Gowin Digital Signal Processing (DSP) User Guide*.

2.7 Clocks

The clock resources and wiring are critical for high-performance applications in FPGA. The GW2AR series of FPGA products provide global clocks (GCLKs) which connect to all the registers directly. In addition, high-speed clocks (HCLKs), PLLs, DQSs, etc. are provided.

Figure 2-13 GW2AR Clock Resources



2.7.1 Global Clocks

The Global Clock(GCLK) resources are distributed across multiple quadrants within the GW2AR series of FPGA products (Automotive).Each quadrant provides eight GCLKs. The clock sources of GCLKs include dedicated clock input pins and CRUs, and better clock performance can be achieved by using the dedicated clock input pins.

2.7.2 PLLs

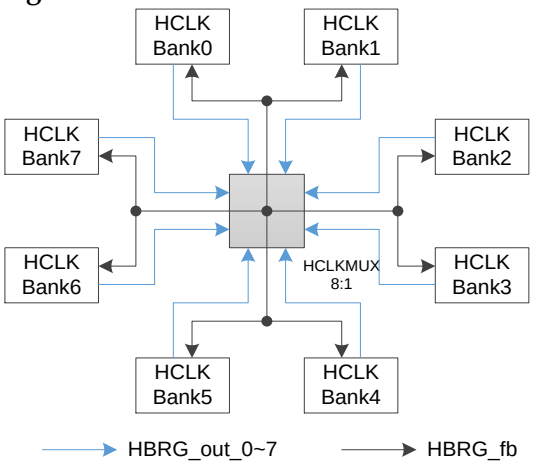
The PLL (Phase-locked Loop) is a feedback control circuit. The frequency and phase of the internal oscillator signal are controlled by the external input reference clock.

PLLs in the GW2AR series of FPGA products can provide synthesizable clock frequencies. Frequency adjustment (multiplication and division), phase adjustment, and duty cycle adjustment can be achieved by configuring the parameters.

2.7.3 High-speed Clocks

The high-speed clocks (HCLKs) are designed to facilitate high-performance I/O data transmission and are specifically tailored for source synchronous data transmission protocols, see Figure 2-14.

Figure 2-14 GW2AR HCLK Distribution



As shown in Figure 2-14, there is an 8:1 HCLKMUX module in the middle of the HCLK. HCLKMUX can send the HCLK signal in any bank to any other bank, which makes the use of HCLK more flexible.

The function modules that are available for the HCLK resources include:

- DHCEN: Dynamic enable modules for the high-speed clocks. Its function is similar to that of DQCE. It is used to turn on/off the high-speed clock signal dynamically.
- CLKDIV/CLKDIV2: Frequency division modules for the high-speed clocks. There is one CLKDIV in each bank. It is used to generate a frequency-divided clock for IO logic with the same phase as the input clock.
- DCS: Dynamic HCLK selectors.
- DLLDLY: Dynamic delay adjustment modules for the clock signals input via the dedicated clock pins.

2.7.4 DDR Memory Interface Clock Management (DQS)

The DQS module of the GW2AR series of FPGA products provides the following features to support the clocking requirements of the DDR memory interface:

- Receives DQS inputs, sorts out waveforms and shifts 1/4 phase
- Provides read/write pointers for the input buffer
- Provides a data valid signal for internal logic
- Provides DDR output clock signals
- Supports DDR3 write voltage control

The DQS module supports multiple modes for different I/O interfaces.

For more information on the GCLKs, HCLKs, and DQSs, see UG286, Gowin Clock User Guide.

2.8 Long Wires

As a supplement to the CRU, the GW2AR series of FPGA products provide another kind of routing resource - the long wire, which can be used for clock, clock enable, set/reset, or other high fan-out signals.

2.9 Global Set/Reset

The GW2AR series of FPGA products offer a dedicated global set/reset (GSR) network that connects directly to the device's internal logic and can be used as asynchronous/synchronous set or asynchronous/synchronous reset, with the registers in the CFUs and I/Os being able to be configured independently.

2.10 Programming & Configuration

The GW2AR series of FPGA products support SRAM configuration, and the configuration data needs to be re-downloaded after each power-up. You can also store the configuration data in an external Flash. In this case, the GW2AR device loads the configuration data from the external Flash to the SRAM after power-up.

In addition to JTAG, the GW2AR series of FPGA products also support Gowin's own GowinCONFIG configuration modes: SSPI, MSPI, SERIAL, and CPU. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

2.11 On-chip Oscillator

The GW2AR series of FPGA products have an embedded programmable on-chip clock oscillator which provides a clock source for the MSPI configuration mode. See Table 2-9 for the output frequencies. The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is used to get the output clock frequency:

f_{out}=250MHz/Param.

Note!

"Param" should be an even number between 2 and 128.

Table 2-9 Output Frequency Options of the On-chip Oscillator

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz

6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note!

- [1] The default frequency is 2.5MHz.
- [2] 125MHz is not available for the MSPI configuration mode.

3 DC and Switching Characteristics

Note!

Please ensure that you use Gowin's devices within the recommended operating conditions and ranges. Data beyond the working conditions and ranges are for reference only. Gowin does not guarantee that all devices will operate normally beyond the operating conditions and ranges.

3.1 Operating Conditions

3.1.1 Absolute Max. Ratings

Table 3-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage	-0.5V	1.1V
V_{CCPLL}	PLL Voltage	-0.5V	1.1V
V_{CCIO}	I/O bank voltage	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
-	I/O voltage applied[1]	-0.5V	3.75V
Storage Temperature	Storage temperature	-65℃	+150℃
Junction Temperature	Junction temperature	-40℃	+125℃

Note!

- [1] Overshoot and undershoot of -2V to (V_{IHMAX} + 2)V are allowed for a duration of <20 ns.

3.1.2 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	Core voltage	0.95V	1.05V
$V_{CCPLLLx}$	Left PLL Voltage	0.95V	1.05V
$V_{CCPLLRx}$	Right PLL Voltage	0.95V	1.05V
V_{CCIOx}	I/O bank voltage	1.14V	3.6V
V_{CCX}	Auxiliary voltage	2.7V	3.6V

T_{JCOM}	Junction temperature for commercial operations	0℃	+85℃
T_{JIND}	Junction temperature for industrial operations	-40℃	+100℃

Note!

- The allowable ripples on V_{CC}, V_{CCIO}, and V_{CCX} are 3%, 5%, and 5% respectively. 1). For devices of which the PLL is powered directly with V_{CC}, the ripple on V_{CC} can affect the jitter characteristics of the PLL output clock; 2). The ripple on V_{CCIO} can eventually be passed on to the output waveform of the IO Buffer.
- For more information on the power supplies, please refer to UG115, GW2AR-18 Pinout.

3.1.3 Power Supply Ramp Rates

Table 3-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
Vcc Ramp	Power supply ramp rates for V_{CC}	0.1mV/μs	-	10mV/μs
V_{CCIO}/Vccx Ramp	Power supply ramp rates for V_{CCIO} and V_{CCX}	0.01mV/μs	-	100mV/μs

Note!

- A monotonic ramp is required for all power supplies.
- All power supplies need to be in the operating range as defined in Table 3-2 before configuration. Power supplies that are not in the operating range need to be adjusted to a faster ramp rate, or you have to delay configuration.

3.1.4 Hot Socketing Specifications

Table 3-4 Hot Socketing Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI,TDO, TMS,TCK	120uA

3.1.5 POR Specifications

Table 3-5 POR Parameters

Name	Description	Name	Min.	Max.
POR Voltage	Power on reset ramp up trip point	VCC	0.7V	0.88V
		VCCX	2.1V	2.6V
		VCCIO	0.85V	0.98V

3.2 ESD performance

Table 3-6 GW2AR ESD - HBM

Device	GW2AR-18
EQ144/EQ144P/EQ144PF	HBM>1,000V
QN88/QN88P/QN88PF	HBM>1,000V
EQ176	HBM>1,000V

Table 3-7 GW2AR ESD - CDM

Device	GW2AR-18

EQ144/EQ144P/EQ144PF	CDM>500V
QN88/QN88P/QN88PF	CDM>500V
EQ176	CDM>500V

3.3 DC Electrical Characteristics

3.3.1 DC Electrical Characteristics over Recommended Operating Conditions

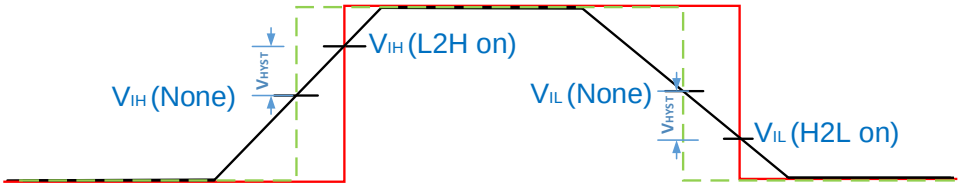
Table 3-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage current	$V_{CCIO}<V_{IN}<V_{IH}$(MAX)	-	-	210μA
		$0V<V_{IN}<V_{CCIO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCIO}$	-30μA	-	-150μA
I_{PD}	I/O Active Pull-down Current	V_{IL}(MAX)$<V_{IN}<V_{CCIO}$	30μA	-	150μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$(MAX)	30μA	-	-
I_{BHHS}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCIO}$	-30μA	-	-
I_{BHLO}	Bus Hold Low Overdrive Current	$0\leq V_{IN}\leq V_{CCIO}$	-	-	150μA
I_{BHHO}	Bus Hold High Overdrive Current	$0\leq V_{IN}\leq V_{CCIO}$	-	-	-150μA
V_{BHT}	Bus Hold Trip Points	-	V_{IL}(MAX)	-	V_{IH}(MIN)
C1	I/O Capacitance	-	-	5pF	8pF
V_{HYST}	Hysteresis for Schmitt Trigger inputs	V_{CCIO}=3.3V, Hysteresis=L2H[1],[2]	-	240mV	-
		V_{CCIO}=2.5V, Hysteresis=L2H	-	140mV	-
		V_{CCIO}=1.8V, Hysteresis=L2H	-	65mV	-
		V_{CCIO}=1.5V, Hysteresis=L2H	-	30mV	-
		V_{CCIO}=3.3V, Hysteresis=H2L[1],[2]	-	200mV	-
		V_{CCIO}=2.5V, Hysteresis=H2L	-	130mV	-
		V_{CCIO}=1.8V, Hysteresis=H2L	-	60mV	-
		V_{CCIO}=1.5V, Hysteresis=H2L	-	40mV	-
		V_{CCIO}=3.3V,Hysteresis=HIGH[1],[2]	-	440mV	-
		V_{CCIO}=2.5V,Hysteresis=HIGH	-	270mV	-
		V_{CCIO}=1.8V,Hysteresis=HIGH	-	125mV	-
		V_{CCIO}=1.5V,Hysteresis=HIGH	-	70mV	-

Note!

- [1] Hysteresis="NONE", "L2H", "H2L", "HIGH" indicates the Hysteresis options that can be set when setting I/O Constraints in the FloorPlanner tool of Gowin EDA, for more details, see SUG935, Gowin Design Physical Constraints User Guide.

- [2] Enabling the L2H (low to high) option means raising V_{IH} by V_{HYST}; enabling the H2L (high to low) option means lowering V_{IL} by V_{HYST}; enabling the HIGH option means enabling both L2H and H2L options, i.e. V_{HYST}(HIGH) = V_{HYST}(L2H) + V_{HYST}(H2L). The diagram is shown below.



3.3.2 Static Current

Table 3-9 Static Current

Name	Description	Device	Typ.
I_{CC}	V_{CC} current (V_{CC}=1V)	GW2AR-18	70mA
I_{CCX}	V_{CCX} current (V_{CCX}=3.3V)	GW2AR-18	15mA
I_{CCIO}	V_{CCIO} current (V_{CCIO}=3.3V)	GW2AR-18	<2mA

Note!

Test conditions: room temperature, speed grade C8/I7.

3.3.3 Recommended I/O Operating Conditions

Table 3-10 Recommended I/O Operating Conditions

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.6	-	-	-
LVCMOS33	3.135	3.3	3.6	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.6	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.6	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.6	-	-	-
LVPECL33E	3.135	3.3	3.6	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-

Name	V_{CCIO} (V) for Output			V_{REF} (V) for Input		
	Min.	Typ.	Max.	Min.	Typ.	Max.
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.6	-	-	-
SSTL33D_II	3.135	3.3	3.6	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

3.3.4 Single-ended I/O DC Characteristics

Table 3-11 Single-ended I/O DC Characteristics

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL}[1] (mA)	I_{OH}[1] (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCIO}	0.65 x V_{CCIO}	3.6V	0.4V	V_{CCIO}-0.4V	2	-2
							4	-4
					0.2V	V_{CCIO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCIO}	0.5 x V_{CCIO}	3.6V	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCIO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCIO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125 V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCIO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Note!

[1] The total DC current limit(sourced and sunk current) of all IOs in the same bank: the total DC current of all IOs in the same bank shall not be greater than n*8mA, where n represents the number of IOs bonded out from a bank.

3.3.5 Differential I/O DC Characteristics

Table 3-12 Differential I/O DC Characteristics

LVDS

Name	Description	Test conditions	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage	-	0	-	2.4	V
V_{CM}	Input Common Mode Voltage	-	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Minimum Input Swing	±100	-	±600	mV
I_{IN}	Input Current	Power On or Power Off	-	-	±10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.6	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T=100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low	-	-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T=100Ω	1.125	1.2	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low	-	-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V outputs short-circuited	-	-	15	mA

3.4 Switching Characteristics

3.4.1 CFU Switching Characteristics

Table 3-13 CFU Timing Parameters

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2AR-18	t_{LUT4_CFU}	LUT4 delay	0.31	0.46	0.39	0.58	ns
	t_{SR_CFU}	Set/Reset to Register output	1.10	1.15	1.37	1.44	ns
	t_{CO_CFU}	Clock to Register output	0.20	0.23	0.25	0.29	ns

3.4.2 BSRAM Switching Characteristics

Table 3-14 BSRAM Timing Parameters

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2AR-18	t_{COAD_BSRAM}	Clock to output from read address/data	2.26	2.26	2.83	2.83	ns

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
	t_{COOR_BSRAM}	Clock to output from output register	0.31	0.31	0.38	0.38	ns

3.4.3 DSP Switching Characteristics

Table 3-15 DSP Timing Parameters

Device	Name	Description	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
GW2AR-18	t_{COIR_DSP}	Clock to output from input register	0.24	0.25	0.30	0.32	ns
	t_{COPR_DSP}	Clock to output from pipeline register	0.07	0.08	0.09	0.10	ns
	t_{COOR_DSP}	Clock to output from output register	0.04	0.04	0.05	0.05	ns

Table 3-16 DSP Max Frequency Specifications

Device	Mode	Max Frequency		Unit
		C8/I7	C7/I6	
GW2AR-18	9 x 9 Multiplier	275	220	MHz
	18 x 18 Multiplier	275	220	MHz
	18 x 18 Multiply-Add/sub	265	211	MHz

3.4.4 Gearbox Switching Characteristics

Table 3-17 Gearbox Timing Parameters

Device	Name	Description	Max.	Unit
GW2AR-18	$FMAX_{IDDR}$	1:2 Gearbox maximum serial input rate	400	Mbps
	$FMAX_{IDES4}$	1:4 Gearbox maximum serial input rate	800	Mbps
	$FMAX_{IDES7}$	1:7 Gearbox maximum serial input rate	1000	Mbps
	$FMAX_{IDESx}$	1:8/1:10 Gearbox maximum serial input rate	1200	Mbps
	$FMAX_{ODDR}$	2:1 Gearbox maximum serial output rate	400	Mbps
	$FMAX_{OSER4}$	4:1 Gearbox maximum serial output rate	800	Mbps
	$FMAX_{OSER7}$	7:1 Gearbox maximum serial output rate	1000	Mbps
	$FMAX_{OSERx}$	8:1/10:1 Gearbox maximum serial output rate	1200	Mbps

3.4.5 Clock and I/O Switching Characteristics

Table 3-18 External Switching Characteristics

Name	Description	Device	C8/I7		C7/I6		Unit
			Min	Max	Min	Max	
Pin-LUT-Pin Delay[1]	Pin(IOxA) to Pin(IOxB) delay	GW2A(2AR)-18	-	3.83	-	4.59	ns
$T_{HCLKdly}$	HCLK tree delay	GW2A(2AR)-18	-	0.82	-	0.98	ns
$T_{GCLKdly}$	GCLK tree delay	GW2A(2AR)-18	-	1.77	-	2.12	ns

Note!

- [1] Test conditions：V_{CCIO}=3.3V, V_{CCX}=3.3V, LVCMOS33, 8mA, 15pF load.

3.4.6 On-chip Oscillator Switching Characteristics

Table 3-19 On-chip Oscillator Parameters

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to +85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

3.4.7 PLL Switching Characteristics

Table 3-20 PLL Timing Parameters

Name	Description	GW2AR-18			Unit
		C9/I8	C8/I7	C7/I6	
F_{INMAX}	Maximum Input Clock Frequency	500	500	400	MHz
F_{INMIN}	Minimum Input Clock Frequency	3	3	3	MHz
F_{PFDMAX}	Maximum Frequency at the Phase Frequency Detector	500	500	400	MHz
F_{PFDMIN}	Minimum Frequency at the Phase Frequency Detector	3	3	3	MHz
$F_{INJITTER}$	Maximum Input Clock Period Jitter	< 20% of clock input period or 1 ns Max			
F_{INDUTY}	Minimum Allowable Input Duty Cycle: 3-49 MHz	25	25	25	%
	Minimum Allowable Input Duty Cycle:	30	30	30	%

Name	Description	GW2AR-18			Unit
		C9/I8	C8/I7	C7/I6	
	50-199 MHz				
	Minimum Allowable Input Duty Cycle: 200-399 MHz	35	35	35	%
F_{VCOMIN}	Minimum PLL VCO Frequency	500	500	400	MHz
F_{VCOMAX}	Maximum PLL VCO Frequency	1250	1250	1000	MHz
$T_{STATPHAOFFSET}$	Static Phase Offset of the PLL Outputs	+/-50	+/-50	+/-50	ps
$T_{JITTER\_CCJ\_HCLK}$[3]	PLL Output cycle-cycle Jitter Thru HCLK≥100MHz	<300	<300	<300	ps
	PLL Output cycle-cycle Jitter Thru HCLK <100MHz	<30	<30	<30	mUI
	PLL Output cycle-cycle Jitter Thru PCLK≥100MHz	<400	<400	<400	ps
	PLL Output cycle-cycle Jitter Thru PCLK<100MHz	<40	<40	<40	mUI
$T_{JITTER\_PJ\_PCLK}$	PLL Output period Jitter Thru HCLK≥ 100MHz	<300	<300	<300	ps
	PLL Output period Jitter Thru HCLK <100MHz	<30	<30	<30	mUI
	PLL Output period Jitter Thru PCLK ≥ 100MHz	<400	<400	<400	ps
	PLL Output period Jitter Thru PCLK <100MHz	<40	<40	<40	mUI
$T_{OUTDUTY}$[1],[4]	PLL Output Clock Duty Cycle Precision	<50	<50	<50	mUI
$T_{LOCKMAX}$	PLL Maximum Lock Time	1	1	1	ms
F_{OUTMAX}	PLL Maximum Output Frequency	625	625	500	MHz
F_{OUTMIN}[2]	PLL Minimum Output Frequency	3.90625	3.90625	3.125	MHz
$T_{EXTFDVAR}$	External Clock Feedback Variation	< 20% of clock input period or 1 ns Max			
$R_{STMINPULSE}$	Minimum Reset Pulse Width	10	10	10	ns

Note!

- [1] These test values are based on integer frequency division.
- [2] In cascade mode, multiple dividers can be connected in series to obtain a lower output frequency.
- [3] The output jitter is related to the input source. These test values are based on the case where a low-jitter crystal oscillator is used as the input source.
- [4] The duty cycle on the IO is also affected by the clock tree.

3.5 Configuration Interface Timing Specification

The GW2AR series of FPGA products support multiple GowinCONFIG modes, including MSPI, SSPI, SERIAL, CPU. For more information, please refer to UG290, Gowin FPGA Products Programming and Configuration User Guide.

4 Ordering Information

4.1 Part Naming

Note!

- For more information about the packages, please refer to 1.2 Product Resources.
- The LittleBee family devices and Arora family devices of the same speed grade have different speeds.
- Both “C” and “I” are used in Gowin’s part name marking for one device. GOWIN devices are screened using industrial standards, so the same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the chip meets speed grade 8 in commercial grade applications, its speed grade will be 7 in industrial grade applications.

Figure 4-1 Part Naming Examples – ES

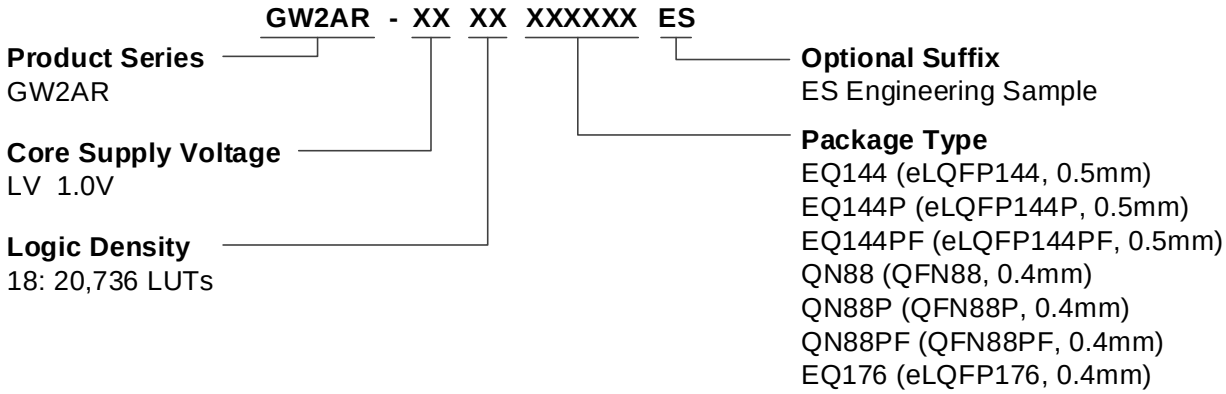
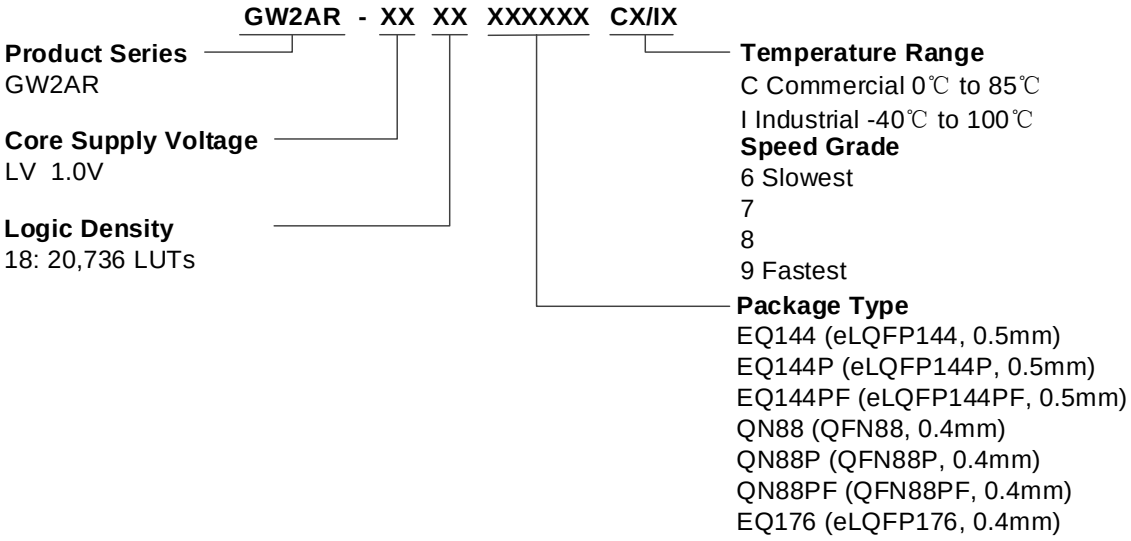


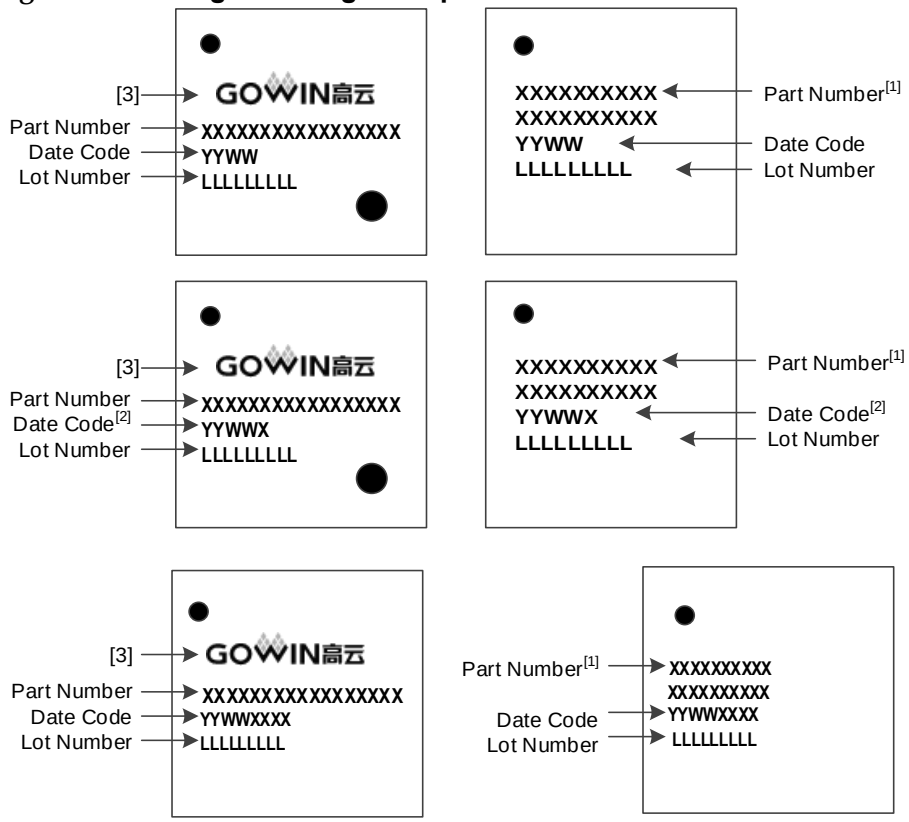
Figure 4-2 Part Naming Examples – Production



4.2 Package Markings

Gowin's devices have markings on the their surfaces, as shown in Figure 4-3.

Figure 4-3 Package Marking Examples



Note!

- [1] The first two lines in the right figure(s) above are both the "Part Number".
- [2] The fifth character of the Date Code denotes the version of the device.

- [3] Whether the package marking bears the Gowin Logo or not depends on the package type, package size, and Part Number length. The above figure are only examples of the package markings.

5 About This Manual

5.1 Purpose

This data sheet provides a comprehensive overview of the GW2AR series of FPGA products, including their features, resources, architecture, AC/DC characteristics, and ordering details.

5.2 Related Documents

The latest documents are available at www.gowinsemi.com.

- DS226, GW2AR series of FPGA Products Data Sheet
- UG290, Gowin FPGA Products Programming and Configuration User Guide
- UG229, GW2AR series of FPGA Products Package and Pinout Manual
- UG115, GW2AR-18 Pinout

5.3 Terminology and Abbreviations

The terminology and abbreviations used in this manual are shown in Table 5-1.

Table 5-1 Terminology and Abbreviations

Terminology and Abbreviations	Full Name
ALU	Arithmetic Logic Unit
BSRAM	Block Static Random Access Memory
CFU	Configurable Function Unit
CLS	Configurable Logic Section
CRU	Configurable Routing Unit
CS	WLCSP(Wafer-Level Chip Scale Package)
DCS	Dynamic Clock Selector
DP	True Dual Port 16K BSRAM

Terminology and Abbreviations	Full Name
DQCE	Dynamic Quadrant Clock Enable
DSP	Digital Signal Processing
EQ	ELQFP(E-pad Low-profile Quad Flat Package)
FPGA	Field Programmable Gate Array
GPIO	Gowin Programable IO
IOB	Input/Output Block
LQ	LQFP(Low-profile Quad Flat Package)
LUT4	4-input Look-up Table
MG	MBGA(Micro Ball Grid Array Package)
PG	PBGA(Plastic Ball Grid Array Package)
PLL	Phase-locked Loop
QN	QFN(Quad Flat No-lead)
REG	Register
SDP	Semi Dual Port 16K BSRAM
SDRAM	Synchronous Dynamic RAM
SIP	System in Package
SP	Single Port 16K BSRAM
SSRAM	Shadow Static Random Access Memory
TDM	Time Division Multiplexing
UG	UBGA(Ultra Ball Grid Array Package)

5.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com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