PART 2

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {c}]
        set_property IOSTANDARD LVCMOS33 [get_ports {c}]
set_property PACKAGE_PIN V16 [get_ports {b}]
        set_property IOSTANDARD LVCMOS33 [get_ports {b}]
set_property PACKAGE_PIN W16 [get_ports {a}]
        set_property IOSTANDARD LVCMOS33 [get_ports {a}]
set_property PACKAGE_PIN W13 [get_ports {e}]
        set_property IOSTANDARD LVCMOS33 [get_ports {e}]

## LEDs
set_property PACKAGE_PIN U16 [get_ports {d0}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d0}]
set_property PACKAGE_PIN E19 [get_ports {d1}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d1}]
set_property PACKAGE_PIN U19 [get_ports {d2}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d2}]
set_property PACKAGE_PIN V19 [get_ports {d3}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d3}]
set_property PACKAGE_PIN W18 [get_ports {d4}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d4}]
set_property PACKAGE_PIN U15 [get_ports {d5}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d5}]
set_property PACKAGE_PIN U14 [get_ports {d6}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d6}]
set_property PACKAGE_PIN V14 [get_ports {d7}]
        set_property IOSTANDARD LVCMOS33 [get_ports {d7}]
```

Inputs(SW[3:0])	Display(an[0]	a	b	c	d	e	f	g
0000	0	0	0	0	0	0	0	1
0001	1	1	0	0	1	1	1	1
0010	2	0	0	1	0	0	1	0
0011	3	0	0	0	0	1	1	0
0100	4	1	0	0	1	1	0	0
0101	5	0	1	0	0	1	0	0
0110	6	0	1	0	0	0	0	0
0111	7	0	0	0	1	1	1	1
1000	8	0	0	0	0	0	0	0
1001	9	0	0	0	0	1	0	0
1010	A	0	0	0	1	0	0	0
1011	b	1	1	0	0	0	0	0
1100	C	0	1	1	0	0	0	1
1101	d	1	0	0	0	0	1	0
1110	E	0	1	1	0	0	0	0
1111	F	0	1	1	1	0	0	0

(a)

zy \ xw	00	01	11	10
00	0	1	0	0
01	1	0	0	0
11	0	1	0	0
10	0	0	1	0

$a = z'yx'w + z'yx'w' + zyx'w + zy'xw$

(b)

zy \ xw	00	01	11	10
00	0	0	0	0
01	0	1	0	1
11	1	0	1	1
10	0	0	1	0

$b = zyw' + zxw + yxw' + z'yx'w$

(c)

zy \ xw	00	01	11	10
00	0	0	0	1
01	0	0	0	0
11	1	0	1	1
10	0	0	0	0

$c = zyx' + zyw' + z'y'xw'$

(d)

zy \ xw	00	01	11	10
00	0	1	0	0
01	1	0	1	0
11	0	0	1	0
10	0	0	0	1

$d = yxw + zy'xw' + z'yx'w' + z'y'x'w$

(e)

	00	01	11	10
00	0	1	1	0
01	1	1	1	0
11	0	0	0	0
10	0	1	0	0

$e = z'w + z'yx' + y'x'w$

(f)

	00	01	11	10
00	0	1	1	1
01	0	0	1	0
11	0	1	0	0
10	0	0	0	0

$f = z'y'x + z'y'w + z'xw + zyx'w$

(g)

	00	01	11	10
00	1	1	0	0
01	0	0	1	0
11	1	0	0	0
10	0	0	0	0

$g = z'y'x' + zyx'w' + z'yxw$

PART 3

Structural Code

```
`timescale 1ns / 1ps
module structural_SW(
  input [3:0] sw,
  output [6:0] seg,
  output [3:0] an
  );

  assign an[3:0] = 4'b1110;

  //a
  assign seg [0] = (~sw[3] & ~sw[2] & ~sw[1] & sw[0]) | (~sw[3] & sw[2] & ~sw[1] & ~sw[0]) |
                   (sw[3] & sw[2] & ~sw[1] & sw[0]) | (sw[3] & ~sw[2] & sw[1] & sw[0]);
  //b
  assign seg [1] = (sw[3] & sw[2] & ~sw[0]) | (sw[3] & sw[1] & sw[0]) | (sw[2] & sw[1] & ~sw[0]) |
                   (~sw[3] & sw[2] & ~sw[1] & sw[0]);
  //c
  assign seg [2] = (sw[3] & sw[2] & sw[1]) | (sw[3] & sw[2] & ~sw[0]) | (~sw[3] & ~sw[2] & sw[1] &
~sw[0]);

  //d
  assign seg [3] = (sw[2] & sw[1] & sw[0]) | (sw[3] & ~sw[2] & sw[1] & ~sw[0]) | (~sw[3] & sw[2] &
~sw[1] & ~sw[0]) |
                   (~sw[3] & ~sw[2] & ~sw[1] & sw[0]);
  //e
  assign seg [4] = (~sw[3] & sw[0]) | (~sw[3] & sw[2] & ~sw[1]) | (~sw[2] & ~sw[1] & sw[0]);

  //f
```

```
  assign seg [5] = (~sw[3] & ~sw[2] & sw[1]) | (~sw[3] & ~sw[2] & sw[0]) | (~sw[3] & sw[1] & sw[0]) | (sw[3] & sw[2] & ~sw[1] & sw[0]);


  //g
  assign seg [6] = (~sw[3] & ~sw[2] & ~sw[1]) | (sw[3] & sw[2] & ~sw[1] & ~sw[0]) | (~sw[3] & sw[2] & sw[1] & sw[0]);


endmodule
```

Testbunch

```
`timescale 1ns / 1ps
module tb_structural_SW;
   reg [3:0] sw;
   wire [6:0] seg;
   wire [3:0] an;

   structural_SW uut (
         .sw(sw),
         .seg(seg),
         .an(an)
   );

   initial begin

   sw[3] = 0;
   sw[2] = 0;
   sw[1] = 0;
   sw[0] = 0;

   #50;
```

```
// case 1
sw[3] = 0;
sw[2] = 0;
sw[1] = 0;
sw[0] = 0;

#50;

//case 2
sw[3] = 0;
sw[2] = 0;
sw[1] = 0;
sw[0] = 1;

#50;

//case3
sw[3] = 0;
sw[2] = 0;
sw[1] = 1;
sw[0] = 0;

#50;

//case4
sw[3] = 0;
sw[2] = 0;
sw[1] = 1;
```

```
sw[0] = 1;

#50;

//case5
sw[3] = 0;
sw[2] = 1;
sw[1] = 0;
sw[0] = 0;

#50;

//case6
sw[3] = 0;
sw[2] = 1;
sw[1] = 0;
sw[0] = 1;

#50;

//case 7
sw[3] = 0;
sw[2] = 1;
sw[1] = 1;
sw[0] = 0;

#50;

//case8
```

```
sw[3] = 0;
sw[2] = 1;
sw[1] = 1;
sw[0] = 1;

#50;

//case 9
sw[3] = 1;
sw[2] = 0;
sw[1] = 0;
sw[0] = 0;


#50;

//case 10
sw[3] = 1;
sw[2] = 0;
sw[1] = 0;
sw[0] = 1;

#50;

//case 11
sw[3] = 1;
sw[2] = 0;
sw[1] = 1;
sw[0] = 0;
```

```
#50;

//case 12
sw[3] = 1;
sw[2] = 0;
sw[1] = 1;
sw[0] = 1;

#50;

//case 13
sw[3] = 1;
sw[2] = 1;
sw[1] = 0;
sw[0] = 0;

#50;

//case 14
sw[3] = 1;
sw[2] = 1;
sw[1] = 0;
sw[0] = 1;

#50;

//case 15
sw[3] = 1;
```

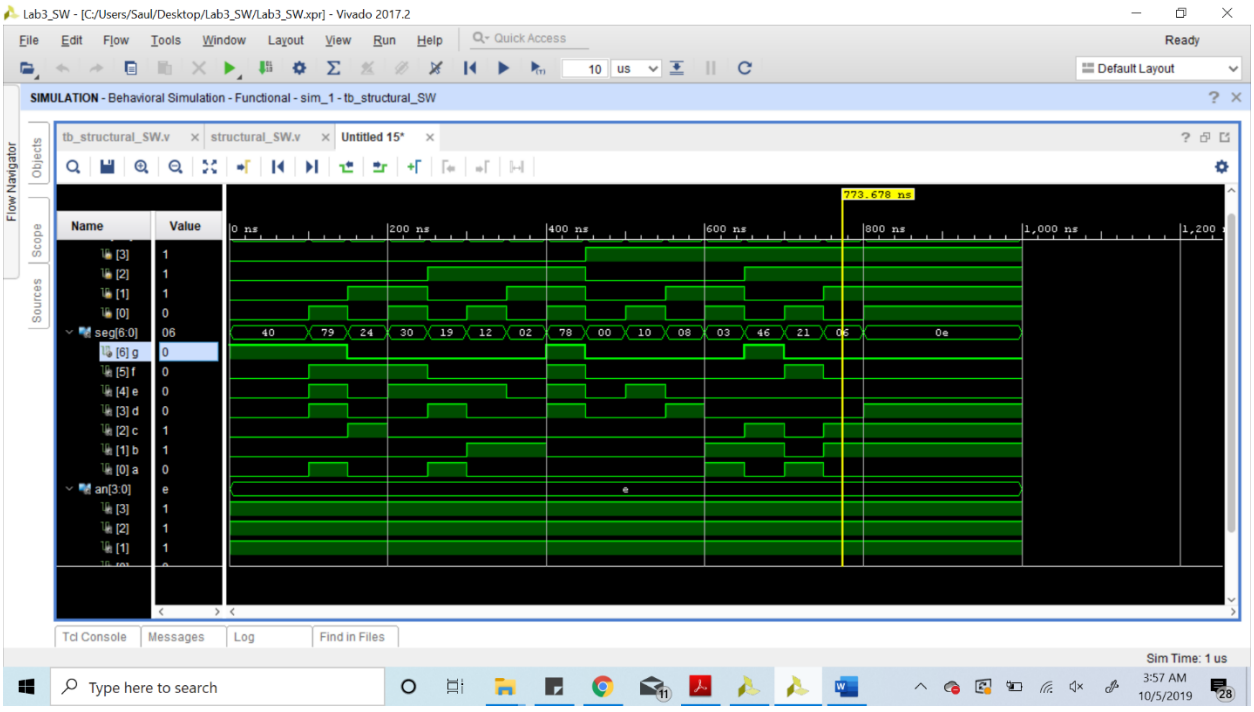
```
    sw[2] = 1;
    sw[1] = 1;
    sw[0] = 0;

    #50;

    //case 16
    sw[3] = 1;
    sw[2] = 1;
    sw[1] = 1;
    sw[0] = 1;

    end

endmodule
```



Constraints

```
## Switches
set_property PACKAGE_PIN V17 [get_ports {sw[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[0]}]
set_property PACKAGE_PIN V16 [get_ports {sw[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[1]}]
set_property PACKAGE_PIN W16 [get_ports {sw[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[2]}]
set_property PACKAGE_PIN W17 [get_ports {sw[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {sw[3]}]


##7 segment display
set_property PACKAGE_PIN W7 [get_ports {seg[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[0]}]
set_property PACKAGE_PIN W6 [get_ports {seg[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[1]}]
set_property PACKAGE_PIN U8 [get_ports {seg[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[2]}]
set_property PACKAGE_PIN V8 [get_ports {seg[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[3]}]
set_property PACKAGE_PIN U5 [get_ports {seg[4]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[4]}]
set_property PACKAGE_PIN V5 [get_ports {seg[5]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[5]}]
set_property PACKAGE_PIN U7 [get_ports {seg[6]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {seg[6]}]
```

```
set_property PACKAGE_PIN U2 [get_ports {an[0]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[0]}]
set_property PACKAGE_PIN U4 [get_ports {an[1]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[1]}]
set_property PACKAGE_PIN V4 [get_ports {an[2]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[2]}]
set_property PACKAGE_PIN W4 [get_ports {an[3]}]
        set_property IOSTANDARD LVCMOS33 [get_ports {an[3]}]
```