Lab 08- ALU

Group Project Members:
Eshetu Wekjira
William Hemric
Matthew Burns
Rashaad Jones
Mason Jordan

Task 1: 1-bit ALU

Depending on a given task1, we used three inputs and three select lines, a total of six

inputs A, B, C, F0, F1, F3, and the two outputs Cout and Q. to implement 1-bit ALU; we used

three logic gets such as and gate, passthrough and not gate and three different multiplexers two

var multiplexer and one variable multiplexer as well as arithmetic logic of addition and

subtraction. We check that our work depends on the given tables of Task1. For example, if we

don't select F1, F2, and F0, our circuit adds the inputs A and B, as shown in **Figure 2.** In the
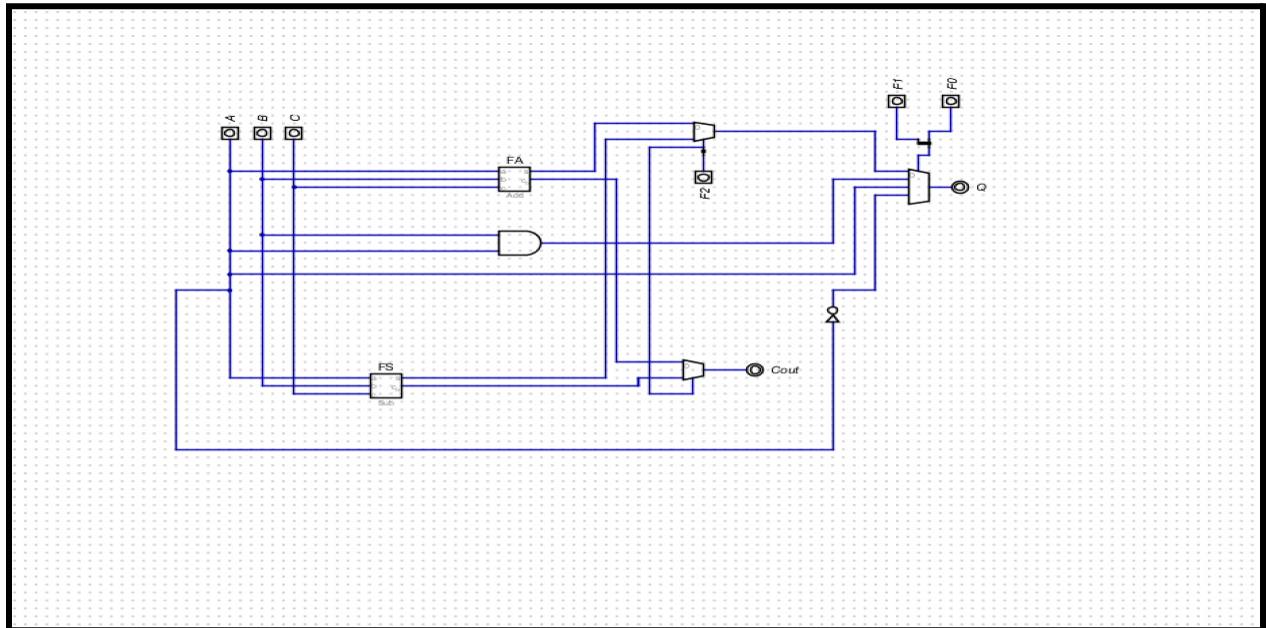
same way, we checked for all tests.

Figure 1: schematic of three select lines for ALU
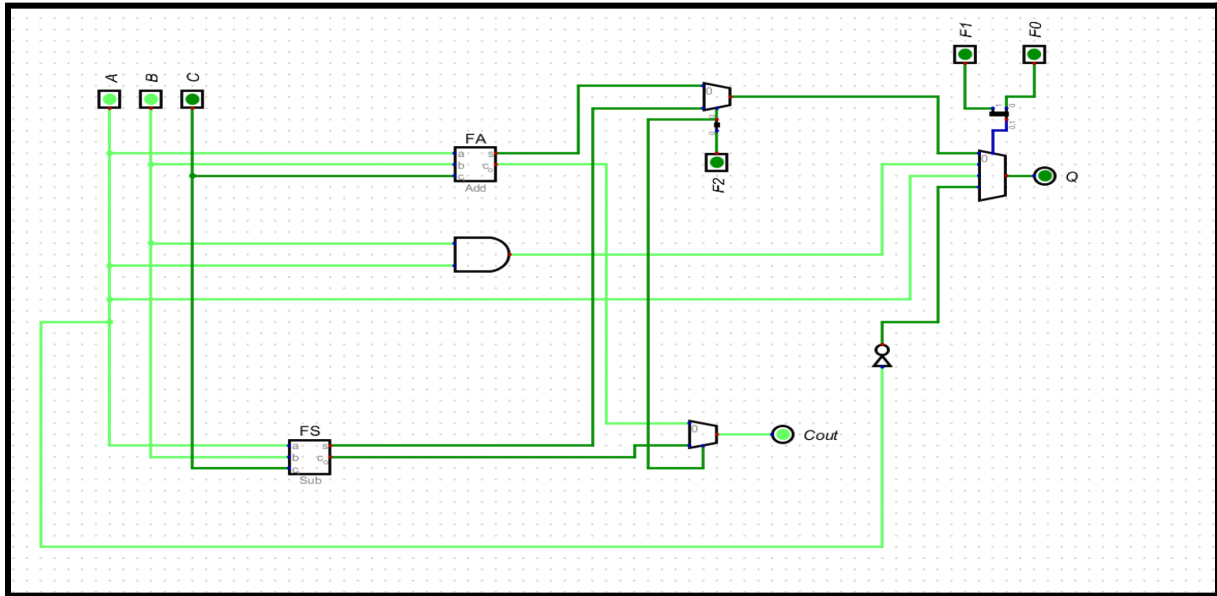
Test case for Addition

Figure 2: schematic for addition test.
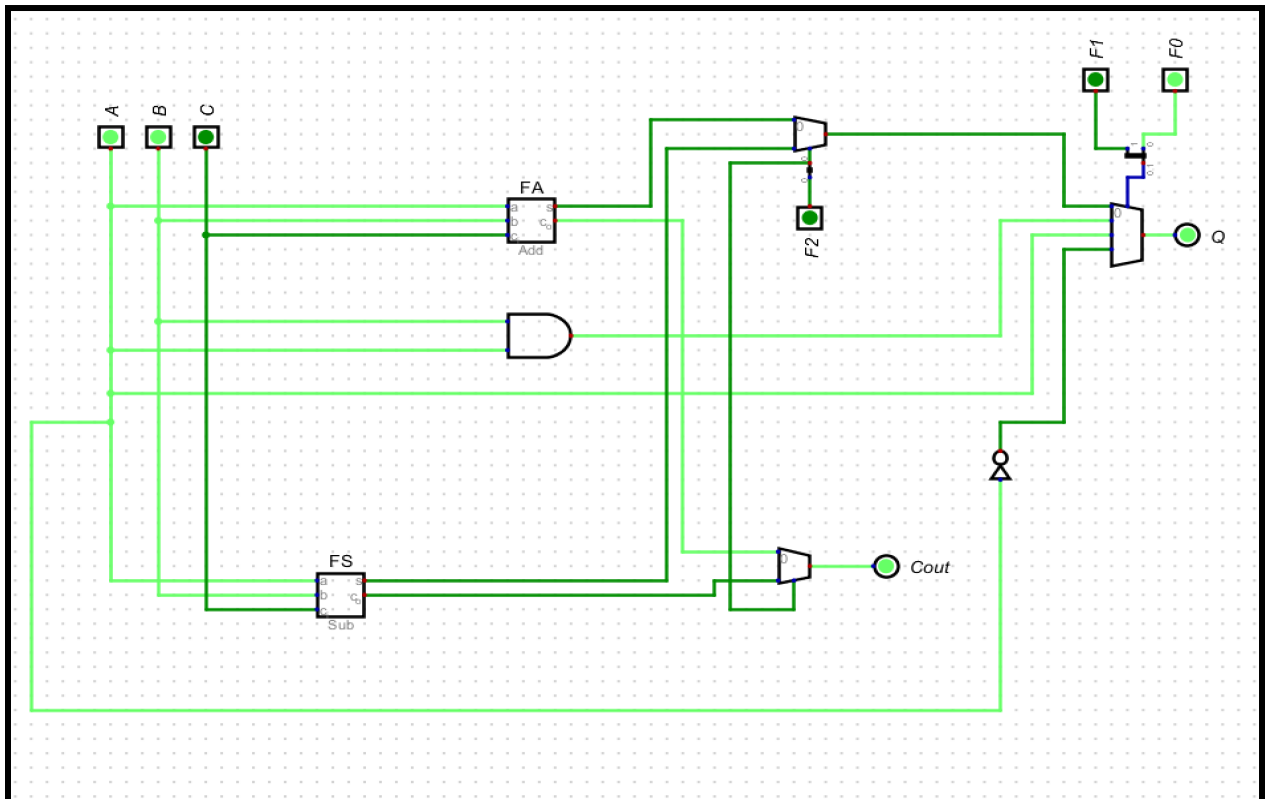
Test case for Bitwise AND

Figure 3: schematic test for Bitwise AND

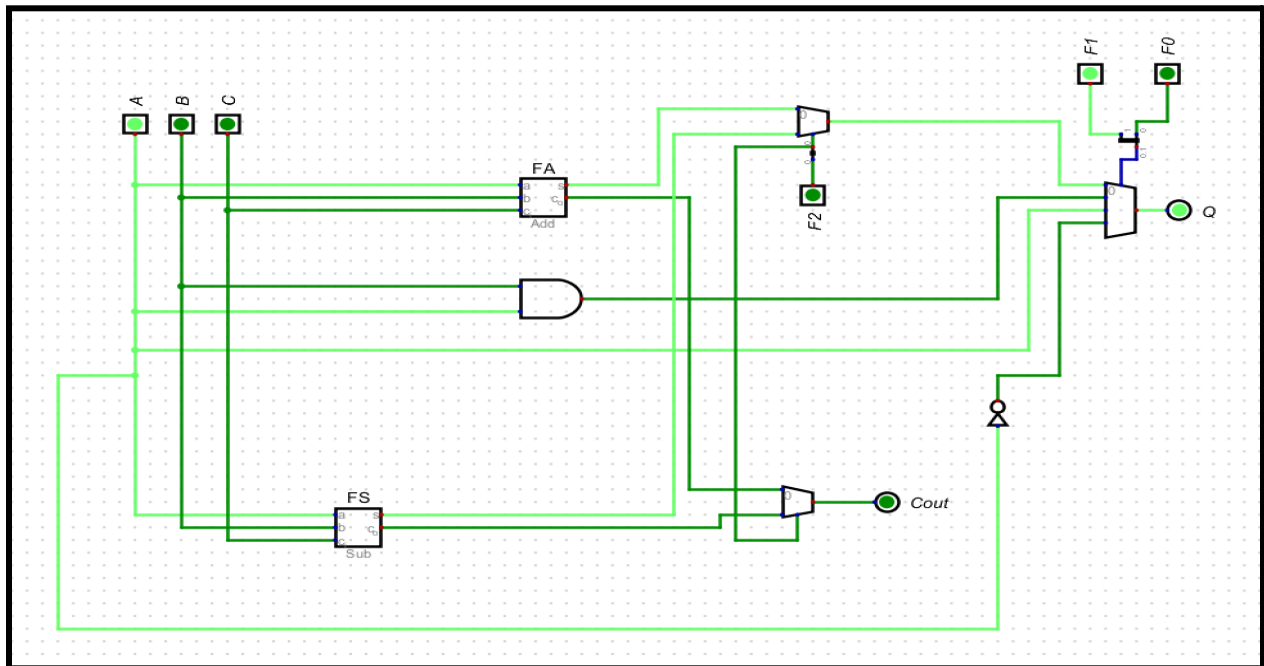**Test case for Passthrough**

Figure 4: schematic test for passthrough.
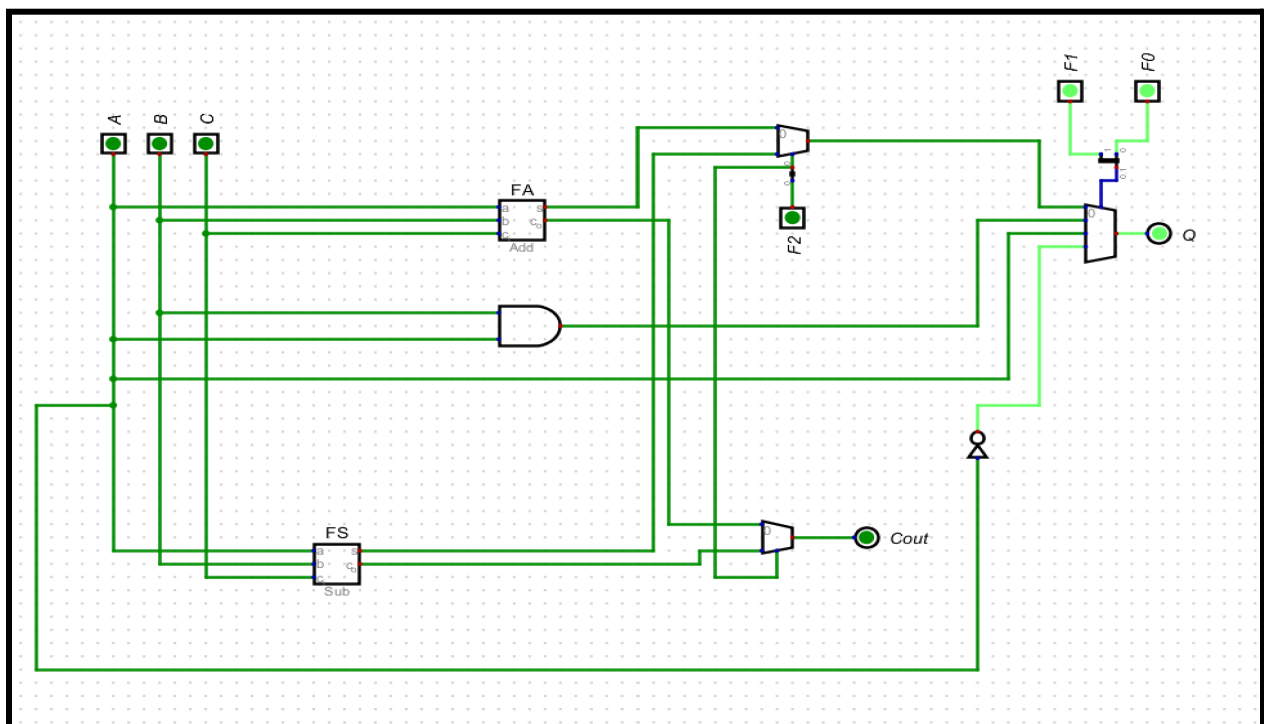
Test case for Bitwise NOT

Figure 5: schematic test case for Bitwise Not.
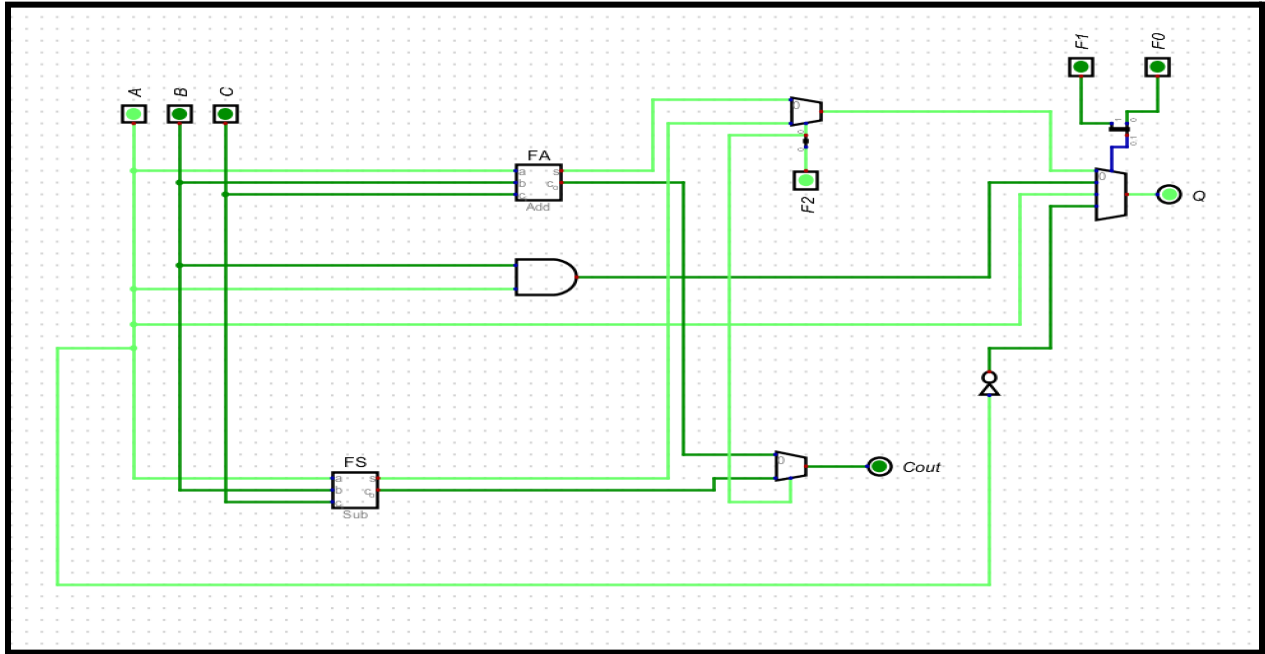
Test case for Subtraction
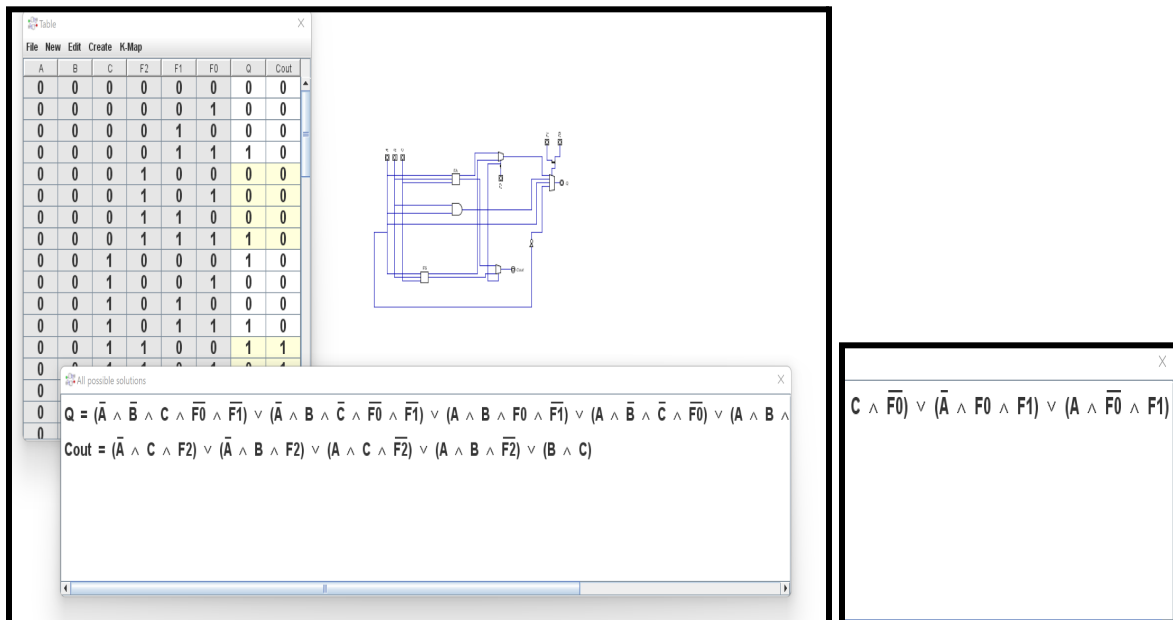

Figure 6: schematic test case for Subtraction.

Table Analysis

Figure 7: tables and equations for the ALU