SY303 Lab 3 **Sequential Logic**

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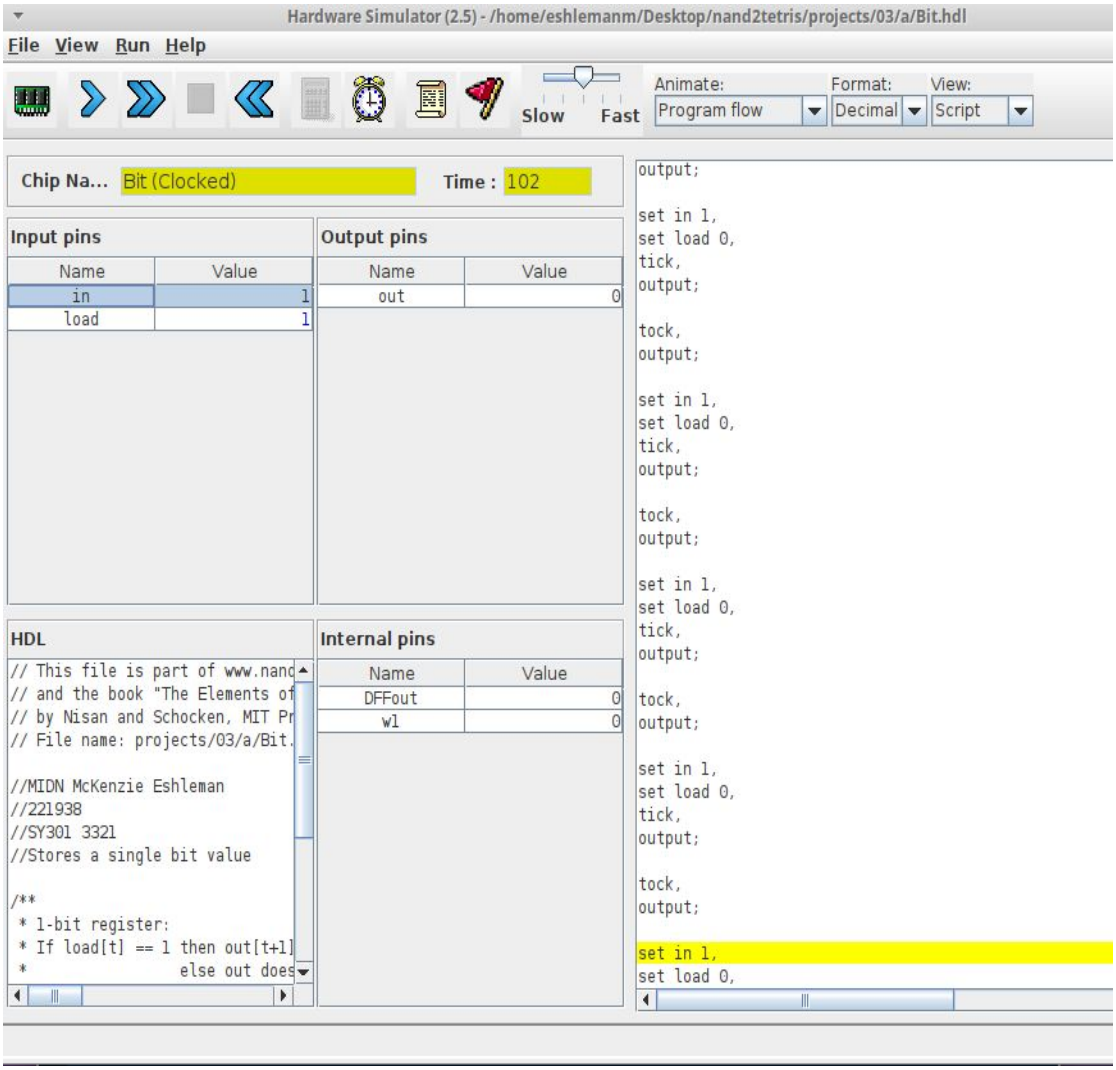
Partner(s):

Section: 3321

Objective: In this lab, you will build on experience gained with the last project and build components capable of maintaining state. These parts will be built using HDL, documentation using Gate Diagrams and commented code will be required.

1) **Pre-Lab: Half Adder**
   a. Screenshot of your **`Bit`** Successfully Completed test in the Hardware Simulator. This chip has already been demonstrated for you. (5 pts)



   b. Describe in detail your understanding of the implementation of the Bit as shown in Figure 3.1. Your discussion should include the rationale for the two internal

elements and a full explanation of the Function as described in an If statement below the diagram. (10 pts)

The Bit chip allows you to store a single bit of information and stores it until it is used by the DFF chip. The Mux Chip uses the selector to take the two inputs and has a single output. The DFF chip keeps the input value from passing until the clock signal goes high.

2) Part: Register

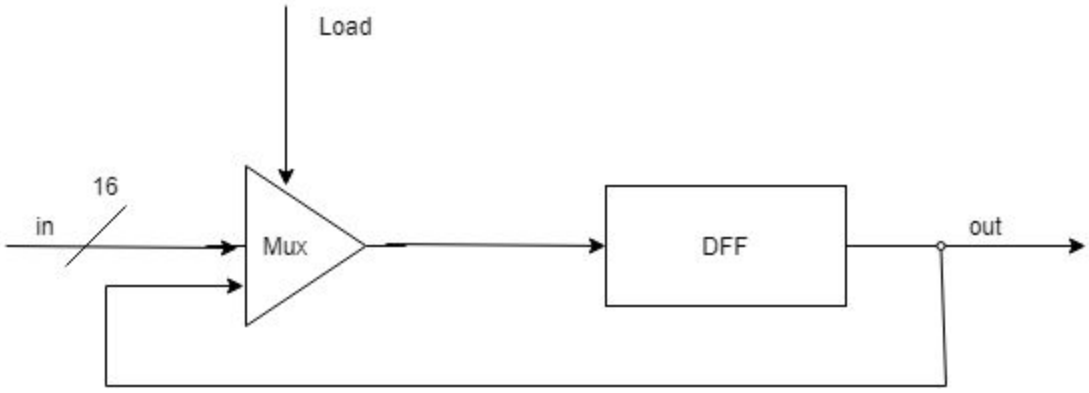
Purpose: The Register, like the Bit, allows you to store and later retrieve data. This is critical for being able to store variables in your program, but also to be able to store files on your hard drive. The Register is much more useful than a Bit, as it combines 16 Bits to store values from 0-65,535 (2^{16}-1) whereas the single Bit can only store values from 0-1. The majority of operations performed by a CPU involve input data retrieved from registers and output data being stored to registers.

Gate Diagram (Insert Drawing or Use Word Art):

The Register is composed of 16 Bit chips. You should think of this much like your Not16 implementation; each input bit should connect to one Bit chip which sends its result to an output bit. Think about the load bit for each of these Bit gates, should they be different or the same (Make your answer bold), and why? (5 pts)

Same / Different

Now draw the Gate diagram for the Register. Remember that if there is a pattern in the implementation, you can use ellipses to clarify the connection between the first couple of iterations and the last couple. Remember to FULLY label all internal and external signals which will be used for the HDL code. (10 pts)

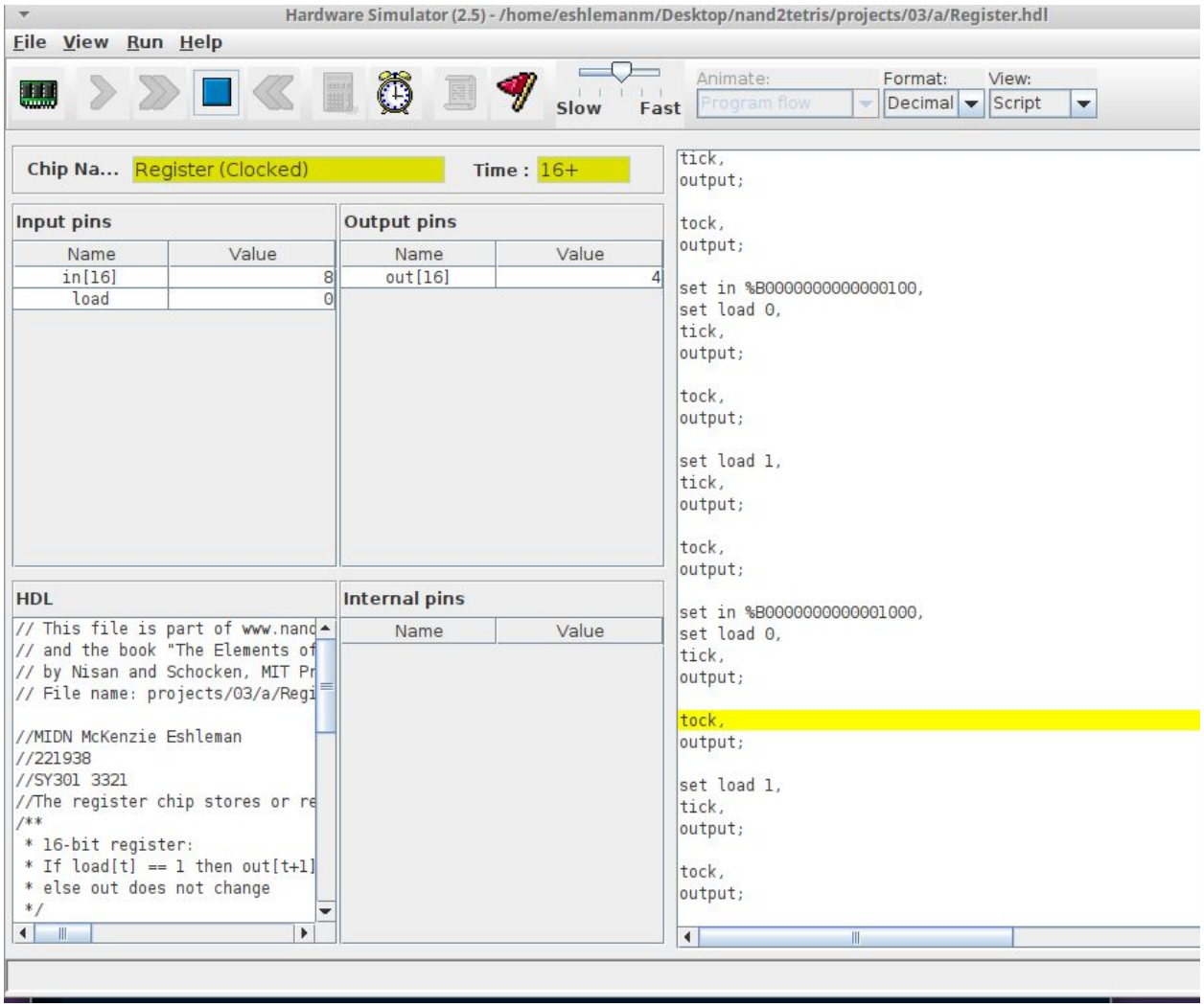


HDL (Screenshot of VM or Raw Text):

Enter your HDL below that describes your gate diagram above. Remember, there will be ONE line of HDL code for each gate in your diagram! (10 pts)

```
// Name: Jack Smith
//  Alpha: XXXXXX
// Section: YYYY
// Description :  The register chip stores or remembers a value over time.

PARTS:
        // YOUR CODE BELOW
//Using the bit function for 16 bits of information
   Bit(in=in[0], load=load, out=out[0]);
   Bit(in=in[1], load=load, out=out[1]);
   Bit(in=in[2], load=load, out=out[2]);
   Bit(in=in[3], load=load, out=out[3]);
   Bit(in=in[4], load=load, out=out[4]);
   Bit(in=in[5], load=load, out=out[5]);
   Bit(in=in[6], load=load, out=out[6]);
   Bit(in=in[7], load=load, out=out[7]);
   Bit(in=in[8], load=load, out=out[8]);
   Bit(in=in[9], load=load, out=out[9]);
   Bit(in=in[10], load=load, out=out[10]);
   Bit(in=in[11], load=load, out=out[11]);
   Bit(in=in[12], load=load, out=out[12]);
   Bit(in=in[13], load=load, out=out[13]);
   Bit(in=in[14], load=load, out=out[14]);
   Bit(in=in[15], load=load, out=out[15]);
}
```

Test in HW Simulator (Screenshot of VM): (5 pts)



Additional Screenshots (as needed):

3) Part: RAM8

Purpose: Describe the function and purpose of this chip in your own words. How does it extend the capability of a single Register in a way that's more useful to a real-world computer system that handles large quantities of data? (5 pts) The RAM Chip can read and write operations, there is no specific order in which the bits can be accessed.

Gate Diagram (Insert Drawing or Use Word Art): You should go straight into conceptualizing your gate diagram now. A RAM8 is made of 8 Register chips, each Register is capable of holding a value (like a variable) that can be used throughout a program. Think about the load bit for each of these Register gates, should they be different or the same (Make your answer bold), and why? Thoughtfully compare this with your answer to the same question in Part 2. (5 pts)

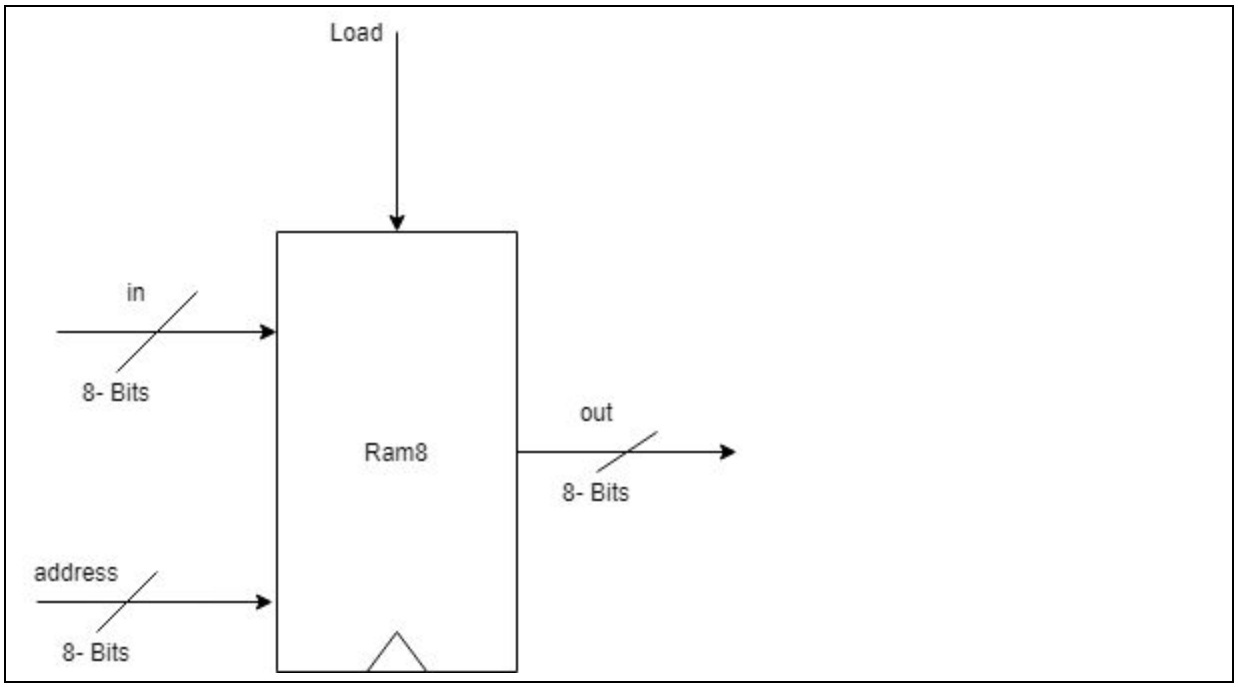
Same / Different **The Ram8 logic gate is very similar to the Register gate except it uses 8 bits of information instead.**

As you attempt to conceptualize the Gate Diagram for a RAM8, consider these questions.

a) What chip has been designed to allow you to write a single input to one of eight possible locations? (3 pts) **We use the Mux8Way16 to take 8 bits of inputs and puts them into specific locations.**

b) What chip has been designed to allow you to read output from eight different locations and select just one of them? (2 pts) **The DMux8Way16 is used to read outputs from 8 different bits and selects one og them.**

Diagram: (10 pts)

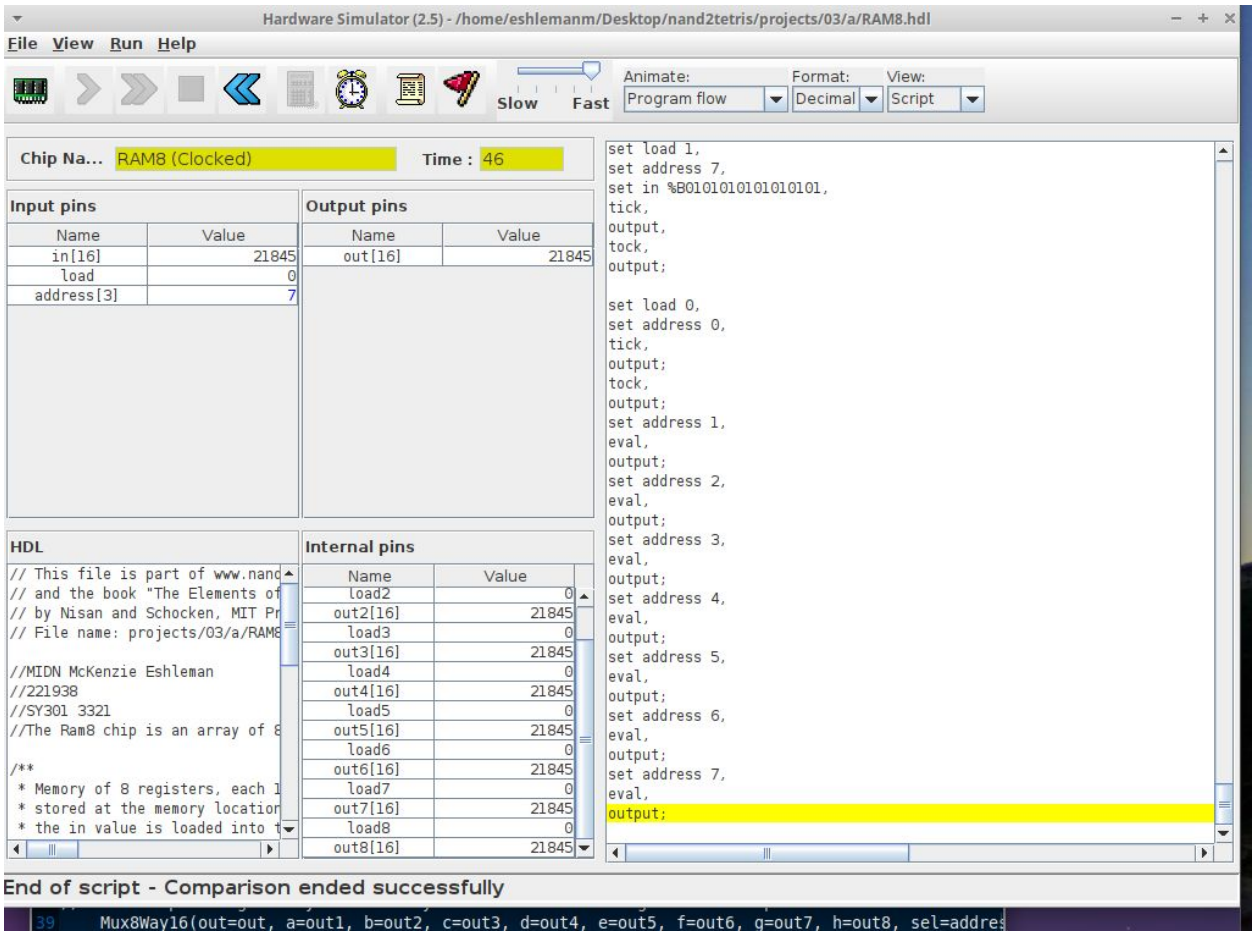


HDL (Screenshot of VM or Raw Text): Enter your HDL below that describes your gate diagram above. (5 pts)

```
// Name: Jack Smith
//  Alpha: XXXXXX
// Section: YYYY
// Description :  The Ram8 chip is an array of 8 bit registers, equipped with direct access circuitry.

PARTS:
        // YOUR CODE BELOW
//Consist of of eight 16 bit registers
//each input is connected to the Rams input
   Register(in=in, load=load1, out=out1);
   Register(in=in, load=load2, out=out2);
   Register(in=in, load=load3, out=out3);
   Register(in=in, load=load4, out=out4);
   Register(in=in, load=load5, out=out5);
```

```
   Register(in=in, load=load6, out=out6);
   Register(in=in, load=load7, out=out7);
   Register(in=in, load=load8, out=out8);

//uses a DMux8 to send load to the appropriate register
   DMux8Way(in=load, a=load1, b=load2, c=load3, d=load4, e=load5, f=load6, g=load7,
h=load8, sel=address);

//Final output is given by the Mux8Way16 to select which register to output
   Mux8Way16(out=out, a=out1, b=out2, c=out3, d=out4, e=out5, f=out6, g=out7, h=out8,
sel=address);
}
```

Test in HW Simulator (Screenshot of VM): (5 pts)



Additional Screenshots (as needed):

4) **The elements being created in this project all incorporate a clock signal to control when new outputs are determined. If a design contains multiple sequential elements, would they share the same clock source or would each have its own independent clock? Why?** (10 pts)

   If a design contained multiple sequential elements, they would share the same clock source. This is because the clock signal is simultaneously broadcasted to every sequential chip throughout the computer platform.

5) **You designed an 8 element RAM in this lab. Explain what is meant by the term Random Access Memory. Compare this to another method of storing and accessing data (for example, a linked list).** (10 pts)

   Random Access Memory is the main memory and can read or write memory. The data that is used during the program is stored in memory. RAM is a primary memory and loses the data once it is powered off. An example of storing and accessing data is through an array list, an array list is a good option for storing data. The ArrayList class can act like a list because that's the implementation for it.