# System-Level Implementation and Evaluation of a Cryogenic CMOS Current Comparator for Spin Qubit Readout

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***Abstract*—Quantum computing requires precise and high-speed readout of qubit states, particularly in silicon spin qubit systems that operate at cryogenic temperatures. In this work, we present a system-level implementation and simulation of a cryogenic CMOS current comparator, originally proposed for on-chip spin qubit readout. The architecture leverages a current integrator and correlation double sampling (CDS) circuit to achieve improved resolution and significantly reduced readout time compared to conventional techniques. Through detailed simulation and analysis, we validate its effectiveness, estimate on-chip capacitor area, and contextualize the benefits through comparative metrics and figures of merit. This paper provides not only a technical walkthrough of the design and its phases of operation but also explores the motivations and challenges addressed by this architecture.**

## I. Introduction

With the promise of solving problems beyond the reach of classical computers, quantum computing has generated significant interest across scientific and industrial communities. At the heart of quantum processors lie quantum bits (qubits), whose quantum states must be read with high accuracy and minimal disturbance.

Among various physical implementations of qubits, silicon-based spin qubits are attractive due to their compatibility with standard CMOS processes. However, their extremely weak signal levels and operation at cryogenic temperatures introduce considerable challenges for readout circuits. Traditional techniques—such as using external amperemeters connected via long cryogenic cables—suffer from parasitic capacitance and thermal loading, leading to readout delays in the millisecond range.

Gate reflectometry, another popular method, employs resonators to detect state transitions by monitoring amplitude and phase shifts of reflected signals. While it allows relatively faster readout, it comes with trade-offs such as increased power consumption, large inductor areas, and additional complexity in RF design and impedance matching. Additionally, high-frequency analog signal processing chains become increasingly error-prone and difficult to manage at deep cryogenic temperatures.

This paper focuses on replicating and analyzing a cryogenic CMOS current comparator originally developed by Fuketa et al. The system is based on a current integrator and a CDS (Correlation Double Sampling) stage that together enable fast, low-noise readout of qubit states entirely on-chip. We elaborate on the system's operation phases, discuss why each component is necessary, and provide insights from simulations performed in Verilog-A.

## II. Background and Design Motivation

### A. History and Significance of CDS

The technique of Correlated Double Sampling (CDS) has its roots in the world of image sensing. It was first introduced in the 1960s to combat low-frequency noise and fixed pattern offset in CCD (Charge-Coupled Device) image sensors. Specifically, Sangster and Shoulders proposed this method to eliminate flicker noise and DC offsets that degrade signal fidelity.

In the context of analog front-ends, CDS is vital when dealing with signals that have small amplitudes and are prone to slow noise sources like flicker (1/f) noise or op-amp offset. It involves sampling the system output during a "reset" condition and again during "signal acquisition," and subtracting the two to isolate the real signal from noise.

In modern cryogenic circuits, where thermal noise is significantly reduced due to low temperature operation, flicker noise becomes more pronounced relative to other noise components. CDS becomes particularly valuable in these settings, as it effectively suppresses such low-frequency noise without requiring complex filtering or calibration.

### B. Significance of an Integrator

Current levels from qubit-related sensors, such as SETs (Single Electron Transistors) or QPCs (Quantum Point Contacts), are typically in the picoampere range. These tiny currents are challenging to digitize directly due to:

- Low SNR (Signal-to-Noise Ratio),
- Susceptibility to offset and noise,
- Limited resolution in ADCs.

A current integrator solves this by accumulating charge on a capacitor over a fixed time. The resulting voltage across the capacitor provides a larger and more stable signal that can be amplified and digitized reliably. This approach transforms a time-varying low-level current into a measurable voltage swing, trading off integration time for resolution.

Additionally, the integrator functions as a low-pass filter, naturally reducing the impact of high-frequency noise while retaining the DC and low-frequency signal components associated with qubit transitions. It also allows compact implementation and tunability via the integration time constant and capacitor size.

## III. System-Level Architecture

### A. High-Level Overview

The cryogenic current comparator is composed of the following stages:

a) **Current Integrator:** Accumulates input current over time on a feedback capacitor using an operational amplifier, converting the current into a voltage linearly over the integration period.
b) **CDS Circuit:** Subtracts reset and signal phases to cancel low-frequency noise and offset.
c) **Amplifier:** Increases voltage swing from the integrator to a level suitable for digitization.
d) **Clocked Comparator:** Outputs a digital level based on whether the amplified signal exceeds a reference threshold.

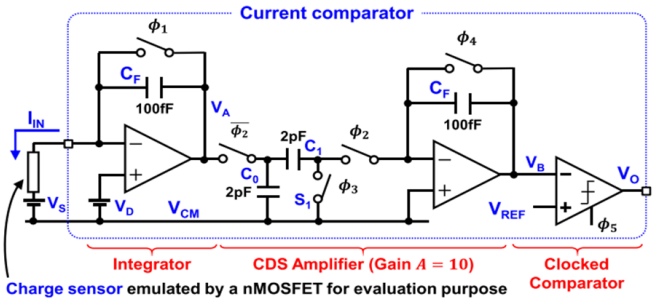


Fig. 1. System Block Diagram

### B. Detailed Operation Phases

Understanding the operation of this architecture requires breaking it down into its sequential phases, synchronized by clock signals.

*1) Reset:* Initially, the system enters a reset phase where the operational amplifier and feedback capacitor in the integrator are cleared. This ensures there is no residual voltage or charge that could affect the measurement. The switch connected across the feedback capacitor is closed, effectively shorting the terminals and resetting the integrator output to a baseline.

*2) Integration:* Once reset, the circuit allows the sensing current to flow into the integrator. Since the input current corresponds to the spin state of a qubit (either spin-up or spin-down), the integrator charges the capacitor accordingly. The voltage across the capacitor grows linearly with time and is directly proportional to the current. This integration is carried out for a carefully timed window, usually on the order of 10 µs, to allow sufficient accumulation for distinction.

*3) CDS Sampling:* In this stage, the CDS circuit samples the voltage from both reset and integration phases. By computing the difference between the two, common-mode offsets and flicker noise are cancelled out. The sampling involves using sample-and-hold circuits, and subtraction is typically done using switched capacitor circuits. This significantly enhances the resolution and repeatability of the measurement, especially important in cryogenic environments where offset voltages can drift with temperature variations.

*4) Amplification:* The differential signal is typically small (in the tens of millivolts) and needs to be amplified before it can be compared with a threshold. A low-noise amplifier provides the required gain (e.g., gain = 10), ensuring the signal is within the comparator's operating range. The amplifier must have low input-referred noise and minimal offset drift to avoid degrading the performance achieved by the integrator-CDS chain.

*5) Comparison:* The amplified signal is finally compared with a reference voltage $V_{REF}$. If the signal exceeds $V_{REF}$, the comparator outputs a logical HIGH, indicating one spin state (say spin-down). Otherwise, it outputs a logical LOW (spin-up). This digital output can then be fed into further digital control or error-correction logic in the quantum system.

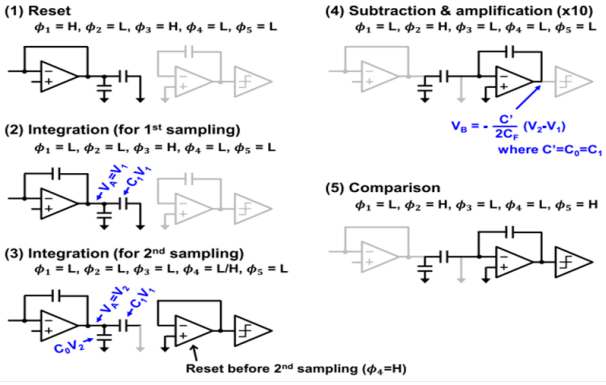


Fig. 2. . The operation of the current comparator is divided into five steps (1)-(5).

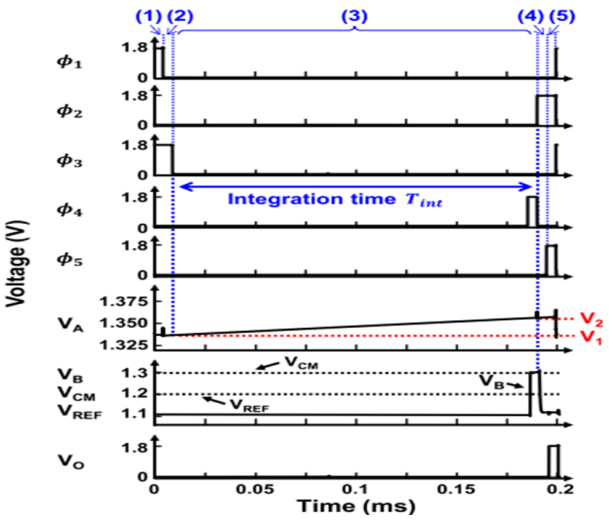


Fig. 3. Timing Diagram of current comparator

## IV. Simulation and Observations

### A. Setup

We modeled the entire system in Verilog-A and simulated it using standard behavioral models. The input current was varied between 25 pA to 50 pA to simulate two qubit states. The system was configured with a 100 fF feedback capacitor, a gain of 10, and a 1.8 V supply.

All stages, including integrator, CDS, amplifier, and comparator, were implemented in a modular manner to validate their standalone and chained operation.

### B. Transient Response

The transient plots showed distinct voltage levels for different current inputs. After amplification, these were easily distinguishable by the comparator. Simulation confirmed that the system can reliably convert current differences of as little as 25–50 pA into measurable digital outputs.

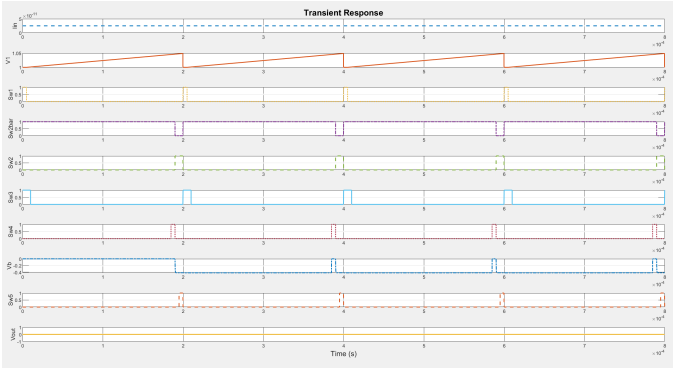


Fig. 4. Transient Response for input current of 25 pA

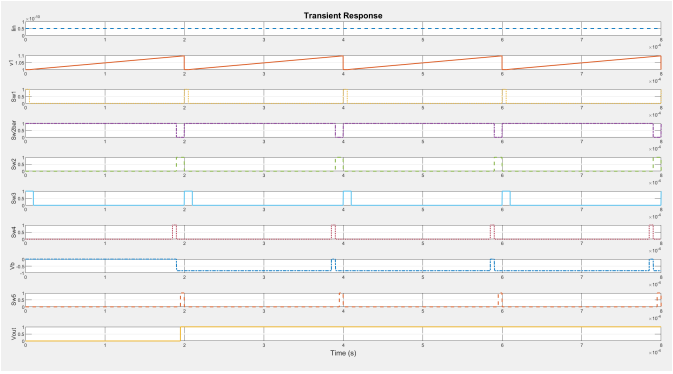


Fig. 5. Transient Response for input current of 50 pA

## V. Figures of Merit and Area Estimation

### A. Performance Comparison

TABLE I
Qualitative Comparison with Existing Qubit Readout Methods

| Method | Power | Time | Area |
|---|---|---|---|
| Conv. Current Sensing [1] | Less | More | Less |
| Reflectometry [1] | More | Less | More |
| **This Work** | Moderate | Less | Less |

TABLE II
Figures of Merit for Proposed Readout Design

| Metric | Description |
|---|---|
| Input Sensitivity | $<$ 1 nA detectable current |
| Integration Window | 1–1000 $\mu$s (tunable) |
| Opamp Gain | $\sim$80 dB |
| Area | $\sim$0.045 mm$^2$ |
| Readout Fidelity | $\sim$99.9% |
| CDS Suppression | $\sim$20 dB |

### B. Capacitor Area Estimation

Assuming a capacitor density of 1 fF/$\mu$m$^2$:

- $C_F$ = 2 capacitors of 100 fF each  200 µm$^2$
- CDS = 2 capacitors of 2 pF each  4000 µm$^2$
- Total capacitor area  0.0042 mm$^2$

The small area footprint and simplicity of passive components make this architecture scalable and practical for quantum SoCs.

## VI. Conclusion

In this paper, we presented a system-level recreation and simulation of a cryogenic CMOS current comparator intended for spin qubit readout. The design uses a current integrator and a CDS circuit to achieve fast, accurate, and low-noise signal conversion, outperforming traditional methods in terms of readout time and integration overhead.

Through detailed operational breakdowns and simulation-based validation, we demonstrated the circuit's suitability for quantum applications. Future work will involve implementing the layout, optimizing noise margins, and possibly integrating with a real charge sensor model. The scalability of the approach also opens doors to multi-channel cryogenic readout systems.

## Acknowledgment

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## References

[1] H. Fuketa et al., "A Cryogenic CMOS Current Integrator and Correlation Double Sampling Circuit for Spin Qubit Readout," *IEEE TCAS-I*, vol. 70, no. 12, pp. 5220–5228, Dec. 2023.

[2] Github Repository - https://github.com/EshwarAllampally/Cryogenic-CMOS-Current-Sensor