University of North Carolina at Charlotte
Department of Electrical and Computer Engineering

Qorvo Radio

Lock Detect AXI Stream Interface - Trigger Version

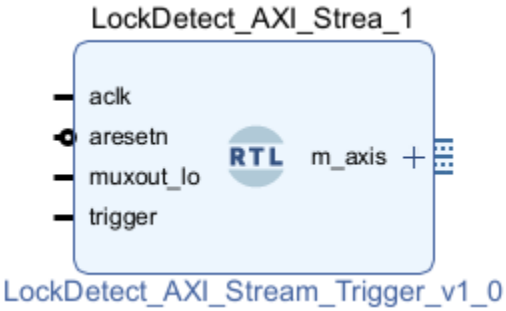

Figure 1-1 Lock Detect – Trigger Module Diagram

Contents

Module Overview

The **LockDetect_AXI_Stream_Trigger** VHDL module interfaces the Lock Detect output (MUXOUT) from the Local Oscillator (LO) chip to the FPGA's AXI Stream interface. It enables the software control layer to trigger and retrieve lock-status signals, allowing integration with higher-level software like GNU Radio.

Module Specifications

1. Inputs

- `aclk` (std_logic): AXI Stream clock input. Drives synchronous logic within the module.
- `aresetn` (std_logic): Active-low synchronous reset input. Resets internal states to default.
- `muxout_lo` (std_logic): Direct Lock Detect status signal from the LO chip (0 for unlocked, 1 for locked).
- `trigger` (std_logic): Pulse-trigger from software, initiating a read of the Lock Detect status.

2. Outputs

- `m_axis_tvalid` (std_logic): AXI Stream validity signal. Indicates when output data is valid.
- `m_axis_tdata` (std_logic_vector(31 downto 0)): AXI Stream data output, embedding the Lock Detect status in the least significant bit.
- `m_axis_tready` (std_logic, input): AXI Stream ready signal from receiver, indicating readiness to accept data.

Operational Description

The module utilizes a two-state finite state machine (FSM):

1. IDLE State

Awaits a high pulse on trigger. In this state:

- `m_axis_tvalid` is low, signaling no data available.
- When triggered, the current state of `muxout_lo` is captured and latched into a 32-bit vector (with only the least significant bit used).

2. SEND State

Outputs the latched Lock Detect value onto the AXI Stream interface.

- `m_axis_tvalid` asserts high, indicating valid data.
- Waits for acknowledgment (`m_axis_tready`) before returning to IDLE.

Integration and Usage

- Instantiate the module within the FPGA block design.
- Connect the AXI Stream outputs (`m_axis_tvalid, m_axis_tdata`) to the respective AXI Stream input on the receiving module or software interface.
- Configure the FPGA software to send a trigger pulse whenever the Lock Detect status is desired.
- In GNU Radio, interpret the received AXI Stream data to present Lock Detect information clearly in the GUI.