University of North Carolina at Charlotte
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Qorvo Radio

SPI Direct Access Module

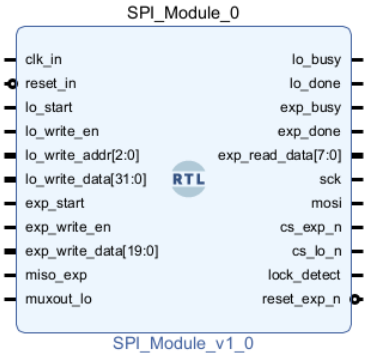

Figure 1-1 SPI Module Diagram

Contents

Module Overview

The **Top_Level** VHDL module is a legacy SPI configuration interface designed before implementing memory-mapped or AXI Stream interfaces. It manages direct register access through discrete input signals, coordinating SPI communication with the Local Oscillator (LO) and an I/O Expander.

Module Specifications

1. Inputs:

- `clk_in` (std_logic): System clock.
- `reset_in` (std_logic): Active-high synchronous reset.
- `miso_exp`: SPI Master-In Slave-Out from peripherals.
- `muxout_lo`: Lock detect input from LO.

a. LO Configuration:

- `lo_start`: Initiates LO SPI transaction.
- `lo_write_en`: Enables register write.
- `lo_write_addr`: Register address selector (3-bit).
- `lo_write_data`: Data input for LO registers (32-bit).

b. Expander Configuration:

- `exp_start`: Initiates Expander SPI transaction.
- `exp_write_en`: Enables data input for Expander.
- `exp_write_data`: Data for Expander configuration (20-bit).

2. Outputs:

- `lock_detect`: LO Lock detect indicator output.
- `reset_exp_n`: Active-low reset line for Expander.

a. LO Status:

- `lo_busy`: LO transaction in progress.
- `lo_done`: LO transaction completion indicator.

b. Expander Status:

- `exp_busy`: Expander transaction in progress.
- `exp_done`: Expander transaction completion indicator.
- `exp_read_data`: Data read from Expander (8-bit).

c. SPI Lines:

- `sck`: SPI clock.
- `mosi`: SPI Master-Out Slave-In.
- `cs_exp_n`: Active-low Chip Select for Expander.
- `cs_lo_n`: Active-low Chip Select for LO.

Operational Description

- **Direct Register Interface:** Registers and control signals for LO and Expander are set via direct input signals.
- **SPI Communication:** The module includes separate controllers (`LO_Controller`, `Expander_Controller`) and a shared `SPI_Master_8bit` module.
- **SPI Arbiter:** Prioritizes LO communication over Expander if simultaneous transactions are requested.
- **Status Outputs:** Indicate transaction progress and completion for software monitoring.

Integration and Usage

- Instantiate directly into FPGA designs that require explicit register-level control without complex bus interfaces.
- Provide discrete control signals to initiate configuration sequences.
- Interface SPI signals (sck, mosi, miso_exp, chip selects) directly to peripheral hardware.