University of North Carolina at Charlotte
Department of Electrical and Computer Engineering

Qorvo Radio

SPI AXI Stream Interface

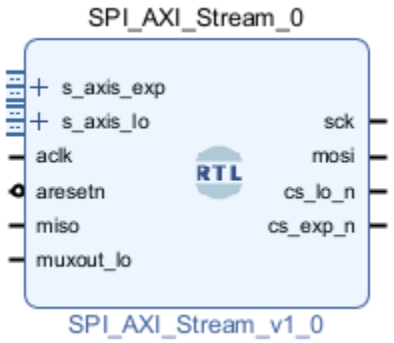

Figure 1-1 SPI Module Diagram

Contents

Module Overview

The **SPI_AXI_Stream** VHDL module provides a unified AXI Stream interface for configuring and controlling the Local Oscillator (LO) and an I/O Expander through SPI communication. It encapsulates dedicated AXI stream wrapper submodules for LO and Expander components, manages SPI transactions via an arbiter, and interfaces with a common SPI master. This design simplifies integration into FPGA-based SDR systems requiring dynamic SPI configurations from high-level software environments.

Module Specifications

1. Inputs

- `aclk` (std_logic): AXI Stream clock, synchronizes logic operations.
- `aresetn` (std_logic): Active-low synchronous reset, initializes internal states.
- `s_axis_lo_tvalid` (std_logic): Indicates valid AXI Stream input data for LO configuration.
- `s_axis_lo_tdata` (std_logic_vector(31 downto 0)): 32-bit data packets for LO registers.
- `s_axis_exp_tvalid` (std_logic): Indicates valid AXI Stream input data for Expander configuration.
- `s_axis_exp_tdata` (std_logic_vector(31 downto 0)): Data packets for Expander.
- `miso` (std_logic): Master-In Slave-Out signal from SPI peripherals.
- `muxout_lo` (std_logic): Lock detect status signal from LO.

2. Outputs

- `s_axis_lo_tready` (std_logic): Indicates readiness to accept LO configuration data.
- `s_axis_exp_tready` (std_logic): Indicates readiness to accept Expander configuration data.
- `sck` (std_logic): SPI clock signal.
- `mosi` (std_logic): Master-Out Slave-In signal to SPI peripherals.
- `cs_lo_n` (std_logic): Active-low Chip Select for LO.
- `cs_exp_n` (std_logic): Active-low Chip Select for Expander.

Operational Description

The module consists of several distinct components:

1. AXI Stream Wrappers

- `axis_to_lo_controller`: Receives 7 sequential 32-bit data packets configuring LO registers and control signals.
- `axis_to_expander`: Receives single 32-bit data packets for configuring Expander settings.

2. Controllers

- `LO_Controller`: Manages SPI transactions to configure LO registers. Exposes SPI signals for arbitration.
- `Expander_Controller`: Handles SPI communications for I/O Expander configurations. Exposes SPI signals for arbitration.

3. SPI Master

- `SPI_Master_8bit`: Provides an 8-bit SPI transaction interface, handling MOSI, MISO, SCK signals for communication with peripherals.

4. SPI Arbiter

- Dynamically selects between LO and Expander SPI requests, prioritizing LO transactions when simultaneous requests occur.

Integration and Usage

- Instantiate the SPI_AXI_Stream module in FPGA block designs.
- Connect AXI Stream inputs (s_axis_lo_tdata, s_axis_exp_tdata) and outputs (s_axis_lo_tready, s_axis_exp_tready) to relevant software or hardware interfaces.
- Attach SPI signals (sck, mosi, miso, cs_lo_n, cs_exp_n) to corresponding peripheral hardware.
- Configure software applications such as GNU Radio to provide configuration data via AXI Stream.