Cover Letter of Transmittal

From: QORVO_RADIO Team

Date: May 02, 2025

To: Senior Design Committee
9201 University City Blvd,
Charlotte, NC 28223

Senior Design Committee,

This document marks the culmination of the QORVO_RADIO project, a modular and reconfigurable Software-Defined Radio (SDR) platform developed as an educational tool for UNC Charlotte students. The attached report details the final hardware, software, and system-level design achievements, including integration efforts, testing procedures, and preparation for development by future teams.

Over the course of this academic year, our team has designed, implemented, and documented a complete SDR platform with a custom designed RF front end, FPGA control system, and GNU Radio user interface. Our key accomplishments of this semester include:

- The custom PCB design and fabrication have been completed, and final validation testing has been conducted.
- Successful integration of SPI communication and GNU Radio user interface for configuration and control of the system.
- Development of a fully enclosed chassis and modular architecture to support both hardware and software upgrades.
- Creation of comprehensive documentation and a setup guide for handoff.

All design elements have been individually verified and integrated. In the event of hardware limitations, we have established fallback demonstrations to validate functionality of the remaining subsystems. We will present our results and demonstrate the system at the Senior Design Expo, where it will serve as an interactive educational exhibit.

We are proud to pass along a well-documented, extensible platform that will support continued research and experience in wireless communication systems at UNC Charlotte. Thank you to both our supporters and staff for your continued guidance throughout this project.

Sincerely,
Nathan Waters, Andrew Nicola, Alan Luecke, Andrew Bowman, & Steven Freinstein.

File Directory

A directory containing all relevant project documents and Senior Design II course deliverables was named QORVO_RADIO_Comprehensive_Submission_SD2 and placed into the QORVO_RADIO zip files and thumb drives which are provided to grading instructor, ISL and Sponsors. The USBs were distributed at the Design Expo and the zip file was submitted on Canvas. The directory's outline is stated below,

Sub-Folder	Content	File Names
Bill of Materials and Budget	Budget Plan	BILL_OF_MATERIALS.XLSX
	Bill of Materials	FINAL BILL OF MATERIALS
Computer Codes and Simulations	Contains computer code for all aspects of the project like GNU radio, FPGA control and SPI controller	MASTER_INDEX.XLSX, README.TXT Folder names: VIVADO_BLOCKS, BACKUP, CURRENT, LEGACY
Correspondence	All emails, meeting notes, and phone call summaries related to the project	Folder names: WEEKLY EMAILS, KICKOFF_LETTER, MEETING NOTES
Drawings	Includes 'native' CAD files (assemblies, models, details, etc)	Folder Names: ENCLOSURE, PCB
Pictures and Videos	Clips and renders of the project video	Folder Name: FINAL VIDEO
Presentations	CDR and PDR Slide presentations	Folder Names: DESIGN_REVIEWS, MENTOR MEETING SLIDES
Reports and Documents	Project plan, timesheets, progress reports, to do list	Folder Names: PROJECT MANAGEMENT
Research	Research done by the team.	Folder Names: COMPUTER, ELECTRICAL, MECHANICAL

Division of Duties Summary Table

Each team member provided a summary of what they have accomplished relative to the project, displayed in the table below. Beside each task is the percentage contributed to the task by each team member.

	Nathan Waters	Andrew Nicola	Alan Luecke	Andrew Bowman	Steve Frienstein	Total
Progress Reports, PSR, PRP	20%	20%	30%	10%	20%	100%
Enclosure Design	10%	0%	90%	0%	0%	100%
PCB Design	90%	7.5%	2.5%	0%	0%	100%
Filter Design and Simulation	10%	90%	0%	0%	0%	100%
BOM	70%	0%	30%	0%	0%	100%
Manufacturing Enclosure	0%	0%	100%	0%	0%	100%
Testing FPGA	0%	5%	0%	80%	15%	100%
Assembling Enclosure and Components	5%	0%	92%	3%	0%	100%
Contingency Plan	0%	70%	0%	30%	0%	100%
Testing Contingency Plan	0%	30%	0%	70%	0%	100%
Documentation	30%	5%	5%	35%	25%	100%
Expo Poster, Final Report, Video	20%	35%	30%	7.5%	7.5%	100%

QORVO_RADIO Project – Final Design Package – Senior Design II

Date	Revision	Author	Comments
2025-02-05	1	QORVO_RADIO Team	

Contents

1 Overview of this Document [A]

The purpose of this project was to design and develop a reconfigurable Software Defined Radio (SDR) platform capable of receiving signals across a wide frequency range. The platform is intended to serve as a flexible educational tool for future student teams, allowing for modular expansion and adaptation for a variety of RF applications. Our primary objective was to create a functioning hardware prototype that could demonstrate reception while laying the foundation for future improvements and enhancements.

This document outlines the key decisions made throughout the design process, including component selection, system architecture, and design trade-offs. It also provides detailed testing results, evaluation against project requirements, and recommendations for further development. The information contained in this report is intended to guide the next phase of the project by documenting lessons learned, verifying baseline performance, and offering a starting point for future system expansions and refinements.

2 Project Overview / Statement of Work Summary [A]

QORVO has tasked us with designing a reconfigurable software defined radio (SDR) that will is modular and flexible, intended as an educational tool for future students of UNC Charlotte. The scope of this project covers the design, development, and testing of a reconfigurable SDR platform and a receiver module. Including the design and model of the platform, development of modular hardware components, software programming for controls, and the testing of the SDR platform.

3 Design Narrative [J] [K]

DN1: PCB

The QORVO_RADIO project was conceived to develop a modular, reconfigurable Software Defined Radio (SDR) platform that could support future student projects while offering the flexibility necessary for testing RF front-end configurations. At the beginning of the project, the team had little hands-on experience with RF hardware, so we began by researching commercially available SDR platforms, such as the Pluto SDR, HackRF One, and CaribouLite. While these systems offered a range of built-in features, the project sponsor preferred a fully custom RF front-end that would allow students to engage more deeply with the analog and mixed-signal aspects of SDR design.

With that in mind, our team committed to building a custom receiver system based on a direct conversion radio (DCR) architecture. This architecture down converts RF signals directly to baseband I/Q, which minimizes analog complexity and simplifies the signal chain. This is particularly desirable in systems that require low latency and high digital integration. We focused our design on creating a dual-path receiver, enabling support for signals both below and above 1 GHz. The sub 1 GHz path was designed to handle differential RF input, while the 1 GHz and above path used a single ended input to suit its corresponding mixer. This split allowed the system to span a frequency range of approximately 50 MHz to 4 GHz, with the LNA and Balun setting the boundaries of that range. The sub 1 GHz path is shown in figure 1.

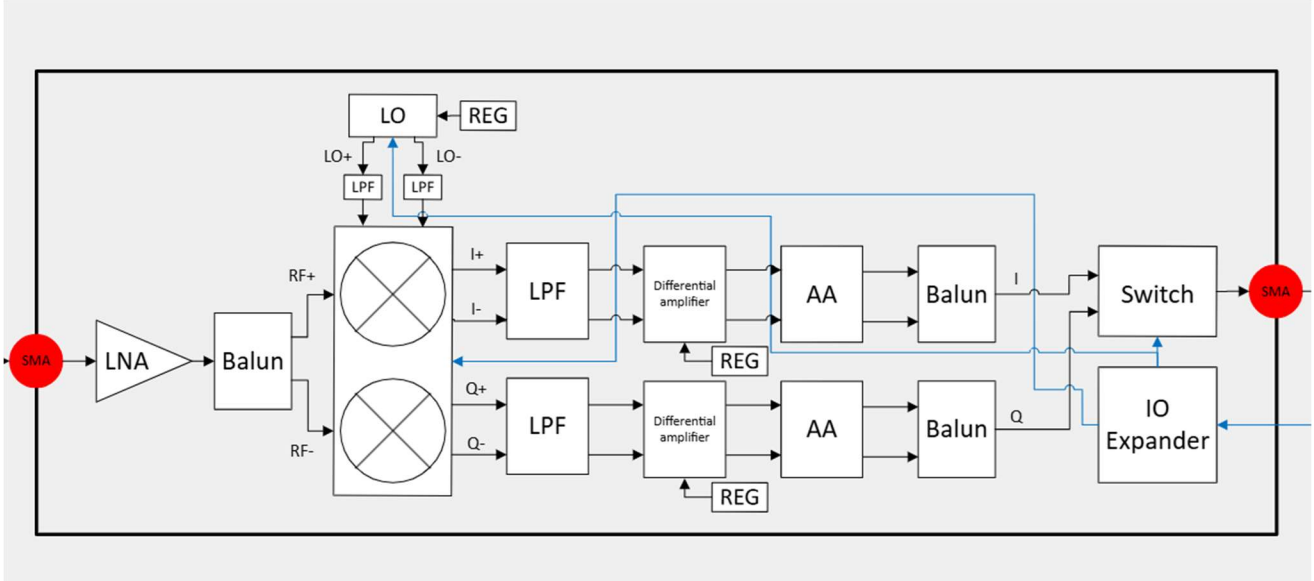

Figure 1: Sub 1 GHz Rx path

Every major component was selected to support this wide-band, direct conversion approach. For amplification, we used the QPL7442 low-noise amplifier from Qorvo, offering excellent gain and minimal noise across our entire target range. The LTC5584 mixer was selected for the sub 1 GHz path, offering differential input and a dynamic range, while the LTC5585 handled the high frequency path using a single ended input. Both mixers generate I/Q output directly from RF input, making them ideal for our chosen architecture. For the Local Oscillator (LO), we selected the ADF4351, which supports both integer N and fractional N synthesis and provides programmable output via SPI. This enabled dynamic LO tuning

through the FPGA and eliminated the need for separate signal generators. To manage the signal directionality and band selection, we implemented a switch (ADG736) to pick between low end and high-end outputs and an I/O expander (MCP23S17) to have more GPIO for enabling chips and other digital controls, giving us flexible digital control.

Filtering and power regulation were also integral to the performance of the board. We designed and simulated all lowpass and antialiasing filters based on manufacturer recommendations and simulation results, adjusting passive values as needed for availability. We regulated power locally with linear voltage regulators to ensure low noise in sensitive analog sections. A 3.3V regulator powered the LO, while a 0.9V regulator served the op-amp stages. All images of schematics and components are in the PCB Documentation slideshow in the google drive.

The six-layer PCB was carefully laid out with separate signal, power, ground, and control layers, following best practices for RF design such as coplanar waveguide routing, differential pair symmetry, and ground stitching to maintain signal integrity. The digital and manufactured PCBs are shown in figures 1 and 2.

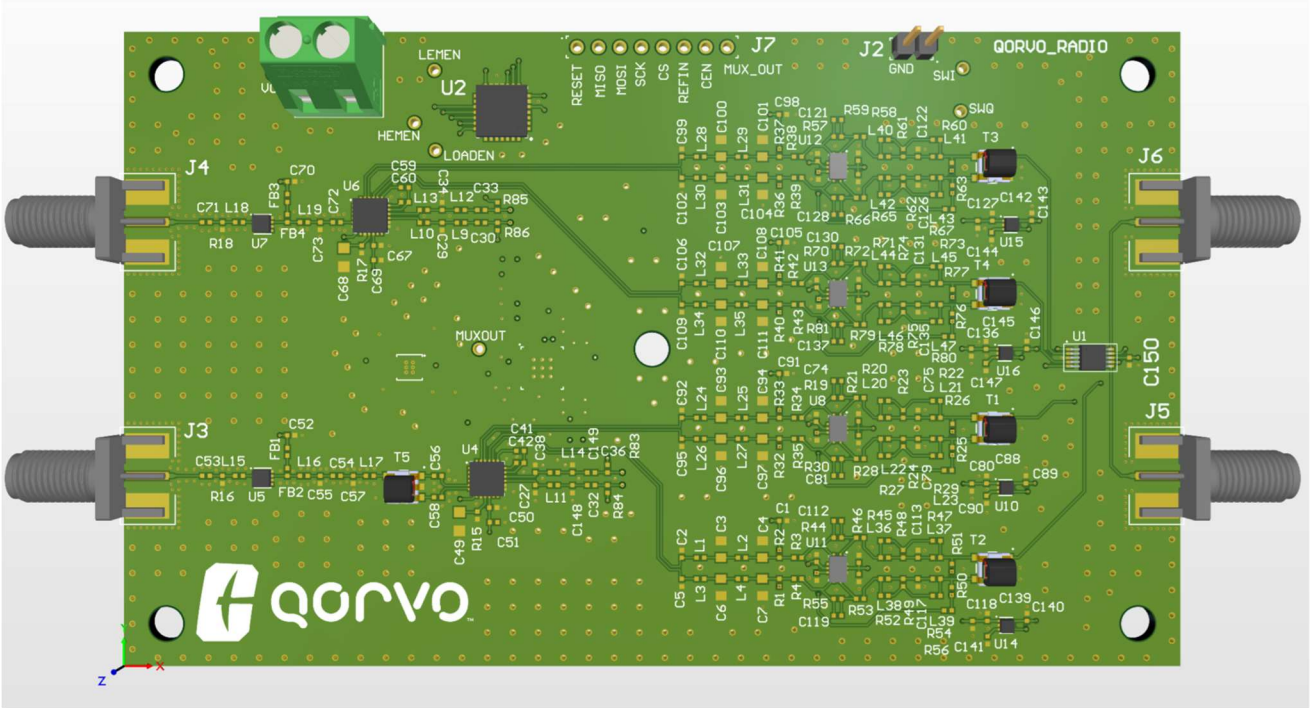

Figure 2: Digital PCB

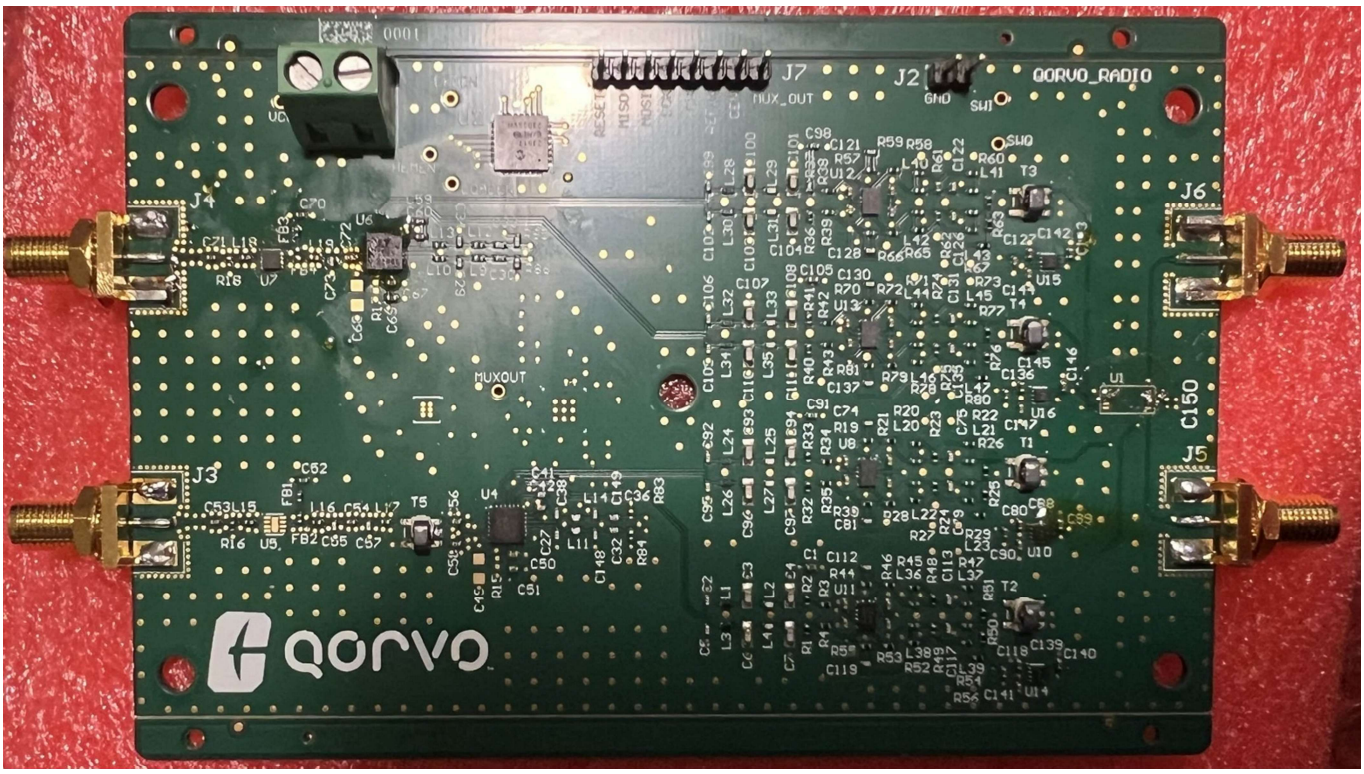

Figure 3: Manufactured PCB

DN2: FPGA

The communication between the PC and FPGA, figure 4, is central to the operation of the SDR receiver system and enables real-time configuration and monitoring by the user. This process begins on the host PC with GNU Radio, where the user selects a desired receive frequency using a custom graphical interface. A TCP socket block in GNU Radio transmits the frequency configuration over Ethernet to the FPGA.

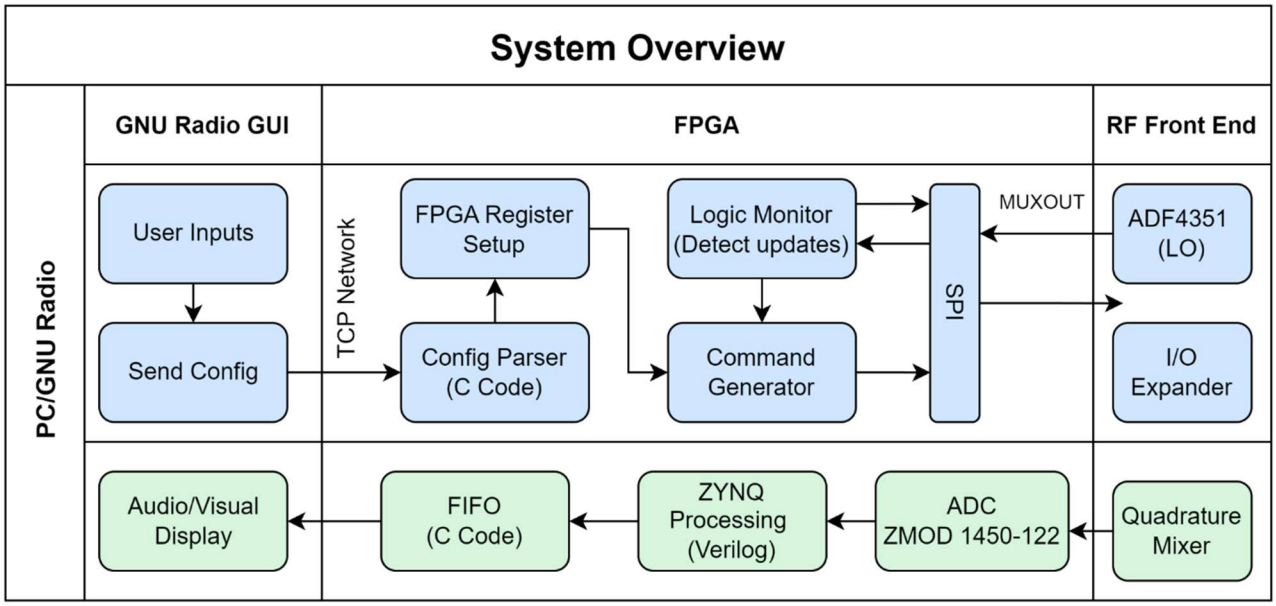

Figure 4: System Overview

Once received, the FPGA's embedded ARM processor (running a lightweight Linux environment) interprets the incoming TCP packet and passes the data to a C program running on the processor. This program computes the appropriate register values needed to configure the ADF4351 LO chip, translating user input into hardware-level commands. These register values are serialized and transmitted via AXI-Stream to an SPI controller implemented in programmable logic.

The SPI controller sends the data out to the RF front-end using SPI protocol, directly programming the LO. Upon successful configuration, the LO asserts a lock-detect signal indicating it has locked onto the target frequency. This lock-detect signal is passed back into the FPGA, where it is monitored and streamed as part of a status signal using AXI-Stream. This status can be configured to be visualized in GNU Radio, giving the user immediate feedback on system performance.

Once locked, the LO begins down-converting RF signals to baseband. These baseband I/Q signals are received through the Zmod SDR ADC, sampled at high speed, and processed on the FPGA. The digitized data is streamed over the FPGA's AXI-Stream infrastructure and routed back to the GNU Radio environment via Ethernet. This allows the user to visualize live baseband signals and spectrum data within GNU Radio's flexible interface.

DN3: Enclosure

The enclosure was designed to house all the components of the project. The main components include the FPGA, PCB, and power supply. Additionally, a fan, power receptacle, circuit breaker, two switches, and shielding were integrated into the enclosure. The components are shown in figure 5.

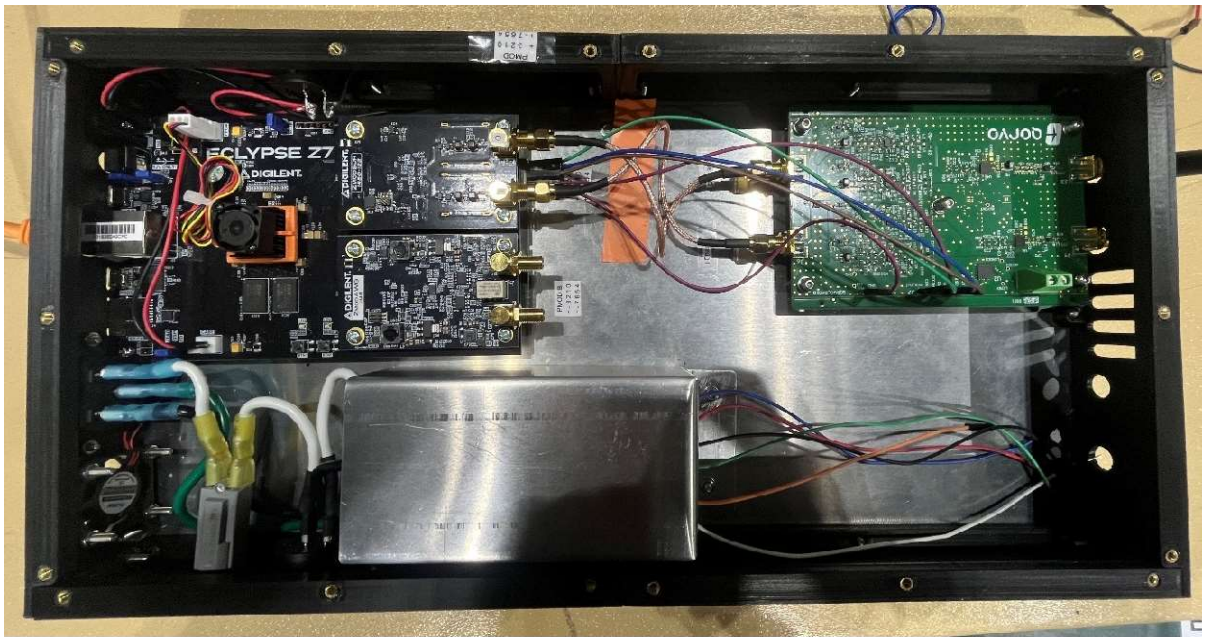

Figure 5: Assembled enclosure top view

Some of these items were added later in the project, so it is important that the enclosure is modular. When we decided that a switch and circuit breaker would be needed between the power receptacle and the power supply, it was as simple as adding a couple mounting holes in the 3D model, printing out one wall, and assembling it into the enclosure. If the enclosure was designed as a solid box that was bent from aluminum, or extruded for the specific components to fit, making changes to the design in the future wouldn't have been as simple, and an entirely new enclosure could possibly be needed. With modularity in mind, space is allocated for a second (future) PCB beside the current one. This will be completed in the future as the project will require transmitting capabilities, and it is important that the future students do not need to build another enclosure for that to be accomplished. As for the mechanical components, there is a base plate, walls, and a lid. The enclosure was designed with the base plate in mind. At 16" x 8" x 1/8", it didn't need to be cut to size, the mounting holes just needed to be drilled. It is made of 6061 T651 Aluminum and is large enough to be used as a chassis ground for the power supply. As for the walls, they are 3D printed with black PLA+ using a Creality Ender 3, 3D printer. There are 6 different walls, and each of them have features useful for the project. There are holes for the FPGA interface, the PCB's SMA ports, power receptacle, fan, circuit breaker, and two switches. Each of the walls has 5-10 threaded inserts and M3 screws. These connect the walls to each other, the base plate, and the lid. The threaded inserts are made of brass and are heated using a soldering iron to melt the PLA around them and sink into the premade holes in the walls. They have special features on the outside that allow the melted plastic to flow into them, and lock into place so that the connections are secure. These features can be seen in figure 6.

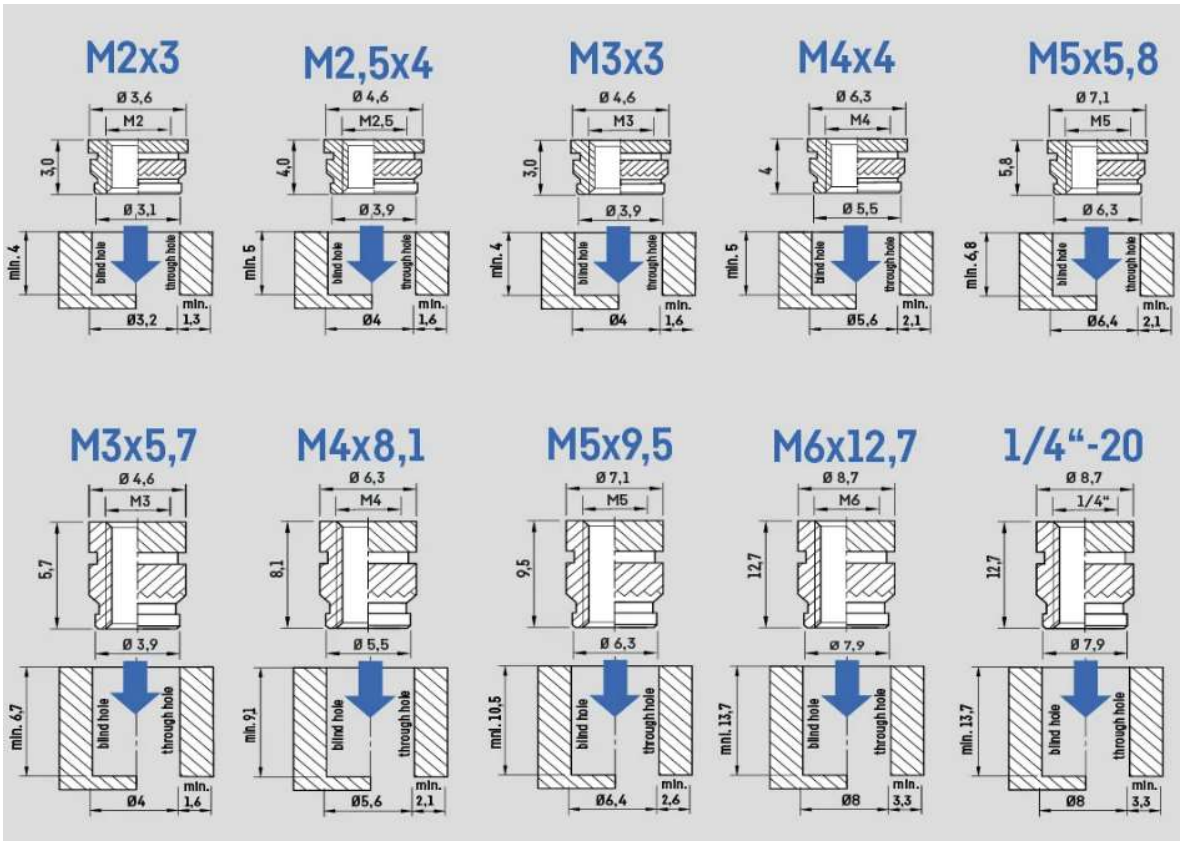

Figure 6: Diagram of different sized threaded inserts.

The screws used to hold everything in place are all M3 size, but range in different lengths. It is important that the lengths are right, so that everything can be assembled properly, and they don't interfere with each other, or other components. The FPGA is mounted by inserting screws directly through the base plate and into the standoffs that came with the FPGA. The power supply has mounting holes, so nuts were used as standoffs. The PCB needs to be higher for clearance of bottom mounted components, so standoffs were used to elevate it off the base plate. Each standoff was 3D printed and has two threaded inserts. Bolts were inserted through the bottom of the base plate and into the standoffs, and more bolts went through the top of the PCB into the standoffs, with a washer and a nut to secure them. The lid was designed to allow for monitoring the system while running. It has the same length and width as the base plate, but it is only 1/32" thick. It is made of plexiglass and is easily removable as it has screws mounting it to the walls. Finally, shielding was needed around the power supply, so we used a 1/32" thick piece of sheet metal and bent it to shape. It needed to fit around multiple faces of the power supply to reduce RF interference on the PCB. A vertical mill was used to cut it to size, and a large sheet metal bender was used to bend it into shape. 6 holes were drilled for each of the power supply outputs.

For future expansion of the project, there is already a location for the future PCB. All that needs to be done is ensure the size fits in the existing location within the enclosure. There are already holes in one of the walls for the SMA ports, so the locations need to be accurate. To find the exact measurements, the 3D model of the wall is in the google drive, saved under DRAWINGS>ENCLOSURE>CAD. There are Creo part files, STL (stereolithography), and GCODE files. Ensure the bolt hole locations are accurate on the new PCB, and drill new mounting holes for it on the base plate. Any mounting method can be used, but the current method can be replicated. The files for the standoffs are saved in the same file location. The heights can be adjusted depending on the thickness of the PCB. If something is wrong with a wall and it just needs to be printed, there are 2 options for reprinting it. A simple option is downloading the GCODE file, sending it to a 3D printer, and printing it. Another option would be downloading the STL file, sending it to a slicing software, and getting a GCODE file from that. If features need to be added to the walls, open the .zip file titled ENCLOSURE NATIVE FILES saved in the same location, and open the Creo Assembly file titled Final_Enclosure.asm. This assembly contains all the parts at the current state of the project. Modifications can be made to any of the walls and reprinted and then assembled into the desired location. The threaded inserts can be removed from the discarded wall using a soldering iron and reused on the new wall. More details on components are on slides 45-48 of the PCB DOCUMENTATION slideshow saved in the google drive.

4 Test Results [J] [D]

During the semester tests were performed to determine if the requirements and specifications described in the appropriate document are met. These tests ranged from simple tests using a Flipper Zero tool to using an Analog Discovery 3 logic analyzer and lab oscilloscope.

Test	Method	Result
PCB Short Circuit Analysis	Testing the impedance, to make sure there are no shorts	The test was successful, and read close to 50-ohms
PCB with Initial SPI	The PCB was set under a current limiter (0.5A) and hooked up like we planned	Power to all chips worked but the output at the Expander and LO were not working properly leading us to the conclusion that SPI was having issues
PCB with Manual switching	The PCB was set under and slightly higher current limiter (0.7A) and the Low end was enabled	Power to the mixers worked, leading us to a higher current draw but the LO and Expander were not performing as they should solidifying that SPI communication was not correct
SPI Interface to Expander	A Flipper Zero was used to read the SPI output	The test was successful, and the expected bits were shown on the Flipper Zero.
SPI Interface to Expander	SPI Control to Expander	The test was unsuccessful. During testing it was discovered that the Expander must be controlled with a logic level of 4 or more Volts. No output was seen with an oscilloscope on any of the output pins.
SPI Interface to LO	A Flipper Zero and Analog Discover 3 were used to read SPI Output	The test was successful, and the expected bits were partially shown on the Flipper Zero. The Flipper Zero can read a maximum of 16 bits of the 32. The Analog Discovery 3 read all the expected bits
SPI Control to LO	An SPI control output was applied to the LO.	The test was unsuccessful. No output was seen with an oscilloscope on any of the output pins.
Low End/High End Enable	3.3 volts was applied to LENEN and HENEN to verify enabling PCB components.	The test was successful. Various PCB components powered on when voltage was applied.
Tuning Range	Verified using a PlutoSDR as a signal generator and receiver for various frequencies across the range.	Device successfully received and processed signals from 85 MHz to 2500 MHz without loss of functionality.
USB Communication	Connected platform to PC; verified communication and command control through GNU Radio.	Successful data exchange and control through USB to Ethernet
MUXOUT to Computer	The data path for MUXOUT from the PCB to the computer was tested by applying 3.3V to the PMOD pin. If MUXOUT output a high signal to indicate a locked	The test was semi-successful. The MUXOUT bit was received by the PC and verified using Wireshark. GNU Radio was unable to display the MUXOUT status due to an issue with the data type/state output from GNU Radio blocks.

	frequency, a logical 1 is displayed in the terminal and sent to the PC. Wireshark was used to verify the packet was received by the PC.	

Figure 7: Expander Output on Flipper Zero

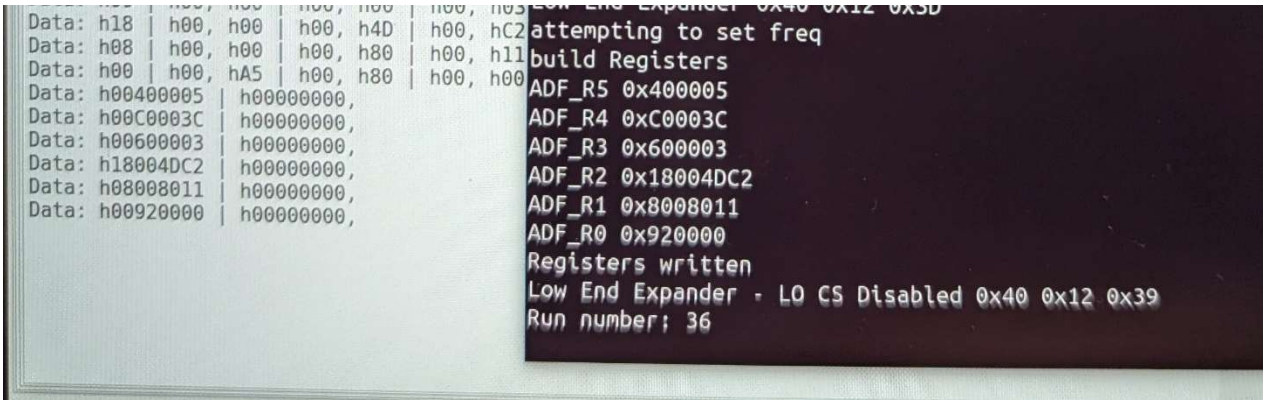

Figure 8: LO Output on Analog Discovery 3

5 Adherence to Engineering Standards and Codes [A]

For this project, our industry sponsors did not require compliance with any specific engineering standards or codes. Nevertheless, the team chose to reference several

recognized standards during the design, development, and testing phases to ensure a robust and well-informed approach. While strict adherence to these standards is not mandated, using them as guiding references helps validate design choices, encourages best practices, and provides a foundation for future improvements or expansions of the educational SDR platform. The engineering standards and codes utilized in the project include but are not limited to; IPC-2221, IPC-6012, IPC-A-600, IPC-A-610, IEEE Std 287.1, IEEE 802.3, IEEE Std 1641, IEEE Std 1900.1, and IEEE Std 1149.1.

ST1: IPC-2221 – PCB Design

IPC-2221 provides useful information for the design of the PCB. It includes layout, spacing, trace routing, and component placement. Meeting all the design parameters in IPC-2221 sets the design on the right path for a functional PCB.

ST2: IPC-A-600/610 – PCB Fabrication and Assembly

IPC-A-600 and IPC-A-610 pertain to PCB fabrication and assembly. The PCB was ordered through and manufactured by JLC PCB, but it was important to ensure that the PCB followed the criteria in this standard before submitting it to them. The PCB was thoroughly reviewed multiple times before ordering, and again by JLC PCB after ordering.

ST3: IEEE Std 287.1-2021 – Precision Coaxial Connectors

IEEE 287.1 offers guidance on selecting and implementing precision coaxial connectors. Adhering loosely to these specifications encourages improved signal integrity, reliability, and repeatability.

ST4: IEEE Std 802.3 – Ethernet Standard

IEEE 802.3 serves as a valuable reference for robust data communication principles. By examining established Ethernet practices, the team can apply similar strategies to ensure stable data transfer and anticipate potential EMI or interference issues.

ST5: IEEE Std 1641-2022 – Signal and Test Definition

IEEE 1641 promotes consistent signal characterization and structured testing. This encourages the team to adopt test procedures that are clear, repeatable, and easily understood by future users.

ST6: IEEE Std 1900.1-2019 – Definitions and Concepts for Dynamic Spectrum Access

IEEE 1900.1 helps ensure that the team's conceptual understanding of dynamic spectrum access is consistent with widely accepted terminology and principles. Applying these concepts as reference aids while creating a design that is conceptually sound and potentially easier for future students to understand and expand upon.

6 Evaluation of Prototype/ Model/ System as Compared Document [J]

Power-up went almost exactly according to plan. As soon as the 5 V rail came on-line the front-end silicon— the LNAs, mixers, driver amplifiers, the I/O-expander, and the ADF4351 local oscillator —each showed a valid enable voltage. Both timing rails behaved, too: the board's 10 MHz reference appeared cleanly at the LO's REFIN and CLK pin as well as at the I/O expander's SCK pin, confirming that the passive routing and level-shifting on those traces are behaving as expected.

Where the design stumbled was the SPI configuration path. Logic-analyzer traces show the microcontroller driving MOSI, SCLK, and CS exactly as scripted, and the waveform reaches the LO and the I/O-expander pins with proper voltage swing. Nevertheless, neither device latches the data. The expander never asserts its output pins, meaning the low end and high end enable pins are not set to logic high and the chips do not receive power on either side. For testing purposes, we hardwired all the chips enables for the low-end paths to try and get some data output. The LO stayed in its power-up idle state with no REFOUT signal after receiving its MOSI signal, this was quintessential to the RF path functioning. Because the mixers get tuned using the local oscillator's reference signal they never down-convert the incoming RF signal, and no signal is output to the I/Q channels. With no IQ channels present, the FPGA's ADC that follows the analog frontend does not receive any signals, so no audio emerges from GNU Radio.

To verify that the FPGA's ADC and communication to the PC functions as expected we set up a test scenario where we used the Pluto SDR as a RF front end; by doing this we were able to receive RF signals on our ADC, those signals were digitized and displayed on GNU radio as well as heard through the speakers as expected.

In summary, the board mostly functions as we would have expected from our prototype, the issue faced with the MOSI and LO bit configuration ultimately prevented us from testing the output of the RF front end and the prototype.

7 Recommendations for Further Development [A]

Since our PCB was powered on, tested, and confirmed to be functioning as designed, the next step for future teams is to focus on getting the digital control flow working properly. The hardware is not the issue, the primary challenge moving forward is correctly configuring the LO and I/O expander registers via SPI. The immediate goal should be to get the register configurations working, starting with writing good values for the ADF4351 and verifying communication using tools like logic analyzers or the MUXOUT signal. While doing this, the team should manually switch between the low-end and high-end signal paths using the enable test points to validate each path independently before tying it into full digital control.

Once reception is working, the team can start preparing for the transceiver portion. It's important to fully understand what's required for transmit-side communication and not just test things for the sake of testing. Every SPI signal, control pulse, and enable line should serve a purpose, so plan ahead. We recommend buying test parts like breakout boards for the LO or GPIO expanders

to validate control logic in isolation before integrating them into the full system. It'll save a lot of debugging time.

If the team remains structured with 3 electrical and 2 computer engineers, we strongly suggest this division of responsibilities: 2 EEs on PCB design and layout, 1 EE focused on FPGA-to-PCB communications, 1 CE on FPGA SPI and embedded control, and 1 CE on PC-side communications and interface (e.g., GUI, GNU Radio). Finally, don't reinvent the wheel. There are many public resources and reference designs that can help with SPI timing, LO register sequencing, and PC-FPGA communication. Use them.

8 Impact [F] [G] [H]

The primary aim of this project is to develop a modular, reconfigurable SDR receiver to serve as a hands-on educational tool for students learning about wireless communication systems. While the broader societal or global impact of this platform may be limited, its value lies in enhancing the learning experience of current and future engineering students at UNC Charlotte. By providing a practical, accessible system for exploring RF concepts and signal processing, the project contributes to the development of technical skills and interdisciplinary collaboration within a university setting. The following sections discuss the potential impacts in terms of public welfare, global relevance, cultural and social dynamics, environmental sustainability, and economic considerations.

IP1: Public Health, Safety, and Welfare
Our SDR system is a receive-only, low-power device designed for use in controlled laboratory environments. Because it does not transmit, there is no risk of electromagnetic interference or violation of RF emission standards. The hardware poses no health or safety hazards beyond standard lab precautions, such as ESD-safe handling. While the system does not directly impact public health or safety, it plays an indirect role by educating students on how to design and evaluate communication systems that *could* be deployed in critical safety applications in the future.

IP2: Global Impact
While the direct reach of this project is limited to UNC Charlotte, its open-source nature expands its potential value beyond the university. By publishing source code, documentation, and design files, the project becomes accessible to students, educators, and hobbyists around the world who may not have access to expensive commercial SDR tools. This contributes to the growing body of openly available RF education resources and reinforces a culture of shared learning and collaboration. Though modest in scope, the project aligns with global efforts to reduce barriers to technical education.

IP3: Cultural Impact
This project does not directly affect cultural norms or behaviors, but it supports broader access to technology in education. By giving students firsthand experience with wireless systems, it contributes to a learning culture that emphasizes exploration, experimentation, and applied problem-solving. In the long term, projects like this continue to aid interdisciplinary project-based learning environments that better reflect industry expectations.

IP4: Social Impact
This project promotes collaboration across disciplines by engaging our students within a variety of engineering majors. Over the course of the semester, students developed skills in FPGA programming, signal acquisition, and system-level integration. The project structure encourages peer learning and cross-semester mentorship, as future teams will build on our foundation. This social continuity strengthens the academic community and fosters collaborative problem-solving, communication, and shared ownership of educational tools.

IP5: Environmental Impact
Environmental impact is minimal due to the reuse of components and the focus on software-defined functionality. Because the system is programmable, enhancements can be made via firmware updates rather than repeated hardware revisions. This reduces electronic waste and extends the platform's usability over several semesters. The passive receive-only design also means there are no emissions or active environmental concerns related to RF transmission.

IP6: Economic Impact
The economic impact of this project is limited to its educational context. By providing a reusable, in-house tool for teaching RF fundamentals, the university may reduce the need for more expensive, commercial SDR hardware. While not intended for commercial deployment, the project gives students practical experience with technologies used in RF and embedded systems industries, potentially improving their job readiness and long-term economic contribution as graduates.

9 Bill of Materials (BOM) [E]

In the bill of materials (BOM), each item number, quantity, part number, product description, unit cost, total cost, and vendors are listed. The BOM can be found in the sub folder titled "BILL OF MATERIALS AND BUDGET" in the comprehensive submission. All components are shown in figures 9, 10, and 11.

QORVO_RADIO BILL OF MATERIALS				Total Remaining	Total	ISL Total
				$568.24	$2,694.73	$2,681.76
ITEM NO.	QTY	PART NUMBER	PRODUCT DESCRIPTION	UNIT PRICE	TOTAL PRICE	Vendor
1	1	584-ADALM-PLUTO	ADALM-PLUTO software defined radio	$230.61	$230.61	Mouser
2	1	1286-410-427-ND	ZMOD SDR ADC 1450-122 SYZYGY POD	$249.00	$249.00	Mouser
3	1	1286-410-393-ND	ECLYPSE Z7 ZYNQ-7000 DEV BOARD	$449.00	$449.00	Mouser
4	1	B0BFPWJ3J9	RG316 Coaxial Cable Jumper for 3G 4G LTE WiFi Antenna Router RTL SDR Dongle Analyzer etc. 5-Pack	$11.97	$11.97	Amazon
5	1	DP_L20_Mix_12(	Wire Length Optional Dupont Cable Assorted Kit Male to Female Male to Male Female to Female Multicolored Ribbon Cables - 7.8 inch	$6.98	$6.98	Amazon
6	1	KCD1-5-101	Circle Toggle Switch 12V for Car Automotive RV 2 Pin Switch 120V Wired KCD1-5Pack	$6.99	$6.99	Amazon
7	1	B0BFR8RPR6	Aluminum Plate Covered with Protective Film, Heat Treatable Rectangle 3MM Aluminum Metal Plate for Industrial, Crafting (2 pack)	$25.99	$25.99	Amazon
8	1	B086Z2Y1D6	Electrical Terminals Kit, Crimp Connector Assortment, Ring Fork Spade Splices	$12.99	$12.99	Amazon
9	1	B0CG19LWMD	FIRMERST 10 Feet 12 Gauge 3 Conductor Power Cable SJTW 300V Pure Copper Wire	$16.99	$16.99	Amazon
10	2	4468	FAN AXIAL 30X8MM 5VDC	$2.95	$5.90	DigiKey
11	6	PCB.SMAFSTJ.E	CONN SMA JACK STR 50OHM EDGE MNT	$3.36	$20.16	DigiKey
12	1	1866-4008-ND	Open Frame AC DC Converters 2 Output 5V 12V 90 ~ 264 VAC, 127 ~ 370 VDC Input	$16.90	$16.90	DigiKey
13	2	Q336-ND	Power Entry Connector Receptacle, Male Blades IEC 320-C14 Panel Mount, Flange	$1.06	$2.12	DigiKey
14	20	RC0402JR-071	62.5mW Thick Film Resistors 50V ±100ppm/°C ±5% 1kΩ 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.01	JLC PCB
15	20	GCM1555C1H	50V 1nF C0G ±1% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.03	$0.59	JLC PCB
16	20	GCM1555C1H	50V 680pF C0G ±5% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.01	$0.17	JLC PCB
17	20	RC0402FR-07	62.5mW Thick Film Resistors 50V ±100ppm/°C ±1% 360Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.01	JLC PCB
18	42	GRM155R61H	50V 1uF X5R ±10% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.03	$1.16	JLC PCB
19	70	CL05B104KO5	16V 100nF X7R ±10% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.00	$0.07	JLC PCB
20	20	GCM155R71H	50V 2.7nF X7R ±10% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.01	$0.16	JLC PCB
21	20	AC0402JR-07	62.5mW Thick Film Resistors 50V ±100ppm/°C ±5% 50Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.02	JLC PCB
22	20	SDCL1005C12	300mA 12nH ±5% 500mΩ 0402 Inductors (SMD) ROHS	$0.00	$0.08	JLC PCB
23	20	C250446 MMZ	2.1Ω ±25% 1.8kΩ@100MHz 0402 Ferrite Beads ROHS	$0.03	$0.53	JLC PCB
24	20	0402WGF4701	62.5mW Thick Film Resistors 50V ±100ppm/°C ±1% 4.7kΩ 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.01	JLC PCB
25	2	M20-9990245	3A Direct Insert Policy 2.54mm 2P 6.1mm -40°C~+105°C 3mm 2.54mm Single Row Brass Black Plugin,P=2.54mm Pin Headers ROHS	$0.11	$0.21	JLC PCB
26	20	GCM1555C1H	50V 39pF C0G ±5% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.01	$0.16	JLC PCB

Figure 9: First part of BOM

27	20	CQ0402BRNP	50V 2.3pF C0G 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.01	$0.20	JLC PCB
28	24	GJM1555C1H3	50V 39pF null ±5% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.02	$0.53	JLC PCB
29	24	GJM1555C1HF	50V 0.5pF C0G 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.02	$0.55	JLC PCB
30	42	CRCW040220	62.5mW Thick Film Resistors 50V ±1% ±100ppm/°C 20Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.13	JLC PCB
31	2	MCP23S17T-E	10MHz SPI QFN-28-EP(6x6) I/O Expanders ROHS	$1.90	$3.80	JLC PCB
32	2	ADF4351BCP2	4.4GHz LFCSP-32(5x5) Clock Generators, PLLs, Frequency Synthesizers ROHS	$13.57	$27.14	JLC PCB
33	2	ADM7150ACP	800mA 68dB@(1MHz) Fixed 3.3V Positive electrode 16V LFCSP-8-EP(3x3) Voltage Regulators - Linear, Low Drop Out (LDO) Regulators ROHS	$6.52	$13.04	JLC PCB
34	20	GJM1555C1H1	50V 1.5pF C0G 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.01	$0.29	JLC PCB
35	20	GJM1555C1HF	50V 0.3pF C0G 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.03	$0.53	JLC PCB
36	20	GRM1555C1H	50V 1nF C0G ±5% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.00	$0.09	JLC PCB
37	20	LQG15HS1N8	950mA 1.8nH 80mΩ 0402 Inductors (SMD) ROHS	$0.01	$0.14	JLC PCB
38	26	CRCW040215	62.5mW Thick Film Resistors 75V ±1% ±100ppm/°C 150Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.06	JLC PCB
39	20	CRCW040210	63mW Thick Film Resistors 50V ±100ppm/°C ±1% 100Ω 0402 Chip Resistor - Surface Mount ROHS	$0.02	$0.38	JLC PCB
40	22	CRCW040210	62.5mW Thick Film Resistors 50V ±1% ±100ppm/°C 10kΩ 0402 Chip Resistor - Surface Mount ROHS	$0.00	$0.09	JLC PCB
41	38	GRM155R71C	16V 10nF X7R ±10% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.00	$0.11	JLC PCB
42	26	GJM1555C1H1	50V 10pF C0G ±5% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.01	$0.35	JLC PCB
43	20	GJM1555C1H4	50V 47pF null ±1% 0402 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.04	$0.71	JLC PCB
44	1159	LQG15HSR15	150mA 150nH ±3% 2.99Ω 0402 Inductors (SMD) ROHS	$0.01	$8.58	JLC PCB
45	362	LQG15HS5N6	650mA 5.6nH 180mΩ 0402 Inductors (SMD) ROHS	$0.02	$8.58	JLC PCB
46	167	GRM188C81C	16V 10uF X6S ±20% 0603 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.05	$8.62	JLC PCB
47	566	MHQ1005PR1	90mA 180nH ±2% 4.86Ω 0402 Inductors (SMD) ROHS	$0.02	$8.60	JLC PCB
48	458	QPL7442TR7	Qorvo QPL7442TR7	$0.02	$8.61	JLC PCB
49	8	TPS71709DSE	70dB@(100Hz) 150mA Fixed 900mV Positive electrode 6.5V WSON-6(1.5x1.5) Voltage Regulators - Linear, Low Drop Out (LDO) Regulators ROHS	$1.39	$11.09	JLC PCB
50	82	VJ0603D151J	25V 150pF C0G ±5% 0603 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	$0.10	$8.58	JLC PCB
51	640	LQG15HN1N2	1A 1.2nH 80mΩ 0402 Inductors (SMD) ROHS	$0.01	$8.58	JLC PCB
52	101	LQG15HN4N7	700mA 4.7nH 160mΩ 0402 Inductors (SMD) ROHS	$0.08	$8.57	JLC PCB
53	5055	CRCW040227	63mW Thick Film Resistors ±100ppm/°C ±1% 27.4Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$8.59	JLC PCB
54	872	CRCW040224	62.5mW Thick Film Resistors ±100ppm/°C ±1% 243Ω 0402 Chip Resistor - Surface Mount ROHS	$0.01	$8.55	JLC PCB
55	5055	CRCW040286	63mW Thick Film Resistors ±100ppm/°C ±1% 86.6Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$8.59	JLC PCB
			1x2P 17.5A 250V Green 14~30 Direct Insert 5.08mm 1 2 Plugin,P=5.08mm	$0.26		

Figure 10: Second part of BOM

56	34	1715721	Screw Terminal Blocks ROHS		$8.72	JLC PCB
57	329	CRCW040211(	62.5mW Thick Film Resistors 75V ±1% ±100ppm/°C 110Ω 0402 Chip Resistor - Surface Mount ROHS	$0.03	$8.59	JLC PCB
58	21	M20-9990845	HEADER 1ROW 8WAY	$0.42	$8.78	JLC PCB
59	12	ADG736BRMZ	2 4Ω SPDT(SPDT) MSOP-10 Analog Switches, Multiplexers ROHS	$0.77	$9.23	JLC PCB
60	2	LTC5584IUF#F	30MHz~1.4GHz 9.9dB 5.4dB QFN-24-EP(4x4) RF Modulators and Demodulators ROHS	$19.31	$38.62	JLC PCB
61	2	LTC5585IUF#F	400MHz~4GHz 12.7dB 2.4dB QFN-24-EP(4x4) RF Modulators and Demodulators ROHS	$19.13	$38.26	JLC PCB
62	8	LTC6409IUDB	QFN-10(2x3) Differential Amplifiers ROHS	$14.98	$119.82	JLC PCB
63	540	MHQ1005PR4	70mA 470nH ±2% 9.6Ω 0402 Inductors (SMD) ROHS	$0.02	$8.59	JLC PCB
64	1944	CW0402402RFK	62.5mW Thick Film Resistors 50V ±1% ±100ppm/°C 402Ω 0402 Chip Resistor - Surface Mount ROHS	$0.00	$8.55	JLC PCB
65	10	TC1-1-13M+	SMD,3.8x3.8mm RF Misc ICs and Modules ROHS	$0.93	$9.26	JLC PCB
66	1	1286-410-397-ND	ZMOD DAC 1411: SYZYGY-COMPATIBLE	$99.00	$99.00	DigiKey
67	3	1715721	TERM BLK 2P SIDE ENT 5.08MM PCB	$0.97	$2.91	DigiKey
68	1	1286-471-060-ND	ANALOG DISCOVERY 3 PRO BUNDLE	$409.00	$409.00	DigiKey
69	2	998-CBW28-2A-N	Circuit Breaker Thermal 2A 250 V AC 32 V DC Push to Reset Panel Mount	$8.93	$17.86	DigiKey
70	6	-ADG736BRMZ-	IC SWITCH SPDT X 2 4OHM 10MSOP	$3.74	$22.44	DigiKey
71	1	NanoVNA-F V3	Analyzer Measuring S-Parameters Voltage Standing Wave Ratio SWR, Phase, Delay, Smith Chart Support RTC Real time	$298.99	$298.99	Amazon
72	2	B099N4M76S	uxcell Aluminum Sheet, 300mm x 150mm x 1mm Thickness 5052 Aluminum Plate	$12.19	$24.38	Amazon
73	1	Travel	Round trip to and from QORVO from UNCC	$116.90	$116.90	N/A
74	1	Travel	Round trip to and from QORVO from UNCC	$115.50	$115.50	N/A
75	1	Travel	Round trip to and from QORVO from UNCC	$116.90	$116.90	N/A

Figure 11: Third part of BOM

10 Budget [E]

We had access to almost all the tools necessary to complete the project and the manufacturing of the enclosure materials, eliminating external labor costs. These tools include a vertical mill and a sheet metal bender to manufacture the shielding, a drill for all the holes in the base plate and lid, a 3D printer to print all required materials, and a soldering iron to insert the threaded inserts. All these tools are either student owned or provided by the ISL lab in Cameron. The tools in the EPIC senior design lab allowed for wiring connections all through the enclosure. The PCB was manufactured by JLC PCB, and the manufacturing cost was included in the order cost. A few components were installed separately by technicians at QORVO in Greensboro, so the cost was included as a travel reimbursement at $116.90. After all required materials were purchased, our remaining budget was $1,582.15, so this money was allocated to use for future project expansion and test equipment.

These items include:

- ZMOD DAC
- Analog Discovery 3
- Nano Vector Network Analyzer

Additional items were purchased to enhance the project including:

- Aluminum sheet for shielding
- 2A 250V Circuit Breaker
- 4OHM IC Switch

- PCB terminal block

The total cost of all the components on the bill of materials without travel came to $2,332.45. Three separate trips to and from QORVO totaled $349.30, bringing the total cost of the project to $2,681.75. With a total budget of $3,250, our project had $568.24 remaining after all expenses.

11 Unrealized Integration and Recommended Next Steps

While the QORVO_RADIO project achieved major milestones in system design, one critical integration goal was not fully realized: incorporating the custom-designed RF front-end PCB into the complete signal chain. Despite successful PCB fabrication and control system implementation, voltage compatibility issues and a failure in SPI behavior, where data sent over MOSI was not acknowledged by the devices, despite signals reaching the devices, no response was observed, prevented full validation of the front-end configuration.

The design called for the use of an MCP23S17 SPI I/O expander to control various enable lines on the front-end, including chip enables, frequency path selection, and the load enable (LE) line for the ADF4351 local oscillator (LO). However, the expander was connected to a 5V input supply causing the logic highs leaving the expander to be at 4.3-5V. This posed a serious compatibility issue with the LO, which is rated for a maximum digital input voltage of 3.6V. Running the MOSI and LE lines from the expander into the LO risked overvoltage damage and unpredictable behavior. As a result, the team opted to bypass the expander entirely for critical signals.

New VHDL modules and accompanying C code were developed to transmit the LE signal independently from the SPI data lines, isolating it on a dedicated PMOD port configured for 3.3V logic (connecting to the LE test point). This separation allowed for safe operation of the LO while preserving timing control of register loading. Additionally, power was manually routed to the expander output enable lines using jumper wires to test direct LO register writes without relying on the expander.

Despite these efforts, the FPGA was never able to control the LO thus preventing the RF front end from producing a confirmed lock signal or output. Multiple attempts were made to configure the LO registers using variations of both VHDL and C implementations, adjusting load timing, chip select behavior, and register order. However, a limited test window between board arrival and final integration testing constrained the team's ability to further debug or rework the system.

Future teams taking over this project should prioritize validation of the LO configuration routine. Several working and experimental versions of the register configuration code are available in the project files (start with Attempted_LO_Fix). Teams should verify that the LO receives and acknowledges correct SPI writes by probing MUXOUT and checking for a lock condition as well as any signs of output.

Because the expander cannot be reliably used in this design, future implementations should consider directly powering either the high-frequency or low-frequency signal path using the

appropriate enable test point. Through-hole test points are available on the PCB for both I/Q channel path selection and load enable control, which can be adapted with jumper wires or soldered headers allowing full control of the board without the I/O expander functioning. With MOSI now dedicated to the LO and the expander bypassed entirely, the system must be reconfigured for minimal control routing and manual enable switching until a redesign is implemented.

12 Lessons Learned [J]

PCB Design

Throughout the design and testing phases of this project, I learned a lot about the challenges and best practices of PCB design, especially for high-frequency RF systems. Here are the key lessons I would carry forward into future work:

- **Use offline component footprints**
  Early in the design, I relied heavily on Altium's online component libraries, which sometimes resulted in mismatched pin mappings or incorrect pad sizes. Going forward, I would download or build every footprint offline and verify it manually before placing it into the schematic.
- **Be more intentional with via placement**
  While stitching vias and ground returns were used throughout the design, I would be more deliberate about via locations—especially around sensitive RF paths and near component grounds. Better placement could improve signal integrity and reduce the risk of noise coupling.
- **Implement second-order controls on mixers**
  We left several pins on the mixers unconnected, including optional controls that could be useful for low-power modes, tuning, or performance adjustment. If given more time, I would have populated these and included software hooks to test their impact on performance.
- **Plan for backup PCB design**
  We had one primary PCB design and no backup. Next time, I would plan out a minimal test version of the front end that isolates the core SPI devices and RF paths. Having a smaller board for early SPI bring-up would have saved us a lot of time debugging.
- **Divide work more effectively**
  As the lead on the PCB, I handled nearly every layout decision myself. In hindsight, I would assign someone else to handle layout-specific documentation or simulation while I focused on placement and routing. That would have helped catch more issues early and improved team efficiency.
- **Allow more time for layout reviews**
  We did multiple reviews but were always pushing against deadlines. I would reserve more time for peer review and manufacturer rule checks to catch layout or footprint issues before fabrication.
- **Design with testing in mind**
  While we added test points, we could have made headers more accessible for jumper wires and signal injection. I would also label test points directly on the silkscreen and include more probing access for low-speed control lines.

Component Selection

The only major design challenge in this project stemmed from voltage compatibility between the I/O expander and the various front-end components discovered while testing. While the expander functioned at a single logic level, several devices on the front end required different voltage domains for enable control, which complicated reliable system-wide configuration.
If given the opportunity to redesign this portion of the system, I would take one of two approaches:

- Option 1: Use a more flexible I/O expander — Specifically, I would select an SPI-based I/O expander capable of driving multiple output voltage levels (e.g., via internal level shifters or dual-supply configuration). This would reduce the need for discrete level-shifting circuitry and increase compatibility across mixed-voltage domains.
- Option 2: Eliminate the I/O expander entirely — Instead of introducing another layer of digital control, I would directly control all enable lines from the FPGA using its PMOD GPIOs. This approach simplifies the design, reduces potential points of failure, and ensures tighter timing control. In our application, the number of enable signals is relatively small, and the FPGA has enough available GPIOs to handle them.

Either of these approaches would have prevented the ambiguous SPI behavior we encountered and made debugging the digital control path more straightforward. Additionally, removing unnecessary intermediate devices would improve system reliability and make the platform easier for future students to understand and modify.

PC Interface

PC integration taught various lessons about the code development process. Engineers learned about the differences in how Windows and Linux operate, and how these differences can affect operation. Certain GNU Radio blocks will only operate properly on Linux. Overall GNU Radio performance is degraded on Windows. Additionally, the C code would not compile in a standard IDE or AMD Xilinx Vitis, the script to create an SD card image had to be used to compile.

FPGA Communications

A key lesson from this project was the importance of integrating software and hardware design, developing logic control through finite state machines (FSMs), managing data path behavior, and configuring external peripherals like the LO. Writing the C program that calculated and transmitted register configurations required a studying the LO's datasheet timing and register structure, as well as how that would be passed through SPI once configured. This experience reinforced how critical it is for software and hardware to follow a shared protocol—not just in timing but also in expectations around signal transitions, such as the load enable pulse and chip select control. On the logic side, FSMs were used to manage write sequencing, monitor lock-detect status, and interface with FIFO buffers and memory-mapped elements. This experience allowed us to learn that communication between subsystems was essential in ensuring correct signal control. Additionally, these challenges in coordinating signal naming, interface timing, and documentation across C code, VHDL, and schematic-level design led to integration issues and resulted in learning through debugging of the resulting problems.

Enclosure Fabrication

During the fabrication phase of the project, it was important to ensure that every component fits properly in the enclosure. Having a good design allows for simple manufacturing and assembly of components, but not everything works the first time. A major lesson learned was with the 3D printing of the walls. I didn't have a lot of experience with 3D printing before this semester, so that was a big learning curve. There are many slicing software options to create GCODE, and each printer has its own parameters that need to be inputted while using the software. I gained a lot of experience using multiple different 3D printers, print beds, and filament types. Additionally, I used a sheet metal bender in the ISL lab for the first time to bend the shielding into shape. While simple to use, it is very important to know exactly how to operate it as it can be very dangerous if used improperly.

13 Conclusions [A]

The QORVO_RADIO project represents a significant step toward developing a modular, reconfigurable SDR platform tailored for hands-on education at UNC Charlotte. Over the course of this two-semester effort, the team successfully designed and fabricated a custom RF front end, developed FPGA-based digital control, integrated the system with GNU Radio, and created a robust enclosure with modular expansion in mind.

While the analog signal chain powered on and initial testing validated impedance matching, clock distribution, and general power sequencing, final integration was limited by SPI control issues—specifically, the inability of the I/O expander and local oscillator to properly respond to MOSI-based register writes. As a result, full end-to-end RF signal reception through the custom front end could not be validated in this iteration. However, tests using a Pluto SDR in place of the front end confirmed that the digital signal path, including ADC digitization and audio playback via GNU Radio, functions correctly.

Despite the integration challenges, the project provides a validated and well-documented hardware and software foundation for future development. The enclosure, modular architecture, and educational focus ensure that the system can be expanded, debugged, and adapted by future teams. With continued refinement of SPI communication and control logic, the QORVO_RADIO platform is positioned to become a powerful learning tool for students exploring RF systems and wireless communication

14 References

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Travis F. Collins, Robin Getz, Di Pu, and Alexander M. Wyglinski. 2018. Software-Defined Radio for Engineers. Accessed 2024. https://www.analog.com/en/resources/technical-books/software-defined-radio-for-engineers.html.

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15 Appendices

[A]

TITLE: QORVO_RADIO_SOW
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD1_QORVO_RADIO_F24/REPORT, DOCUMENTS AND PROJECT PLAN/REPORTS

[B]

TITLE: TIMESHEET
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/REPORTS AND DOCUMENTS/PROJECT MANAGEMENT

[C]

TITLE: MEETING MINUTES
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/CORRESPONDENCE/ MEETING MINUTES

[D]

TITLE: EMAILS WITH QORVO
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/ CORRESPONDENCE/WEEKLY EMAILS

[E]

TITLE: BILL OF MATERIALS
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/BILL OF MATERIALS

[F]

TITLE: EXPO POSTER
AUTHOR: QORVO RADIO DESIGN TEAM

FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/ REPORTS AND DOCUMENTS

[G]

TITLE: PRP SLIDES
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/PRESENTATIONS/ DESIGN REVIEWS

[H]

TITLE: PSR SLIDES
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/PRESENTATIONS/ DESIGN REVIEWS

[I]

TITLE: BI-WEEKLY MEETING PRESENTATIONS
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/PRESENTATIONS

[J]

TITLE: PCB DOCUMENTATION
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/RESEARCH/ ELECTRICAL

[K]

TITLE: VHDL & C CODE
AUTHOR: QORVO RADIO DESIGN TEAM
FILE LOCATION: QORVO_RADIO/SD2_QORVO_RADIO_S25/COMPUTER CODE