University of North Carolina at Charlotte
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Qorvo Radio

SPI Memory-Mapped Module

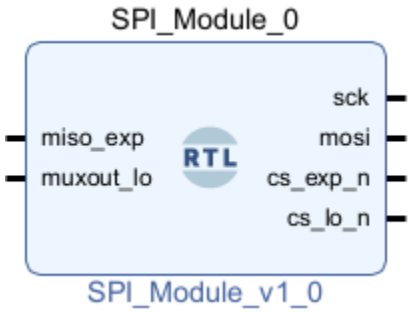

Figure 1-1 SPI Module Diagram

Contents

Module Overview

The **SPI_Module** VHDL entity is a legacy implementation providing direct, memory-mapped control for SPI-based communication with two peripheral devices: a Local Oscillator (LO) and an I/O Expander. This version predates the use of AXI Stream, utilizing explicit memory-mapped addresses to configure peripherals and manage SPI transactions.

Module Specifications

1. Inputs:

- `miso_exp` (std_logic): Master-In Slave-Out shared line for SPI peripherals.
- `muxout_lo` (std_logic): Lock detect signal from the LO chip.

2. Outputs:

- `s_axis_lo_tready` (std_logic): Indicates readiness to accept LO configuration data.
- `sck` (std_logic): SPI clock.
- `mosi` (std_logic): Master-Out Slave-In line.
- `cs_exp_n` (std_logic): Active-low Chip Select for Expander.
- `cs_lo_n` (std_logic): Active-low Chip Select for LO.

Memory-Mapped Interface

1. Local Oscillator Registers:

- LO_REG5_ADDR: `0x45000100`
- LO_REG4_ADDR: `0x45000104`
- LO_REG3_ADDR: `0x45000108`
- LO_REG2_ADDR: `0x4500010C`
- LO_REG1_ADDR: `0x45000110`
- LO_REG0_ADDR: `0x45000114`
- LO_START_ADDR: `0x45000118` (Write to initiate LO configuration)

2. Expander Configuration:

- EXP_DATA_ADDR: `0x45000120` (Lower 20 bits used for configuration)
- EXP_START_ADDR: `0x45000124` (Write to initiate Expander configuration)

Operational Description

1. Bus Write Operation:

- Writing data to the specified addresses configures LO registers or the Expander's 20-bit data field.
- Trigger signals (`lo_start_bit`, `exp_start_bit`) initiate SPI transactions when specific addresses receive data.

2. SPI Communication:

- The module contains separate controllers for LO and Expander configurations (`LO_Controller`, `Expander_Controller`).
- An `SPI_Master_8bit` handles the physical SPI transaction.
- An internal SPI arbiter prioritizes LO communication over Expander communication.

3. Bus Read Operation:

- Read operations from the bus provide feedback of the current register values for diagnostic or verification purposes.

Integration and Usage

- Instantiate in FPGA designs requiring direct memory-mapped SPI peripheral control.
- Connect external bus interface to specified memory addresses for control and status.
- Interface SPI signals (sck, mosi, miso_exp, chip selects) to respective hardware peripherals.