University of North Carolina at Charlotte
Department of Electrical and Computer Engineering

Qorvo Radio

Lock Detect AXI Stream Interface – No Trigger Version

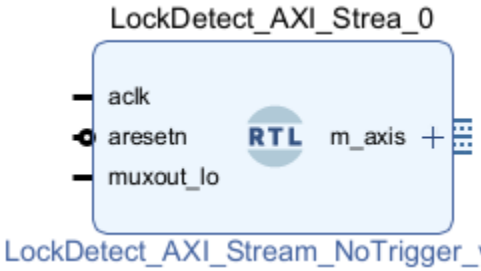

Figure 1-1 Lock Detect – No Trigger Module Diagram

Contents

Module Overview

The **LockDetect_AXI_Stream_NoTrigger** VHDL module interfaces the Lock Detect output (MUXOUT) from the Local Oscillator (LO) chip directly to the FPGA's AXI Stream interface. Unlike the Trigger Version, this module continuously monitors the lock detect signal, debounces it with multiple stable samples, and periodically transmits the lock status automatically, eliminating the need for a software trigger pulse. This functionality allows straightforward integration into continuous monitoring applications and higher-level software environments like GNU Radio.

Module Specifications

1. Inputs

- `aclk` (std_logic): AXI Stream clock input. Drives synchronous logic within the module.
- `aresetn` (std_logic): Active-low synchronous reset input. Resets internal states to default.
- `muxout_lo` (std_logic): Direct Lock Detect status signal from the LO chip (0 for unlocked, 1 for locked).

2. Outputs

- `m_axis_tvalid` (std_logic): AXI Stream validity signal. Indicates when output data is valid.
- `m_axis_tdata` (std_logic_vector(31 downto 0)): AXI Stream data output, embedding the Lock Detect status in the least significant bit.
- `m_axis_tready` (std_logic, input): AXI Stream ready signal from receiver, indicating readiness to accept data.

Operational Description

The module utilizes three main logic processes:

1. Debounce Lock Detection

- Continuously samples `muxout_lo`.
- Requires 16 consecutive high samples to consider the lock stable.
- Resets stability counter and status immediately if `muxout_lo` goes low at any point.

2. Periodic Tick Generation

- Generates a periodic tick approximately every 1 million clock cycles (frequency dependent on system clock), used as a periodic trigger to send lock status.

3. Continuous Lock Status Streaming

- On each periodic tick, the current debounced lock status is latched into `m_axis_tdata`.
- `m_axis_tvalid` is set high, signaling data availability.
- Waits for acknowledgment via `m_axis_tready` before clearing the valid signal.

Integration and Usage

- Instantiate within the FPGA block design.
- Connect AXI Stream outputs (m_axis_tvalid, m_axis_tdata) to the respective AXI Stream input on downstream modules or software interfaces.
- Continuously monitor AXI Stream data in GNU Radio or other software environments, interpreting the least significant bit of received data as the current lock status.
- No external trigger required; status is automatically updated at periodic intervals, ensuring constant lock state monitoring.