THE AMERICAN UNIVERSITY IN CAIRO

Digital Design II

Project I

Stick Diagrams

&

Estimated Cell Height

Mohamed A. Abdel Hamed

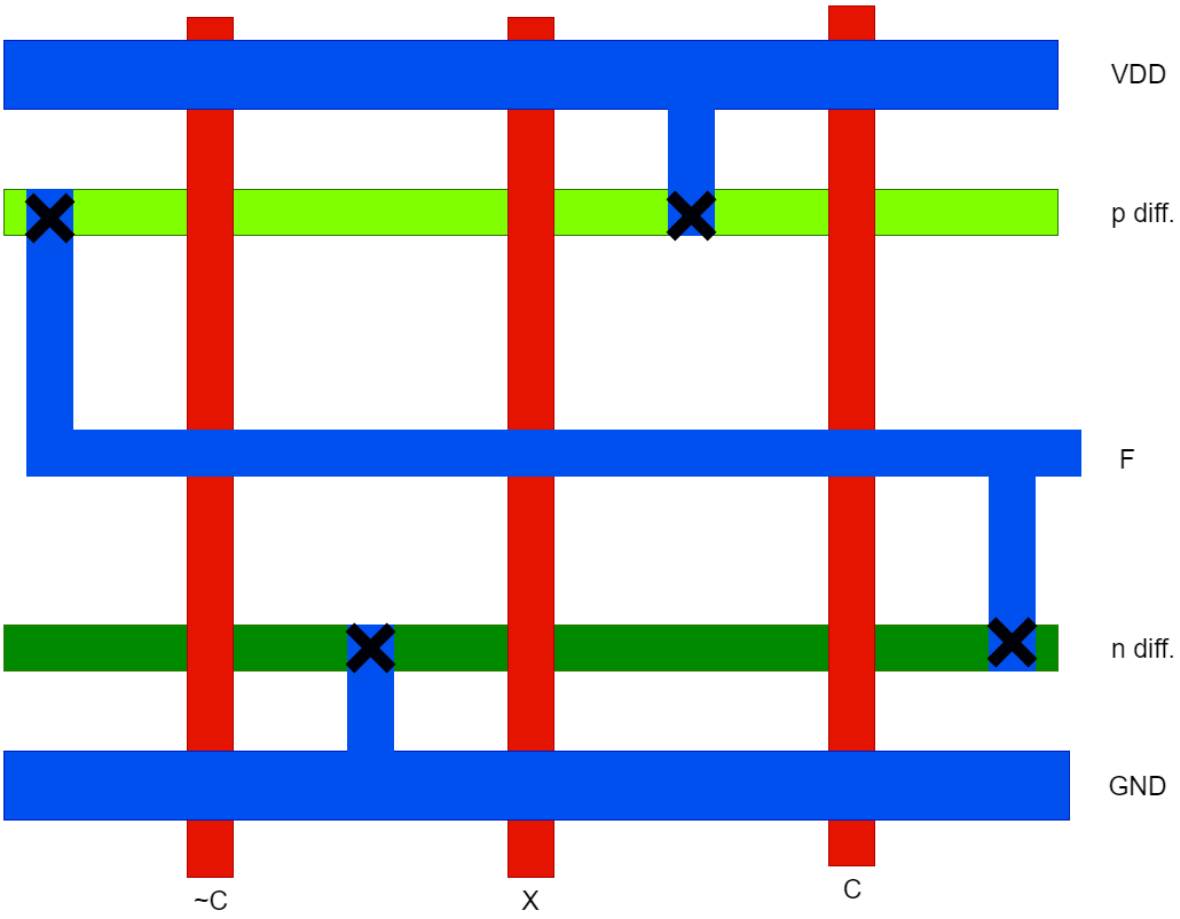
Fadi A. Dawoud

Eslam A. Soliman

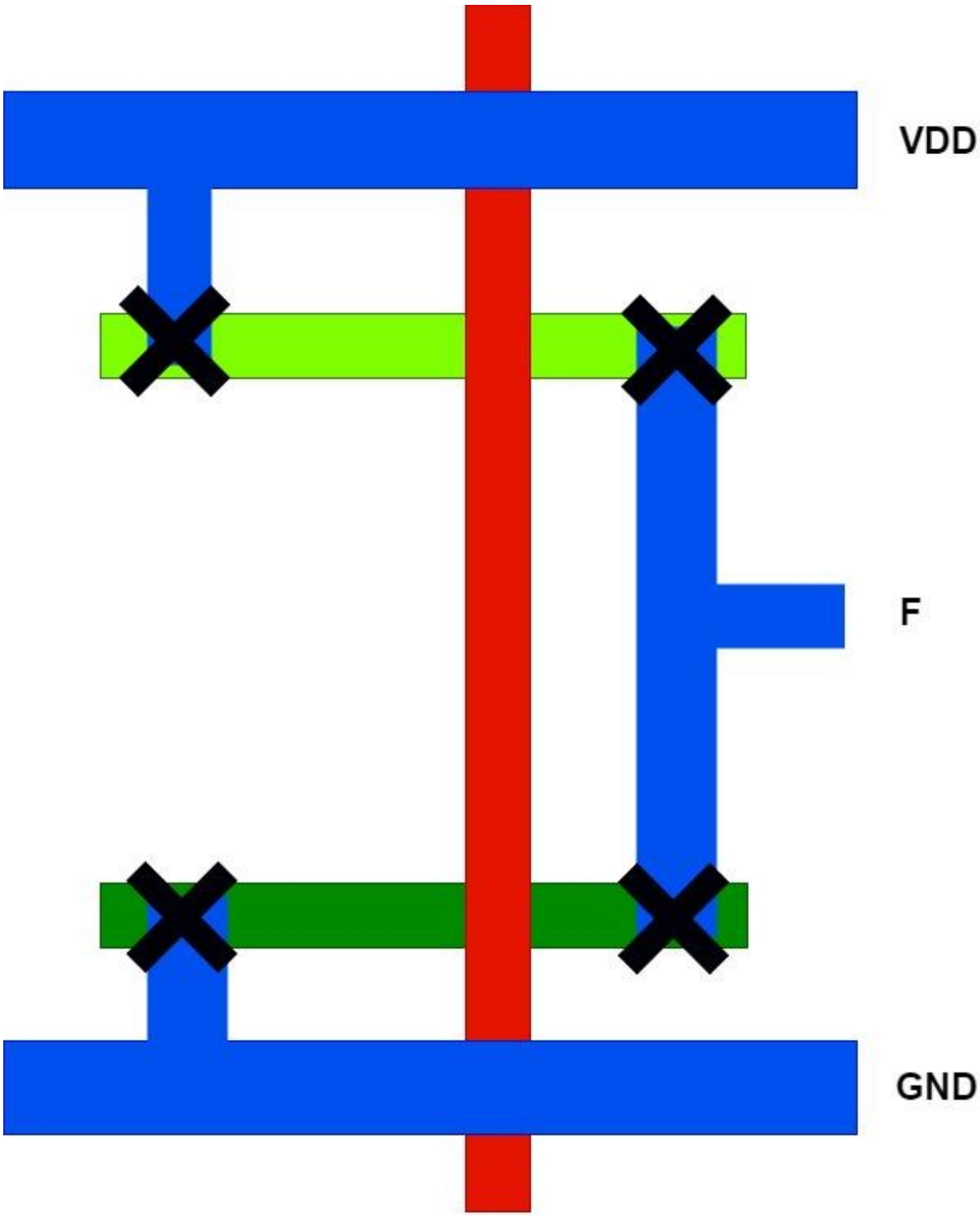
Dr. Mohamed Shalan

Stick Diagrams:

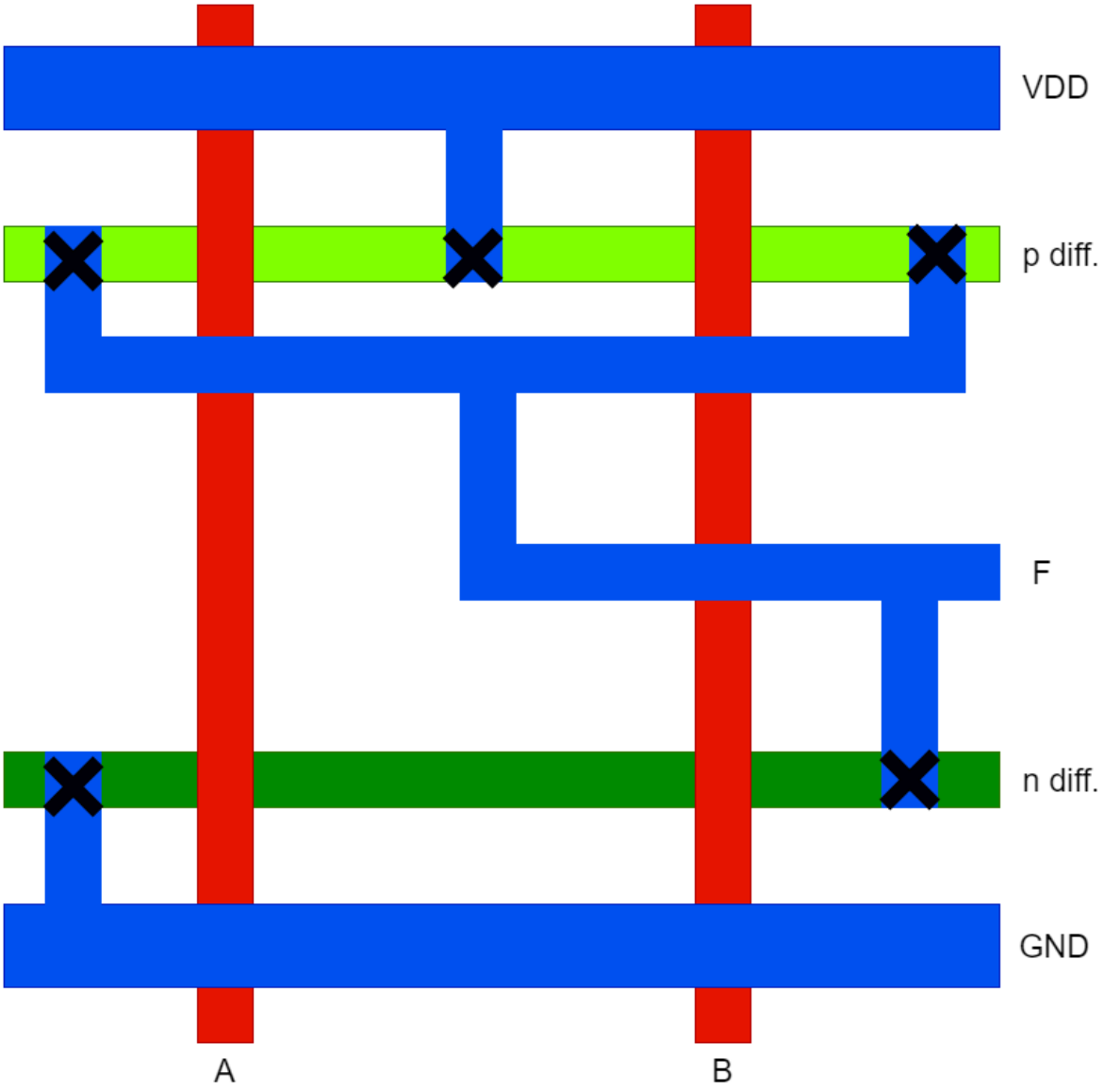
I. Tri state Inverter



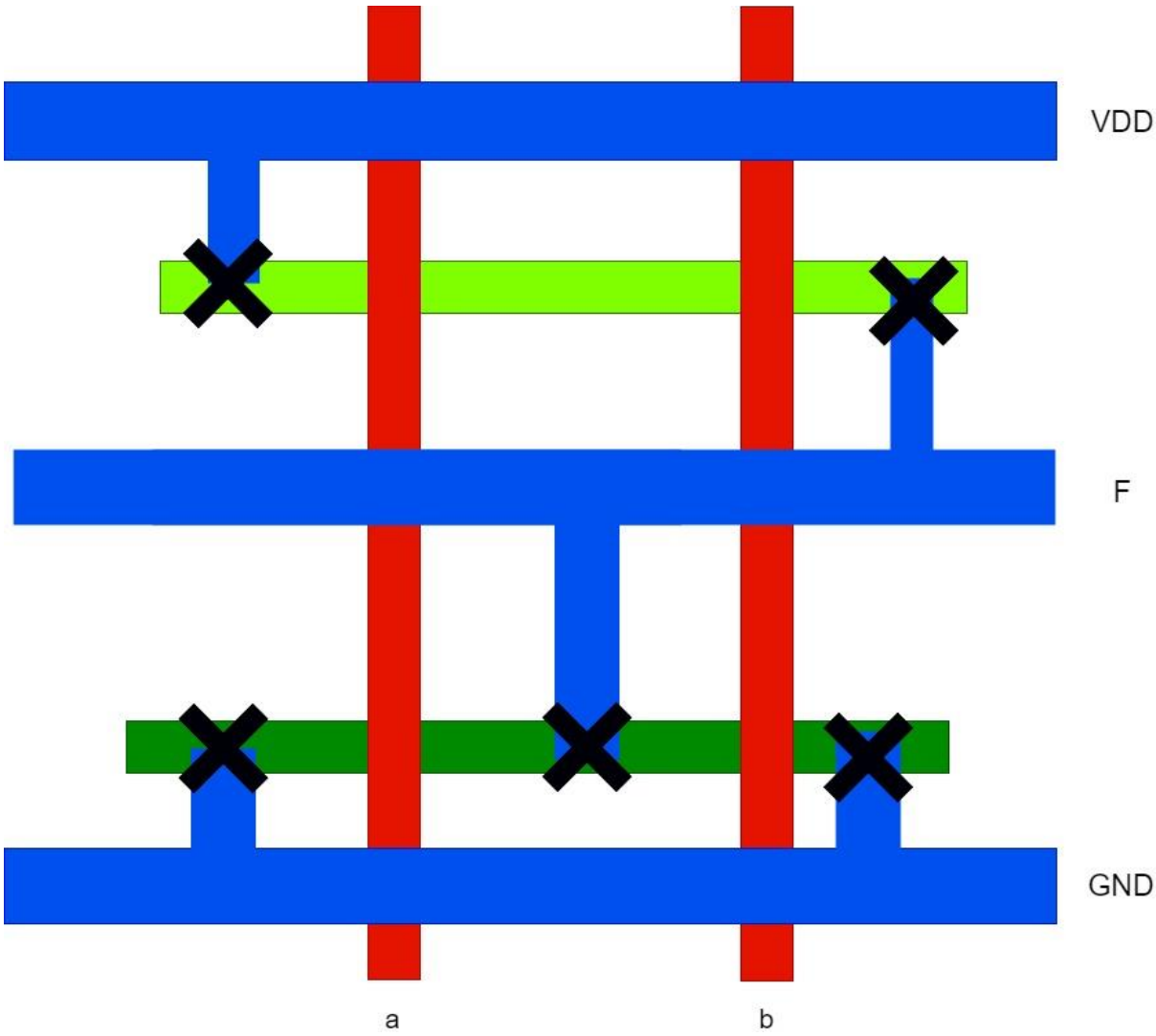
II. Inverter



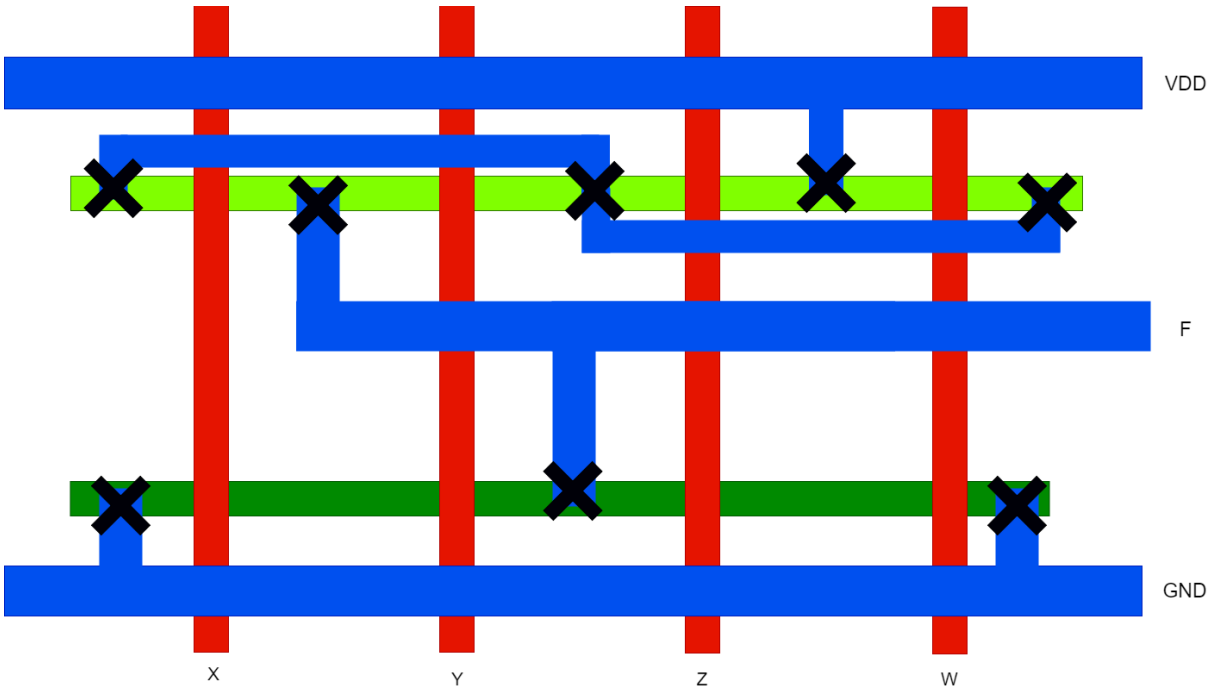
III. 2-input NAND



IV. 2-input NOR



V. The Complex Function f(x, y, z, w) = $\overline{xy + wz}$



Estimated Cell Height

By inspection of the five required cells and their sizes, the largest cell in height should be the inverter gate of size 8 since it has the tallest pull-up and pull-down networks:

$$pMOS\ network = 8 * K_p * minimum\ nMOS\ width$$

$$= 8 * 2.4 * 4\lambda = 76.8\lambda$$

$$nMOS\ network = 8 * minimum\ nMOS\ width$$

$$= 8 * 4\lambda = 32\lambda$$

Note that the above calculations do not include the needed spacing.

After doing the Layout of the x8 inverter while keeping spacing to the minimum, the cell height was $151\ \lambda$