THE AMERICAN UNIVERSITY IN CAIRO

Digital Design II

Project I

Stick Diagrams

&

Estimated Cell Height

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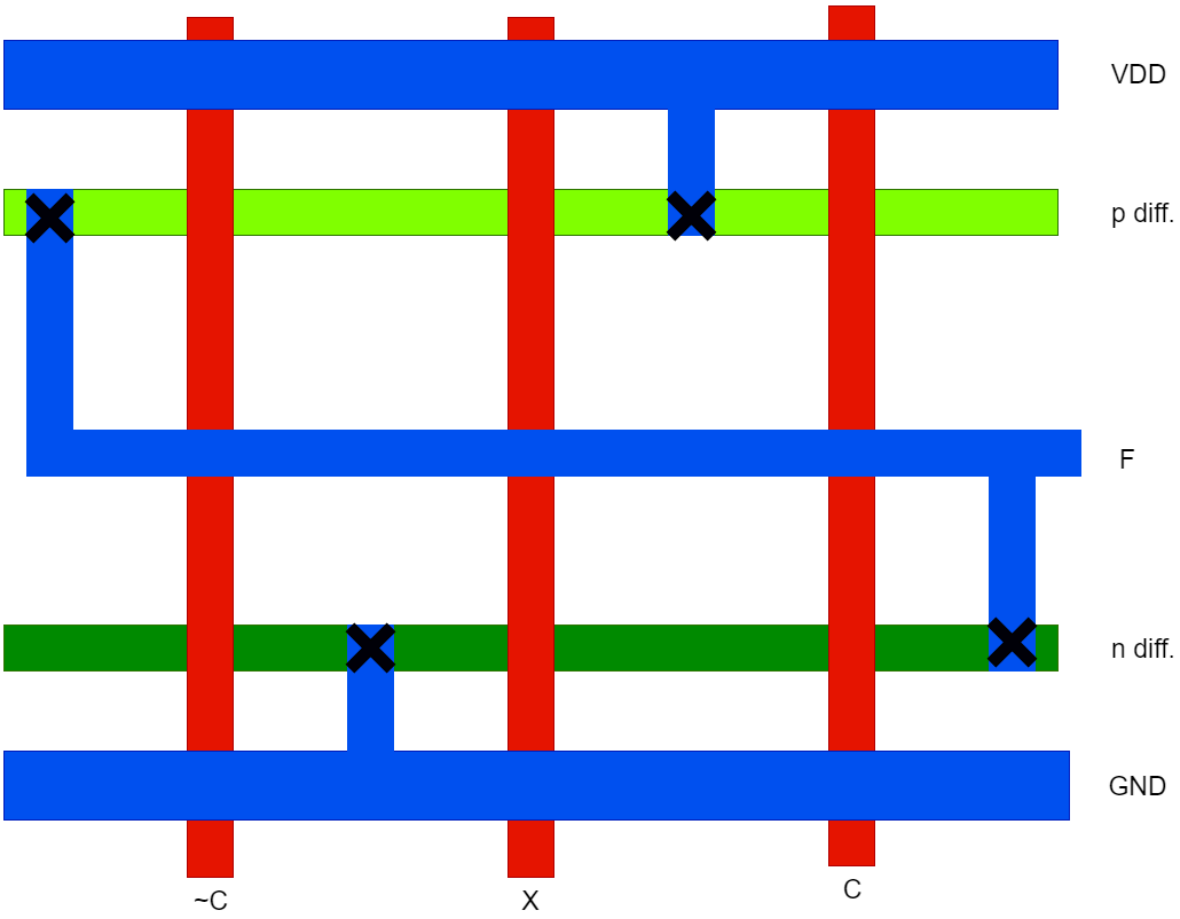
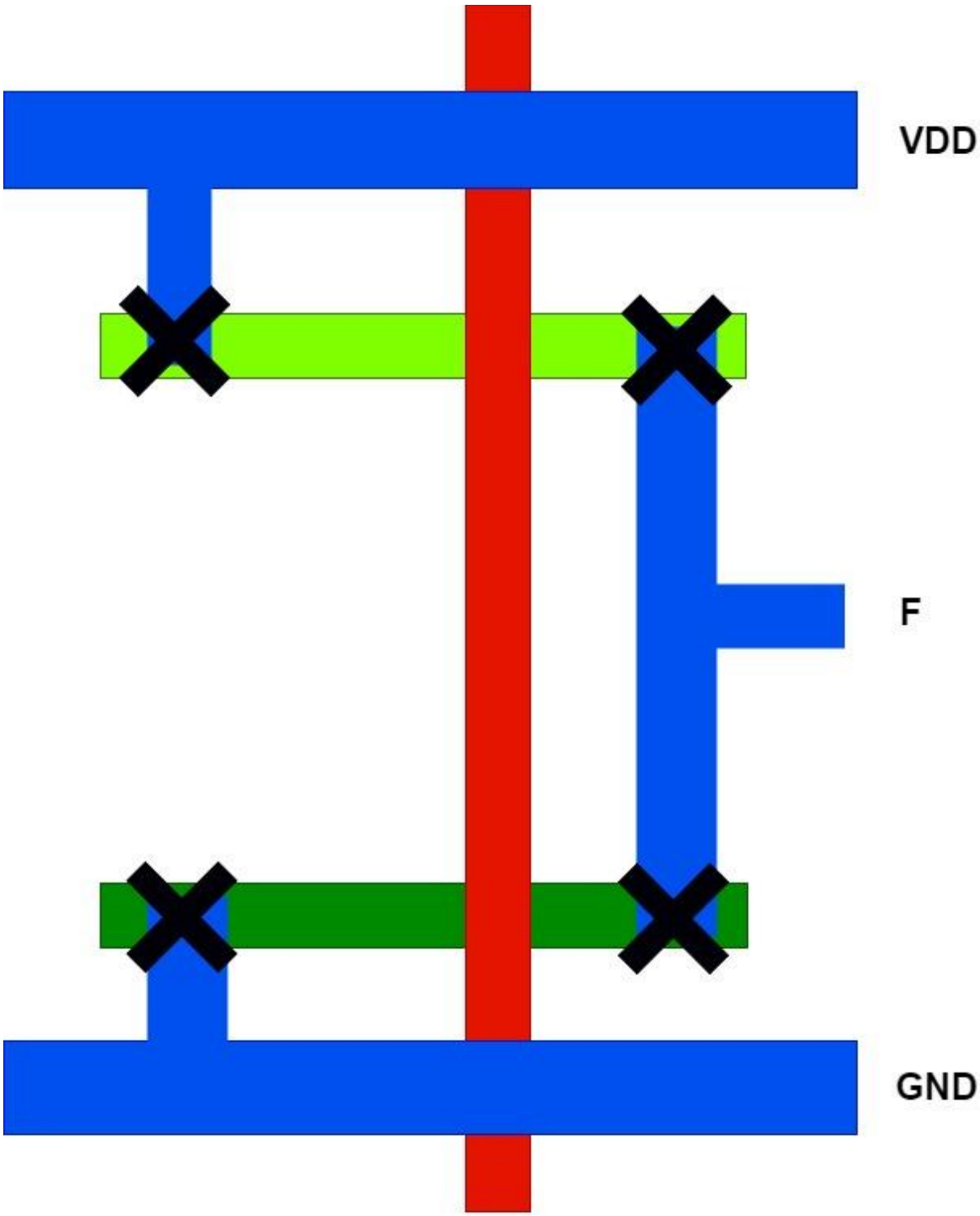
Stick Diagrams:

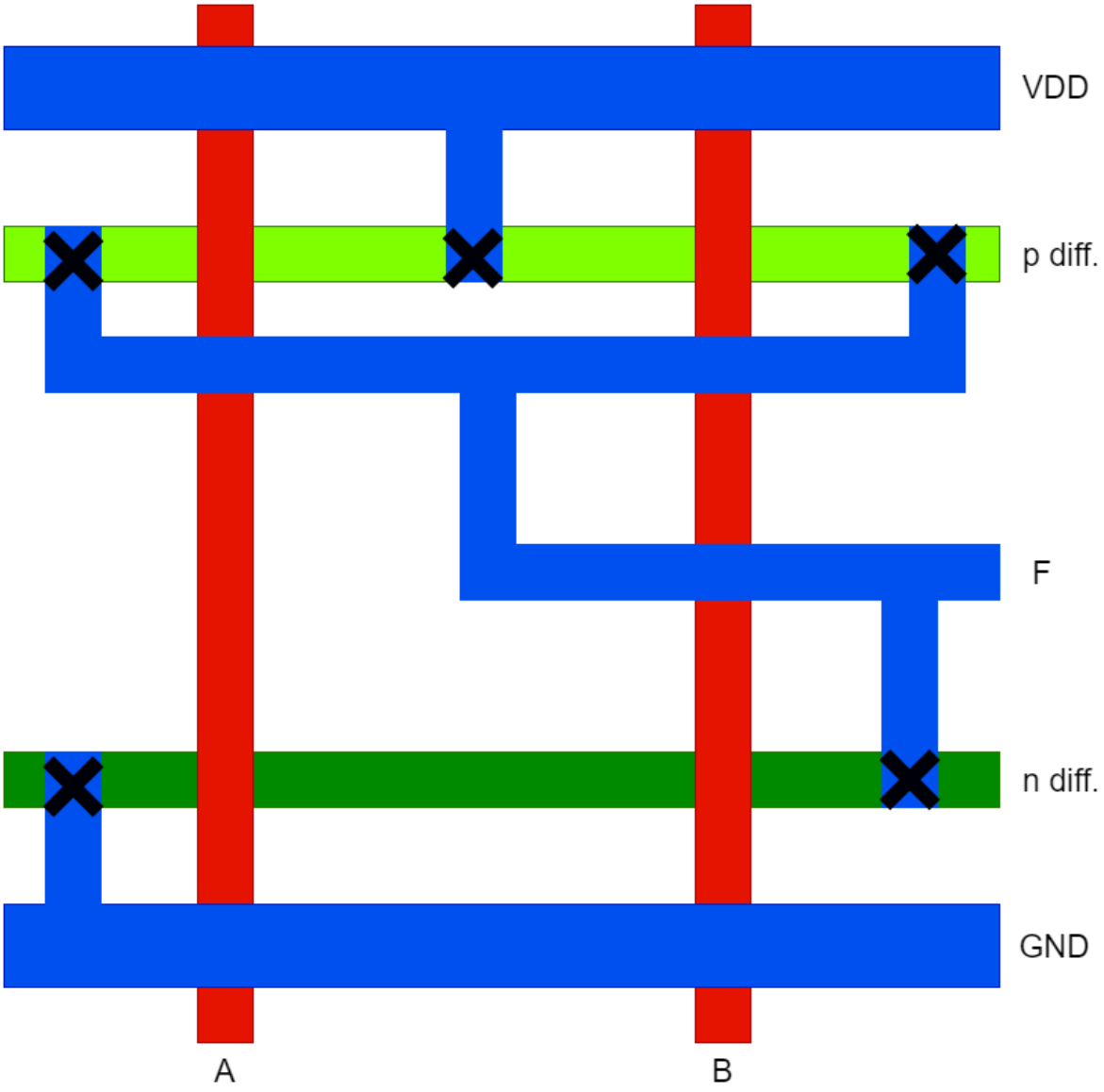
I. Tri state Inverter



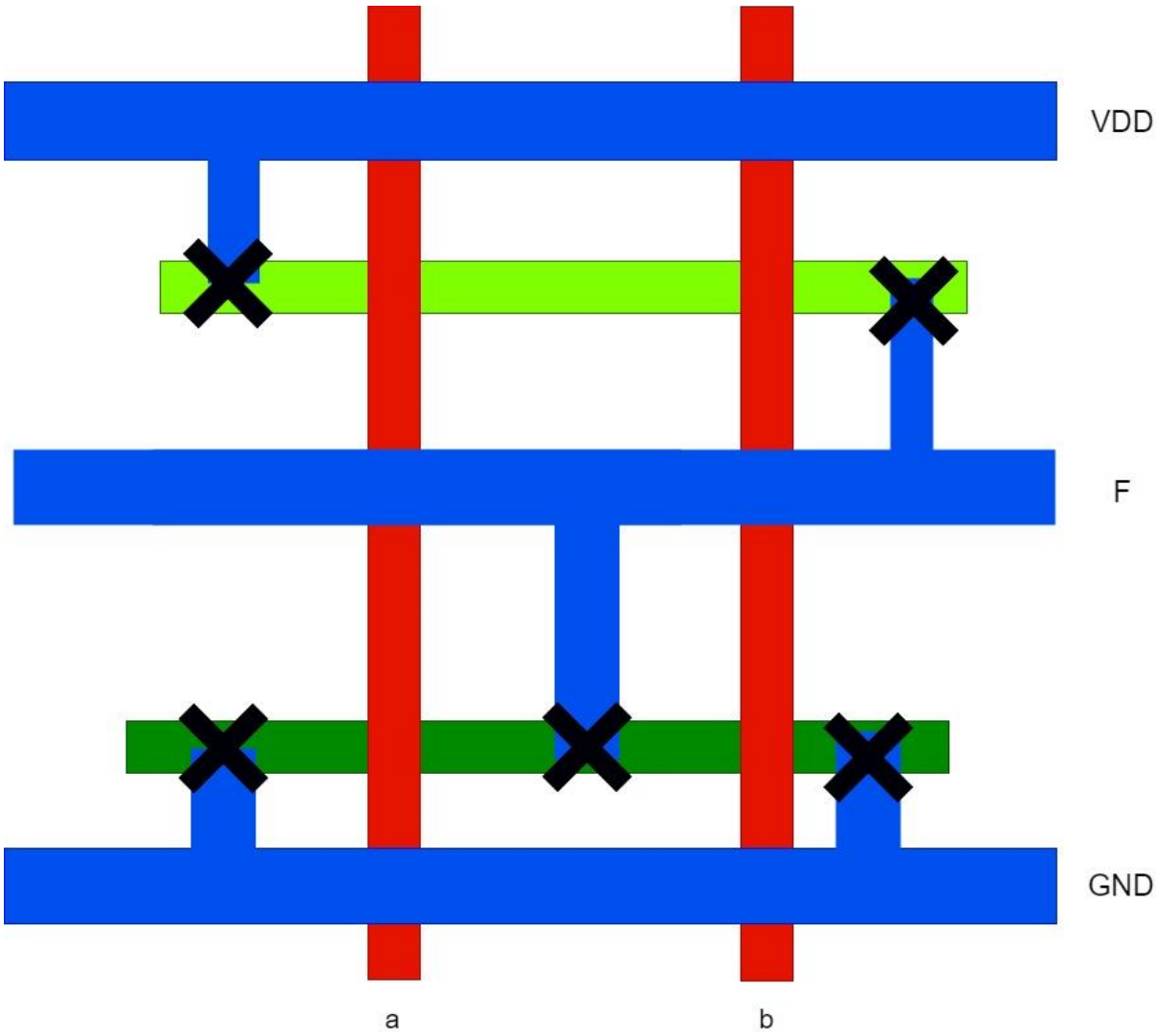
II. Inverter



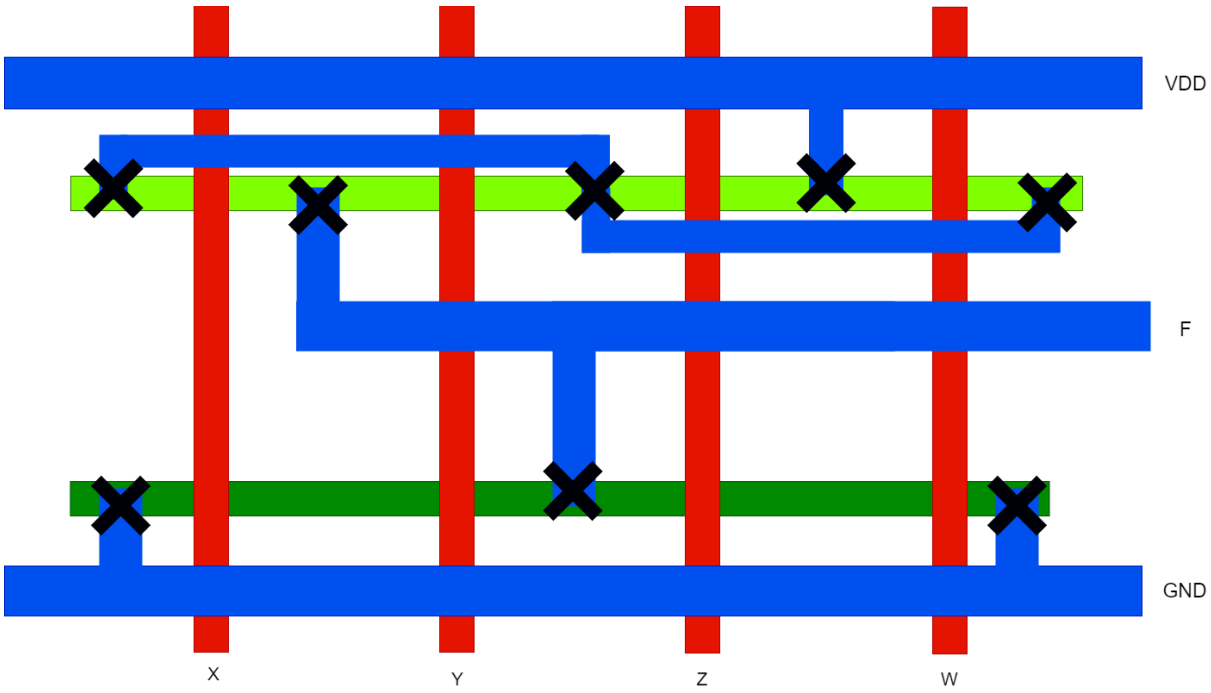
III. 2-input NAND



IV. 2-input NOR



V. The Complex Function f(x, y, z, w) = $\overline{xy + wz}$



Estimated Cell Height

Originally, the tristate inverter of size x8 should be the largest cell in terms of height; however, after compromising between cell height and width using Transistor folding, we settled for folding size x8 tristate inverter twice, which will approximately reduce its height to 1/3 of its original one. Also, folding the size x4 tristate inverter should roughly halve its height. In doing so, in addition to folding size x8 inverter once, the largest cell should be NOR2x4 with the following specs in terms of pull-up and pull-down networks' heights:

$$pMOS\ network = 2 * 4 * K_p * minimum\ nMOS\ width$$

$$= 2 * 4 * 2.4 * 4\lambda = 76.8\lambda \approx 77\lambda$$

$$nMOS\ network = 4 * minimum\ nMOS\ width$$

$$= 4 * 4\lambda = 16\lambda$$

Note that the above calculations do not include the needed spacing.

After doing the Layout of the NOR2x4 while keeping spacing to the minimum, the cell height was $135\ \lambda$