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what is the maximum number allowed of nesting interrupt in arm cortex m4?

In the ARM Cortex-M4 processor, the maximum number of allowed nested interrupts is determined by the implementation of the Nested Vectored Interrupt Controller (NVIC) in the microcontroller device. The NVIC is responsible for managing and prioritizing interrupts in the Cortex-M4 core.

The number of interrupt channels and the maximum level of nesting supported can vary between different microcontrollers that utilize the Cortex-M4 core. While the Cortex-M4 core itself supports up to 256 interrupt channels, the actual number of available channels and nesting levels may be limited in specific microcontroller implementations.