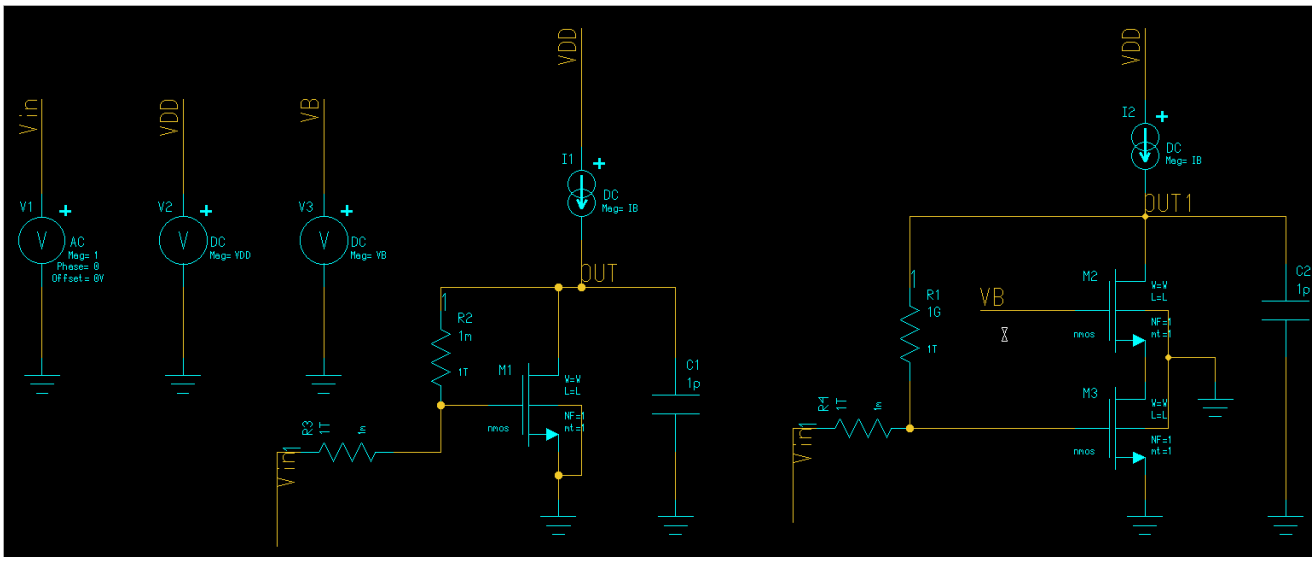
Analog IC Design
Lab 03
Cascode Amplifier

In this lab you will investigate the biasing, gain, bandwidth, and GBW product of cascode amplifier.

Part 1: Sizing Chart

a) Before going into the cascode amplifier design, we will create a sizing chart to help us in choosing the width of every transistor.
b) Create a test bench using a diode connected NMOS (W is a parameter and $L = 0.5\mu m$) biased by an ideal current source of $I_B = 20\mu A$. Run DC sweep for W = $1\mu m$: $1\mu m$: $20\mu m$.
c) Plot vth_d and vdss overlaid on the same figure. Use the following commands:
   - .plot dc s(M1->vth_d)
   - .plot dc s(M1->vdss)
d) Choose W such that vdss = 100mV.
e) Note that if we use higher current, we simply multiply W by the ratio between the new current and I_B that we used in this testbench (I_D is always proportional to W).

Part 2: Cascode for Gain



1. OP Analysis

a) Construct the circuit shown above. Use $I_B = 20\mu A$, $L = 0.5\mu A$, W as selected in Part 1, and $C_L = 1pF$.
b) Choose V_B (the cascode device bias voltage) such that M3 has $V_{DS} \approx vdss + 100mV$.
c) Note that the output node is a high impedance node; thus, it is difficult to control its DC voltage. As a workaround in simulation, we use a feedback loop and resistors with different resistances in DC/AC to change the circuit connections in DC/AC simulations (use the AC property in ideal resistor). The input device is diode connected for DC simulation, while in AC simulation the feedback is

disconnected and the AC input source is connected. We will study how to do biasing practically later in this course inshaAllah.

d) Simulate the DC OP point of the above CS and cascode amplifiers. Report the following parameters in a table.

	M1	M2	M3
vgs			
vth			
vdss			
vth_d			
vds			
region			
gm			
gmb			
gds			
cgs			
cgd			
csb			
cdb			

e) Check that all transistors operate in saturation.
f) Do all transistors have the same vth? Why?
g) What is the relation $(<, \ll, =, >, \gg)$ between gm and gmb?
h) What is the relation $(<, \ll, =, >, \gg)$ between cgs and cgd?
i) What is the relation $(<, \ll, =, >, \gg)$ between csb and cdb?
j) Report the schematics of CS and cascode amplifiers with DC node voltages clearly annotated.

2. AC Analysis

a) Perform AC analysis (1Hz:1GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.
b) Use the following expressions in the command to quickly calculate circuit parameters. To access the results, open the file that has .aex extension from AMS Results Browser (terminal >> amsrb).
   - EXTRACT AC LABEL=bandwidth 'CROSSING(VDB(OUT), Max(VDB(OUT))-3)'
   - EXTRACT AC LABEL=Gain (Max(VDB(OUT)))
   - EXTRACT AC LABEL=GBW ('CROSSING(VDB(OUT), 0)')
c) Report the Bode plot (magnitude) of CS and cascode appended on the same plot.
d) Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.
e) Report a table comparing the DC gain, BW, and GBW of both circuits from simulation and hand analysis.
f) Comment on the results.

Part 3: Cascode for BW

1. OP Analysis

a) Create a new cell and schematic. Copy the old schematic instances to the new one. Make the following modifications: remove the feedback, remove C_L, replace the current source with a resistor RD, make the signal source resistance $= 100k\Omega$. Set VGS = vth + vth_d as calculated in Part 2.
b) Choose RD such that the voltage drop on it is $\approx \frac{2}{3}V_{DD}$.
c) Choose V_B (the cascode device bias voltage) such that M3 has $V_{DS} \approx vdss + 100mV$.

d) Note that the DC voltage of the output node is set by the resistance (RD); thus, we don't need a feedback loop as in the previous case.

e) Simulate the DC OP point of the above CS and cascode amplifiers. Report the following parameters in a table.

	M1	M2	M3
vgs			
vth			
vdss			
vth_d			
vds			
region			
gm			
gmb			
gds			
cgs			
cgd			
csb			
cdb			

f) Check that all transistors operate in saturation.

g) Report the schematics of CS and cascode amplifiers with DC node voltages clearly annotated.

2. AC Analysis

a) Perform AC analysis (1Hz:1GHz, logarithmic, 10points/decade) to simulate gain and bandwidth.

b) Use the following expressions in the command to quickly calculate circuit parameters. To access the results, open the file that has .aex extension from AMS Results Browser (terminal >> amsrb).
   - EXTRACT AC LABEL=bandwidth 'CROSSING(VDB(OUT), Max(VDB(OUT))-3)'
   - EXTRACT AC LABEL=Gain (Max(VDB(OUT)))
   - EXTRACT AC LABEL=GBW ('CROSSING(VDB(OUT), 0)')

c) Report the Bode plot (magnitude) of CS and cascode appended on the same plot.

d) Using small signal parameters from OP simulation, perform hand analysis to calculate DC gain, BW, and GBW of both circuits.

e) Report a table comparing the DC gain, BW, and GBW of both circuits from simulation and hand analysis.

f) Comment on the results.