Analog IC Design
Lab 02
Common Source Amplifier

1. Amplifier Design

a) We would like to design a resistive loaded CS amplifier. First, we will create a design chart to help in the design process.

b) Create a testbench for an NMOS transistor similar to the NMOS characterization testbench that you used in Lab 01. Use $W = 10\mu m$ and $L = 2\mu m$.

c) Sweep VGS from 0 to 0.7V with 10mV step. Set $V_{DS} = \frac{1}{3}V_{DD}$.

d) Report the following parameters vs VGS:
   a. vdss and vth_d overlaid on the same plot (vdss is the drain-source saturation voltage, i.e., VDS > vdss for saturation. It is equivalent to V_{ov} for a square-law device. It is also known as vdsat. vth_d is equal to $V_{ov} = V_{GS} - V_{TH}$)
   b. ID

e) What is the relation between vdss and vth_d? Why?

f) Find the point at which vdss = 100mV. Report VGS, vth_d, and ID at this point. We will use these parameters for our amplifier.

g) Choose RD (the resistive load) such that the voltage drop across it is roughly $\frac{2}{3}V_{DD}$.

2. OP Analysis

a) Create a testbench for the resistive loaded CD amplifier using the VGS and the RD that you got from the previous part.

b) Simulate the DC OP. Report the following parameters in a table:
   - vgs
   - vth
   - vth_d
   - vdss
   - vds
   - region (region is one of the small signal parameters of the transistor model)
   - gm
   - gds

c) What is the relation ($<, \ll, =, >, \gg$) between vth_d and (vgs – vth)? Why?

d) What is the relation ($<, \ll, =, >, \gg$) between vth_d and vdss? Why?

e) What is the relation ($<, \ll, =, >, \gg$) between vds and vdss? What is the operating region? Why?

f) What is the relation ($<, \ll, =, >, \gg$) between gm and gds?

g) What is the intrinsic gain?

h) Calculate the amplifier gain analytically. What is the relation ($<, \ll, =, >, \gg$) between the amplifier gain and the intrinsic gain?

i) Report a snapshot of the amplifier with DC voltages annotated.

3. Gain Non-Linearity

a) Perform a DC sweep for the input voltage from 0 to V_{DD} with 2mV step.

b) Report VOUT vs VIN. Is the relation linear? Why?

c) Calculate the derivative of VOUT using the calculator. The derivative is itself the small signal gain. Is the gain linear (independent of the input)? Why?
d) Apply a transient stimulus (sine wave of 1kHz frequency and 10mV amplitude superimposed on the DC input voltage). Run transient simulation for 2ms. Plot gm vs time using this command ".plot tran S(M1->gm)". Does gm vary with the input signal? What does that mean?
e) Is this amplifier linear? Comment.

4. Maximum gain

a) We want to find RD that will give max gain. Run a nested DC sweep (not a parametric sweep) with VIN as the primary variable and RD as the secondary variable.
b) Report the derivative of VOUT (i.e., the gain) vs VIN with RD as a parameter. You should adjust the sweep range of RD such that the max gain (the peak) increases with RD then decreases again.
c) Use .EXTRACT command to plot the max gain vs RD.
d) What is the value of RD that gives the highest gain? What is the highest gain?
e) Find an analytical expression for the highest gain while ignoring ro. Compare with the simulated max gain. Is scaling down the supply voltage good for gain? Comment.