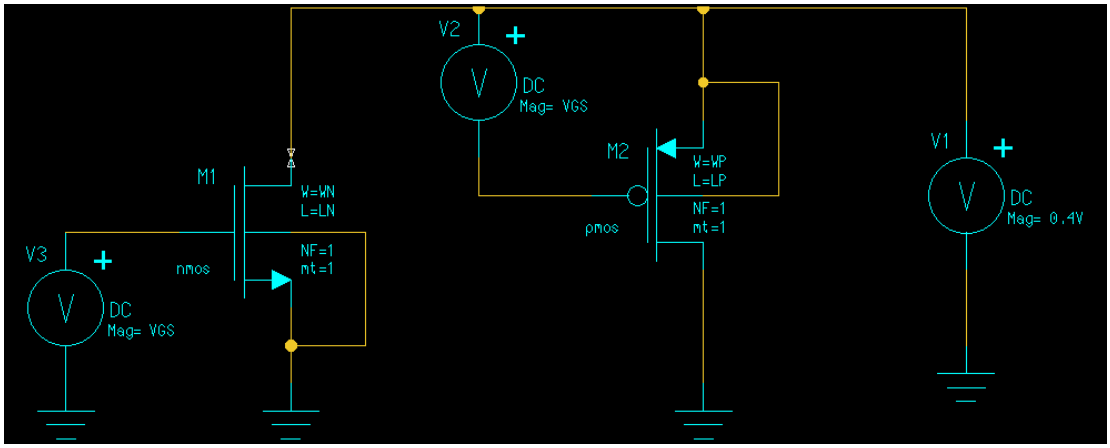
Analog IC Design
Lab 04
Common Drain Frequency Response

CD amplifier may suffer from ringing in time domain (and peaking in frequency domain) when driving large capacitive loads. The ringing problem becomes worse when the source resistance (Rsig) is large. In this lab we will investigate this problem. We use PMOS CD to avoid body effect.

Part 1: Sizing Chart

a) First, we will create a design chart to help in the design process as shown below. **We will use the PMOS only in this lab.**



b) Use $W = 10\mu m$ and $L = 1\mu m$.

c) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = 0.4V$.

d) For the PMOS, report the following parameters vs VGS:
   a. vdss (vdss is the drain-source saturation voltage, i.e., VDS > vdss for saturation. It is equivalent to V_{ov} for a square-law device. It is also known as vdsat).
   b. ID

e) Place a cursor on the point at which vdss = 100mV. Report ID at this point (let's refer to it as IDx).

f) I_D is always proportional to W. We want to design our amplifier for ID = $10\mu A$. Calculate the corresponding W.

W	ID
$10\mu m$	IDx
?	$10\mu A$

Part 2: CD Amplifier

1. OP (Operating Point) Analysis

a) Create a new schematic for the CD amplifier. Use a PMOS and use a $10\mu A$ ideal current source for biasing (note that the current source will be connected to the source terminal). Connect the source to the bulk. Use $L = 1\mu m$ and W as determined in Part 1. Use $C_L = 2pF$, $R_{sig} = 2M\Omega$, and a DC input voltage = 0V.

b) Simulate the OP point. Report the following parameters in a table.

	M1
vgs	
vth	
vdss	
vds	
region	
gm	
gds	

c) Check that the transistor operates in saturation.

2. AC Analysis

a) Perform AC analysis to investigate the frequency domain peaking. Use logarithmic sweep with 20 points per decade.
b) Report the Bode plot magnitude.
c) Do you notice frequency domain peaking? Use the following expression to calculate the peaking in dB (open the .aex file from amsrb):
   - .EXTRACT AC LABEL= Peak(Max(VDB(OUT)))
d) Analytically calculate the input and output poles (use approximate expressions). What is the relation between the poles? Comment.
e) Perform parametric sweep: CL = 20f, 200f, 2p.
   - Report Bode plot magnitude overlaid on same plot.
   - Report the peaking vs CL. Use this command: .PLOT EXTRACT(Peak)
   - Comment.
f) Perform parametric sweep: Rsig = 20k, 200k, 2M.
   - Report Bode plot magnitude overlaid on same plot.
   - Report the peaking vs Rsig.
   - Comment.

3. Transient Analysis

a) Use vsource as your transient stimulus and set it as follows (delay = 2us, initial = 0V, period = 8us, pulse_value = 100mV, t_fall = 1ns, t_rise = 1ns, width = 4us). Run transient analysis (max step = 10n) for 10us to investigate the time domain ringing.
b) Report Vin and Vout overlaid vs time.
c) Calculate the DC voltage difference (DC shift) between Vin and Vout.
   - What is the relation between the DC shift and VGS?
   - How to shift the signal down instead of shifting it up?
d) Do you notice time domain ringing? Use the overshoot function to calculate the maximum overshoot as a percentage (replace Vfinal and Vstep with the actual numbers from simulation):
   - .EXTRACT TRAN LABEL=overshoot abs((MAX(V(OUT)) -Vfinal)/Vstep)*100
e) Perform parametric sweep: CL = 20f, 200f, 2p.
   - Report Vout vs time overlaid on same plot.
   - Report the overshoot vs CL. Use this command: .PLOT EXTRACT(overshoot)
   - Comment.
f) Perform parametric sweep: Rsig = 20k, 200k, 2M.
   - Report Vout vs time overlaid on same plot.
   - Report the overshoot vs Rsig.
   - Comment.

4. Z_{out} (Inductive Rise)

a) Replace CL with an AC current source with magnitude = 1.
b) Perform AC analysis (1Hz:10GHz, 20points/decade). The voltage across the current source is itself the output impedance.
c) Plot the output impedance (magnitude and phase) vs frequency. Do you notice an inductive rise? Why?
d) Does Z_{out} fall at high frequency? Why?
e) Analytically calculate the zeros, poles, and magnitude at low/high frequency for Z_{out}. Compare with simulation results in a table.

5. How to solve the peaking/ringing problem?

f) Place the input/output poles away from each other (as we did when we swept CL and Rsig).
g) A compensation network can be used to compensate for the negative input impedance and prevent overshoots. See [Johns and Martin, 2012] Section 4.4 for more details.