وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog IC Design

Lecture 01
Introduction

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Faculty of Engineering
Ain Shams University

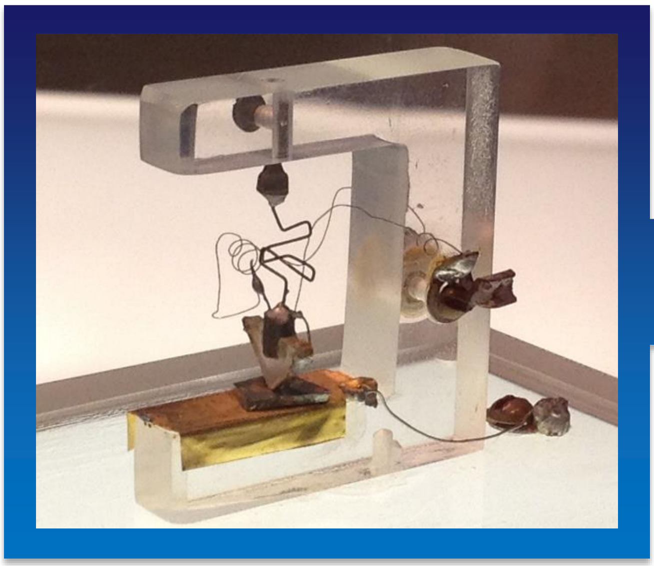
Introduction

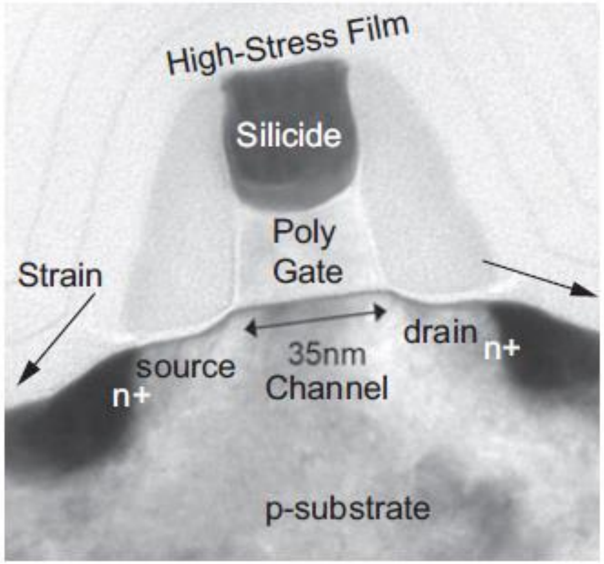
ENIAC, U.S. Army, 1946
Size → Large hall (> 150m^2)
Power Consumption ≈ 150kW

Smart phone, 2016
Size → Your pocket
Power consumption < 1W

Electronics All Around Us

Transistor Evolution

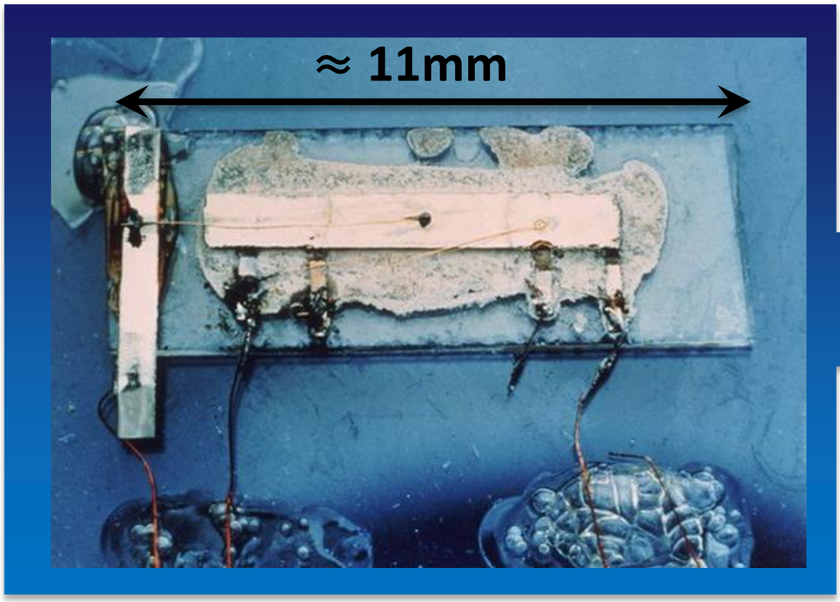


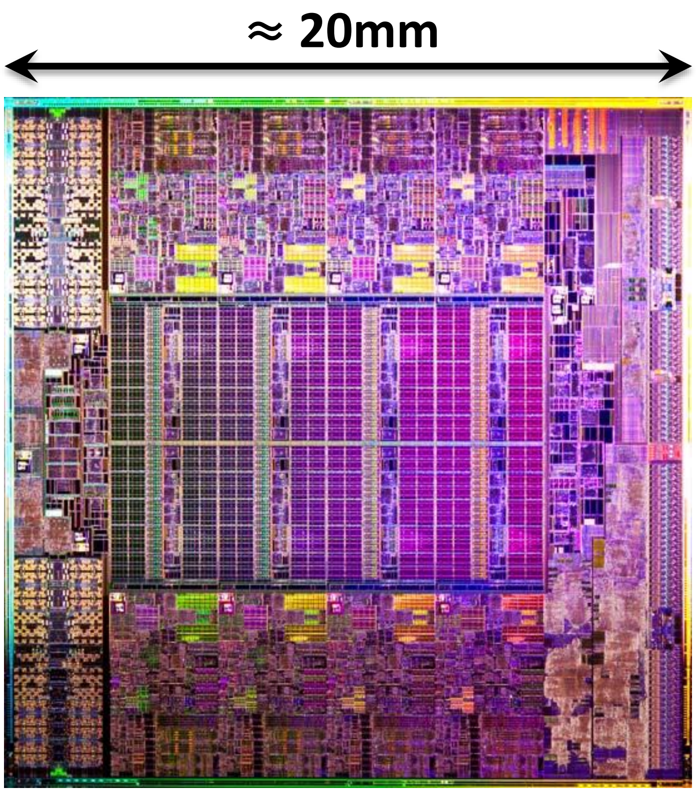


First transistor
Emitter and Collector contacts
separation ≈ 100μm
Bell Labs, 1947

Modern MOSFET
Effective channel
length ≈ 35nm
Intel, 2006

Integrated Circuit Evolution

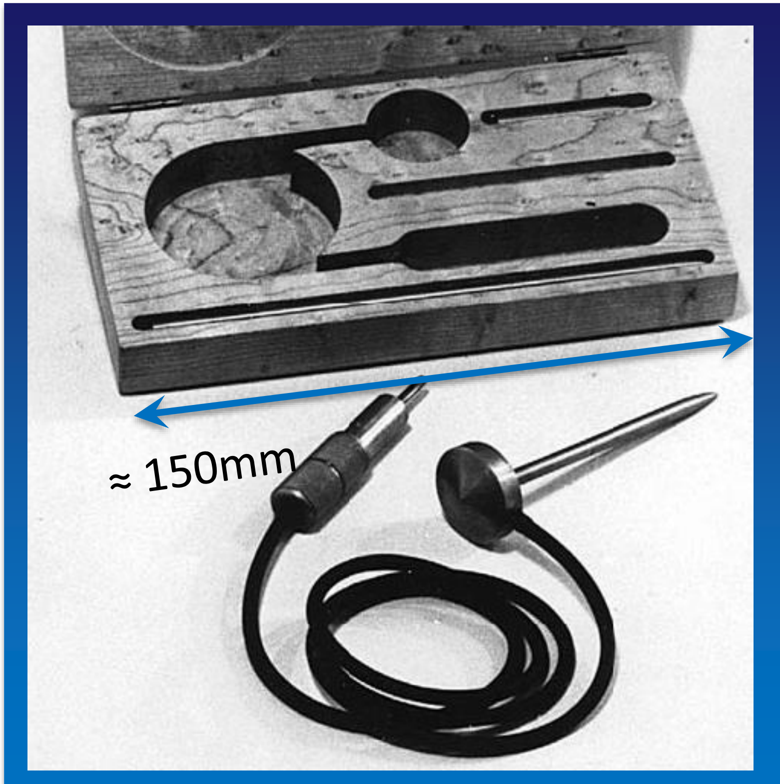




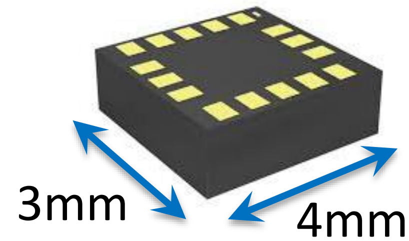
First IC
Only one transistor!
Texas Instruments (TI), 1958

Xeon E5 Microprocessor
2.26 billion transistors!
Intel, 2012

Sensing Microsystems



First accelerometer
B&K, 1940s
Simple bulky transducer
Acceleration → Voltage



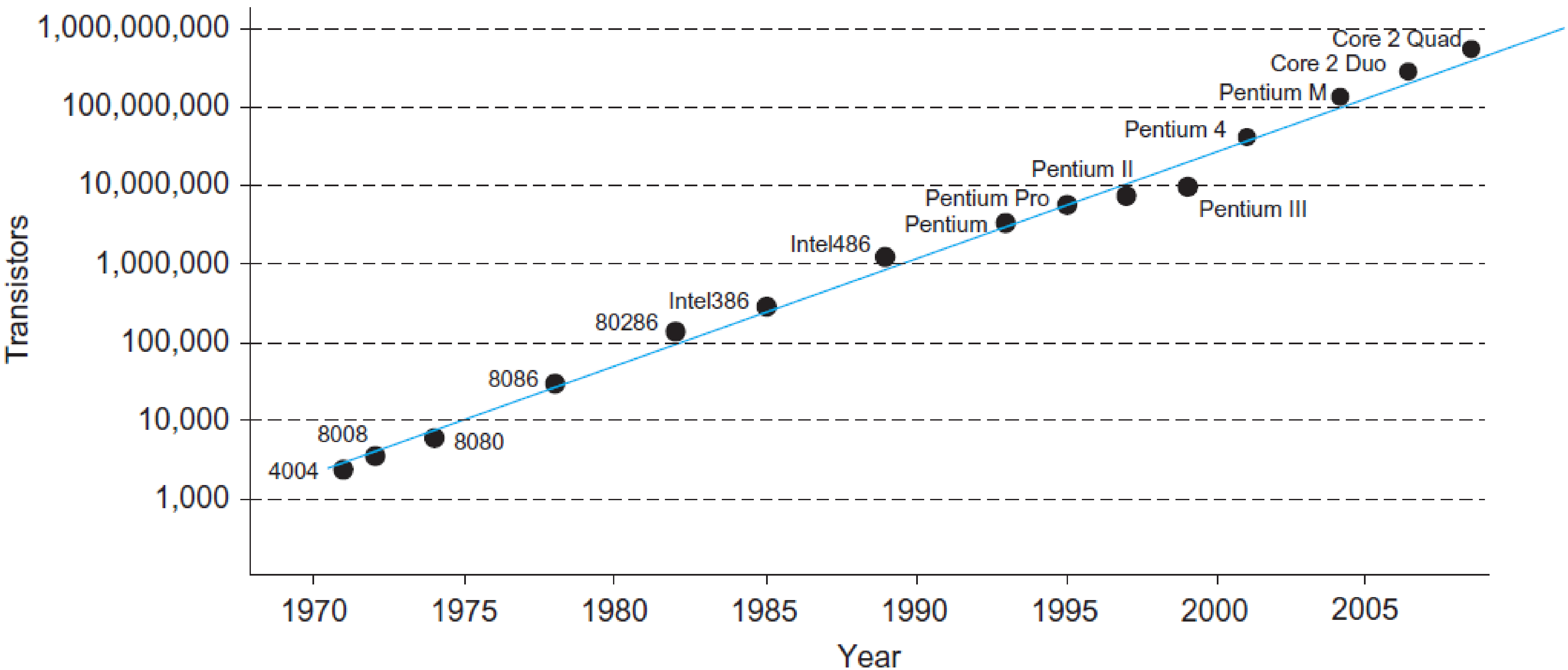
ADXL350
Analog Devices, 2012
Complete system on a tiny chip

- 3-axis MEMS* accelerometer
- Interface electronics
- Analog-to-digital conversion
- Memory
- Control logic
- Power management
- Digital interface

*MEMS = Micro-Electro-Mechanical Systems

Moore's Law

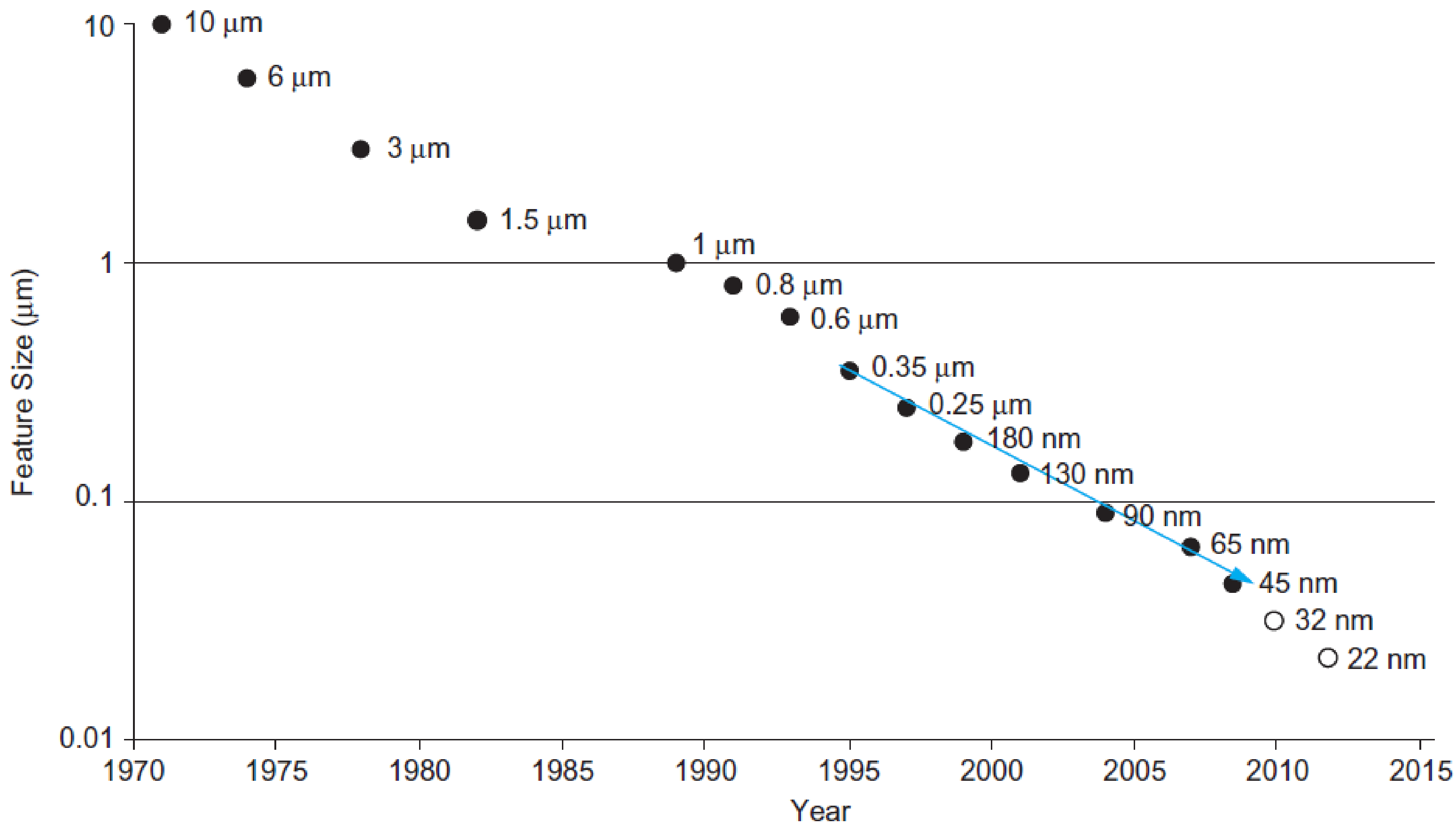
- Moore's law [1965]: Transistor count doubles every 18 months
- Practically: It doubled every 26 months since the 4004 [1970s]
- At the end of the day: It is exponential!



[Weste and Harris, 2010]

Technology Minimum Feature Size

- Minimum feature size shrinking 30% ($\approx 1/\sqrt{2}$) every 2-3 years
  - Transistor area (and cost) are reduced by a factor of 2
- Device scaling brings new challenges in analog design



[Weste and Harris, 2010]

Modern "Moore" Concepts

- **More Moore**
  - Further miniaturization of transistor
  - New materials for performance enhancement (HK, SOI, III-V)
  - High throughput conventional lithographic limitations
- **More than Moore**
  - Adding functionalities **not** associated with transistor scaling to increase device value (sensors, MEMS, bio, passives, etc.)
- **Beyond Moore**
  - Exploring new device architectures (non-planar)
  - 3D Integrated Circuits
  - Gate-All-Around transistors, Nanowires (NW-FET), Nanotubes (CNT), etc.

IC Industry in Egypt

Si-Ware Systems

Silicon Vision
Innovative IC Solutions

Mentor Graphics®

Analog Devices

Microchip®

Mentronix

mipex
Mixed-Signal IP Excellence

MEMS Vision

ICpedia

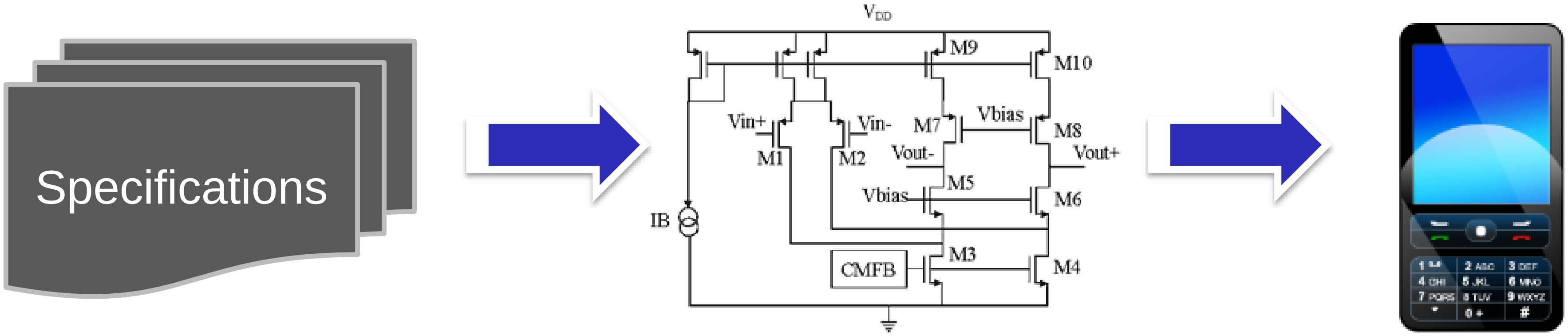
Axxcelera
BROADBAND WIRELESS

ENPIRION
The Leader of Integrated Power IC Solutions

vidatronic

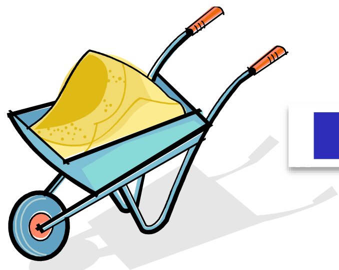
Course Objective

- To teach the basic knowledge required for
  - Analog IC analysis and design using CMOS technology
  - Moving from specifications (specs) to block design
  - Simulating the analog circuit using professional IC design tools

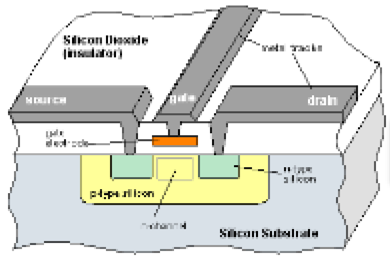


Your Learning Journey

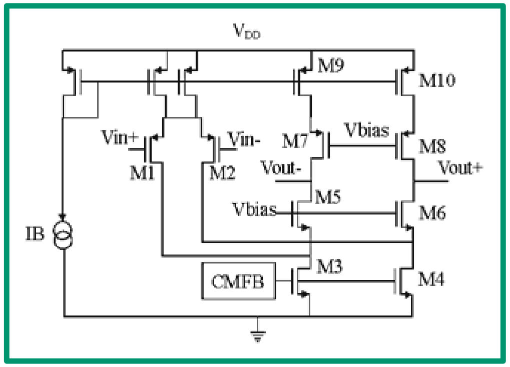
Material



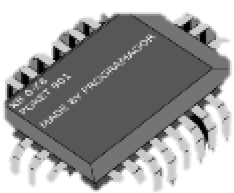
Devices



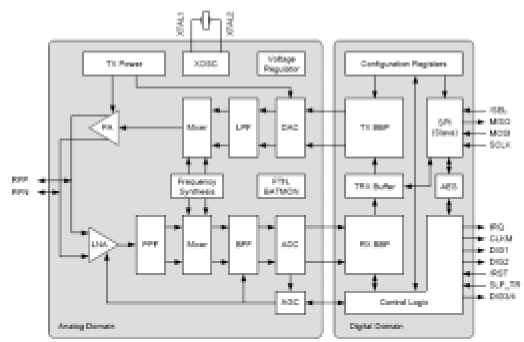
Circuits



Product



System



What Are We Going to Learn?

- MOSFET operation and models
- Single stage amplifiers
- Cascode amplifiers
- Frequency response of amplifiers
- Current mirrors
- Differential amplifiers
- Gm/ID design methodology
- Negative feedback systems
- Stability and frequency compensation
- Noise analysis and modeling
- **Operational (transconductance) amplifier (op-amp/OTA) Design**
- **Practical hands-on labs using professional IC design tools**

References

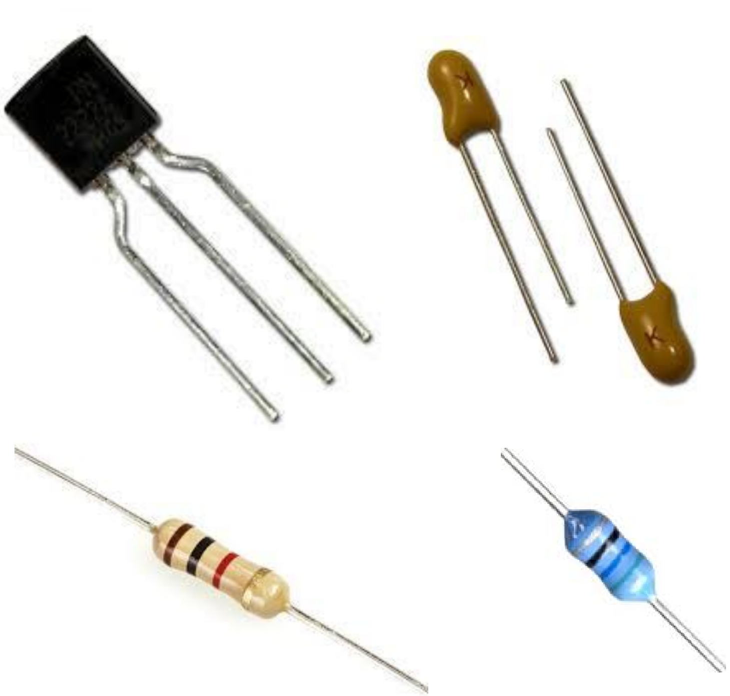
- References for beginners
  - T. **Floyd,** “Electronics Fundamentals, Circuits, Devices, and Applications,” 8th ed., Pearson, 2014
  - B. **Razavi**, “Fundamentals of microelectronics,” 2nd ed., Wiley, 2014
  - A. **Sedra** and K. Smith, “Microelectronic circuits,” Oxford University Press, 7th ed., 2015
- References for professionals
  - B. **Razavi**, “Design of analog CMOS integrated circuits,” McGraw-Hill Ed., 2nd ed., 2017
  - T. C. Carusone, D. **Johns**, and K. W. **Martin**. “Analog integrated circuit design,” 2nd ed., Wiley, 2nd ed., 2012
  - P. **Gray**, P. Hurst, S. Lewis, and R. **Meyer**, “Analysis and design of analog integrated circuits,” Wiley, 5th ed., 2009
  - W. **Sansen**, “Analog design essentials,” Springer, 2006

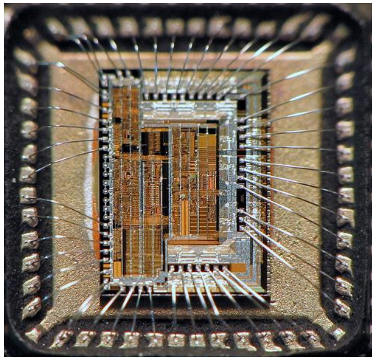
Canvas

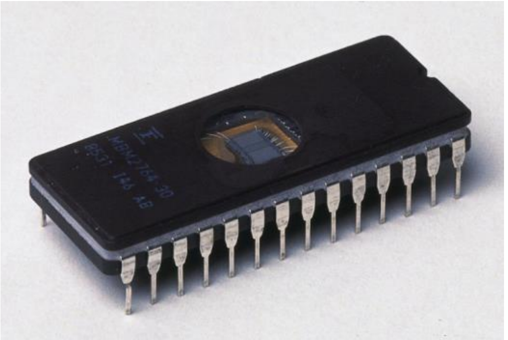
- Canvas is a learning management system (LMS) used in many universities in the US and around the world
- We will use Canvas for
  - Posting lectures, notes, etc.
  - Questions and answers
  - Announcements and discussions
  - Quizzes
  - Submitting and grading assignments, reports, etc.
- **Everyone must register at Canvas today!**

What is an Integrated Circuit (IC)?

- Various circuit elements: transistors, capacitors, resistors, and even small inductances can be integrated on one chip

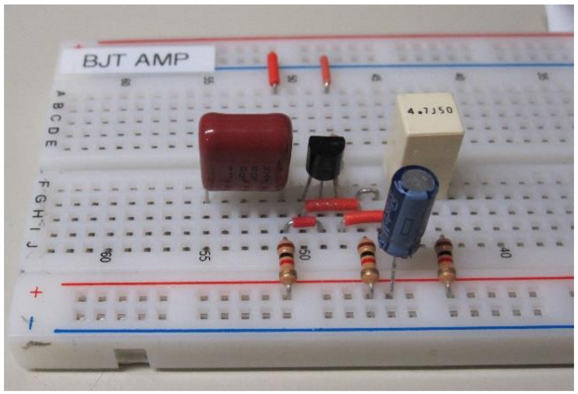


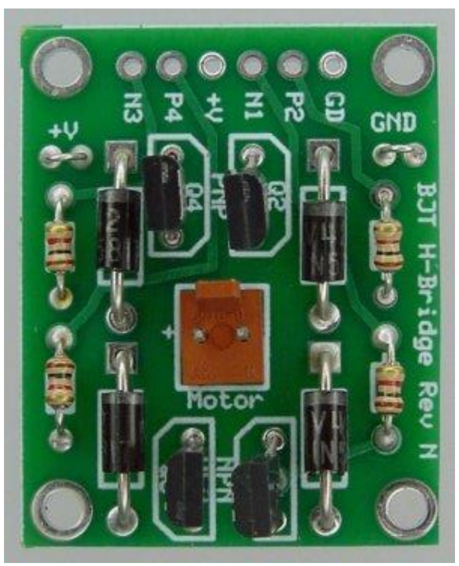


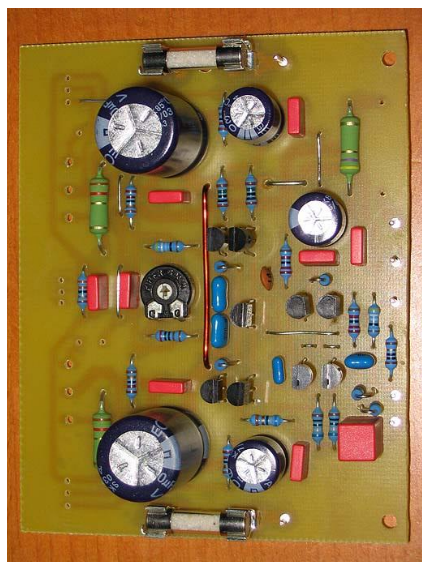


Discrete vs. Integrated Electronics

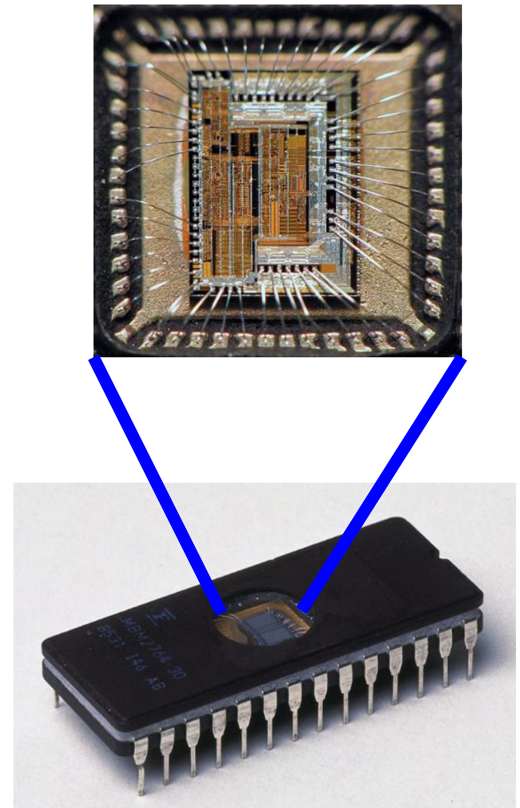
Circuits using discrete components







Integrated circuit



What is an Integrated Circuit (IC)?

- Transistors:
  - Billions of tiny transistors can be integrated on the same chip
  - Very Large Scale Integration (VLSI): > 10,000 transistors
- Capacitors:
  - Capacitors as large as 100s of pF can be integrated on-chip
  - But they consume a lot of chip area → Use sparingly
- Resistors:
  - Resistors as large as few MOhms can be integrated on-chip
  - But they consume a lot of chip area → Use sparingly
- Inductors:
  - Small inductors (few nH) can be integrated on-chip
  - But they consume a lot of area with relatively poor performance
  - Only in RF circuits

IC Technology Generations

- Early integrated circuits primarily used bipolar transistors (BJTs)
- 1960s: MOS ICs became attractive for their low cost
  - MOS transistor occupied less area
  - The fabrication process was simpler
  - Early commercial processes used only PMOS transistors and suffered from poor performance, yield, and reliability
- 1970s: Processes using only NMOS transistors became common
- Digital circuits in all the previous technologies have quiescent power
  - Power is dissipated when the circuit is idle, i.e., not switching
  - This limits the maximum number of transistors that can be integrated on one die

IC Technology Generations (Cont'd)

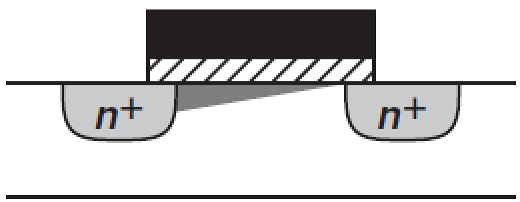
- 1980s: The VLSI era
  - Power consumption became a major issue
  - CMOS processes were widely adopted and replaced NMOS and bipolar processes for nearly all digital logic applications
  - A key advantage for "digital" CMOS is that it has negligible idle (static) power consumption
- Nowadays:
  - With aggressive scaling and billions of transistors, CMOS idle leakage current is not negligible any more
  - But no better technology is available yet…

How to Design a Billion Transistor Chip?

1. Abstraction
   – Hiding details until they become necessary
2. Structured design
   – Hierarchy: Block, sub-blocks, … → Tree structure (from root to leaf cells)
   – Regularity: Min no. of different blocks → Block reuse (e.g., standard cells)
   – Modularity: Blocks are black boxes that have well-defined interfaces → Combine to build larger system without surprises!
3. CAD Tools
   – Automation, automation, automation!
   – Analog automation is way behind digital automation

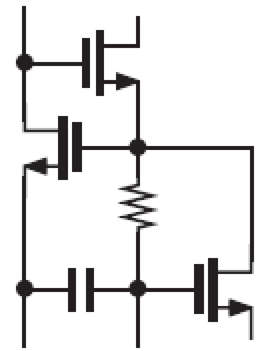
Levels of Abstraction

Device



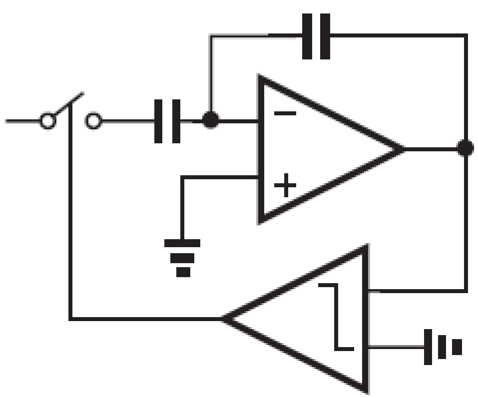
(a)

Circuit



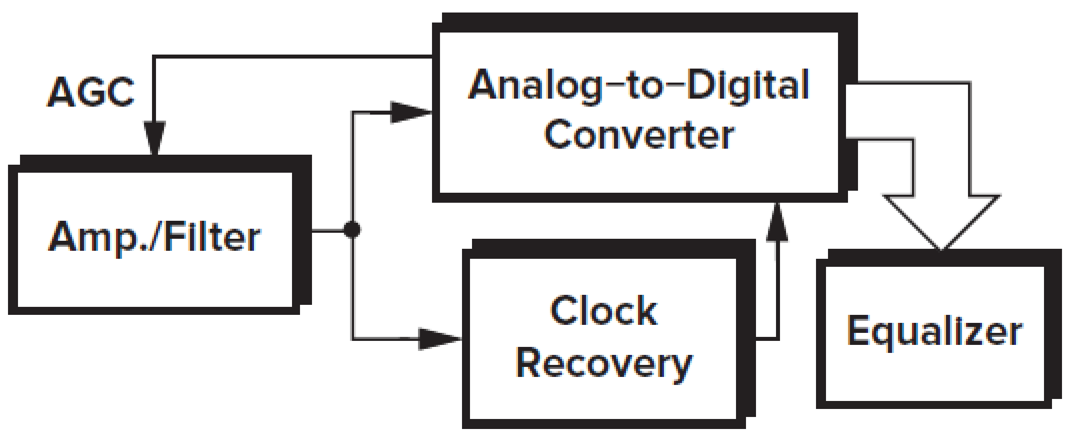
(b)

Architecture



(c)

System



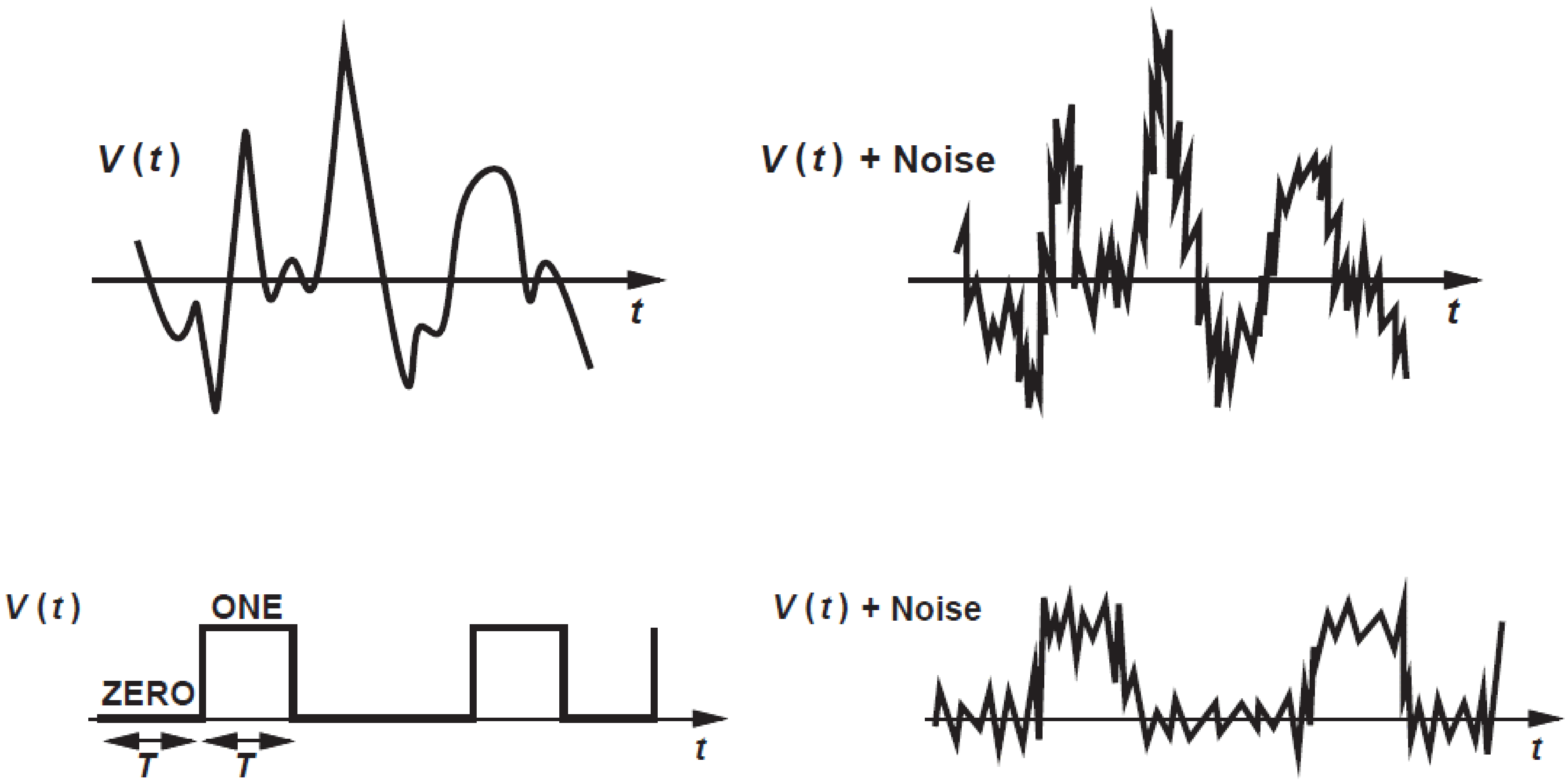
(d)

[Razavi, 2017]

CAD/EDA

- **Analog design**
  - **Design entry (schematic), simulation, layout, and extraction**
  - **Verification (LVS: layout vs schematic, DRC: layout design rule check)**
- Digital design
  - Design entry (e.g., HDL) and simulation
  - Automated synthesis (from HDL to gates)
  - Automated place and route (from gates to transistor layout)
  - Verification
- System design
  - Behavioral modeling and high level simulation/verification
- EM simulation, process simulation, device simulation, etc.

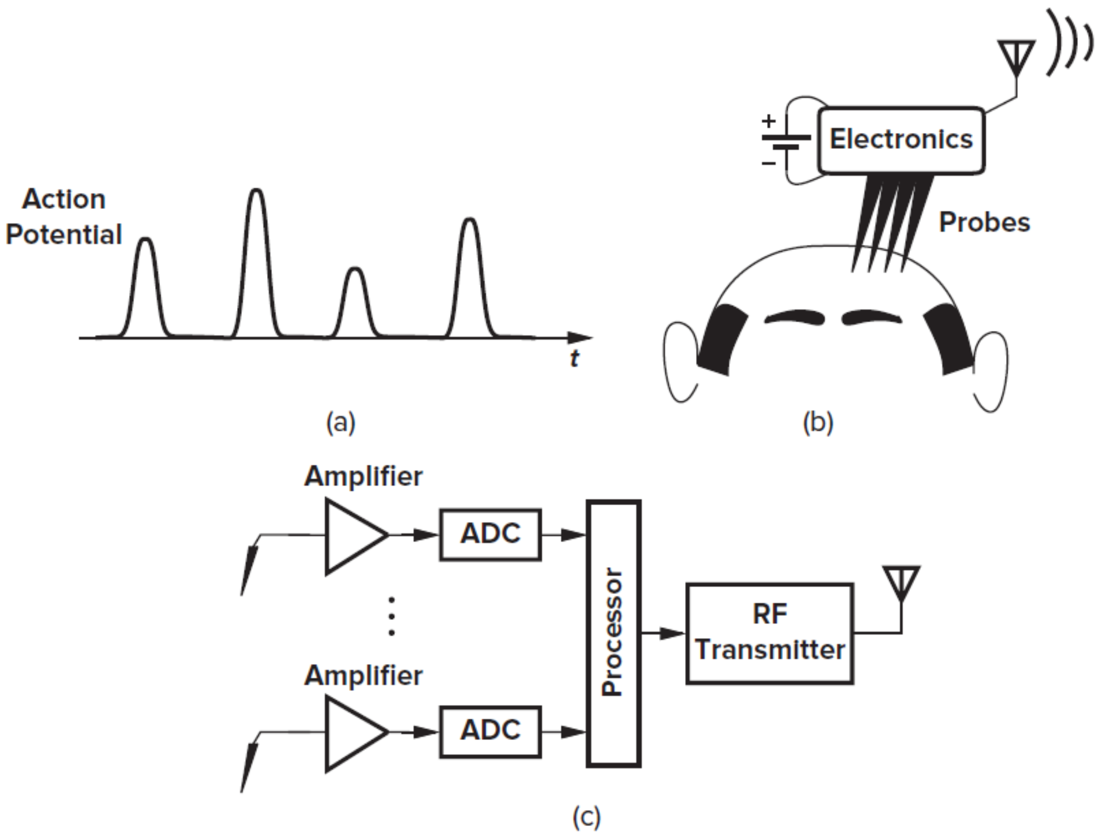
Analog vs Digital Signals



[Razavi, 2014]

Why Analog?

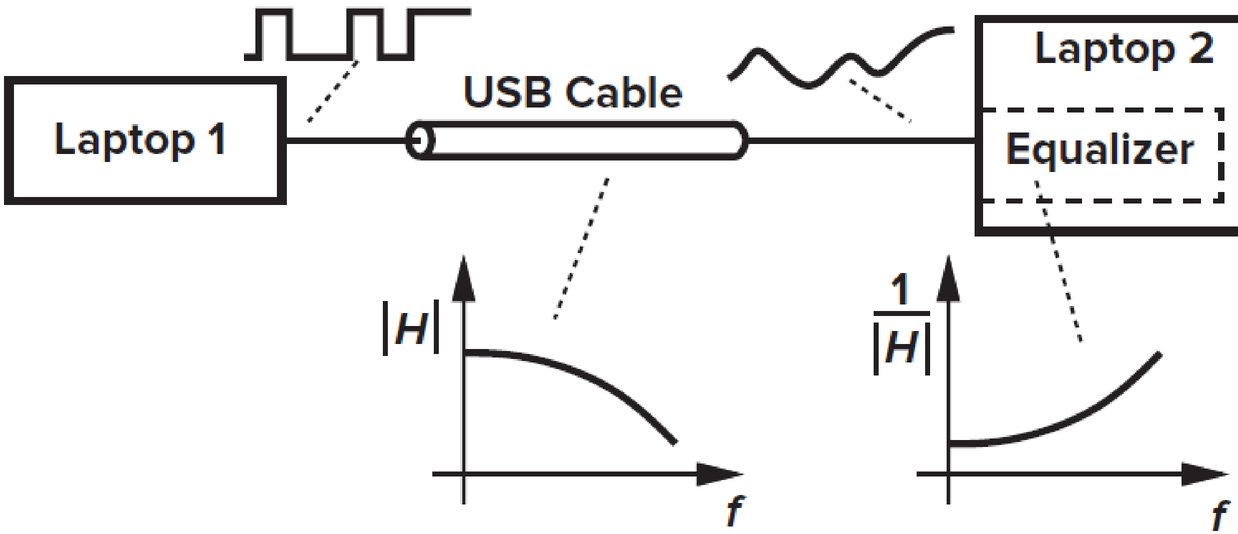
- ❑ All the physical signals in the world around us are analog
  - Voice, light, temperature, pressure, etc.
- ❑ We (will) always need an "analog" interface circuit to connect between our physical world and our digital electronics



[Razavi, 2017]

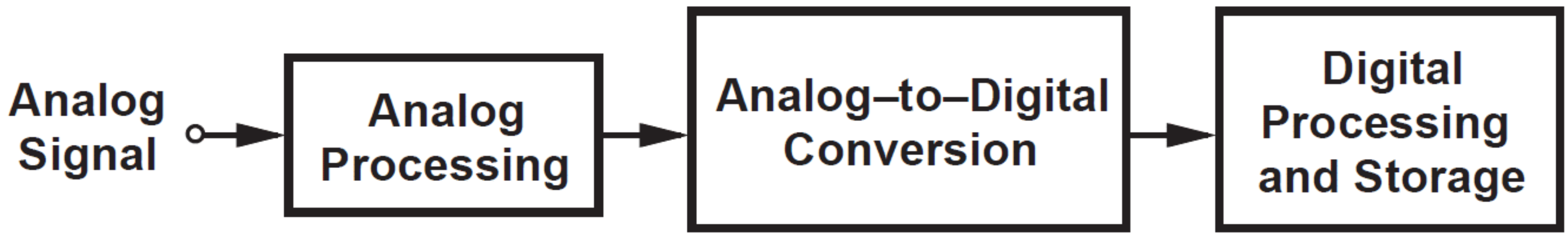
Why Analog?

- High speed digital design is actually analog design!
- At low speeds, we may directly digitize the signal and perform the signal processing in the digital domain
- At high speeds, signal processing in the analog domain is much more energy efficient
- The boundary between high and low speed has risen over time



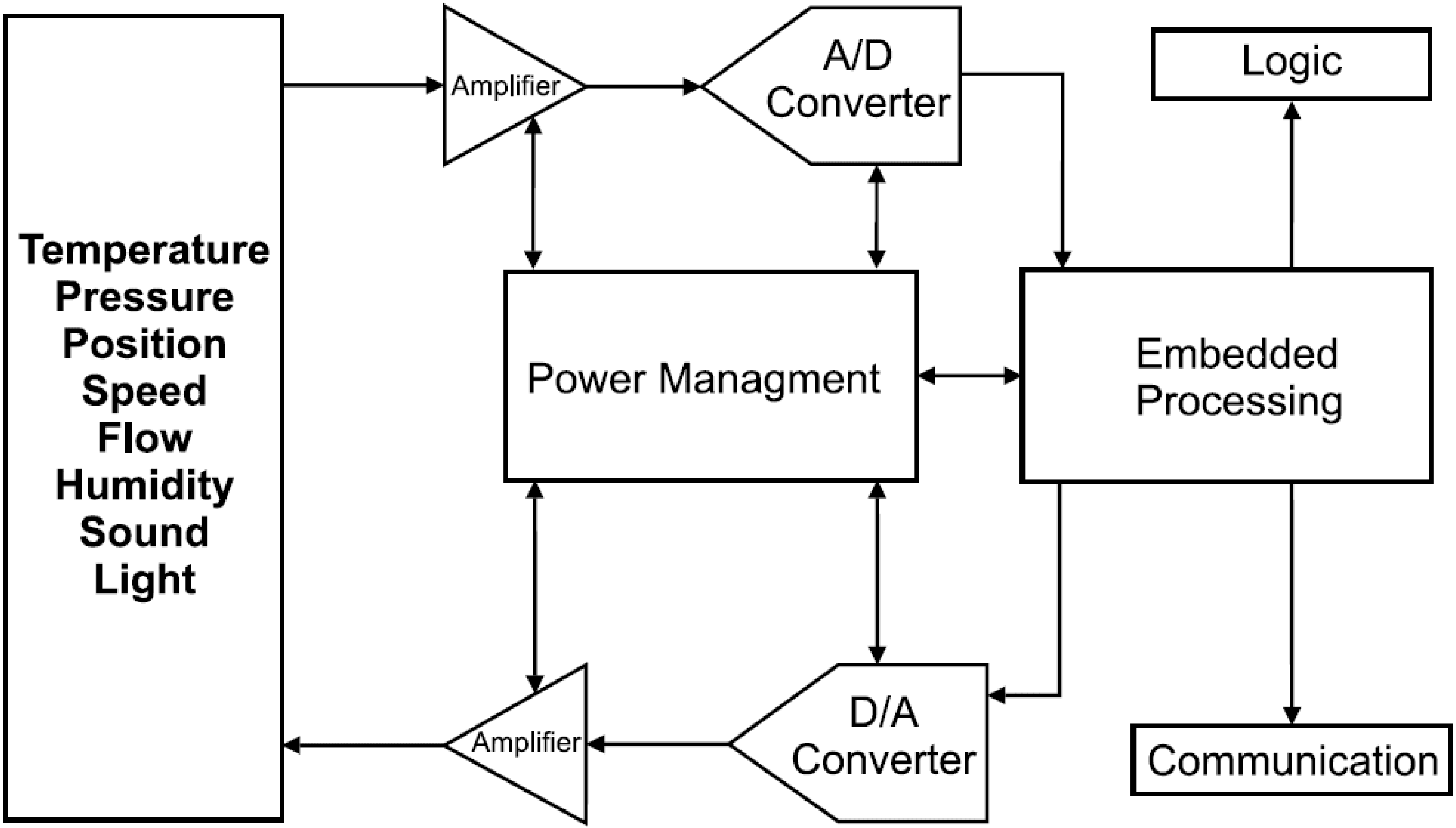
[Razavi, 2017]

Signal Processing Chain



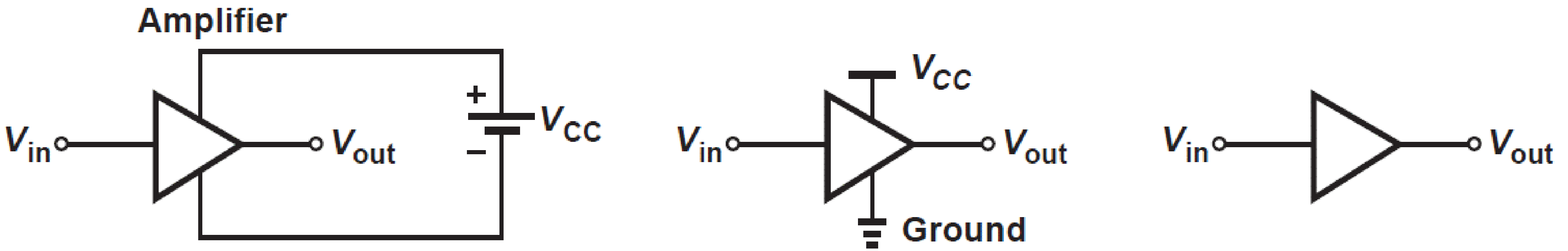
[Razavi, 2014]

Signal Processing Chain

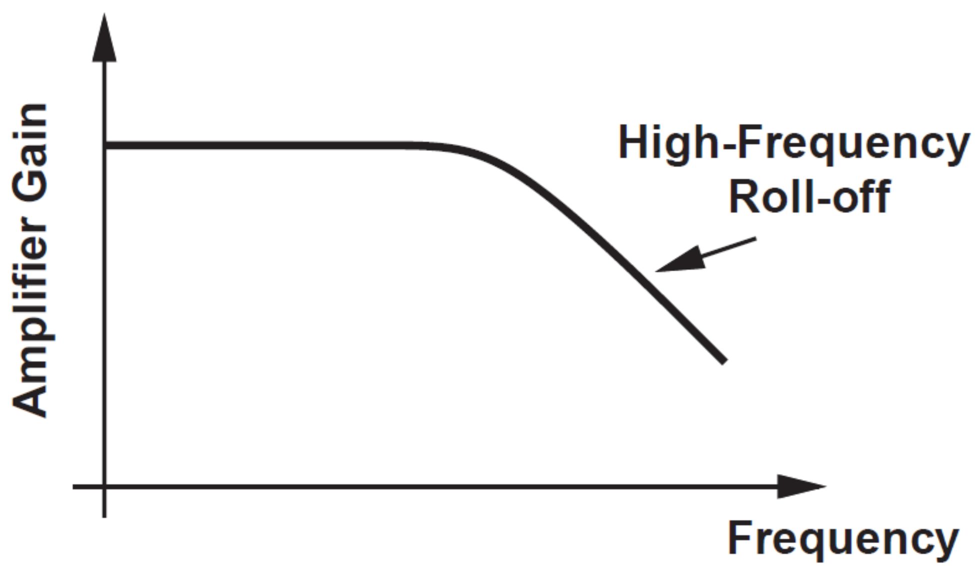


[TI, ASLK-PRO]

Analog Amplifier



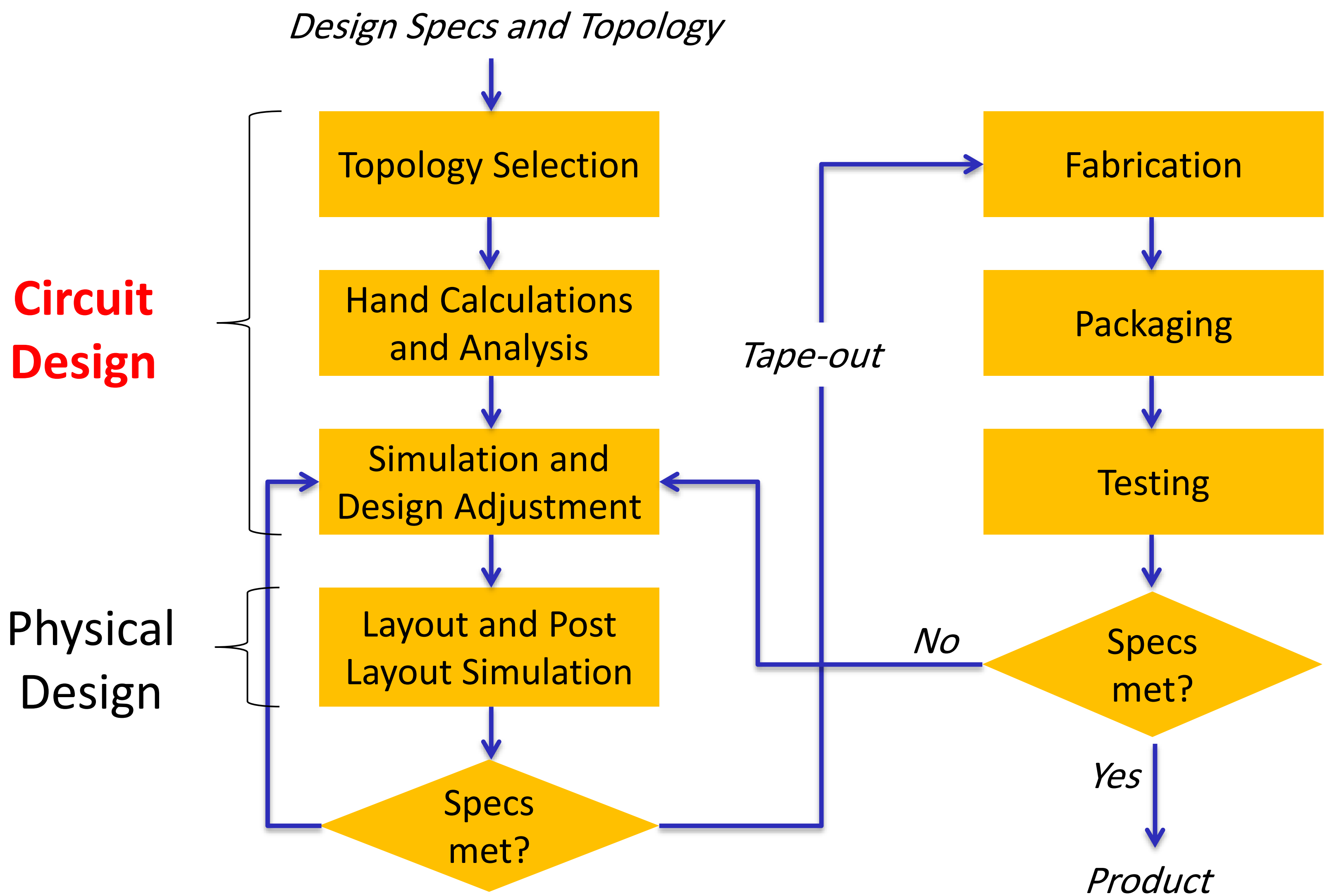
- The amplifier has finite gain and bandwidth (speed)



Analog Design Challenges

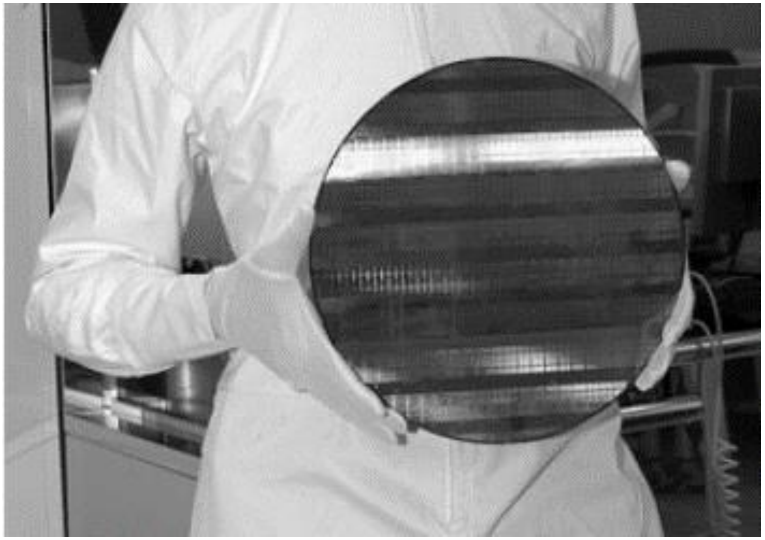
- Device scaling
  - Transistors become faster, but the gain declines
- Supply voltage scaling
  - From 12V in 1970s to less than 1V
- Low power consumption
  - Increase battery lifetime, decrease cost and heat emissions
- Complexity
  - Continuous increase in transistor count and system complexity
- PVT variations
  - Tolerate large process, voltage, and temperature variations

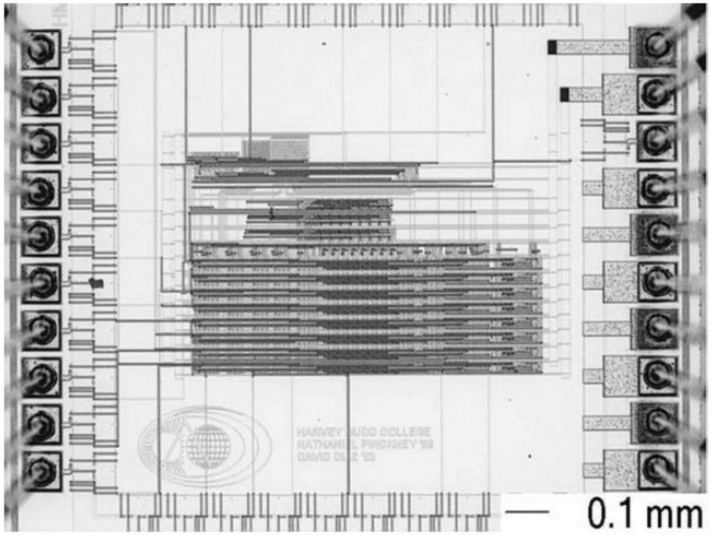
Analog IC Design Flow



Tape-Out

- The layout is sent to the fab in a format called GDS II
  - Previously it was sent on a magnetic tape → tape-out
  - Now by email (small design) or FTP (large design)

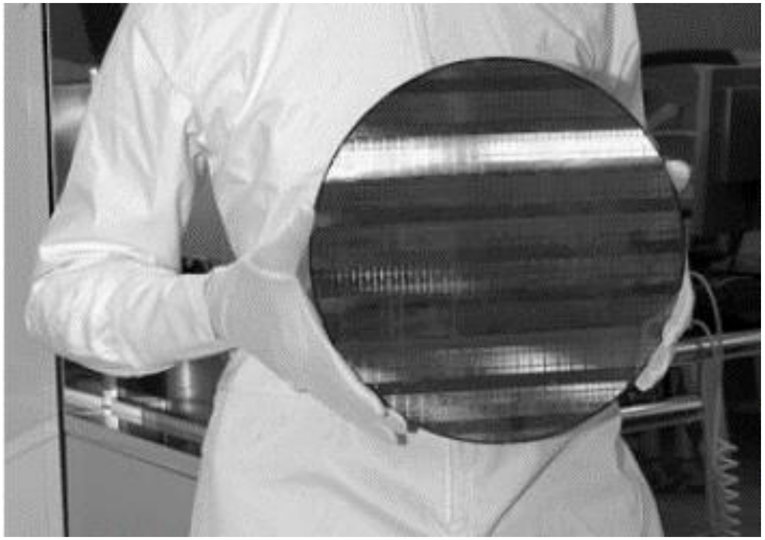
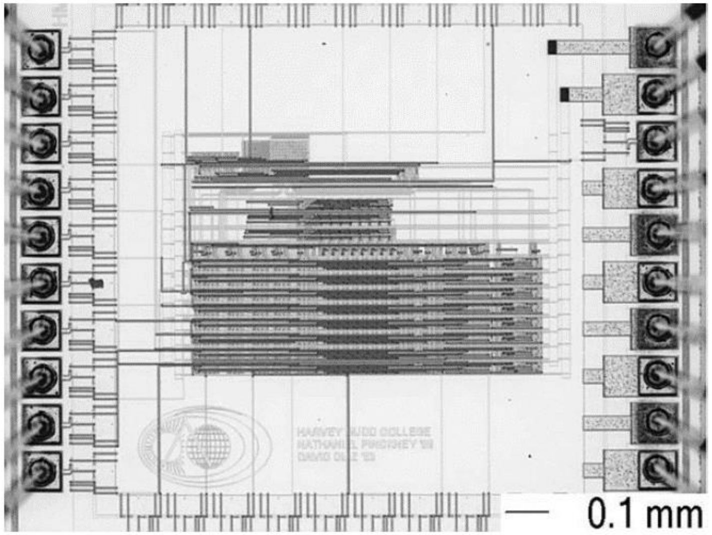




[Weste and Harris, 2010]

Tape-Out

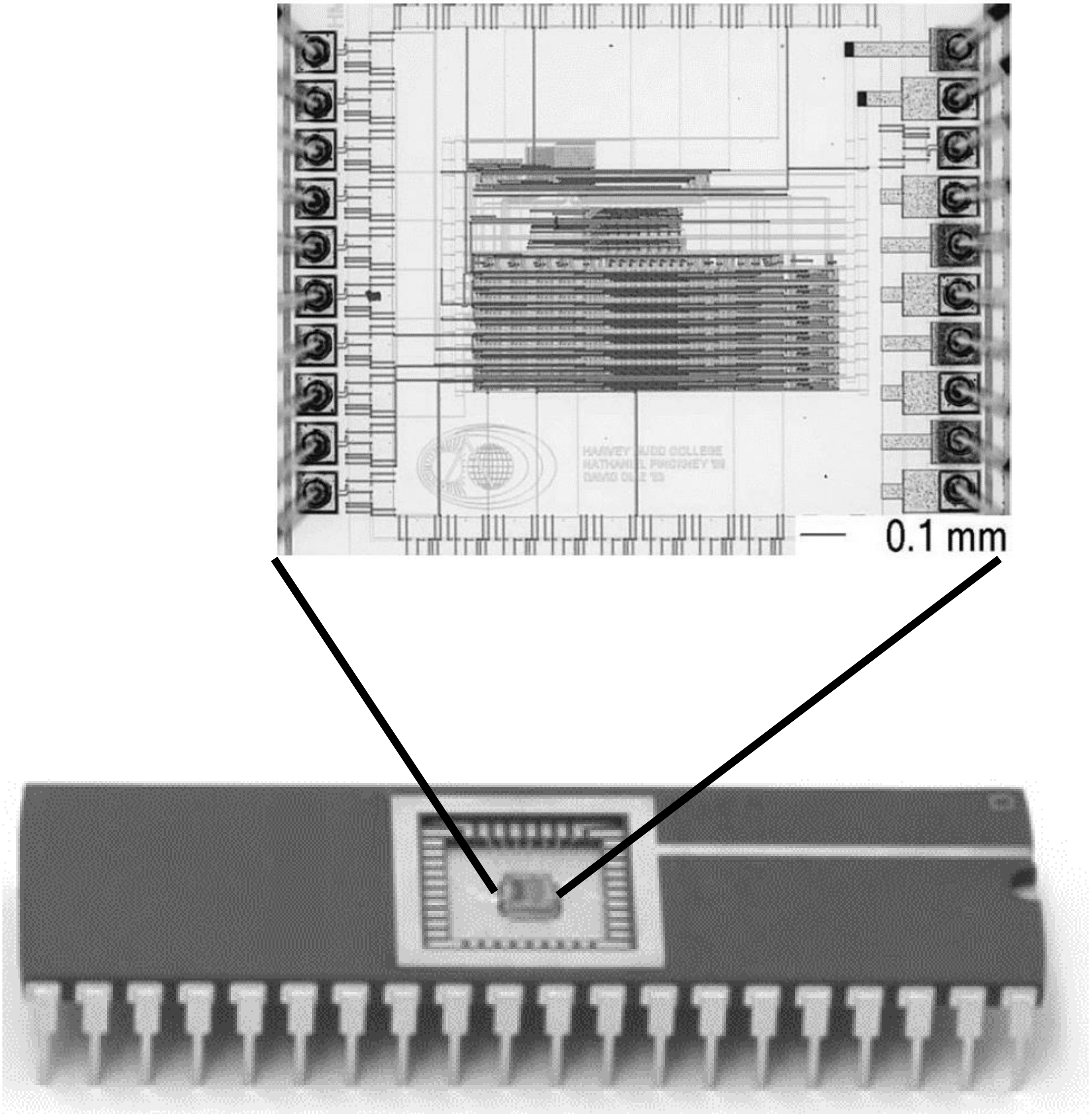
- ICs are fabricated on silicon wafers
  - Turnaround time ~ 3months
- A fabrication run in 65nm process costs about $3 million
  - Cost sharing using MPW (multi-project wafer)
    - US: MOSIS
    - Europe and MENA: Europractice
    - Saudi Arabia: WaferCat

[Weste and Harris, 2010]

Packaging and Testing

- Wafer diced into dies
- Gold bond wires from die I/O pads to package
- Packaging is now much more advanced than the simple DIP



[Weste and Harris, 2010]

Thank you!