وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog IC Design

Lecture 10
Current Mirrors

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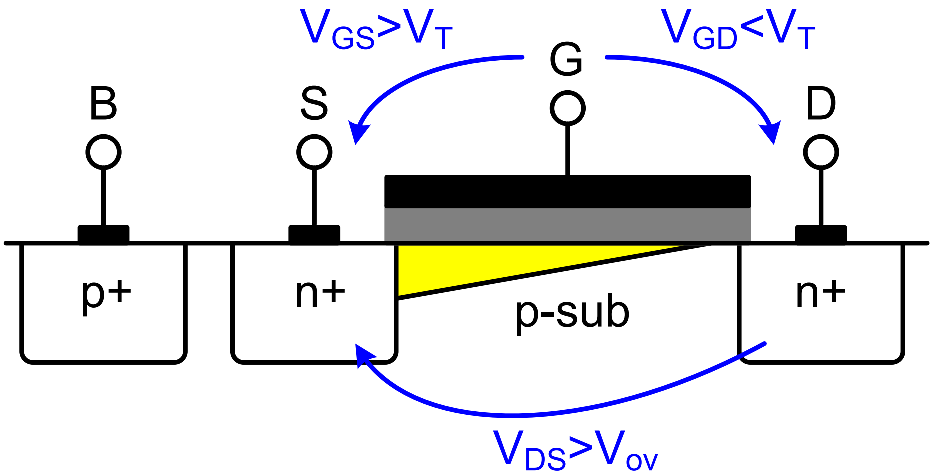
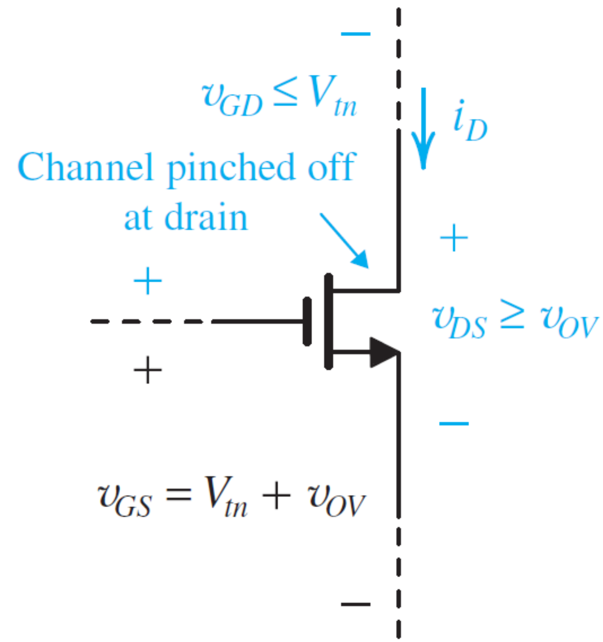
MOSFET in Saturation

- The channel is pinched off if the difference between the gate and drain voltages is not sufficient to create an inversion layer

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \cdot V_{ov}^2 (1 + \lambda V_{DS})$$





[Sedra/Smith, 2015]

Regions of Operation Summary

OFF (Subthreshold)

$V_{GS} < V_T$

ON

$V_{GS} > V_T$

Triode

$V_{DS} < V_{ov}$

Or

$V_{GD} > V_T$

$$I_D = \mu C_{ox} \frac{W}{L} \left(V_{ov} V_{DS} - \frac{V_{DS}^2}{2} \right)$$

Pinch-Off (Saturation)

$V_{DS} \geq V_{ov}$

Or

$V_{GD} \leq V_T$

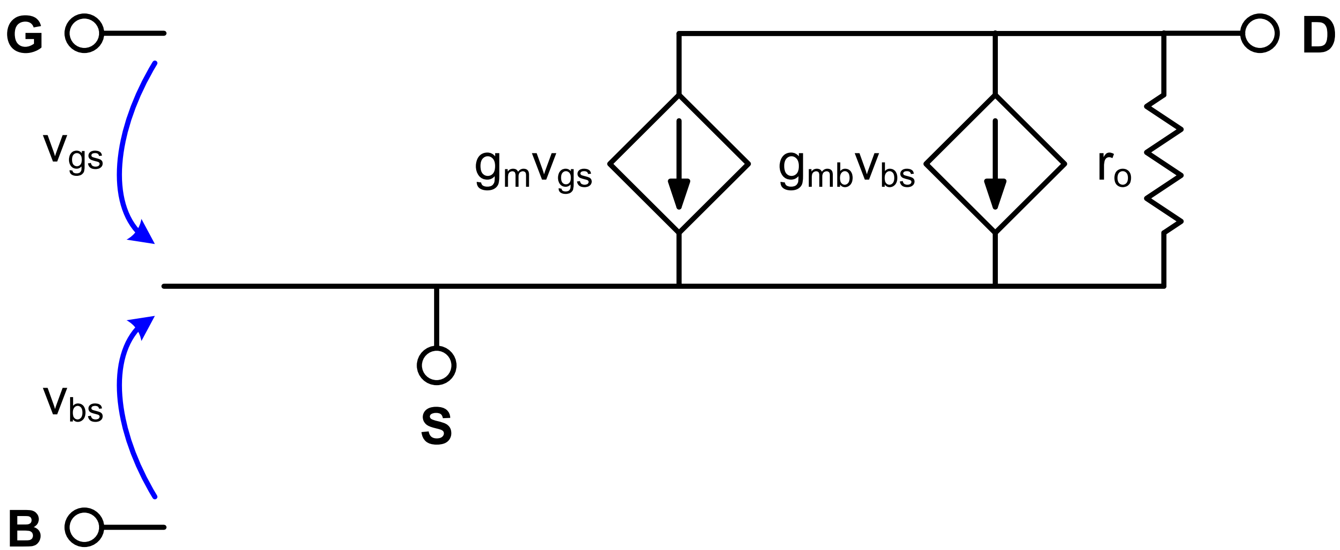
$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS})$$

Low-Frequency Small-Signal Model

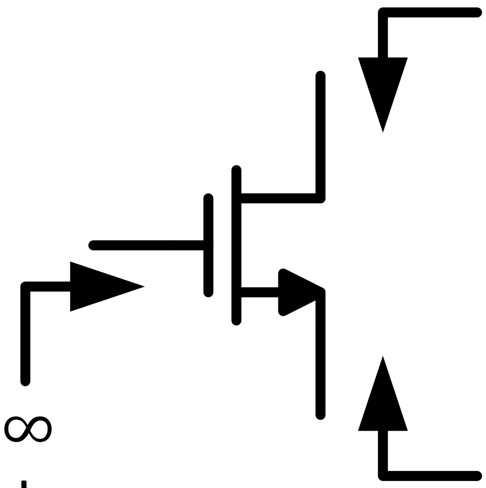
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox}\frac{W}{L}V_{ov} = \sqrt{\mu C_{ox}\frac{W}{L}\cdot 2I_D} = \frac{2I_D}{V_{ov}}$$

$$g_{mb} = \eta g_m, \qquad \eta \approx 0.1 - 0.25$$

$$r_o = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{1}{\lambda I_D}, \qquad \lambda \propto \frac{1}{L}$$



Rin/out Shortcuts Summary



$$r_o[1 + (g_m + g_{mb})R_S]$$

H.I.N.

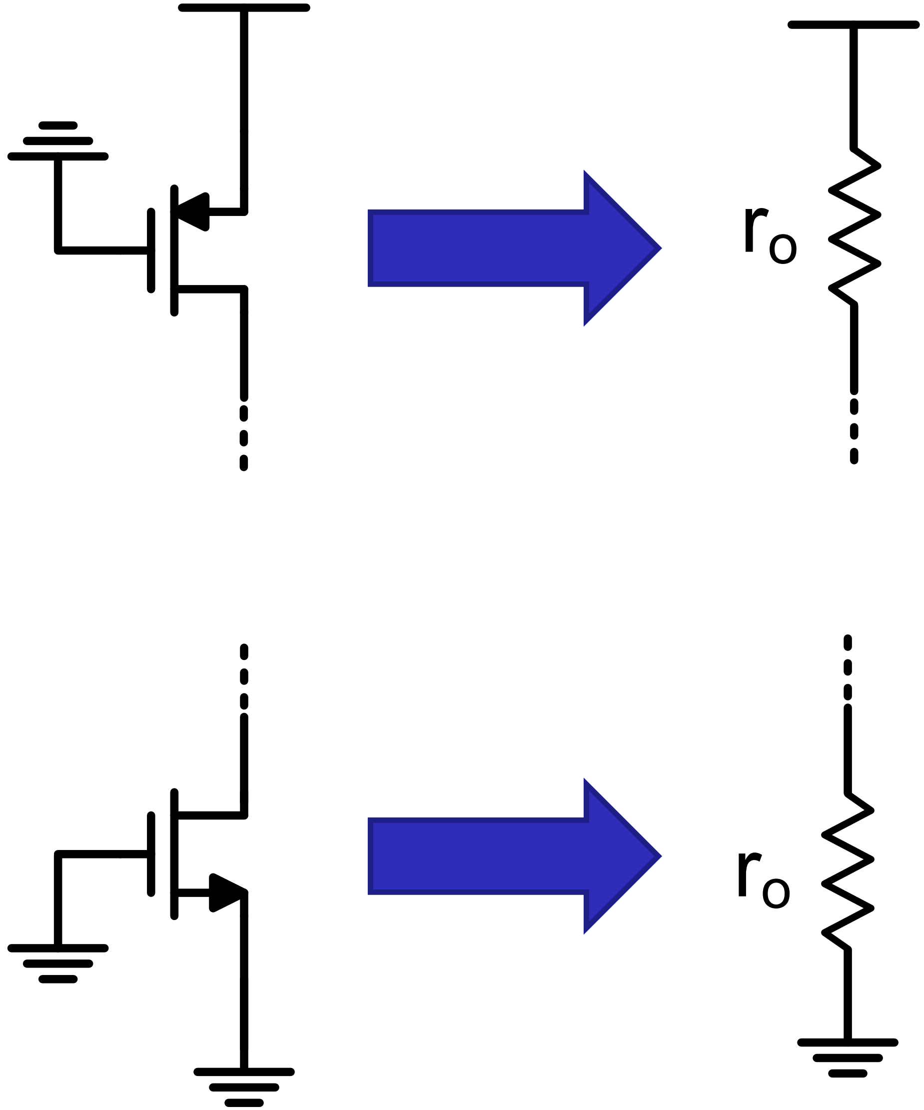
∞

At low frequencies **ONLY**

$$\frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$$

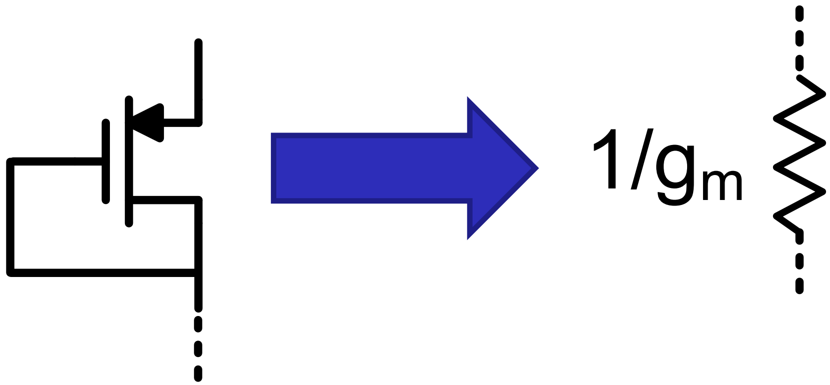
L.I.N.

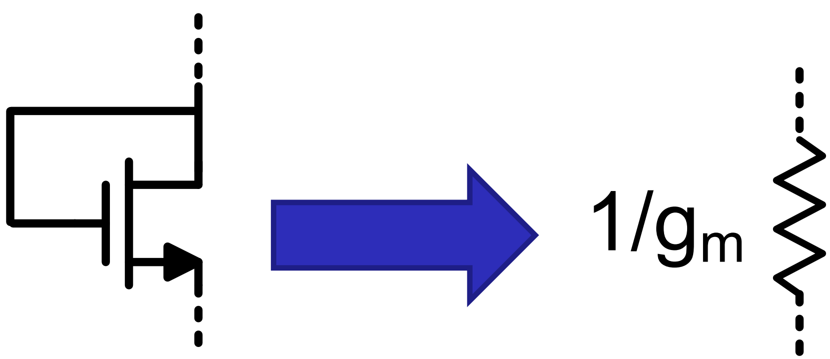
Active Load (Source OFF)



Diode Connected (Source Absorption)

- Always in saturation
- Bulk effect: $g_m \rightarrow g_m + g_{mb}$





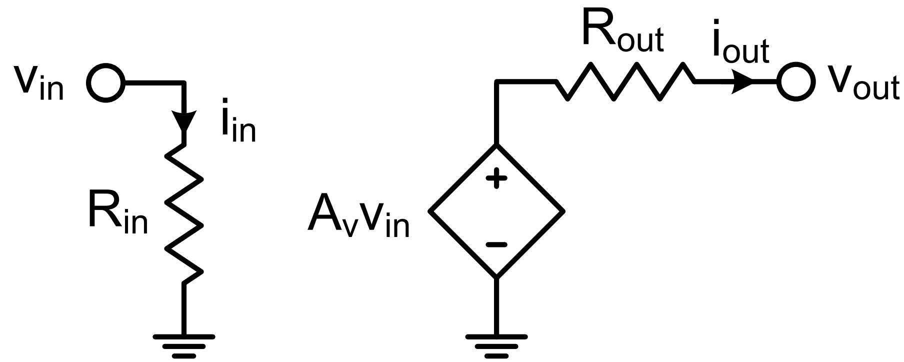
Why GmRout?

$$R_{out} = \frac{v_x}{i_x} @ v_{in} = 0$$

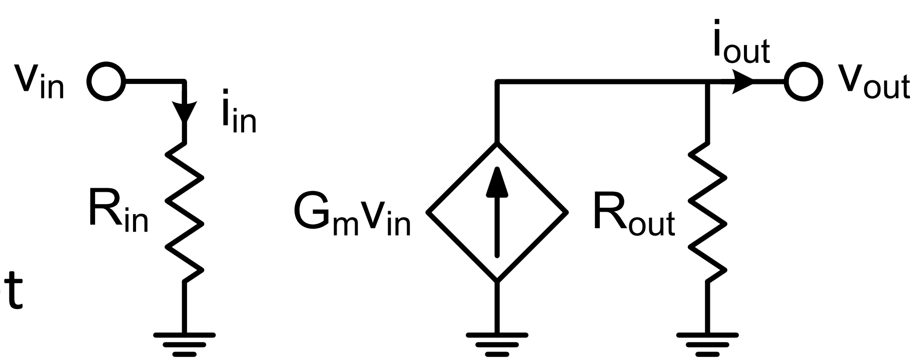
$$G_m = \frac{i_{out,sc}}{v_{in}}$$

$$A_v = G_m R_{out}$$

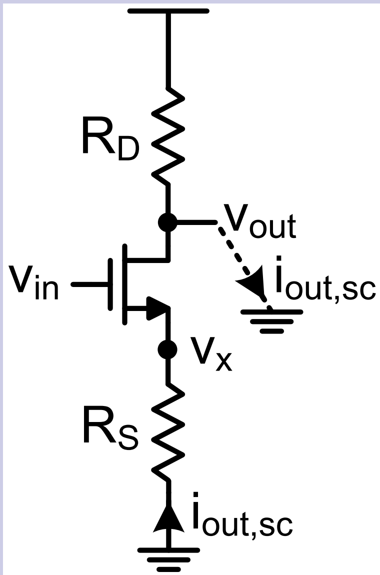
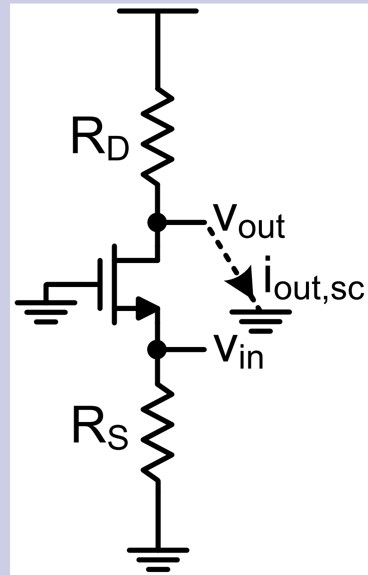
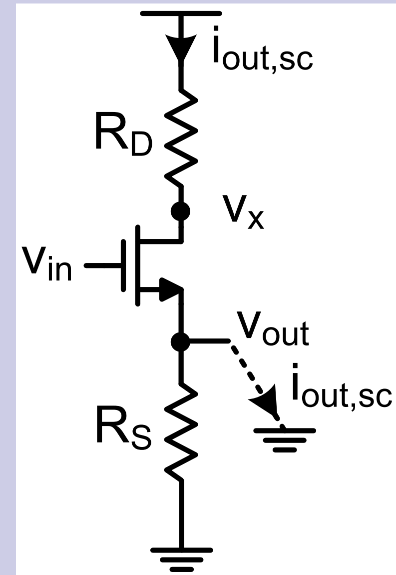
$$A_i = G_m R_{in}$$



- Divide and conquer
  - Rout simplified: vin=0
  - Gm simplified: vout=0
  - We already need Rin/out
  - We can quickly and easily get Rin/out from the shortcuts

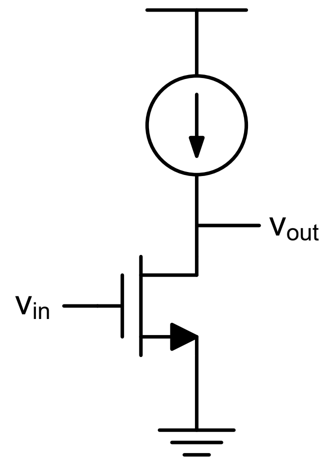


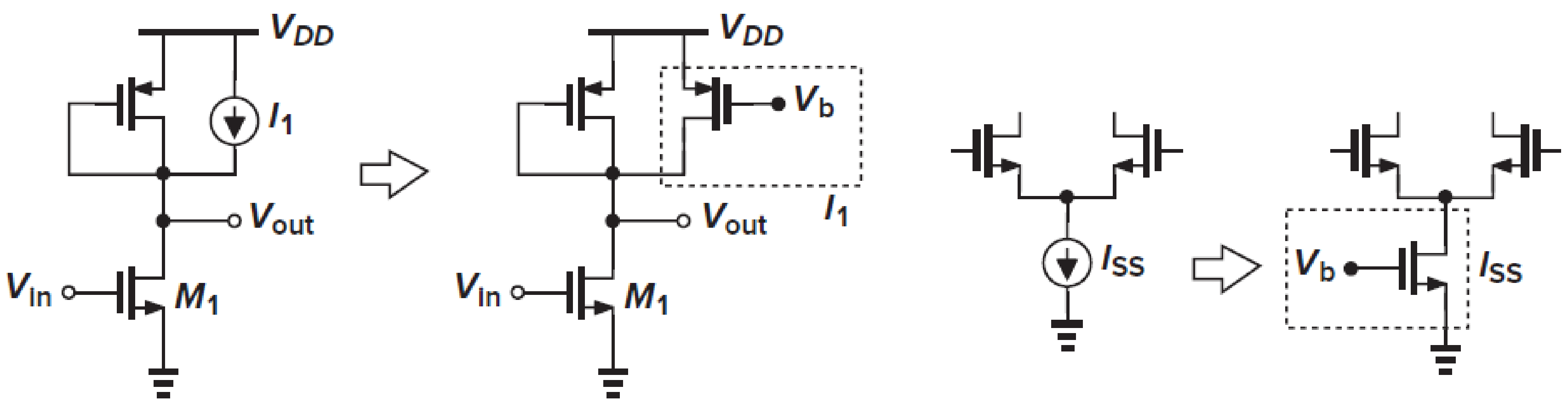
Summary of Basic Topologies

	CS	CG	CD (SF)
			
	Voltage & current amplifier	Current buffer	Voltage buffer
Rin	∞	$R_S // \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$	∞
Rout	$R_D // r_o[1 + (g_m + g_{mb})R_S]$	$R_D // r_o$	$R_S // \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$
Gm	$\frac{-g_m}{1 + (g_m + g_{mb})R_S}$	$g_m + g_{mb}$	$\frac{g_m}{1 + R_D / r_o}$

Why Current Source?

- Current sources act as a large resistor without consuming excessive voltage headroom (and without consuming excessive chip area)

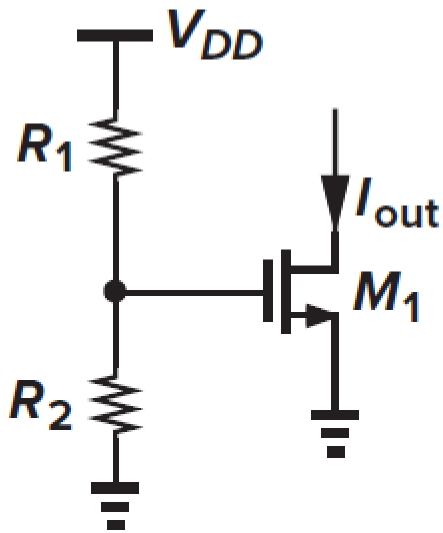




 [Razavi, 2017]

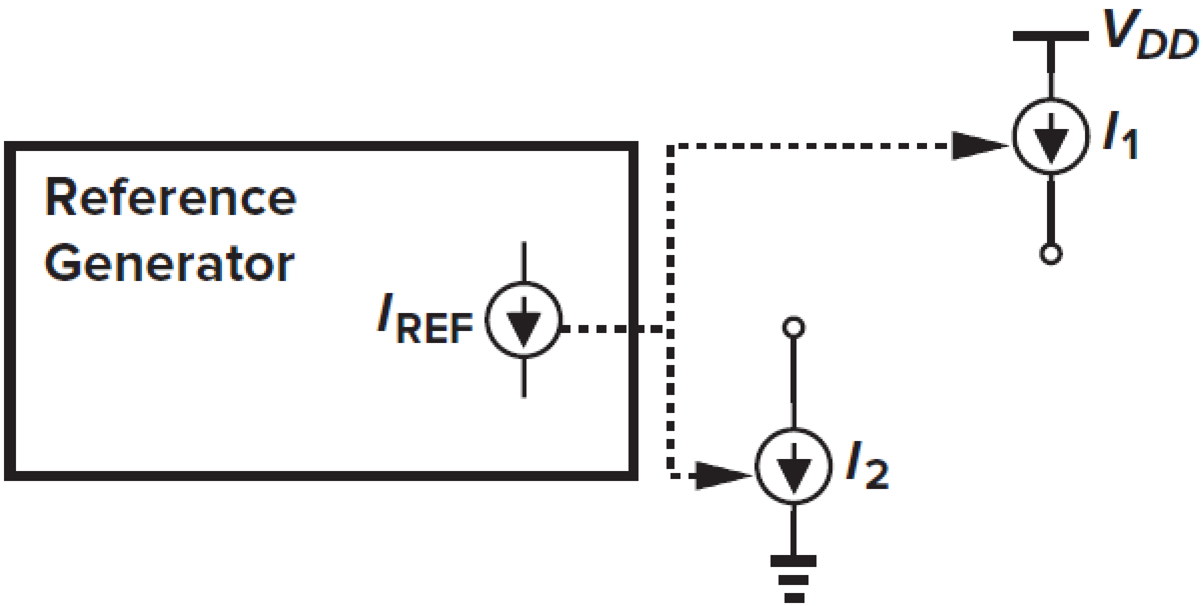
BAD Current Source

- Sensitive to PVT (process, voltage, and temperature) variations



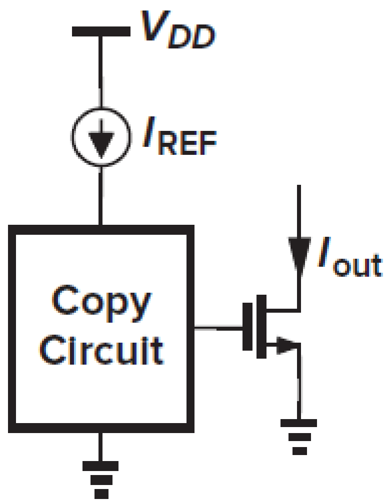
$$I_{out} \approx \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_2}{R_1 + R_2}V_{DD} - V_{TH}\right)^2$$

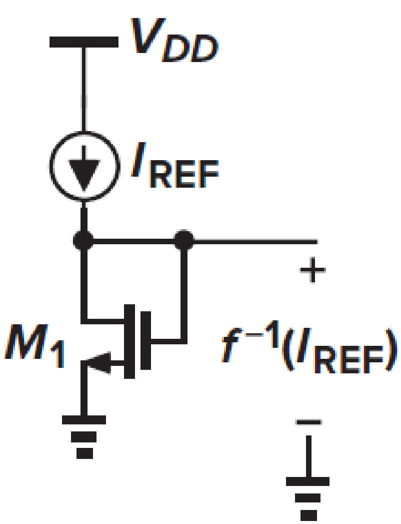
How to Generate Robust Currents?

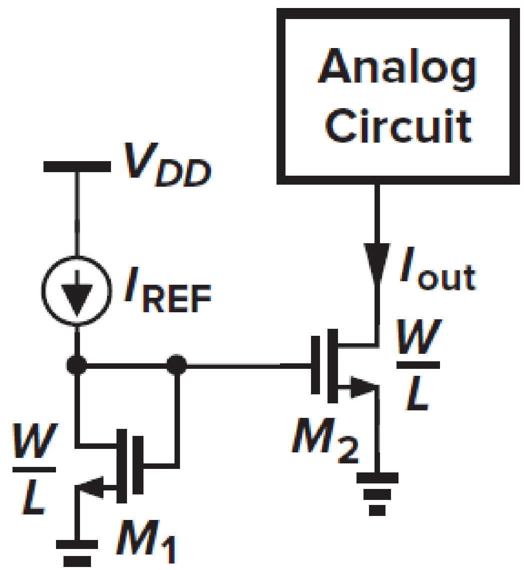


[Razavi, 2017]

How to Copy (Mirror) Currents?



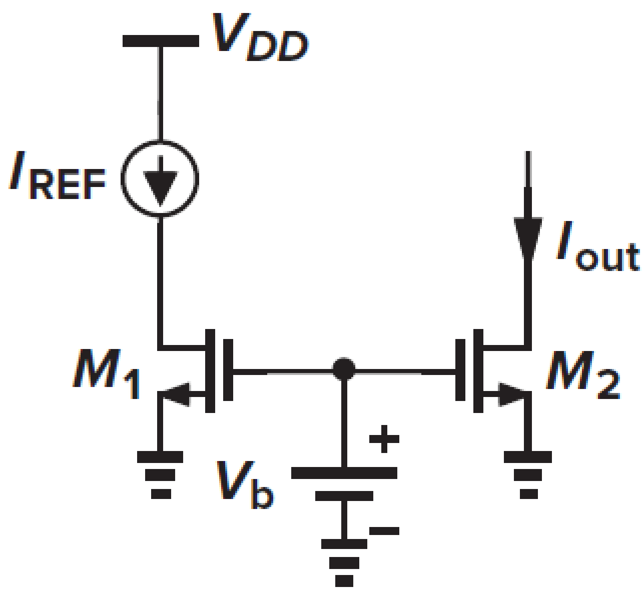




$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{REF}$$

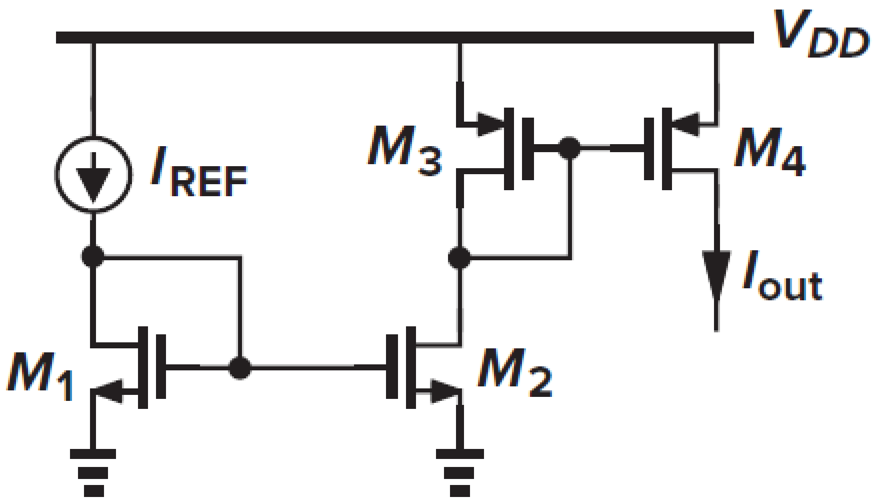
[Razavi, 2017]

Is This a Current Mirror?



[Razavi, 2017]

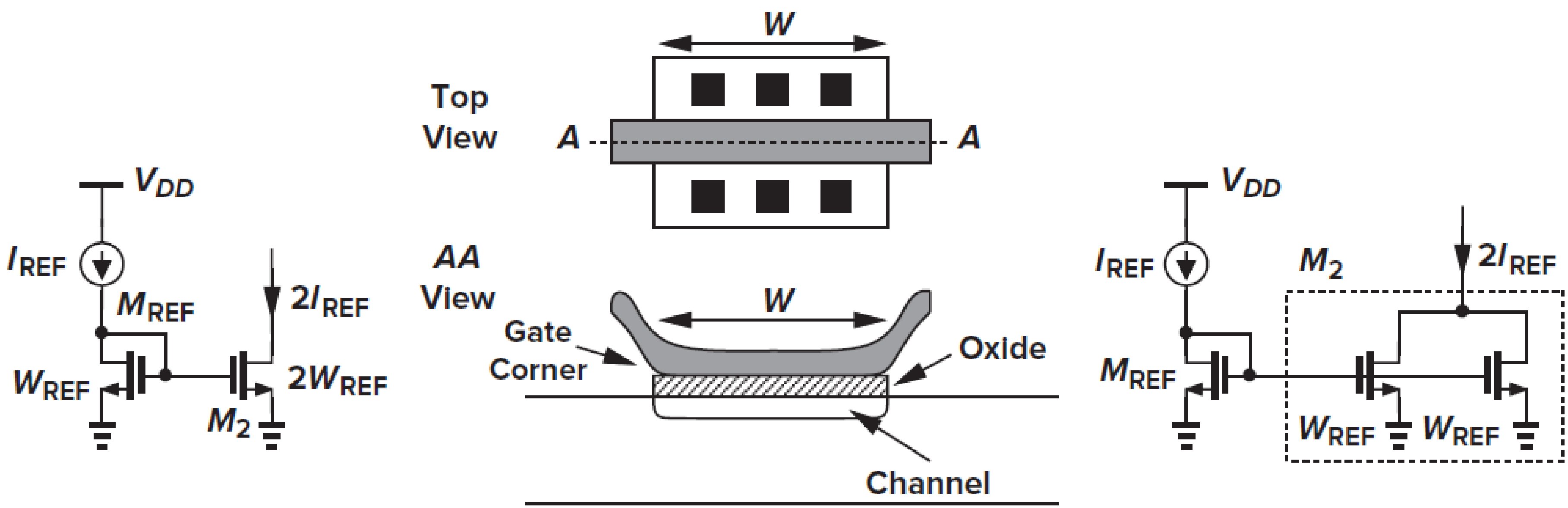
Sink and Source Currents



[Razavi, 2017]

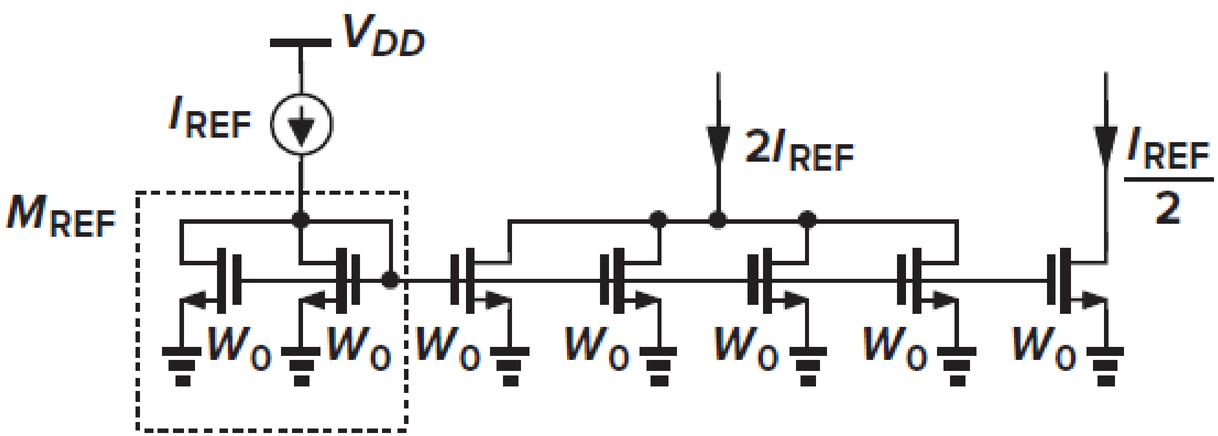
Accurate Mirroring

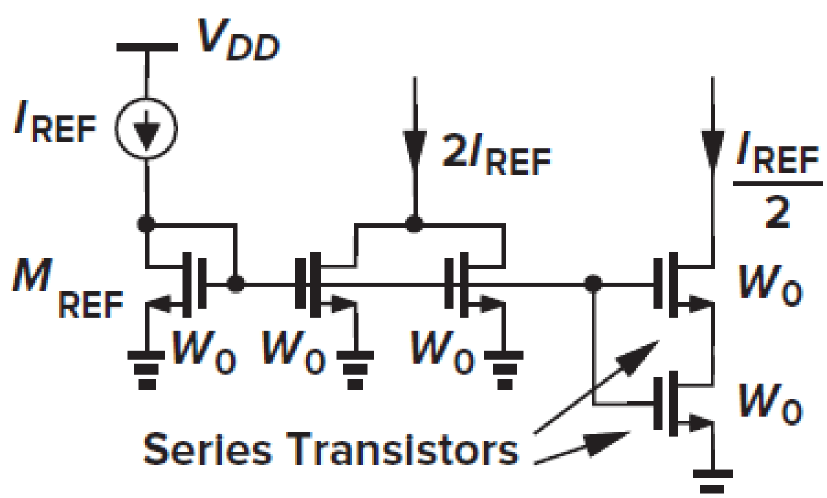
- ALWAYS use matched unit transistors (same L, W, orientation, etc.)



[Razavi, 2017]

Scale Current Up and Down



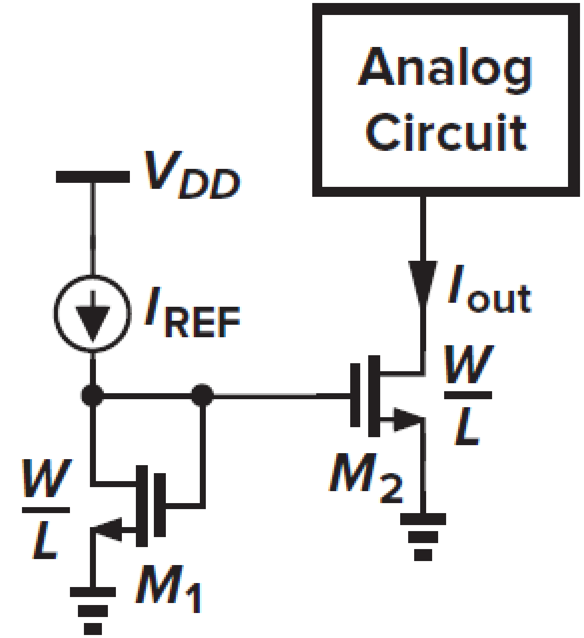


V_{DS} Dependence

$$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS1})$$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{TH})^2(1 + \lambda V_{DS2})$$

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \cdot \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

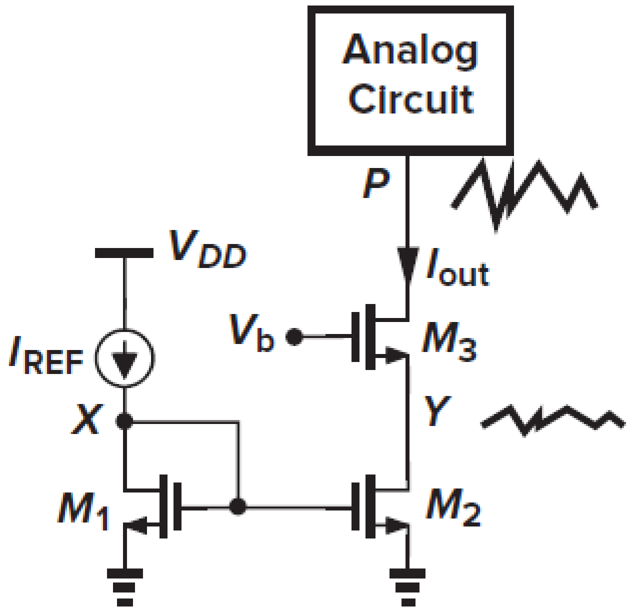


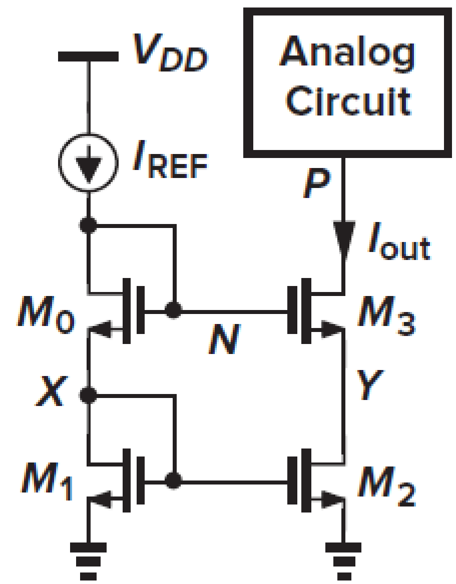
- First solution: Force VDS2 to be equal to VDS1

 [Razavi, 2017]

Cascode Current Mirror

- $V_{DS2} = V_{DS1} = V_{GS1} = V_{TH1} + V_{ov1}$
- The cascode also boosts $R_{out} = \frac{\Delta V_{out}}{\Delta I_{out}}$ → Less current variation

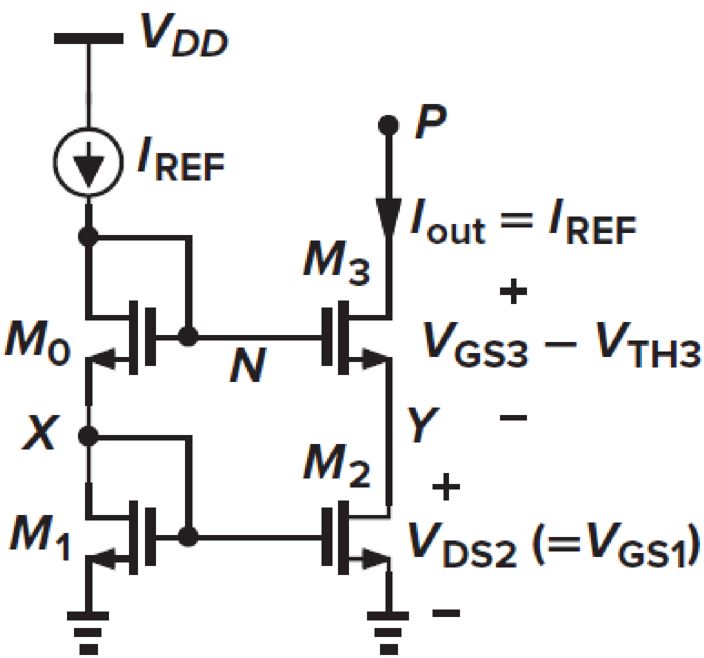


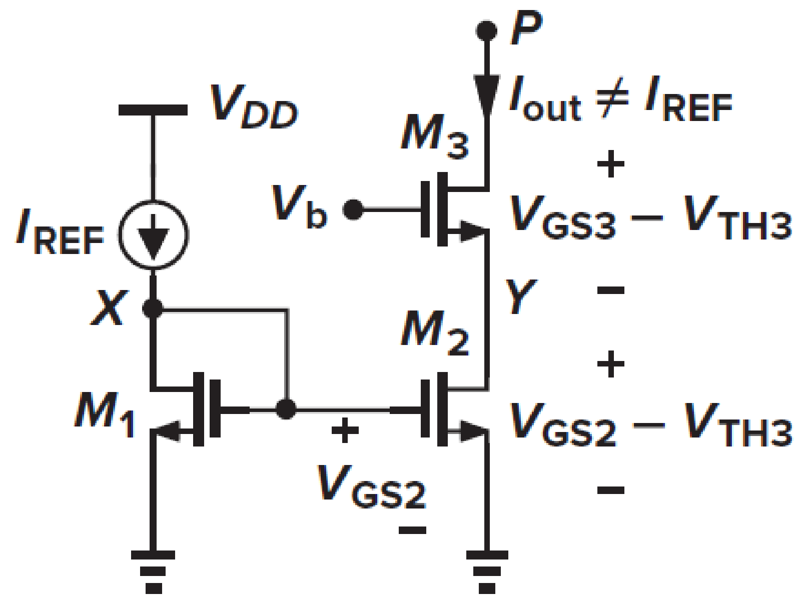


[Razavi, 2017]

Cascode CM Wastes Headroom

- Cascode wastes headroom, but we need to keep VDS equal
- First solution wastes headroom: Do not force VDS2 to be equal to VDS1
- Second solution: force VDS1 to be equal to VDS2 ☺





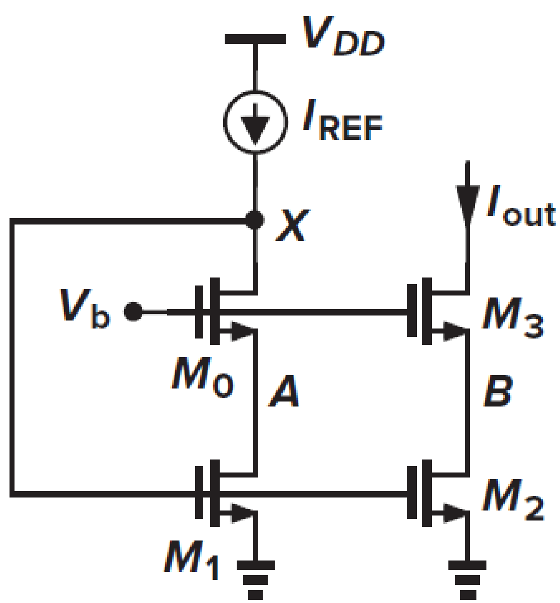
 [Razavi, 2017]

Low Voltage Cascode CM

- A.k.a. wide swing current mirror, low compliance current mirror

$$V_{TH0} + V_{ov0} + V_{ov1} < V_b < V_{TH0} + V_{TH1} + V_{ov1}$$

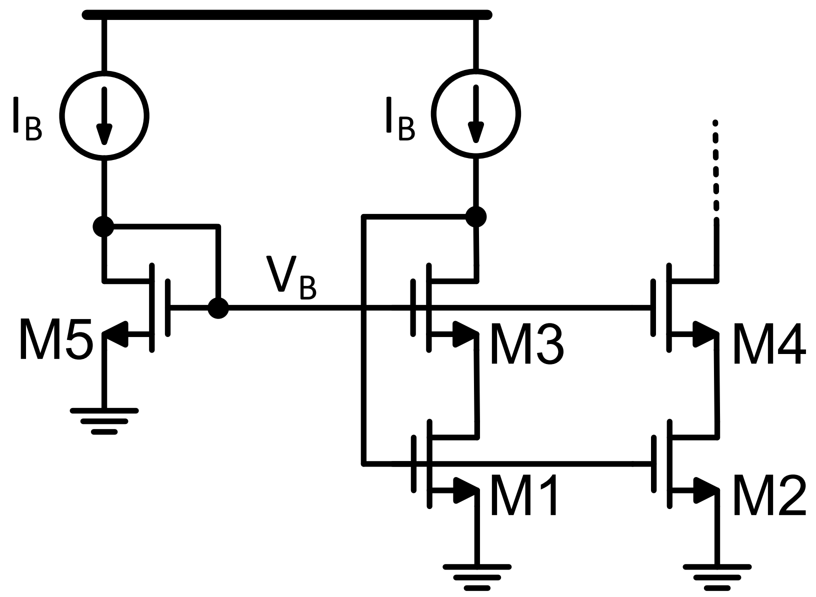
- What is the magic battery that will generate V_b?



 [Razavi, 2017]

How to Generate Vb?

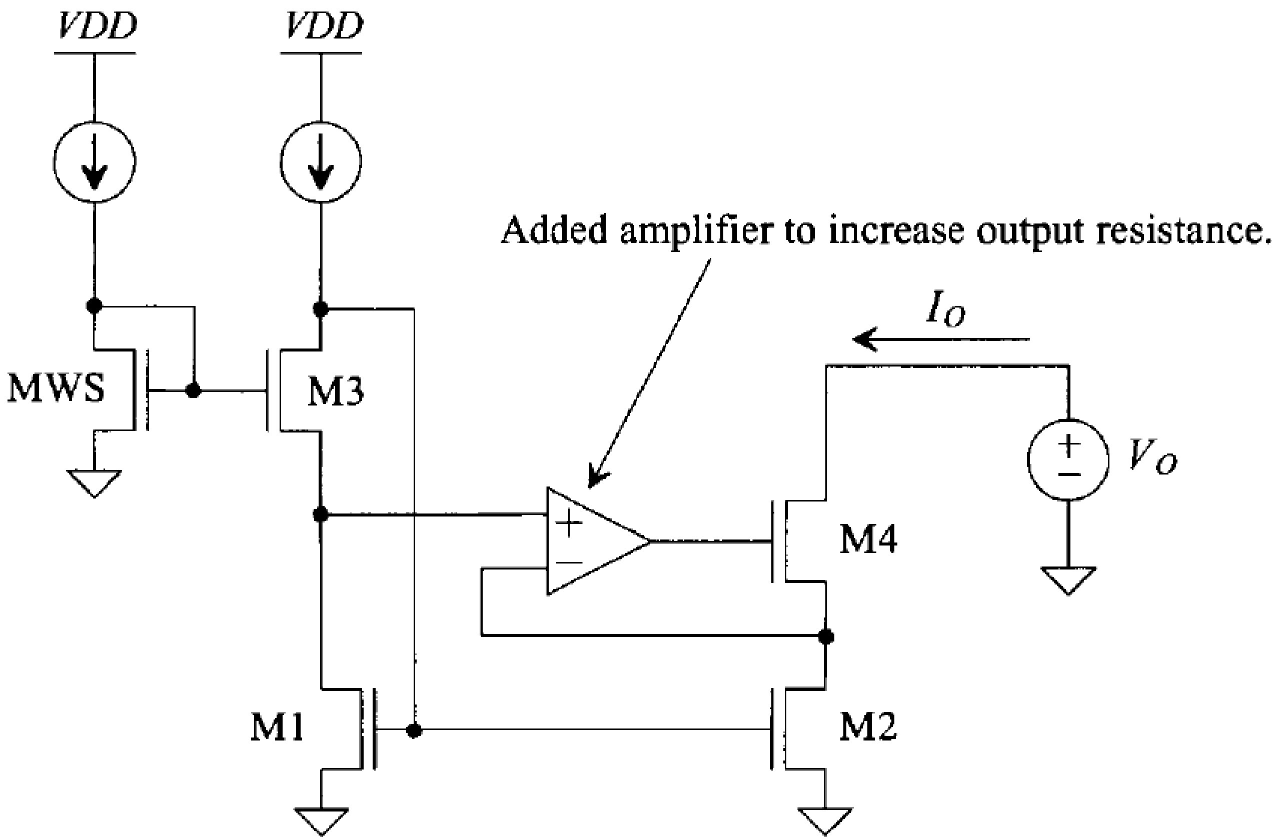
- Assume M1-M4 have the same W/L
- Length of M5 should be a little > $4L$
  - Bias M1 and M2 a little more into saturation
  - Account for body effect of M3 and M4
- M5 may be implemented as unit transistors in series



Regulated (Super) Cascode CM

- Feedback keeps $V_{DS1} \approx V_{DS2}$ and boosts R_{out}

$$R_{out} \approx r_{o,super}\left(1 + g_{m,super}R_S\right) = r_{o4}(Ag_{m4}r_{o2}) \sim A(g_m r_o^2)$$



[Baker, 2010]

Thank you!