وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Analog IC Design

Lecture 17
Slew Rate, PSRR, and Mismatch

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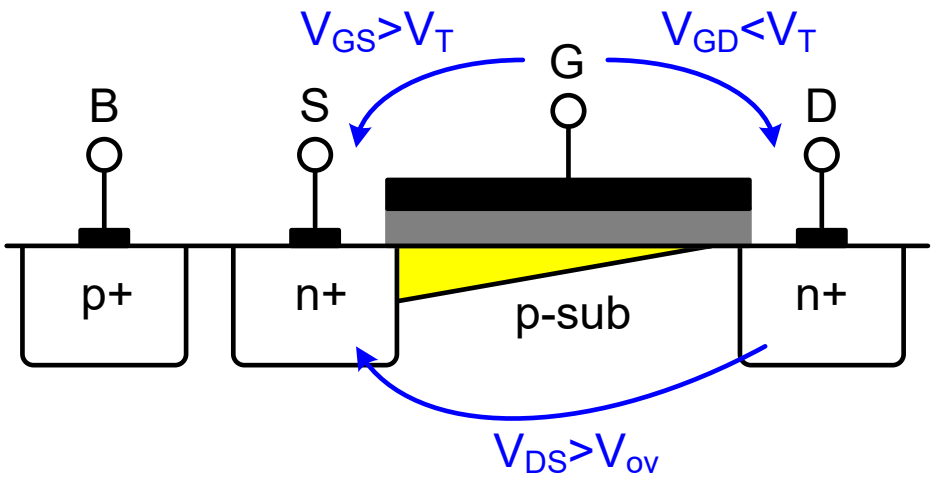
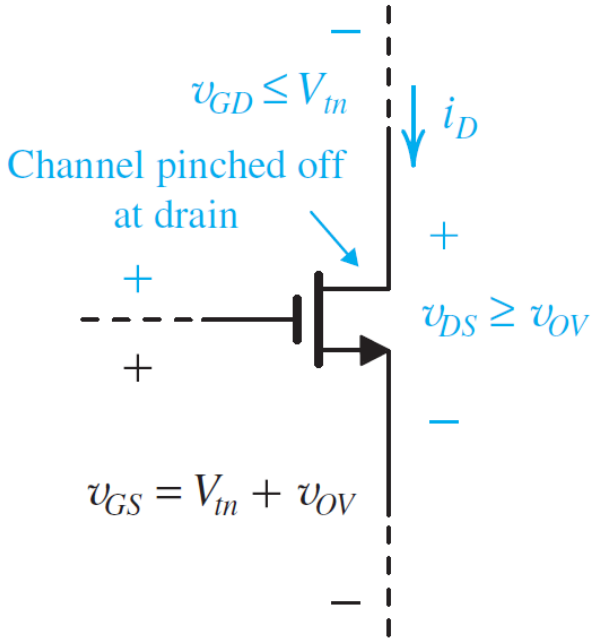
MOSFET in Saturation

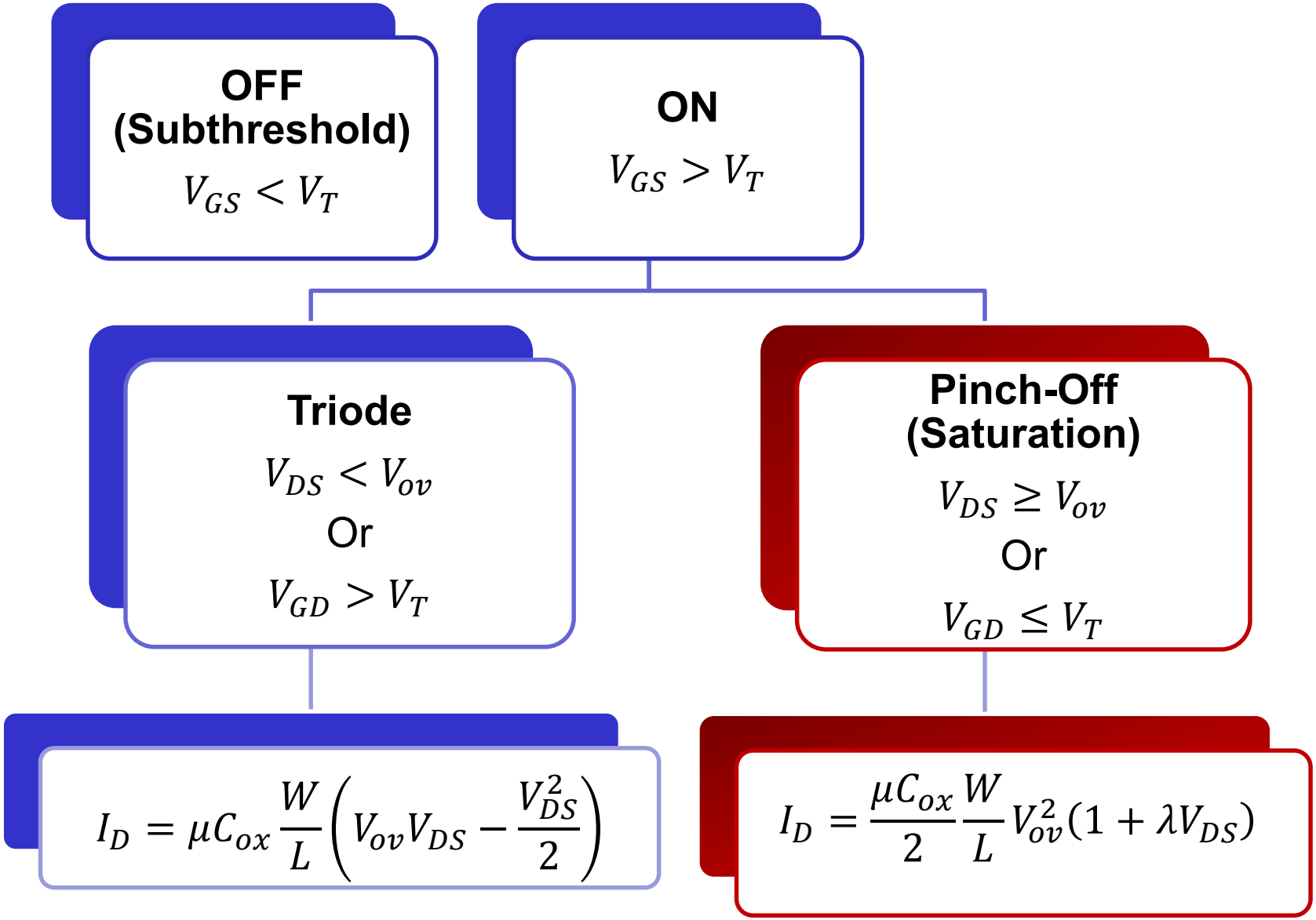
- The channel is pinched off if the difference between the gate and drain voltages is not sufficient to create an inversion layer

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L} \cdot V_{ov}^2(1 + \lambda V_{DS})$$





Regions of Operation Summary

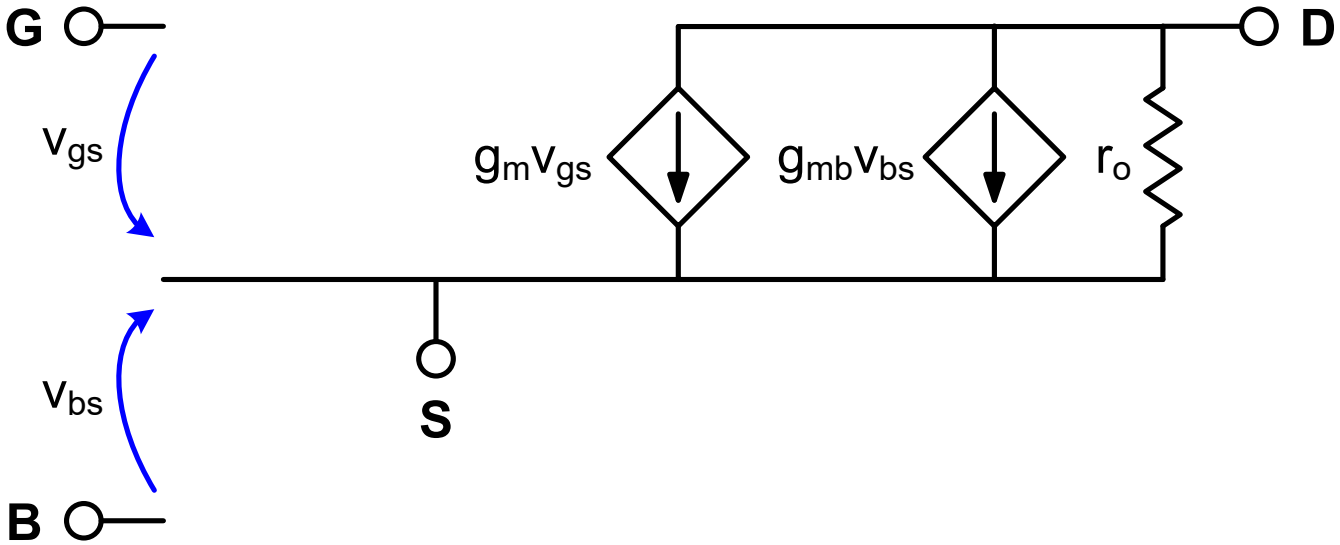


Low-Frequency Small-Signal Model

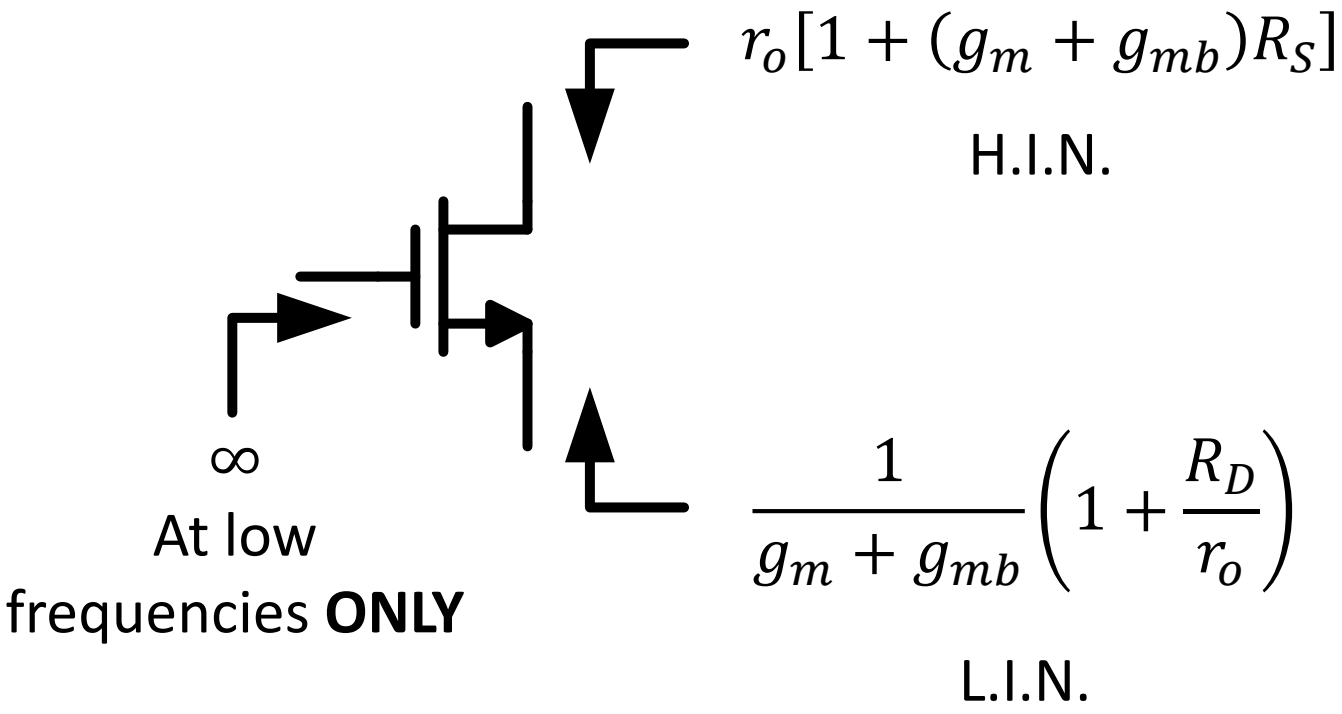
$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox}\frac{W}{L}V_{ov} = \sqrt{\mu C_{ox}\frac{W}{L}\cdot 2I_D} = \frac{2I_D}{V_{ov}}$$

$$g_{mb} = \eta g_m, \qquad \eta \approx 0.1 - 0.25$$

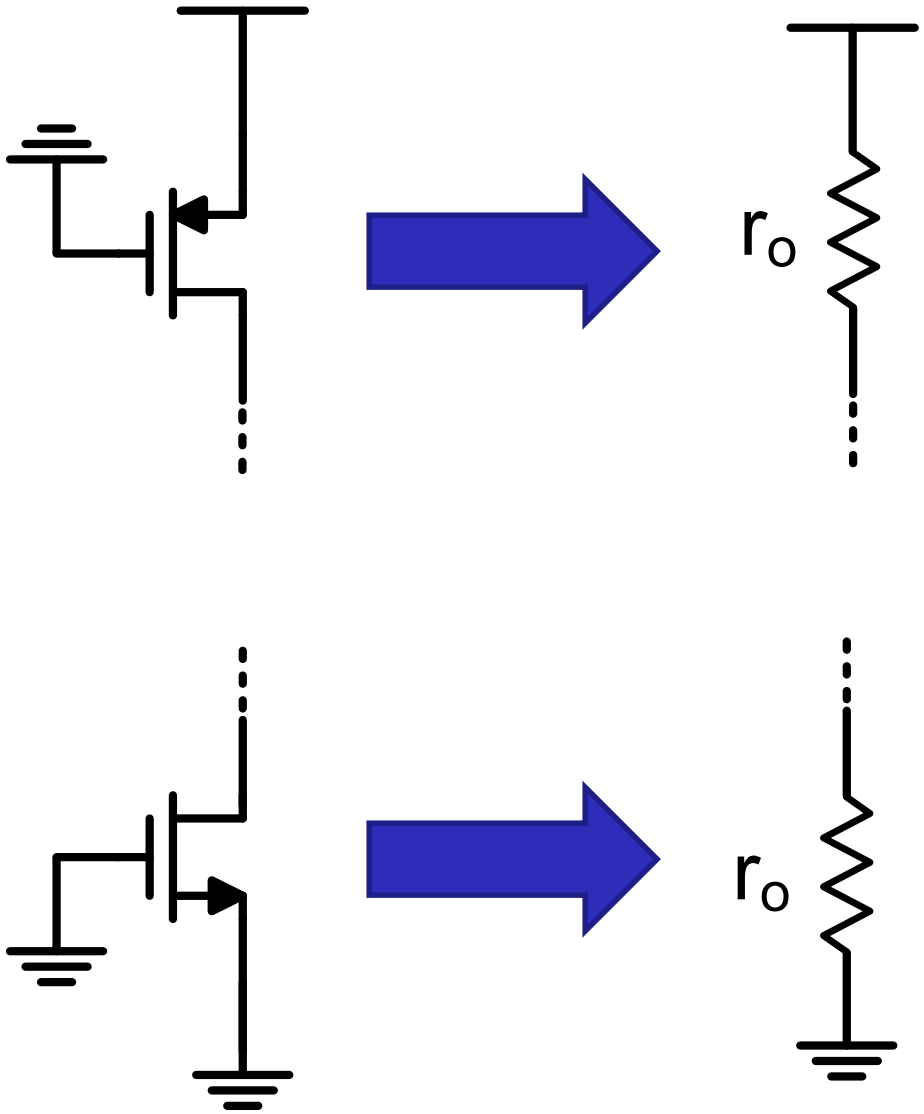
$$r_o = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{1}{\lambda I_D}, \qquad \lambda \propto \frac{1}{L}$$



Rin/out Shortcuts Summary

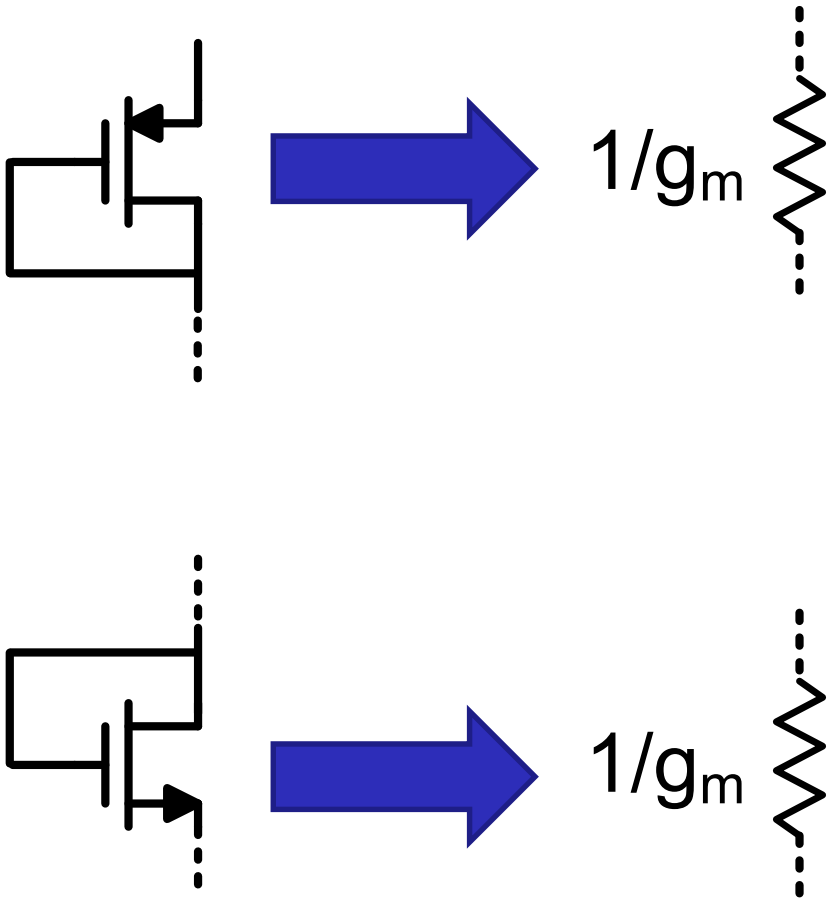


Active Load (Source OFF)



Diode Connected (Source Absorption)

- Always in saturation
- Bulk effect: $g_m \rightarrow g_m + g_{mb}$



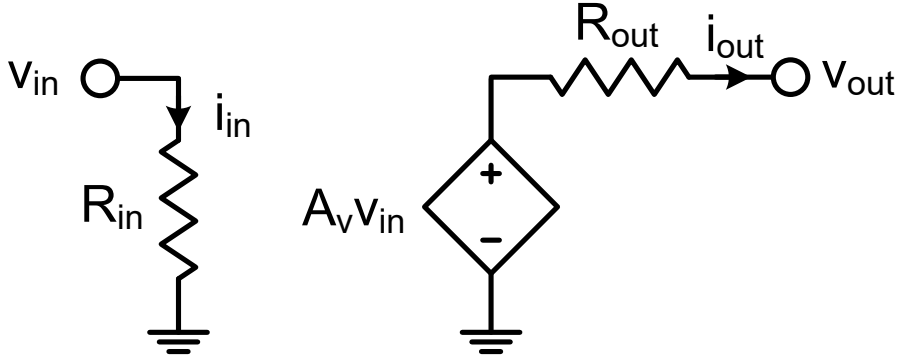
Why GmRout?

$$R_{out} = \frac{v_x}{i_x} \; @ \; v_{in} = 0$$

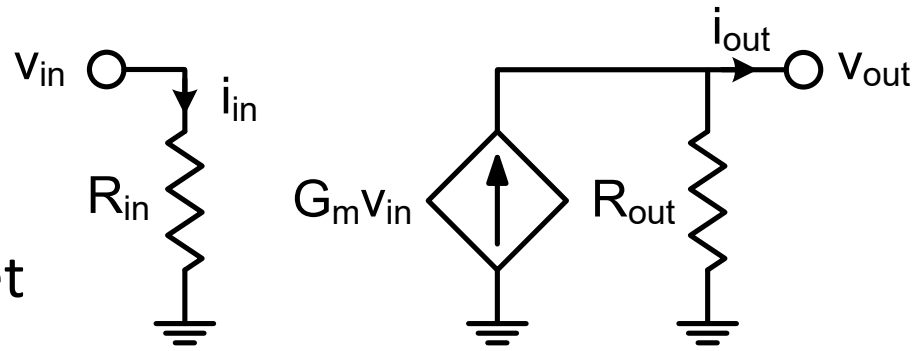
$$G_m = \frac{i_{out,sc}}{v_{in}}$$

$$A_v = G_m R_{out}$$

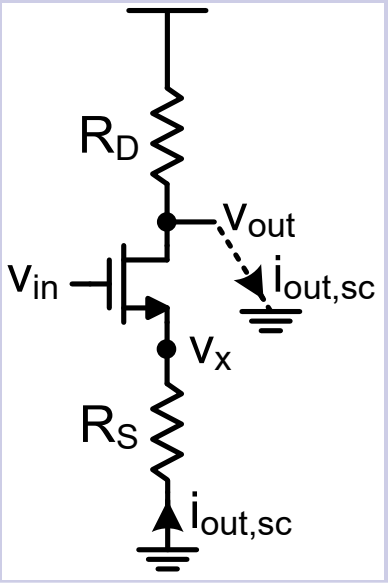
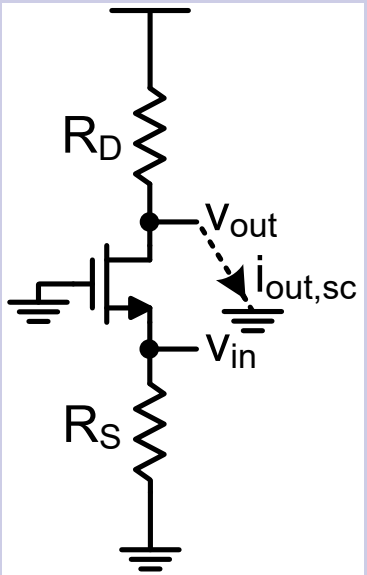
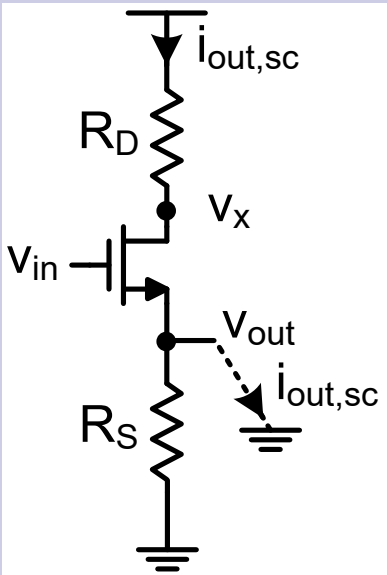
$$A_i = G_m R_{in}$$



- Divide and conquer
  - Rout simplified: vin=0
  - Gm simplified: vout=0
  - We already need Rin/out
  - We can quickly and easily get Rin/out from the shortcuts



Summary of Basic Topologies

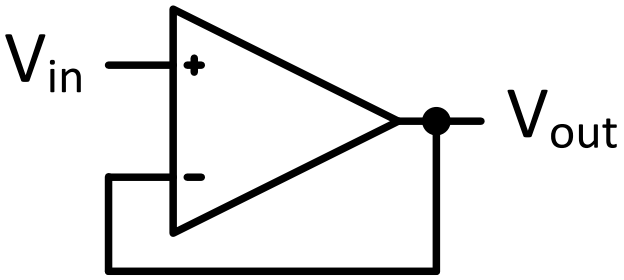
	CS	CG	CD (SF)
			
	Voltage & current amplifier	Current buffer	Voltage buffer
Rin	∞	$R_S // \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$	∞
Rout	$R_D // r_o[1 + (g_m + g_{mb})R_S]$	$R_D // r_o$	$R_S // \frac{1}{g_m + g_{mb}}\left(1 + \frac{R_D}{r_o}\right)$
Gm	$\frac{-g_m}{1 + (g_m + g_{mb})R_S}$	$g_m + g_{mb}$	$\frac{g_m}{1 + R_D/r_o}$

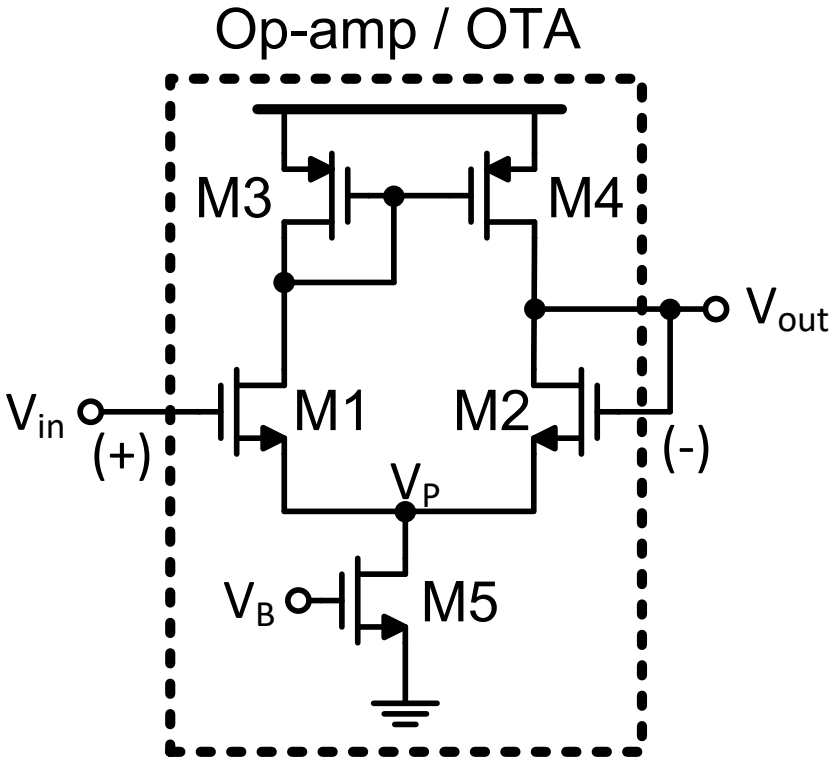
Differential Amplifier

	Pseudo Diff Amp	Diff Pair (w/ ideal CS)	Diff Pair (w/ R_{SS})
A_{vd}	$-g_m R_D$	$-g_m R_D$	$-g_m R_D$
A_{vCM}	$-g_m R_D$	0	$\frac{-g_m R_D}{1+2(g_m+g_{mb})R_{SS}}$
A_{vd}/A_{vCM}	1	∞	$2(g_m+g_{mb})R_{SS} \gg 1$

What is an OTA / Op-Amp?

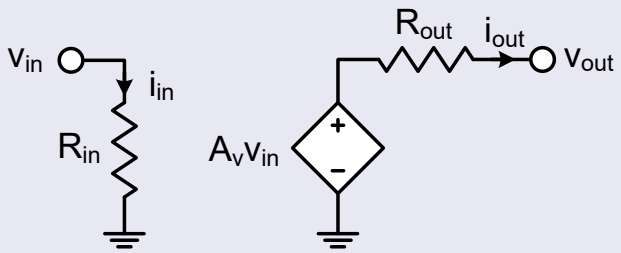
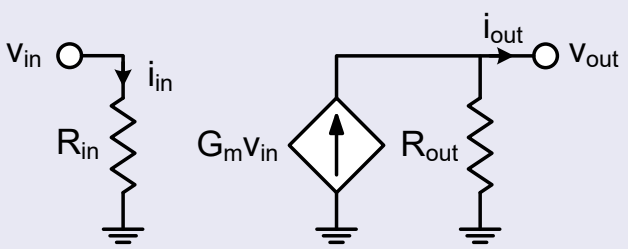
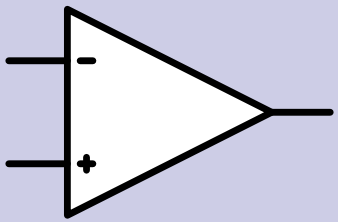
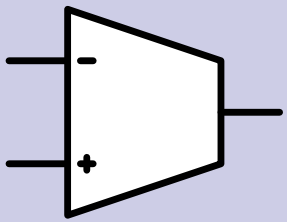
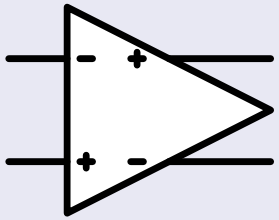
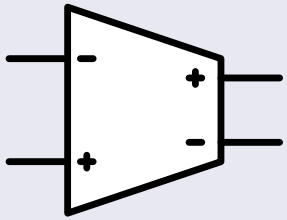
- An op-amp is simply a high gain differential amplifier
- The gain can be increased by using cascodes and multi-stage amplifiers





Op-Amp vs OTA

- An OTA is an op-amp without an output stage (buffer)
- Some designers just use op-amp name and symbol for both

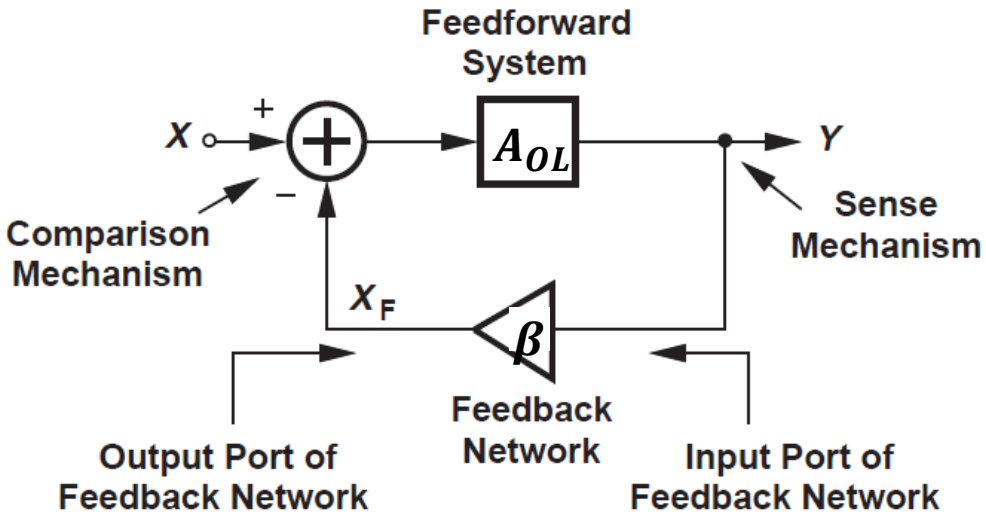
	Op-amp	OTA
Rout	**LOW**	**HIGH**
Model		
Diff input, SE output		
Fully diff		

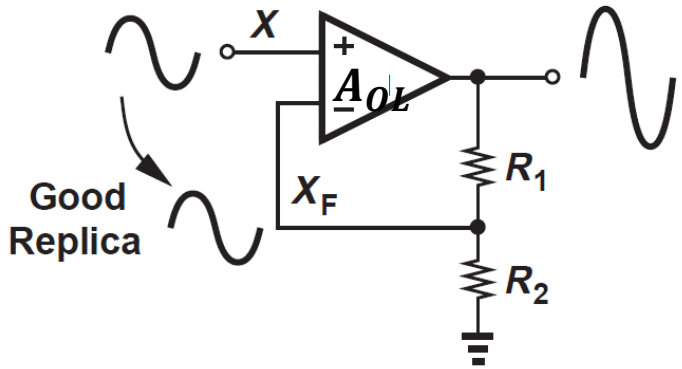
Negative Feedback

- A_{OL} = Open loop (OL) gain $\gg 1$
- $A_{CL} = \frac{Y}{X}$ = Closed loop (CL) gain
- Error signal = $X - X_F$

$$Y = A_{OL}(X - X_F) = A_{OL}(X - \beta Y)$$

$$A_{CL} = \frac{Y}{X} = \frac{A_{OL}}{1 + \beta \cdot A_{OL}} \approx \frac{1}{\beta}$$

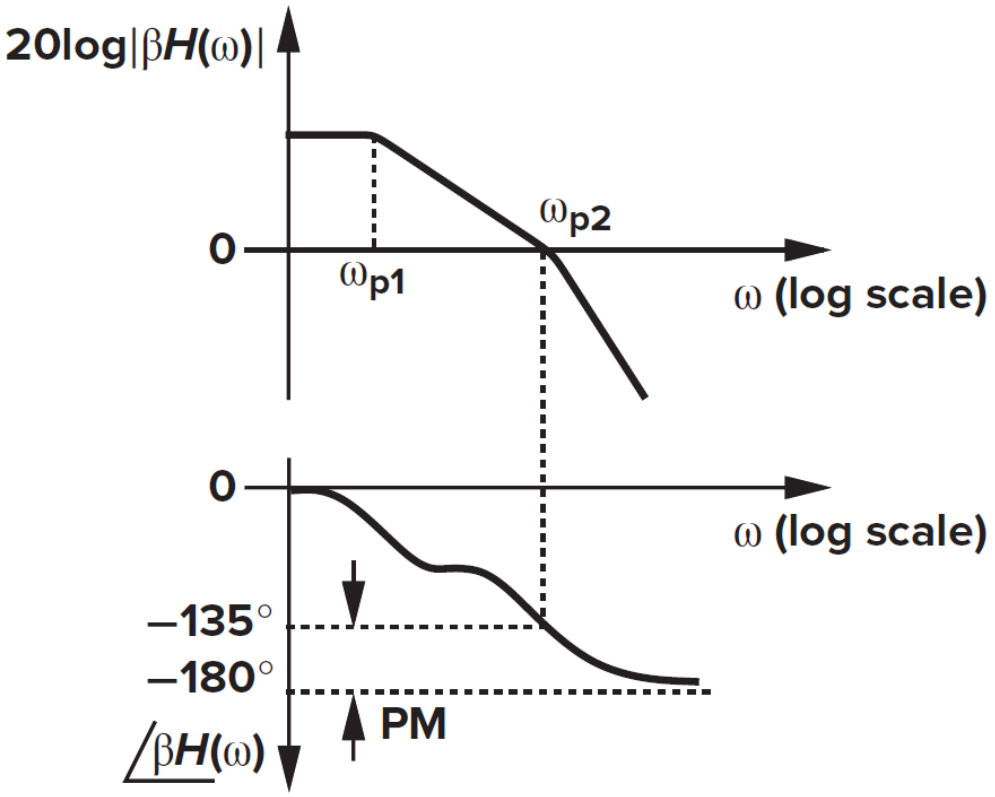


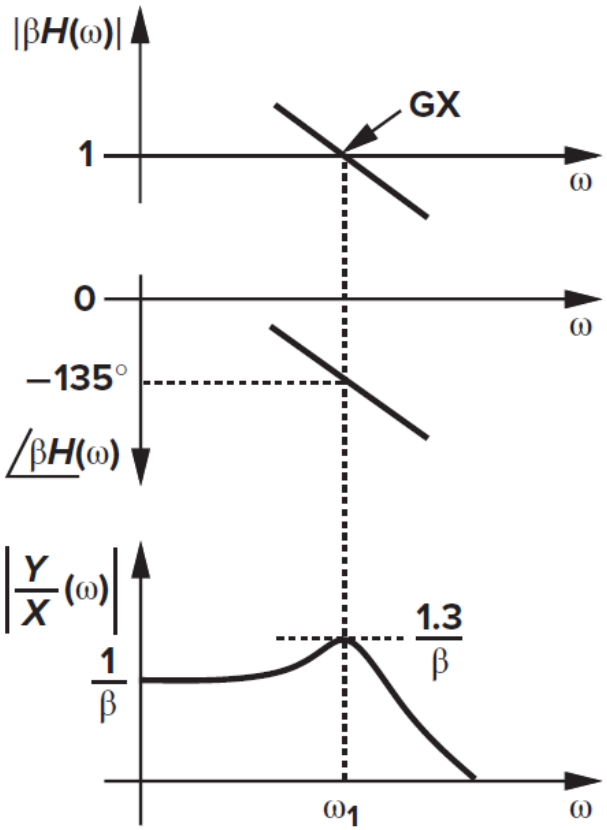


[Razavi, 2014]

Stability: Phase Margin

- If $\omega_{p2} = \omega_u$: PM = 45° → typically inadequate (peaking/ringing)
- The ultimate ω_u cannot exceed ω_{p2} → $\omega_{p1} < \omega_u < \omega_{p2}$
  - For $\omega < \omega_u$ the Bode plot is similar to a 1st order system

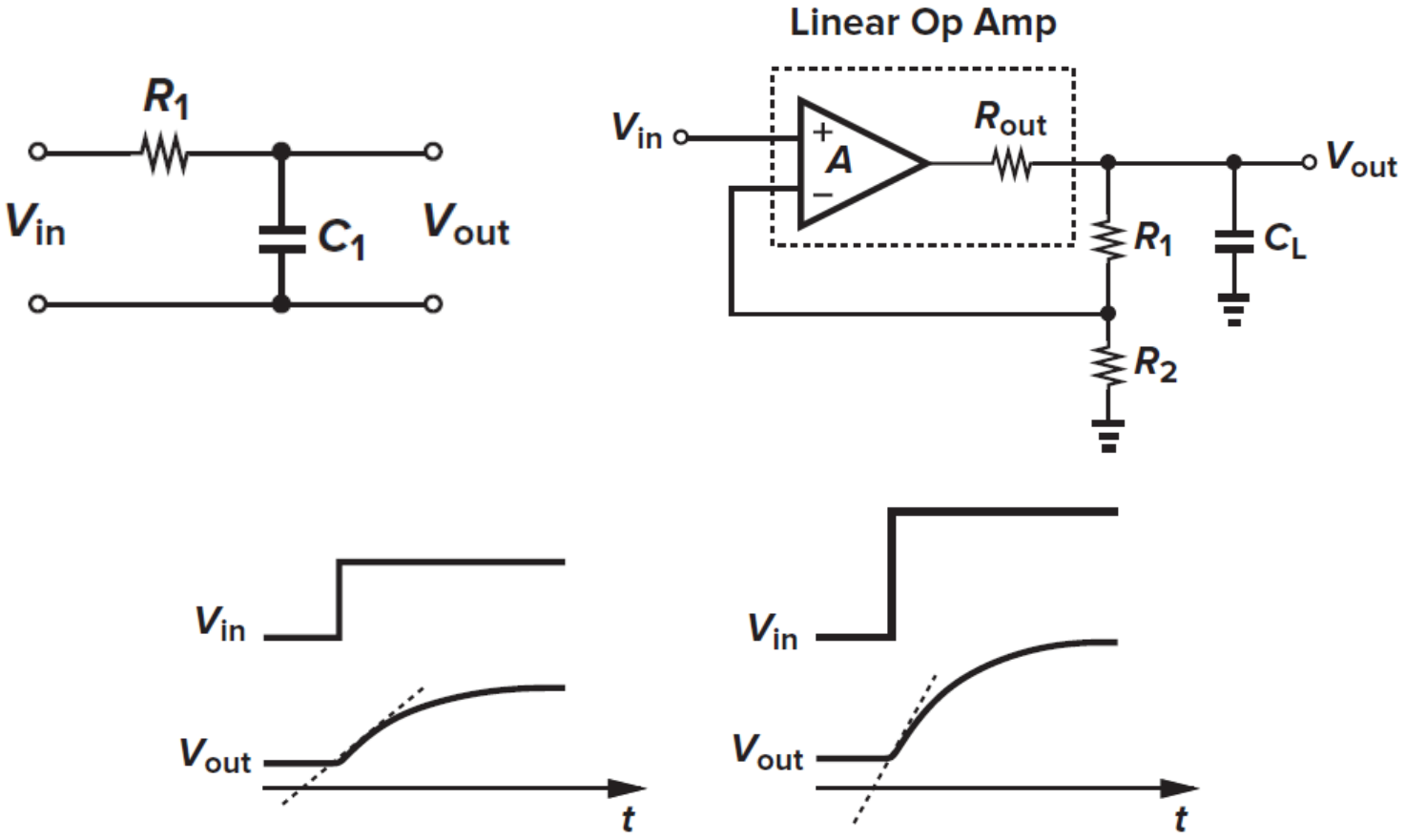




[Razavi, 2017]

Linear System

- One important property of linear systems: doubling the input doubles the output (and doubles the slope)
  - More generally: scaling the input scales the output

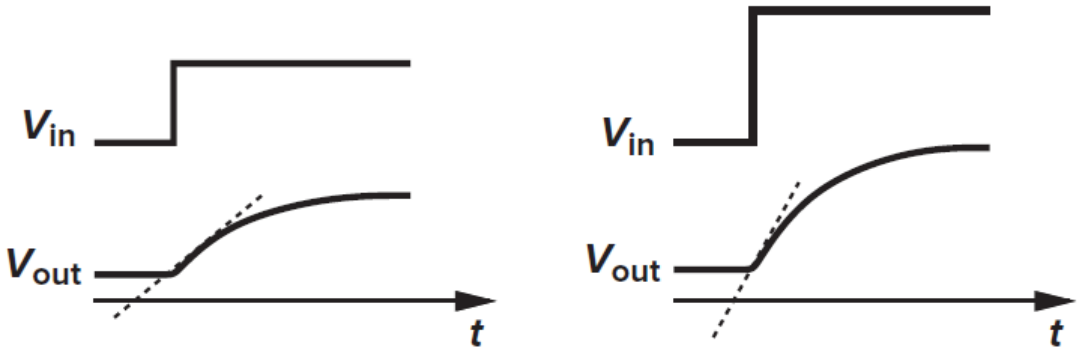


Linear System

- One important property of linear systems: doubling the input doubles the output (and doubles the slope)
  - More generally: scaling the input scales the output
- **Linear settling:** step response is exponential (slope ∝ input)

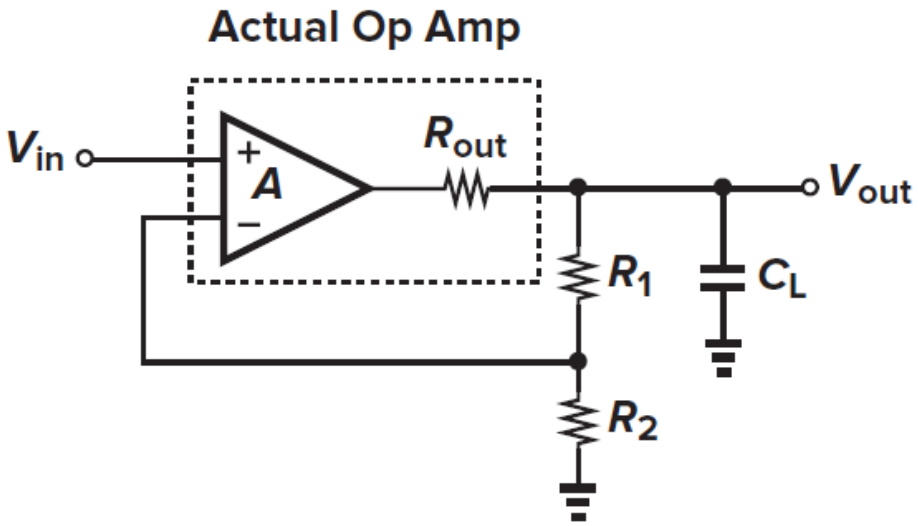
$$V_{out} = V_0[1 - \exp(-t/\tau)]$$

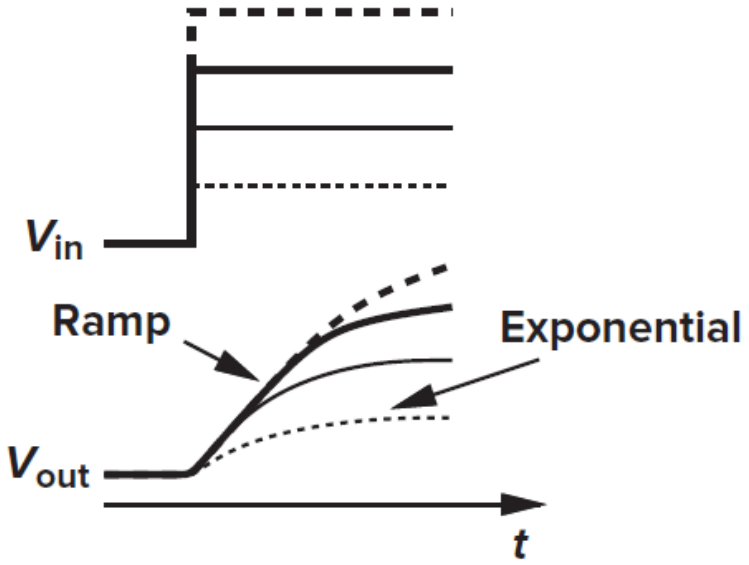
$$\frac{dV_{out}}{dt} = \frac{V_0}{\tau} \exp \frac{-t}{\tau}$$



Slewing

- **Nonlinear settling:** at large input step, the output is a linear ramp (finite constant slope)
- Slew Rate (SR $[V/\mu s]$): the maximum possible slope of the op-amp output
  - Independent of the input level → nonlinear behavior
- Linear ramp → constant current (current source) charging a capacitor

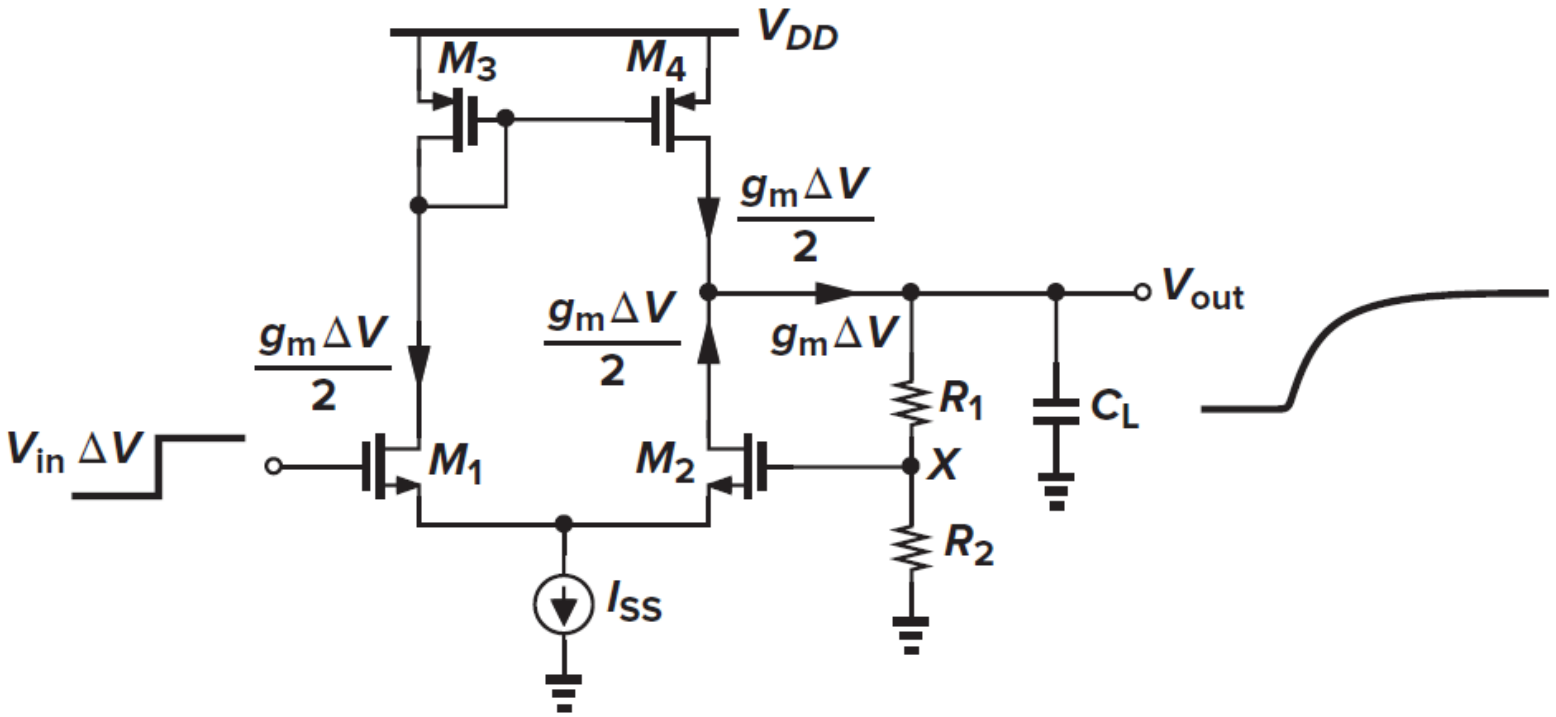




[Razavi, 2017]

Small Input Step: Linear Settling

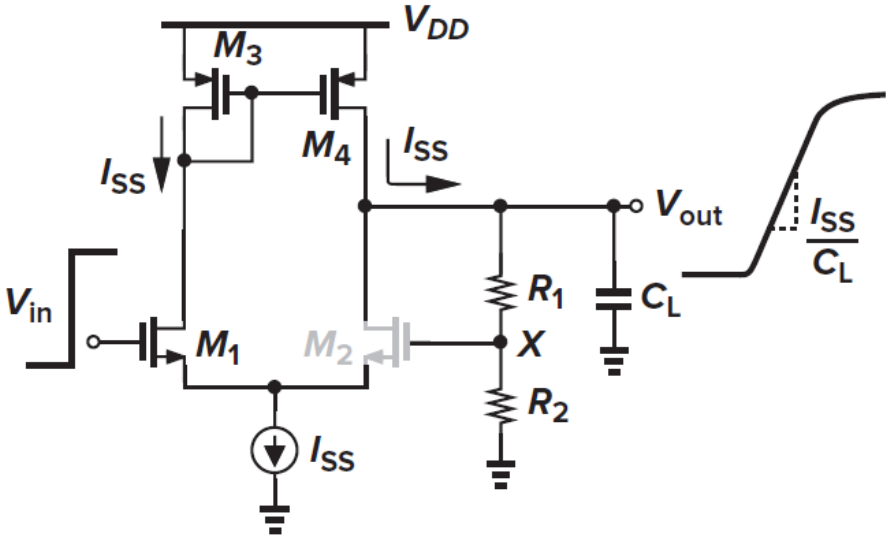
- Assume R_1 *and* R_2 are very large
- Linear settling: charging current (and consequently slope) is proportional to input signal

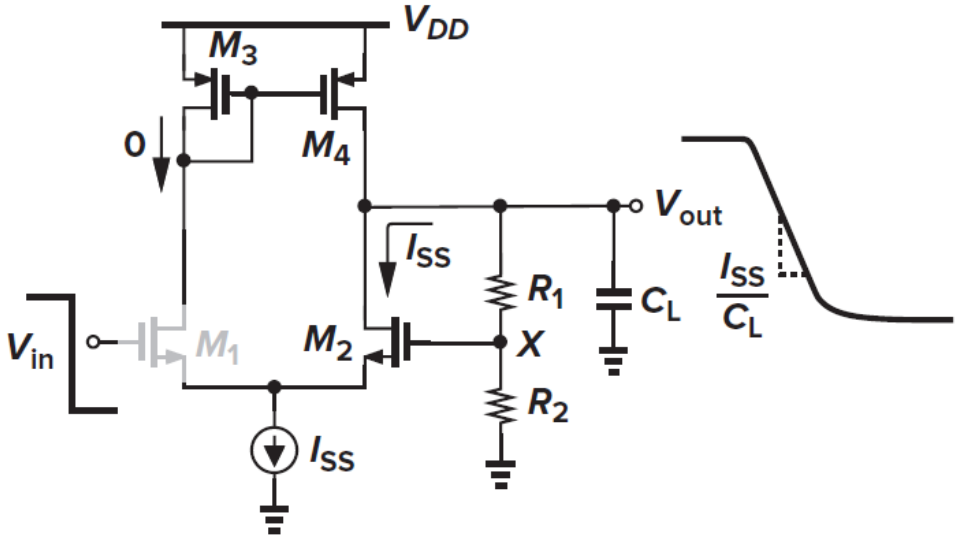


[Razavi, 2017]

Large Input Step: Slewing

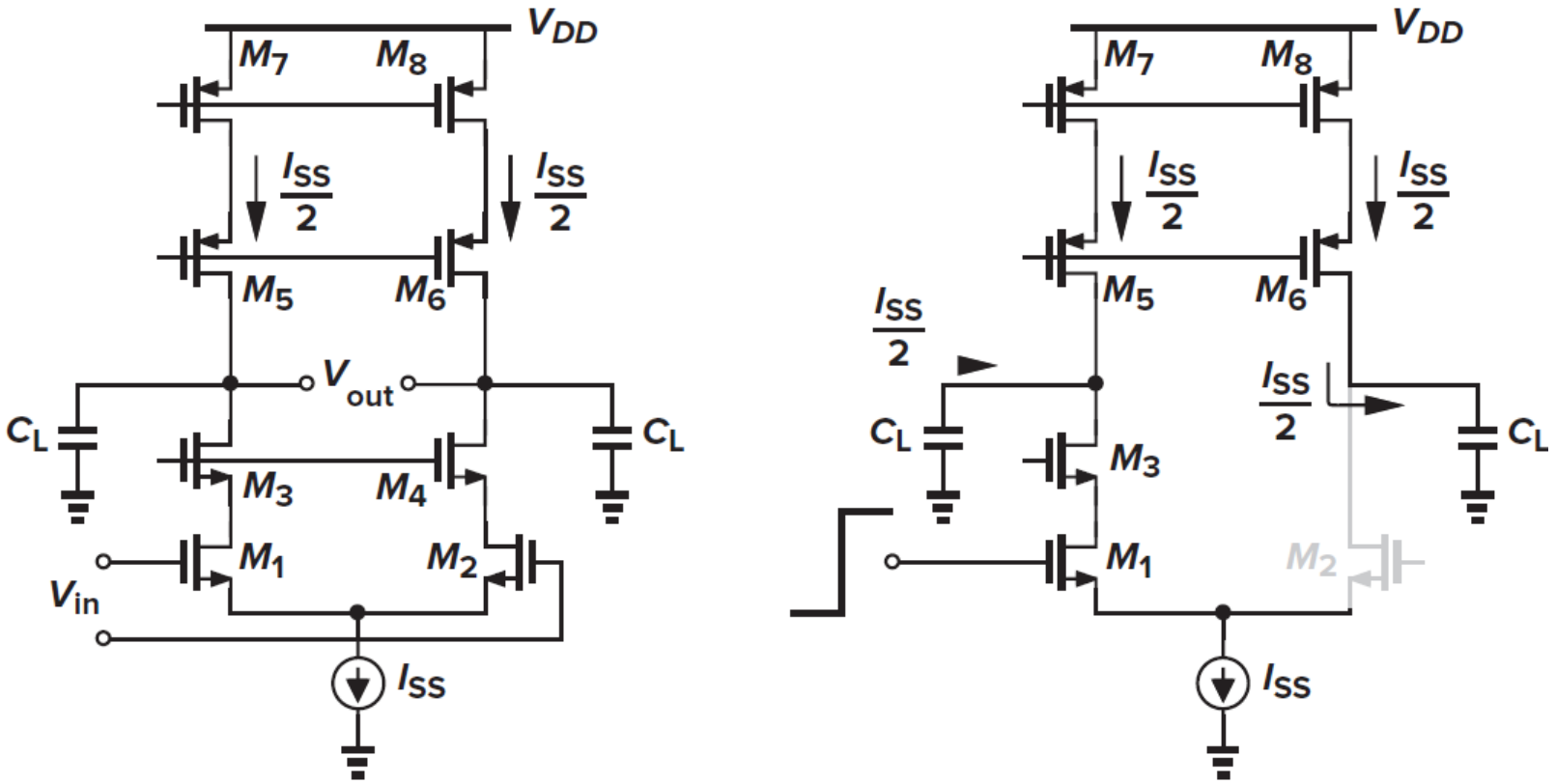
- Assume R_1 and R_2 are very large
- M2 OFF, I_{SS} is fully steered to M1 → M3 → M4 then to C_L
- Non-linear settling: charging current (and consequently slope) is constant (I_{SS}) independent of input signal
- As V_X approaches V_{in} the circuit resumes linear settling (exp)





SR of Telescopic Cascode

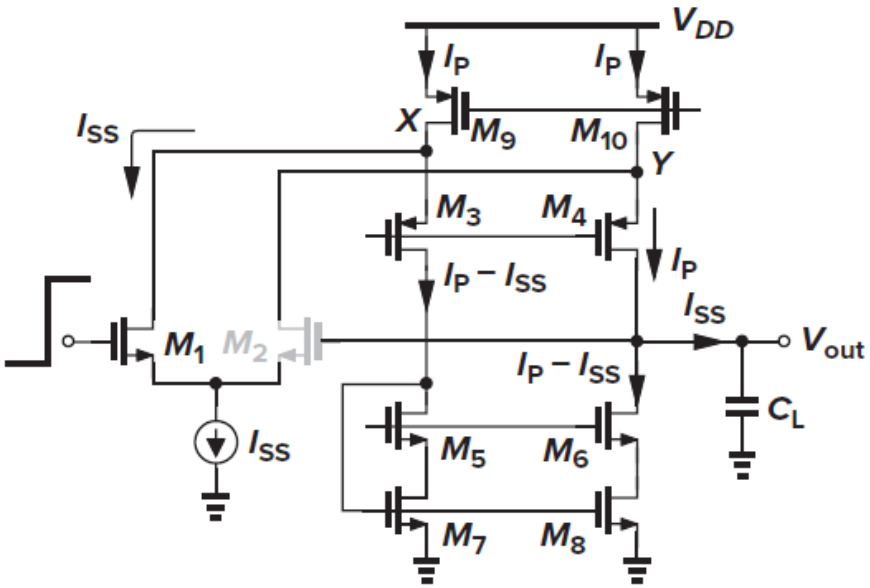
- $V_{out1}\ and\ V_{out2}: SR = \frac{I_{SS}}{2}/C_L$
- $V_{od} = V_{out1} - V_{out2}: SR = I_{SS}/C_L$

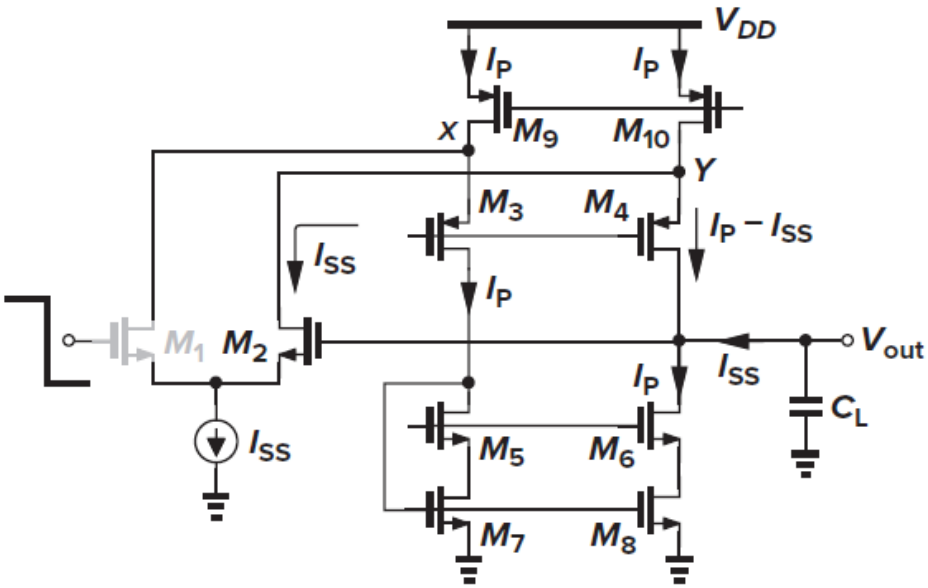


[Razavi, 2017]

SR of Folded Cascode

- $SR = I_{SS}/C_L$
- Select I_P slightly larger than I_{SS}
- SR is independent of I_P

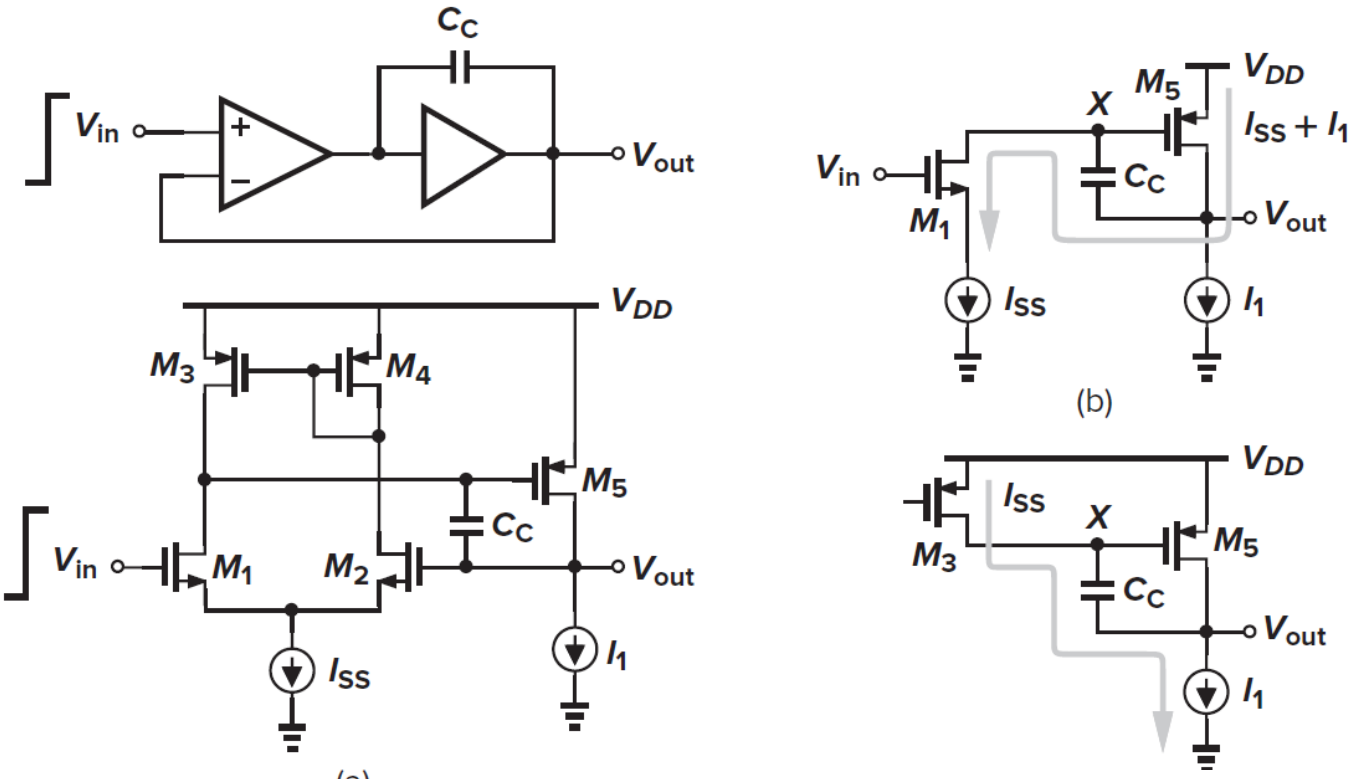




[Razavi, 2017]

SR of Two-Stage Miller OTA

- Step UP: M2 OFF → M4 OFF → M3 OFF, I_{SS} steered to M1 then C_C
- Step Down: M1 OFF, I_{SS} steered to M2 → M4 → M3 then C_C
- $SR = I_{SS}/C_C$
- I_1 much larger than I_{SS} → SR is independent of I_1

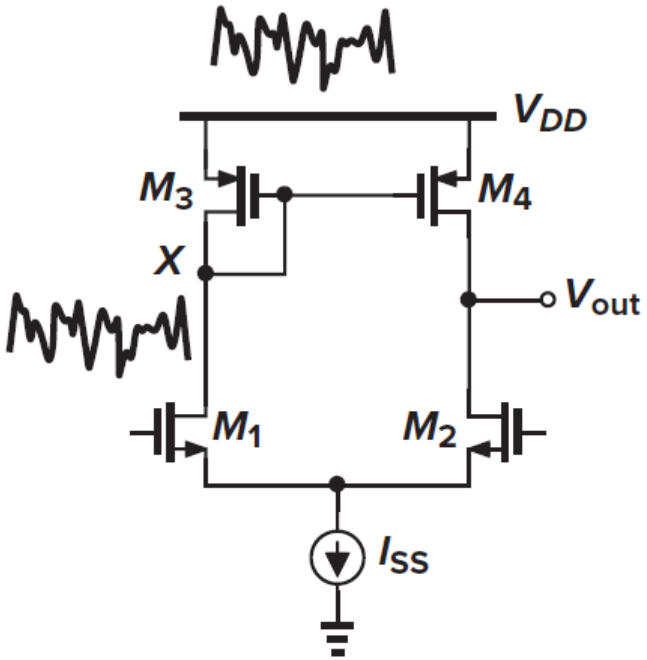


[Razavi, 2017]

Power Supply Rejection (PSR)

- The OTA should reject noise on the supply line
  - The diode-connected device "clamps" node X to VDD
  - Vx and Vout experience approximately the same change as VDD

$$PSRR = \frac{V_o/V_{in}}{V_o/V_{DD}} \approx g_{m1,2}(r_{o2}//r_{o4})$$



Quiz: PSRR of 5T OTA

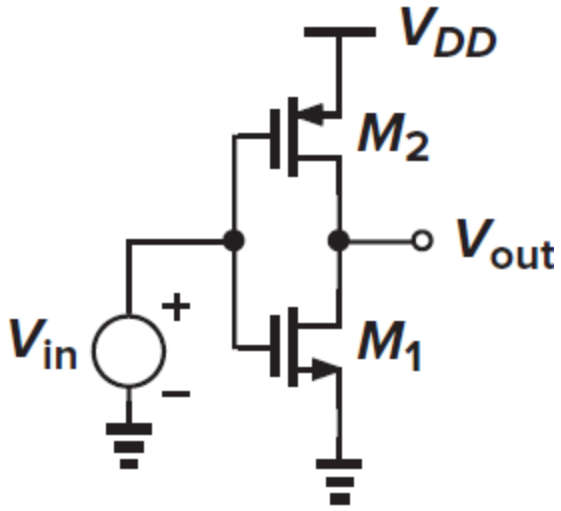
- Derive the PSRR for a 5T OTA with PMOS input pair
  - Assume the tail current source is generated by a simple current mirror.
- What is the relation between the PSRR you derived and the CMRR?

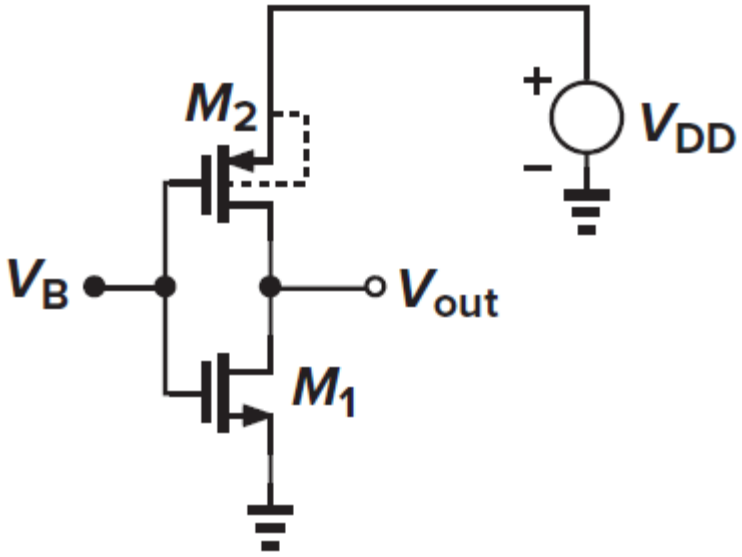
Quiz: PSRR of Complementary CS

- Find the PSRR of the complementary CS amplifier (inverter-based amplifier)

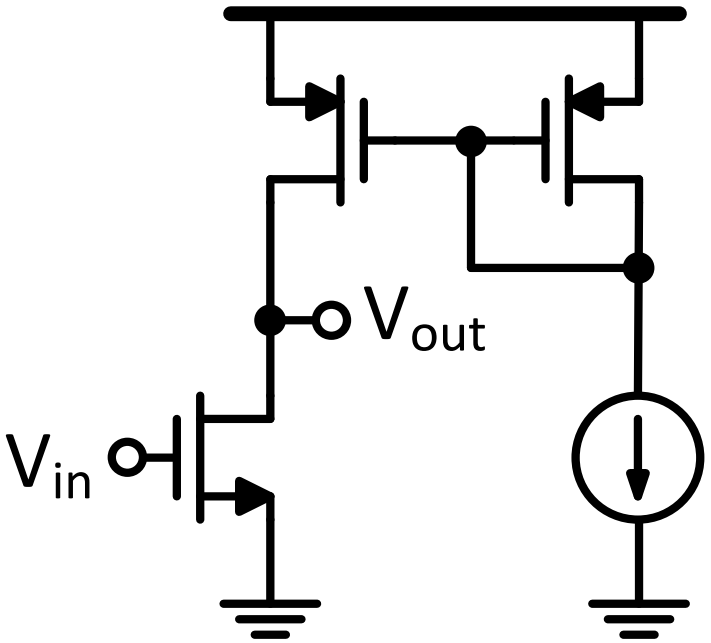
$$PSRR = \frac{V_{out}/V_{in}}{V_{out}/V_{DD}}$$

- It is worth noting that it has a very poor PSRR!



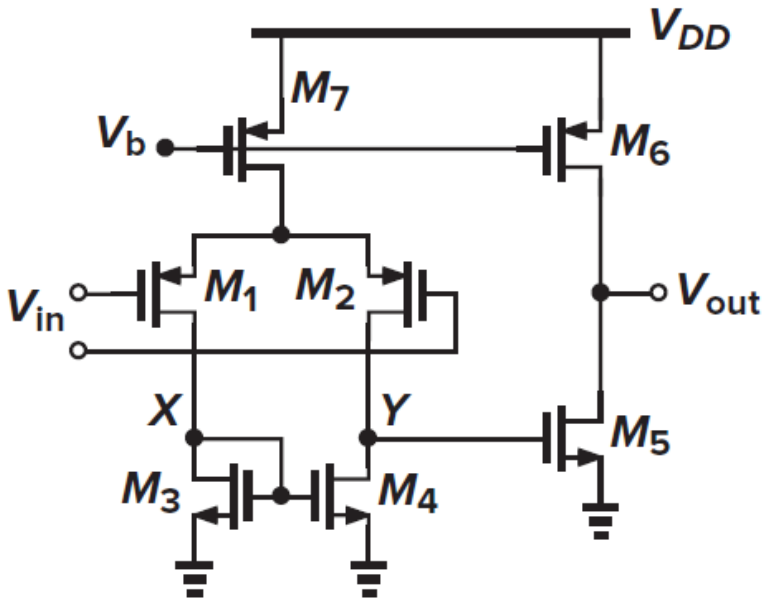


Quiz: PSRR of CS with Active Load



Quiz: PSRR of Miller OTA

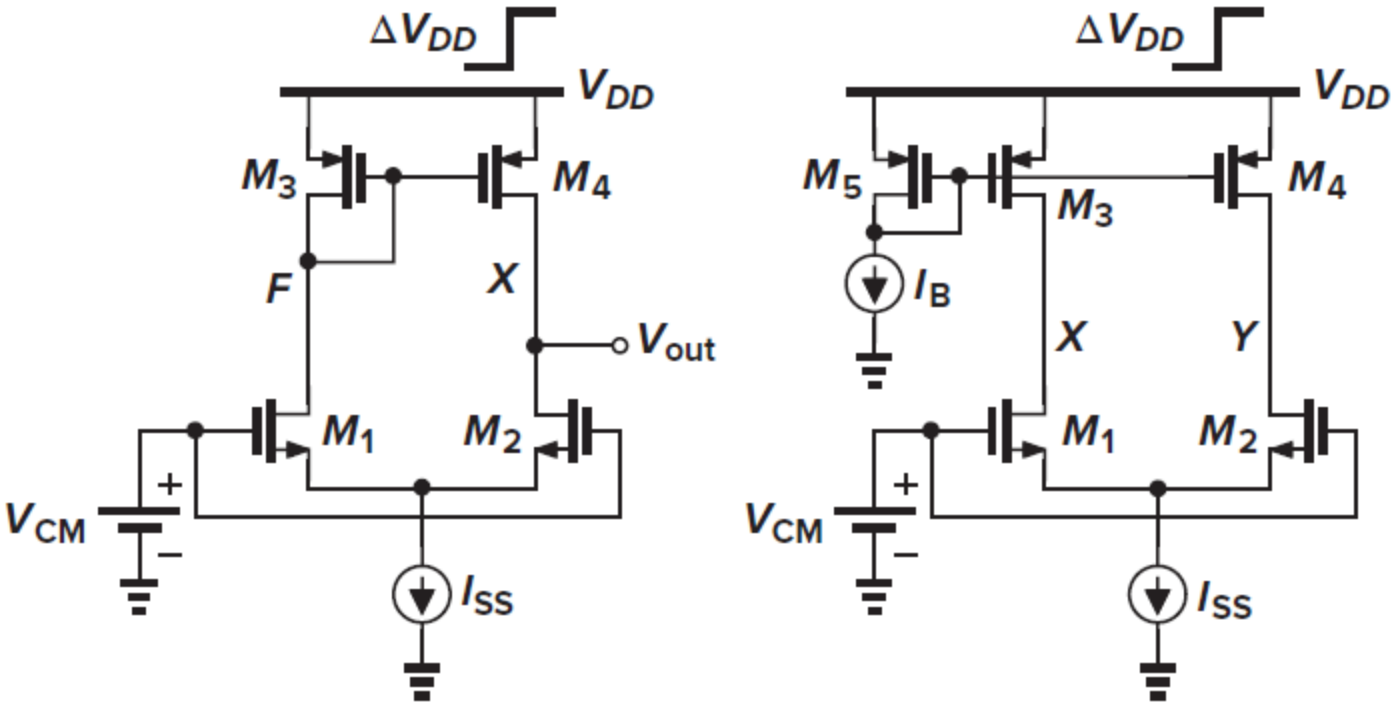
- Assume all transistors have the same λ (not the same ro)
- Note that $v_{gs6} = v_{gs7} = 0$ (why?) → M6 and M7 are source OFF
- First stage: VDD → VY → Vout: $\left(\frac{V_{out}}{V_{DD}}\right)' = \frac{V_Y}{V_{DD}} \cdot \frac{V_{out}}{V_Y}$
- Second stage: $\left(\frac{V_{out}}{V_{DD}}\right)'' = \frac{V_{out}}{V_{DD}}$



[Razavi, 2017]

PSRR: SE Output vs Fully Differential

- In both cases ΔV_{DD} gets transferred to the output
  - But for the fully diff amp, the differential output is not affected

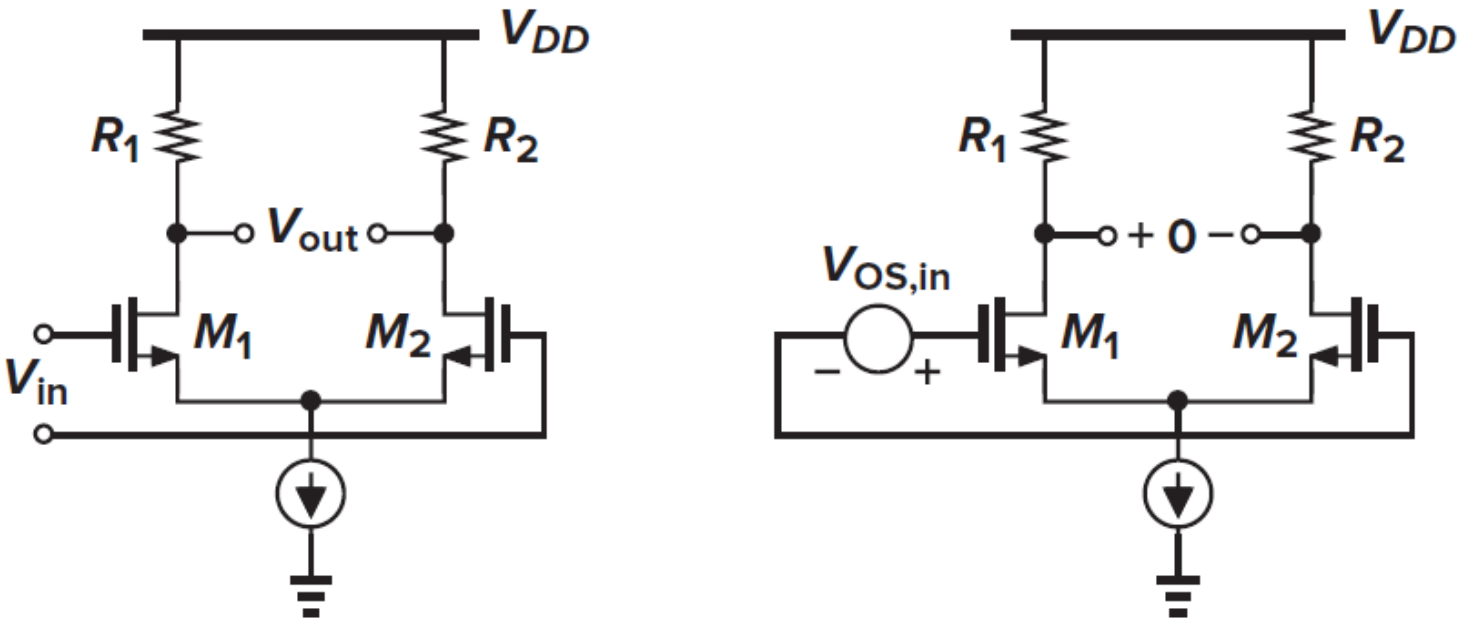


Mismatch

- We mostly assumed the two sides of differential amplifiers are perfectly symmetric
- In reality, however, nominally-identical devices suffer from a finite mismatch due to variations in the manufacturing process
- One of the most important mismatch effects in MOS devices is the threshold voltage mismatch
  - VTH is a function of the doping levels in the channel, and these levels vary randomly from one device to another

Mismatch Effects: DC Offset

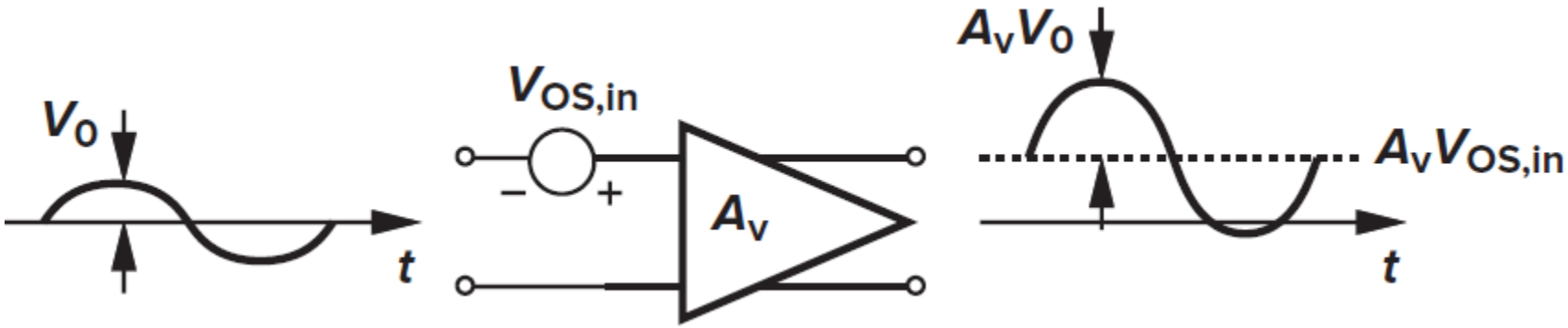
- With Vin = 0 and perfect symmetry: Vout = 0
- But in the presence of mismatches Vout ≠ 0
- The input-referred offset voltage: the input level that forces the output voltage to go to zero



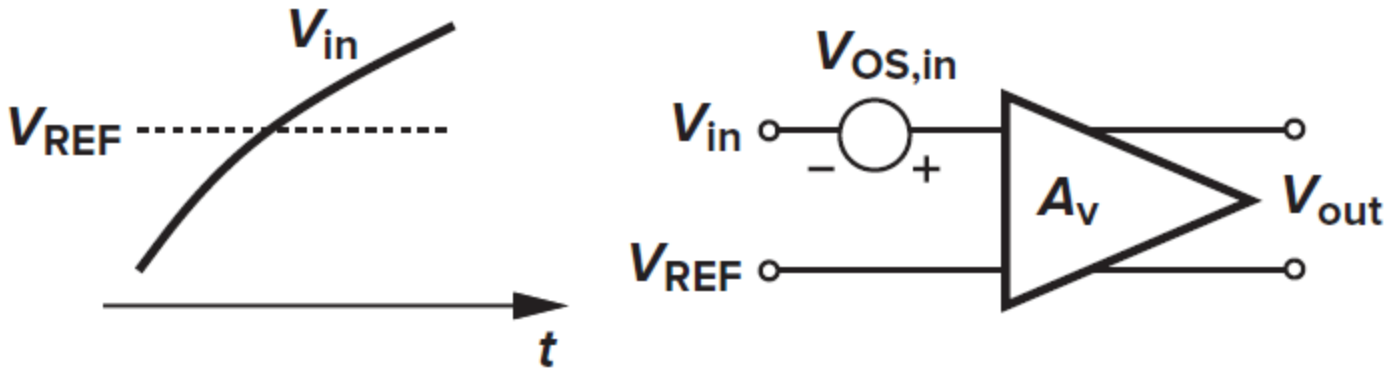
[Razavi, 2017]

Effect of Offset Voltage

- For high gain amplifier, dc offset may drive the amplifier into nonlinear operation

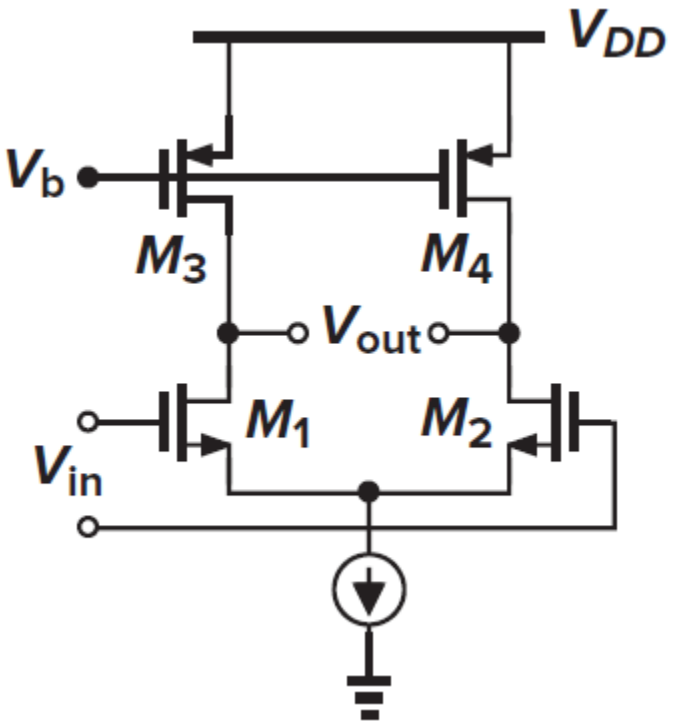


- Finite error when comparing a signal to a reference



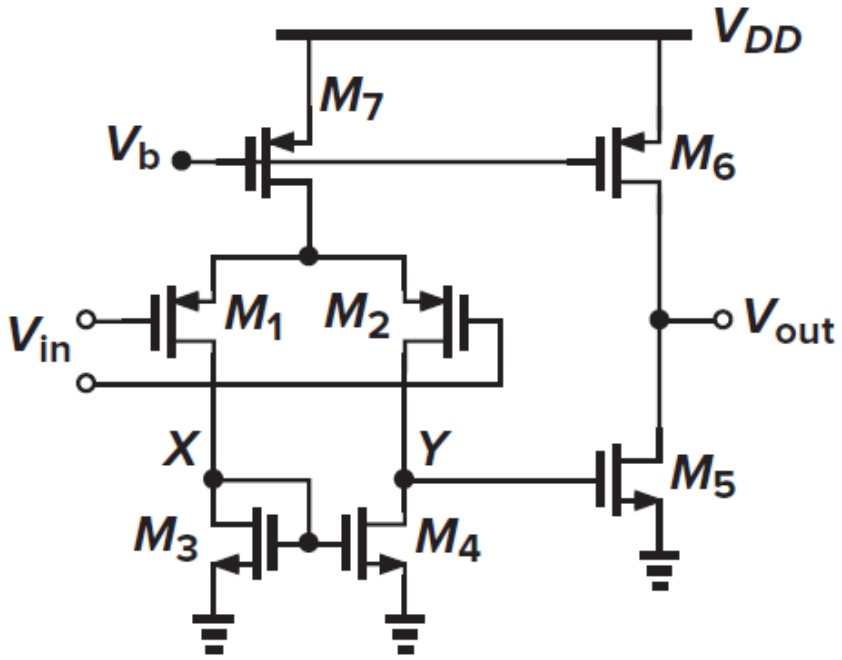
Bonus Question

- If the PMOS load has threshold voltage mismatch equal to ΔV_{THP}, calculate the input referred offset voltage



Miller OTA: Systematic Mismatch/Offset

- To avoid systematic mismatch, X and Y must have the same voltage
  - Design the 2nd stage such that $V_{GS5} = V_{GS3}$



Pelgrom's Model

- The standard deviation of random within die (WID) variations is inversely proportional to the square root of the transistor area (WL)
- This makes sense intuitively because variations tend to average out over a larger area

$$\Delta V_{TH} = \frac{A_{VTH}}{\sqrt{WL}}$$

$$\Delta\left(\mu C_{OX}\frac{W}{L}\right) = \frac{A_K}{\sqrt{WL}}$$

- $A_{VTH}\ and\ A_K$ are constants (Pelgrom's coefficients) obtained from measurements

Quiz

- $\sigma_{V_t} = A_{V_t}/\sqrt{WL}$, $A_{V_t} = 2\ mV \cdot \mu m$ for 45nm process
- Calculate the standard deviation in threshold voltage for the following devices
  1. $\frac{W}{L} = \frac{2\mu m}{0.5\mu m}$
  2. $\frac{W}{L} = \frac{200nm}{50nm}$
- If the subthreshold slope is 100mV/decade, what is the percent increase in subthreshold current for three sigma variation?

$$I_{\text{off}} \propto \frac{W}{L} 10^{-\frac{V_t}{S}} = \frac{W}{L} \mathrm{e}^{-\frac{V_t}{n v_T}}$$

Quiz

- $\sigma_{V_t} = A_{V_t}/\sqrt{WL}$, $A_{V_t} = 2\ mV \cdot \mu m$ for 45nm process

1. $\frac{W}{L} = \frac{2\mu m}{0.5\mu m}$

   10^(3*2/100) – 1 = 15%

2. $\frac{W}{L} = \frac{200nm}{50nm}$

   10^(3*20/100) – 1 = 300%

Thank you!