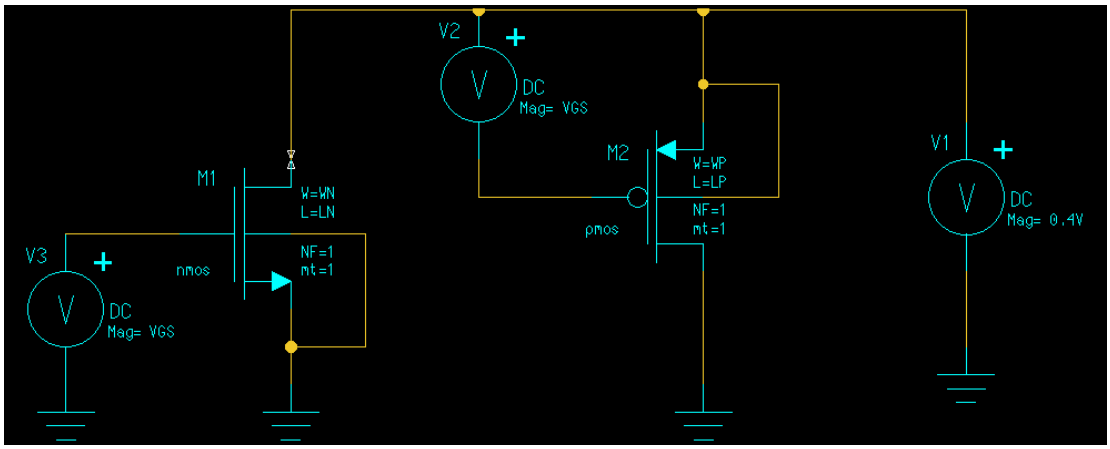
Analog IC Design
Lab 05
Simple vs Low Compliance Cascode Current Mirror

In this lab, we will compare a low voltage current mirror with a simple current mirror. We will also learn how to use hierarchical cell-based design.

Part 1: Sizing Chart

a) First, we will create a design chart to help in the design process as shown below. **We will use the both NMOS and PMOS in this lab.**

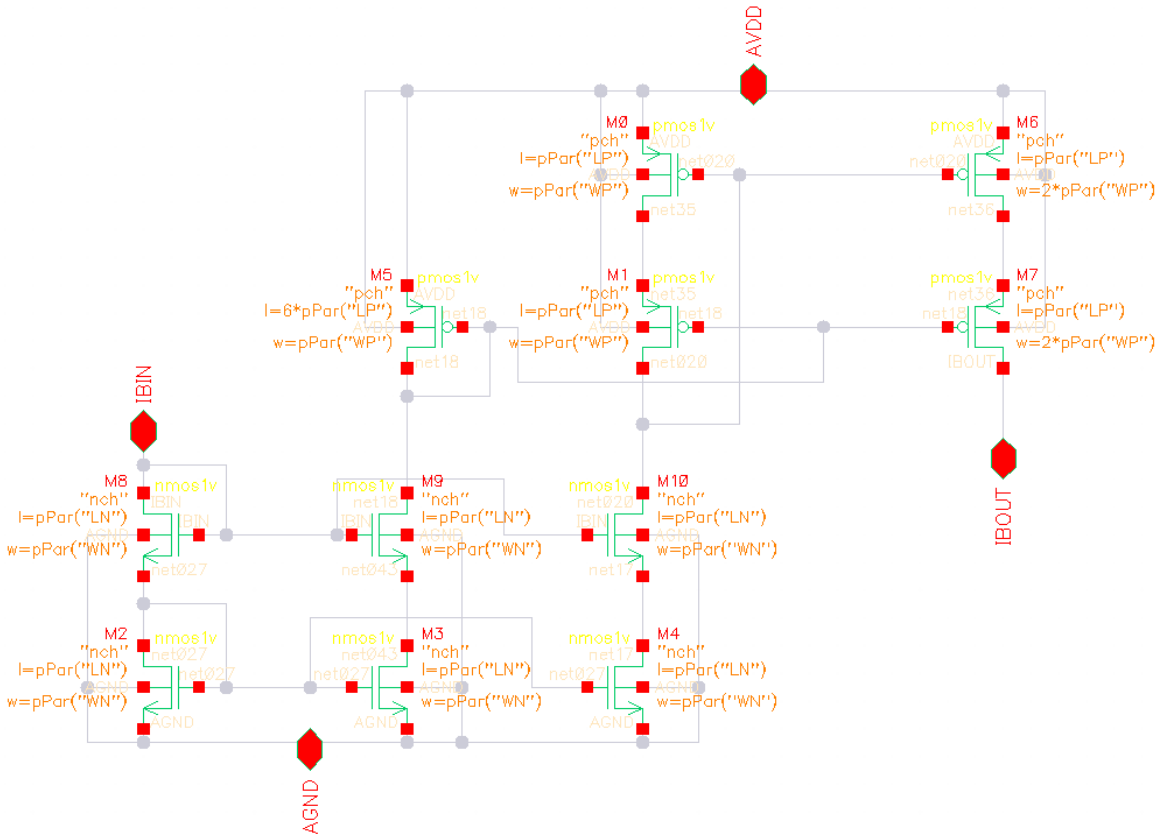


b) Use $W = 10\mu m$ and $L = 1\mu m$.
c) Sweep VGS from 0 to $\approx V_{TH} + 0.4V$ with 10mV step. Set $V_{DS} = 0.4V$.
d) For both the NMOS and PMOS, report the following parameters vs VGS:
   a. vdss (vdss is the drain-source saturation voltage, i.e., VDS > vdss for saturation. It is equivalent to V_{ov} for a square-law device. It is also known as vdsat).
   b. ID
e) Place a cursor on the point at which vdss = 100mV. Report ID at this point (let's refer to it as IDx).
f) I_D is always proportional to W. We want to design our circuit for ID = $20\mu A$. Calculate the corresponding W.

W	ID
$10\mu m$	IDx
?	$20\mu A$

Part 2: Current Mirror

a) Construct the circuit shown below.
b) For M5 we use longer length as shown below.
c) The current mirror takes input current IBIN and generates output current IBOUT = 2*IBIN (note the sizing of M6 and M7).

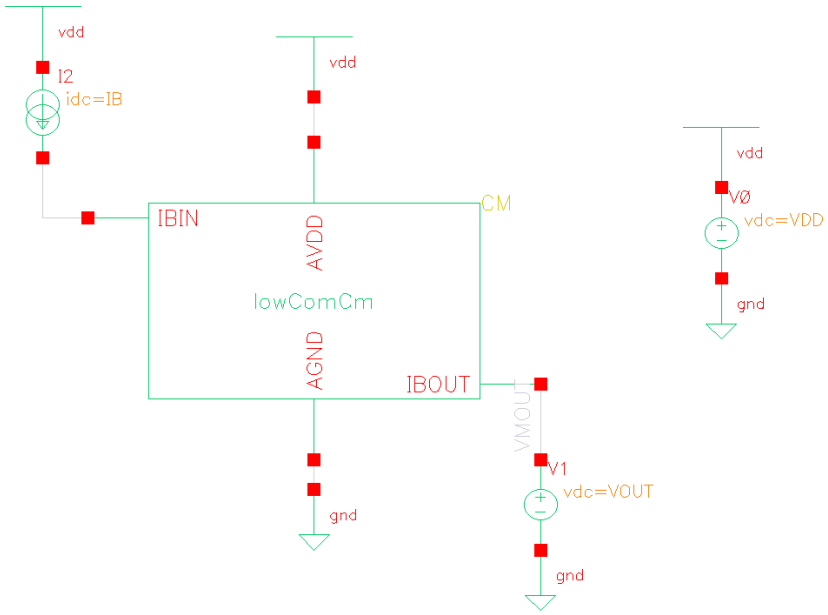


d) Create a symbol for the CM (From the menu bar: Add -> Generate Symbol)

e) Create a testbench in a higher level of hierarchy as shown below to test the current mirror.

f) Use IB = 20uA. Choose L = 1um and W as designed in Part 1. This should give you vdss around $100mV$.

g) Design another simple current mirror using two PMOS transistors only (similar to M0 and M6). We will compare this simple mirror with the wide swing cascode you have just designed.



Report the following:

a) Schematic of the two CMs with DC node voltages clearly annotated @ VOUT = VDD/2.

b) The following parameters for all transistors in a table:
   - vgs
   - vth
   - vdss
   - vds
   - gm
   - gmb
   - gds
   - region

c) Check that all transistors have vdss = 100mV as set in Part 1.

d) Are all transistors operating in saturation?

e) Perform DC sweep (not parametric sweep) using VOUT = 0:10m:VDD. Report IBOUT vs VOUT for the two CMs overlaid in the same plot.
   - Comment on the difference between the two circuits.
   - In the previous plot, the two curves intersect at a specific value of VOUT. Why?

f) Percent of error in IBOUT vs VOUT (ideal IBOUT should be IBIN*2) for the two CMs in the current mirror operating region (VOUT = 0 to VDD – vdss) overlaid in the same plot.
   - Comment on the difference between the two circuits.

g) Rout vs VOUT (take the derivative of IBOUT plot) for the two CMs in the current mirror operating region (VOUT = 0 to VDD – vdss) overlaid in the same plot (log scale). Add a cursor at VOUT = VDD/2.
   - Comment on the difference between the two circuits.
   - Does Rout change with VOUT? Why?

h) Analytically calculate Rout of both circuits at VOUT = VDD/2. Compare with simulation results in a table.