Chapter 12. Data and instructions

Instructions and data

instructions can also be called program code. They include the commands which you constantly via user programs send to your PC using your keyboard and mouse. Commands to print, save, open, etc.

Data is typically user data. Think about that email you are writing. The actual contents (the text, the letters) is user data.

Instructions and compatibility

All processors, whether they are in PC's or other types of computers, work with a particular instruction set. These instructions are the language that the CPU understands, and thus all programs have to communicate using these instructions.

The program code produced has to match the CPU's instruction set. Otherwise it cannot be run.

The x86 instruction set is common to all PC's.

The entire software industry built up around the PC is based on the common x86 instruction, which goes back to the earliest PC's. Extensions have been made, but the original instruction set from 1979 is still being used.

Extensions to the instruction set

Another innovation is the 64-bit extension, which both AMD and

Intel use in their top-processors. Normally the pc operates in 32-bit mode, but one way to improve the performance is using a 64-bit mode. This requires new software, which is not available yet.

Inside the CPU

Instructions have to be decoded, and not least, executed, in the CPU.

Pipelines

instructions are sent from the software and are broken down into micro-ops in the CPU. This decomposition and execution takes place in a pipeline.

The problems of having more pipelines

It is not possible to feed a large number of pipelines with data. The memory system is just not powerful enough.

Another problem of having several pipelines arises when the processor can decode several instructions in parallel – each in its own pipeline. It is impossible to avoid the wrong instruction occasionally being read in (out of sequence).

The actual pipeline in the Pentium 4 is longer than in other CPU's; it has 20 stages. The disadvantage of the long pipeline is that it takes more clock ticks to get an instruction through it. 20 stages require 20 clock ticks, and that reduces the CPU's efficiency.