# CSE 3203 CT 4 Assignment Roll No: 1803017

# **Assignment Problem:**

**Build CPU based on following requirements:** 

- 1. Word Size of CPU = 4
- 2. ALU Operations = OR, ADD, ROR
- 3. Register Number = 6
- 4. Size of RAM = 10
- 5. Word size of ISA and RAM = 16
- 6. CPU Instructions = Register Mode, Immediate Mode, JMP, JG

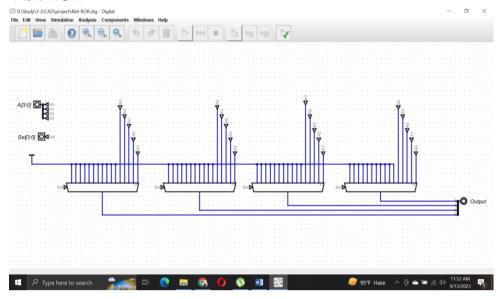
### Solution:

# Simulator Design:

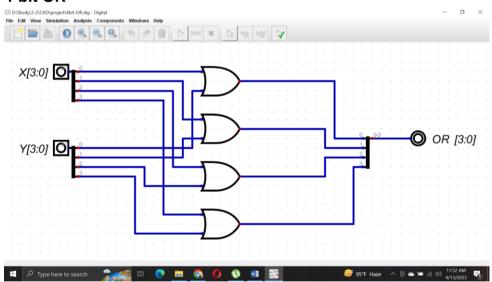
1. ALU Circuit (Top to Bottom all circuits):

# 4-bit Adder Stockholy 2000 (2000 point Augus of Companents Windows Help Court Type here to search Alt 30 () Type here to search Type here to search

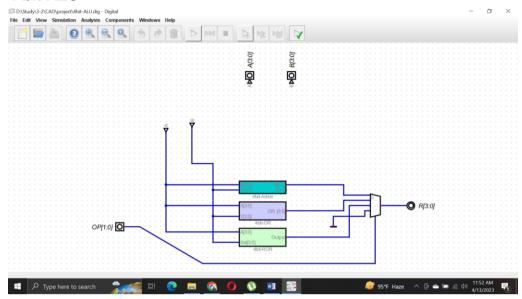
# 4-bit ROR



### 4-bit OR

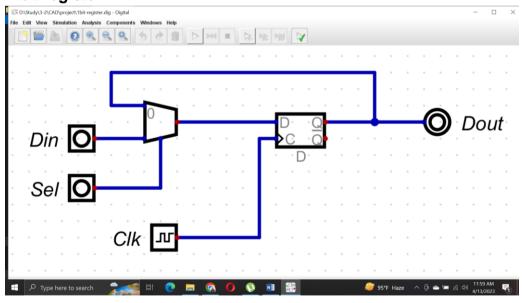


# 4-bit ALU

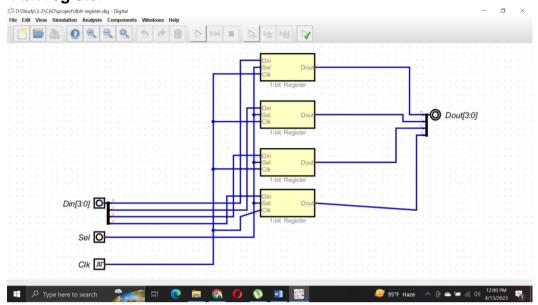


# 2. Register Set Circuit (Top to Bottom all circuits):

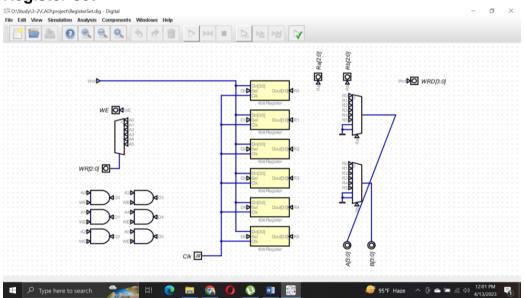
# 1-bit register



# 4-bit register

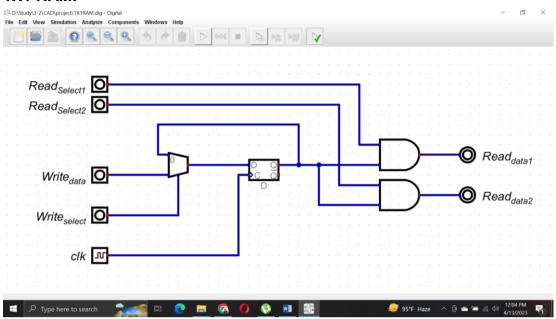


# Register-set

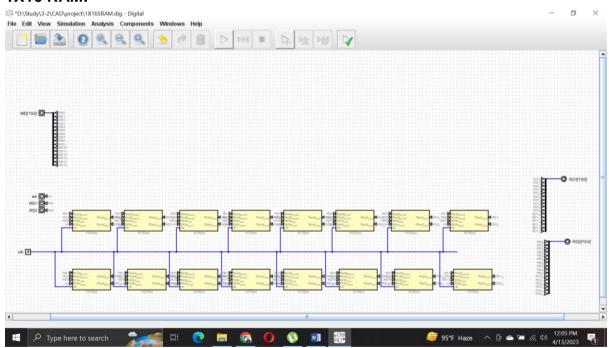


# 3. RAM Circuit (Top to Bottom all circuits):

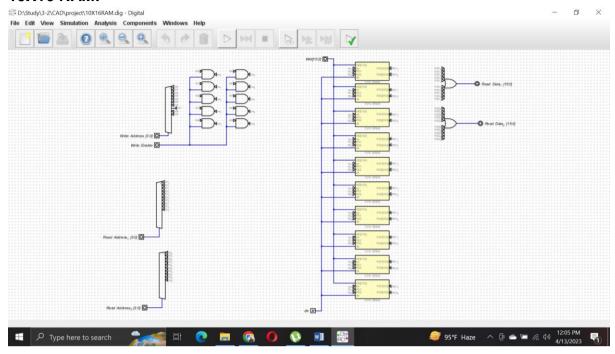
### **1X1 RAM:**



### 1X16 RAM:



### 10X16 RAM:



### 4. ISA

Register mode (type of op:00) type of op(2bit) + op(2bit) + reg1(3bit) + reg2(3bit) + 6bit (dont care)

Immediate mode (type of op:01) type of op(2bit) +op(2bit) +reg1(3bit) +imm value(4bit) + 5bit (dont care)

Branching mode (type of op:10) type of op(2bit) +op(2bit) +Address(4bit) + 6bit (dont care)

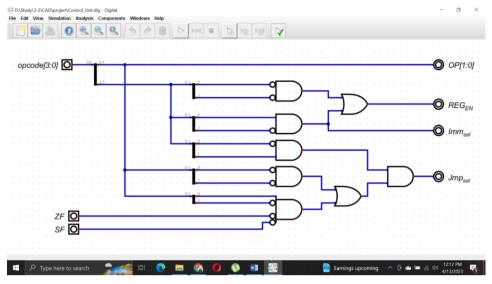
Operations:

ADD (00), OR (01) ,ROR(10)

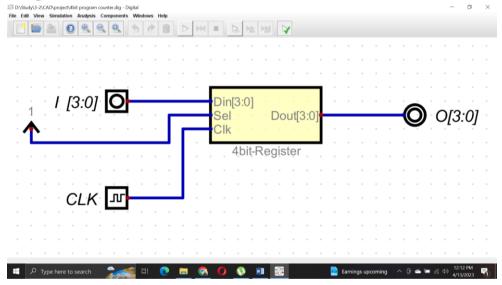
JMP (00), JG (01)

# 5. CPU (Top to Bottom all circuits):

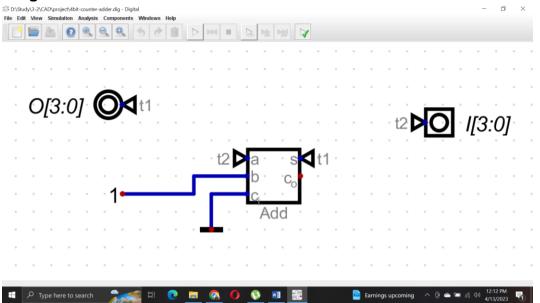
# **Control Unit:**



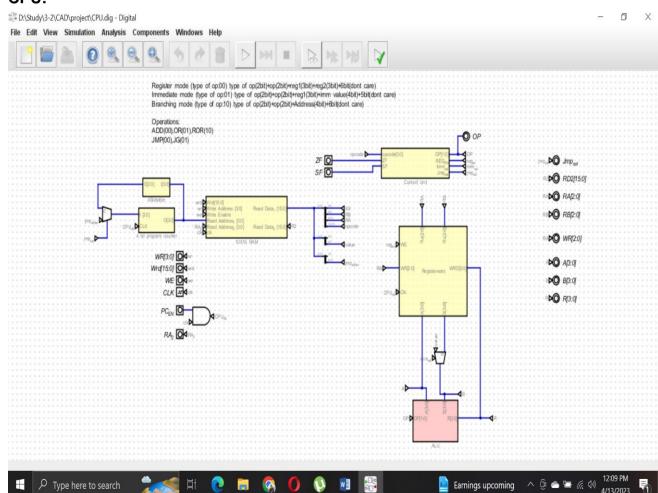
# **Program Counter:**



# **Program counter Adder:**



### CPU:



Verilog Code:	
1.	ALU Circuit (Top to Bottom all circuits):
2.	Register Set Circuit (Top to Bottom all circuits):
3.	RAM Circuit (Top to Bottom all circuits):
4.	CPU (Top to Bottom all circuits):