Tutorial 7

Tuesday, June 1, 2021 12:30 PM

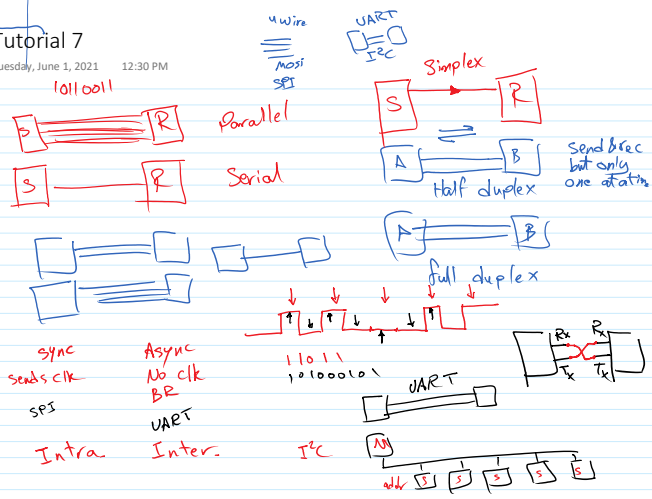


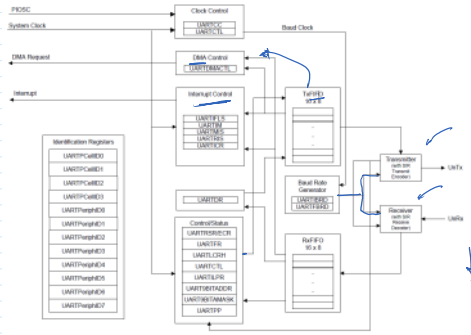
Table 14-1. UART Signals (64LQFP)

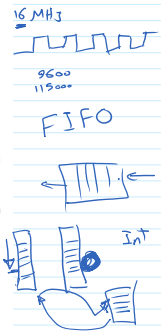
Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type*	Description
U0Rx	17	PA0 (1)	I	TTL	UART module 0 receive.
U0Tx	18	PA1 (1)	O	TTL	UART module 0 transmit.
U1CTS	15 29	PC5 (8) PF1 (1)	I	TTL	UART module 1 Clear To Send modem flow control input signal.
U1RTS	16 28	PC4 (8) PF0 (1)	O	TTL	UART module 1 Request to Send modem flow control output line.
U1Rx	16 45	PC4 (2) PB0 (1)	I	TTL	UART module 1 receive.
U1Tx	15 46	PC5 (2) PB1 (1)	O	TTL	UART module 1 transmit.
U2Rx	53	PD6 (1)	I	TTL	UART module 2 receive.
U2Tx	10	PD7 (1)	O	TTL	UART module 2 transmit.
U3Rx	14	PC6 (1)	I	TTL	UART module 3 receive.
U3Tx	13	PC7 (1)	O	TTL	UART module 3 transmit.
U4Rx	16	PC4 (1)	I	TTL	UART module 4 receive.
U4Tx	15	PC5 (1)	O	TTL	UART module 4 transmit.
U5Rx	59	PE4 (1)	I	TTL	UART module 5 receive.
U5Tx	60	PE5 (1)	O	TTL	UART module 5 transmit.
U6Rx	43	PD4 (1)	I	TTL	UART module 6 receive.

Table 14-1. UART Signals (64LQFP)

Pin Name	Pin Number	Pin Mux / Pin Assignment	Pin Type	Buffer Type[a]	Description
U0Rx	17	PA0 (1)	I	TTL	UART module 0 receive.
U0Tx	18	PA1 (1)	O	TTL	UART module 0 transmit.
U1CTS	15 29	PC5 (8) PF1 (1)	I	TTL	UART module 1 Clear To Send modem flow control input signal.
U1RTS	16 28	PC4 (8) PF0 (1)	O	TTL	UART module 1 Request to Send modem flow control output line.
U1Rx	16 45	PC4 (2) PB0 (1)	I	TTL	UART module 1 receive.
U1Tx	15 46	PC5 (2) PB1 (1)	O	TTL	UART module 1 transmit.
U2Rx	53	PD6 (1)	I	TTL	UART module 2 receive.
U2Tx	10	PD7 (1)	O	TTL	UART module 2 transmit.
U3Rx	14	PC6 (1)	I	TTL	UART module 3 receive.
U3Tx	13	PC7 (1)	O	TTL	UART module 3 transmit.
U4Rx	18	PC4 (1)	I	TTL	UART module 4 receive.
U4Tx	15	PC5 (1)	O	TTL	UART module 4 transmit.
U5Rx	59	PE4 (1)	I	TTL	UART module 5 receive.
U5Tx	60	PE5 (1)	O	TTL	UART module 5 transmit.
U6Rx	43	PD4 (1)	I	TTL	UART module 6 receive.
U6Tx	44	PD5 (1)	O	TTL	UART module 6 transmit.
U7Rx	9	PE0 (1)	I	TTL	UART module 7 receive.
U7Tx	8	PE1 (1)	O	TTL	UART module 7 transmit.

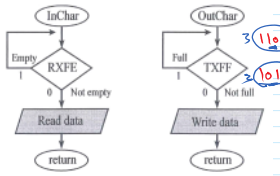
a. The TTL designation indicates the pin has TTL-compatible voltage levels.





Offset	Name	Type	Reset	Description	See page
0x000	UARTDR	RW	0x0000.0000	UART Data	906
0x004	UARTRSR/UARTECR	RW	0x0000.0000	UART Receive Status/Error Clear	908
0x018	UARTFR	RO	0x0000.0090	UART Flag	911
0x020	UARTILPR	RW	0x0000.0000	UART IrDA Low-Power Register	913
0x024	UARTIBRD	RW	0x0000.0000	UART Integer Baud-Rate Divisor	914
0x028	UARTFBRD	RW	0x0000.0000	UART Fractional Baud-Rate Divisor	915
0x02C	UARTLCRH	RW	0x0000.0000	UART Line Control	916
0x030	UARTCTL	RW	0x0000.0300	UART Control	918
0x034	UARTIFLS	RW	0x0000.0012	UART Interrupt FIFO Level Select	922
0x038	UARTIM	RW	0x0000.0000	UART Interrupt Mask	924
0x03C	UARTRIS	RO	0x0000.0000	UART Raw Interrupt Status	927
0x040	UARTMIS	RO	0x0000.0000	UART Masked Interrupt Status	930
0x044	UARTICR	W1C	0x0000.0000	UART Interrupt Clear	933
0x048	UARTDMACTL	RW	0x0000.0000	UART DMA Control	935
0x0A4	UARTNINTADDR	RW	0x0000.0000	UART 9-Bit Self Address	936
0x0A8	UARTNINTAMASK	RW	0x0000.00FF	UART 9-Bit Self Address Mask	937
0xFC0	UARTPP	RO	0x0000.0003	UART Peripheral Properties	938
0xFC8	UARTCC	RW	0x0000.0000	UART Clock Configuration	939
0xFD0	UARTPeriphID4	RO	0x0000.0000	UART Peripheral Identification 4	940
0xFD4	UARTPeriphID5	RO	0x0000.0000	UART Peripheral Identification 5	941
0xFD8	UARTPeriphID6	RO	0x0000.0000	UART Peripheral Identification 6	942
0xFDC	UARTPeriphID7	RO	0x0000.0000	UART Peripheral Identification 7	943
0xFE0	UARTPeriphID0	RO	0x0000.0060	UART Peripheral Identification 0	944
0xFE4	UARTPeriphID1	RO	0x0000.0000	UART Peripheral Identification 1	945
0xFE8	UARTPeriphID2	RO	0x0000.0018	UART Peripheral Identification 2	946
0xFEC	UARTPeriphID3	RO	0x0000.0001	UART Peripheral Identification 3	947
0xFF0	UARTPCellID0	RO	0x0000.000D	UART PrimeCell Identification 0	948
0xFF4	UARTPCellID1	RO	0x0000.00F0	UART PrimeCell Identification 1	949
0xFF8	UARTPCellID2	RO	0x0000.0005	UART PrimeCell Identification 2	950
0xFFC	UARTPCellID3	RO	0x0000.00B1	UART PrimeCell Identification 3	951

Figure 14-2. UART Character Frame



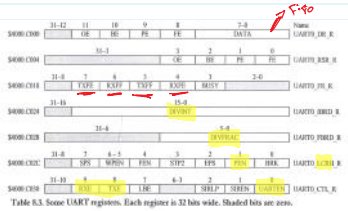


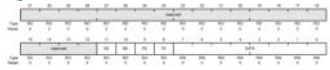
Table 8.3. Some UART registers. Each register is 32 bits wide. Shaded bits are zero.

FIFO disabled
RxFF Can't read
TxFF Can't send

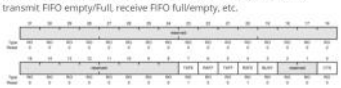
Data Register (UARTDR)

This register for both transmitter and receiver modules. This is also a 32-bit register. First, 0 to 7 bits contain the data that we want to transmit or data that is received on an Rx pin of TM4C123G microcontroller. Bits 8-11 provides error information such as framing error, parity error, break error, and overrun error.

FIFO full data lost

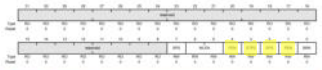


UART Flag/status Register (UARTFR) register provides flag bits such as transmit FIFO empty/Full, receive FIFO full/empty, etc.



TM4C123 UART Line Control (UARTLCRH)

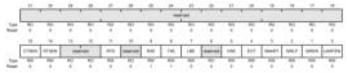
This register is used to define the format of UART data frame such as number of bits data, data length (bits 5 and 6), parity bit and stop bits implementation, FIFO enable,disable and break conditions, etc.



Bit	Name	Function
0	Send Break	When set to 1, a logic low signal is generated on the UART Tx line. For the proper generation of break conditions, the software should set this bit to 1 for at least a duration of two UART frames.
1	Parity Enable	To enable generation and checking of parity, this bit field should be set to1
2	Even Parity	Setting to 1 enables even parity, which generates and checks for even number of 1's in the data and parity bits during transmission and reception.
3	Stop bits	When this bit is cleared to 0, one stop bit is transmitted at the end of UART frame. Setting it to 1 transmits two stop bits.
4	FIFO Enable	This bit enables or disables FIFO buffers. When cleared to the FIFOs are disabled.
5	Word length	The word length bit field configures the number of data bits transmitted or received in a UART frame. A value of 0, 1, 2 or 3 configures the data length equal to 5, 6, 7 or 8 bits in the UART frame.
6	Stick Parity	This bit field enables or disables the stick parity. When this bit is set and bits 1 and 2 of this register are also set to 1 then parity bit is transmitted and checked as 0. If bit 1 is set and bit 2 is cleared then parity bit is transmitted and checked as 1.

TM4C123 UART Control Register

UARTCTL is a UART module configuration control register. Besides various other functions, its main function is to enable or disable UART module. For this tutorial, we will be using only three bits of UARTCTL register which are used to enable UART(UARTEN), enable transmitter (TXE) and receiver (RXE).



1. Enable UARTx clk
2. Enable GPIOx clk
3. Enable Alternate fn
4. Set Port ctrl PCTL

1. Disable CTL UART. Programming Register after disable.
2. BRD → Integer Part IBRD; Fractional Part FBRD
3. Parameters → sig. of data, No. of stop bits, parity → LCRH
4. clk src CC
   optional µDMA
5. Enable CTL

Q3. Write a C function to initialize UART0 with baud rate 9600 bits/s, 8 bits word length, no parity, one stop bit, and FIFO enabled.
Q4. Write a C function to check if there is data available to be received by UART0.
Q5. Write a C function to receive one byte using UART0.
Q6. Write a C function to transmit one byte using UART0.
Q7. Write a C program that receives from Device1 a lower-case character and transmits its upper-case to Device2.

clear bit 5 of ...

Q1. Assume System clock frequency=16MHz. Find the values for the divisor registers of UARTIBRD and UARTFBRD for the following standard baud rates:
(a) 4800 (b) 9600 (c) 57,600 (d) 115,200

BRD = SysClk / (16 * BR)

$\frac{16*10^6}{16*4800} = 208.33...$ $0.333*64+0.5 = 21.833$

$\frac{16*10^6}{16*9600} = 104.1667$

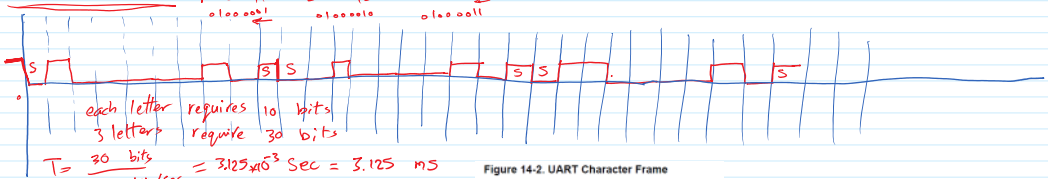
$\frac{16*10^6}{57600} = 17.3611$

$\frac{16*10^6}{115200} = 8.68$

	BR	UARTIBRD	UARTFBRD
a)	4800	208	21
b)	9600	104	11
c)	57600	17	23
d)	115200	8	44

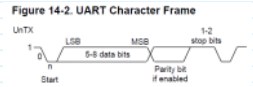
Q2. Assume the baud rate is 9600 bits/sec. Show the serial port output versus time waveform that occurs when the ASCII characters "ABC" are transmitted one right after another. What is the total time to transmit the three characters?

A = 0x41 = 0100 0001 B = 0x42 = 0100 0010 C = 0x43 = 0100 0011



each letter requires 10 bits
3 letters require 30 bits

$T = \frac{30 \text{ bits}}{9600 \text{ bits/sec}} = 3.125*10^{-3} \text{ Sec} = 3.125 \text{ ms}$



9600 bits/sec