بسم الله الرحمن الرحيم

# ⇒ ARM Cortex-M4 Architecture

Every microcontroller out there contains a processor which is responsible for performing all the actions on that microcontroller. Each processor is designed, based on a certain instruction set Architecture architecture. That architecture can be based on any type, for instance, ARM. Being our topic of discussion today let's explore ARM Cortex-M4 microcontrollers architecture in detail.

→ ARM: ① Acron Risk machines upgraded to Advanced RISK Machines.

② doesn't develop microcontrollers silicon chip but it only provides IP core for a microprocessor and other building blocks of a microcontroller

not for PC-Processor, but for mobile.

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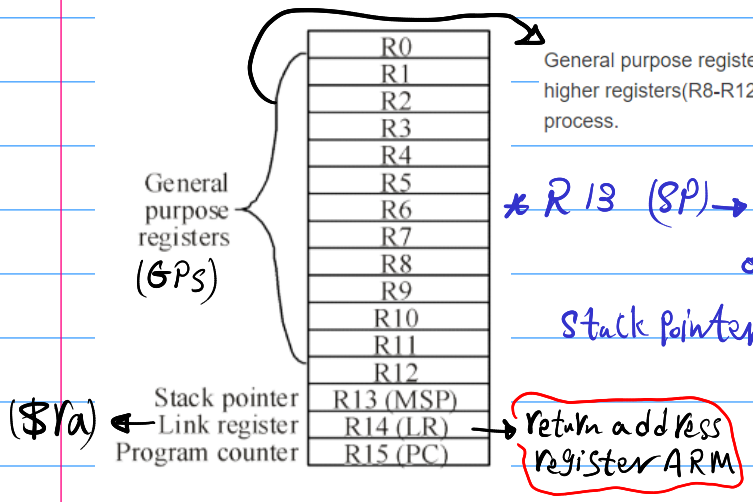
like MIPS-Processor in ARM there are registers




General purpose registers are divided into two groups .i.e. lower registers (R0-R7) and higher registers(R8-R12). GPR are used to store addresses and data which is currently under process.

* R13 (SP) → holds the address of the top element of stack and we will use main Stack pointer (MSP) not Process stack Pointer (PSP)

* (PC) R15 → holds the address of next instr. to be executed.

Program counter value automatically increases by 4 after every instruction execution so that it points to the next instruction address.

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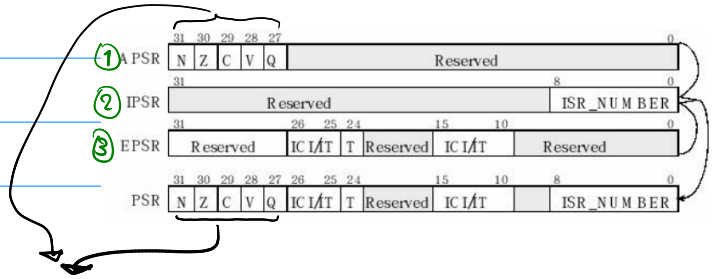
* PSR [Program Status Register]:
  ① Application PSR → [APSR]
  ② Interrupt PSR → [IPSR]
  ③ Execution PSR → [EPSR]




→ in MIPS they are flags (wires) but in ARM they are bits

N - bit → whether or not the result is negative

Z - bit → is set if the result is zero

C - bit → means carry and is set on an unsigned overflow

V - bit → signifies signed overflow.

Q - bit → indicates that "saturation" has occurred

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## * Reset : initialization Special Registers [SP - PC - linked register]
(R13) (R15) (R14)

(i) SP [R13] : The 32-bit value at flash ROM location 0 is loaded into the SP. All stack accesses are word aligned. Thus, the least significant two bits of SP must be 0. divisible by 4

(ii) PC [R15] : loads the 32-bit value at location 4 into the PC. This value is called the reset vector. All instructions are halfword aligned. Thus, the least significant bit of PC must be 0.

divisible by 2

(iii) linked register (R 14) : set the least significant bit in the reset vector, so the processor will properly initialize the Thumb bit (T) in the PSR. On the ARM ® Cortex™-M processor, the T bit should always be set to 1. On reset, the processor initializes the LR to 0xFFFFFFFF.

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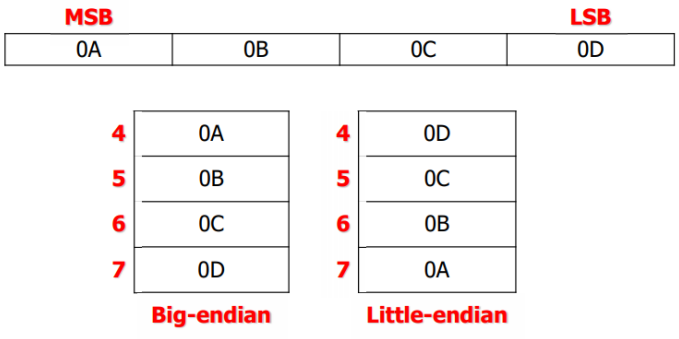
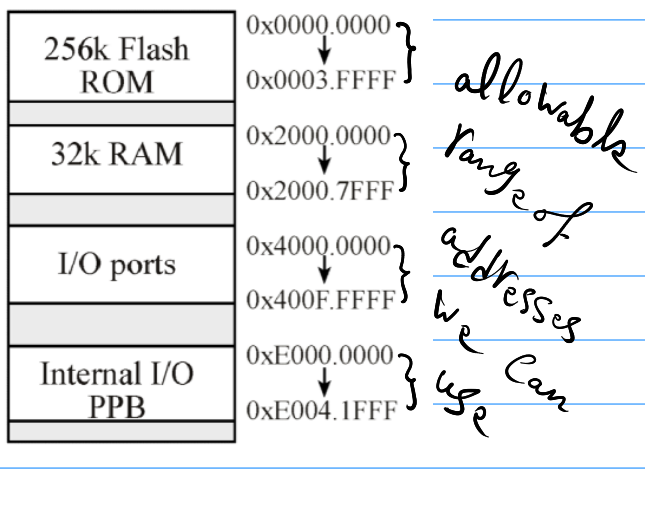
## * memory :

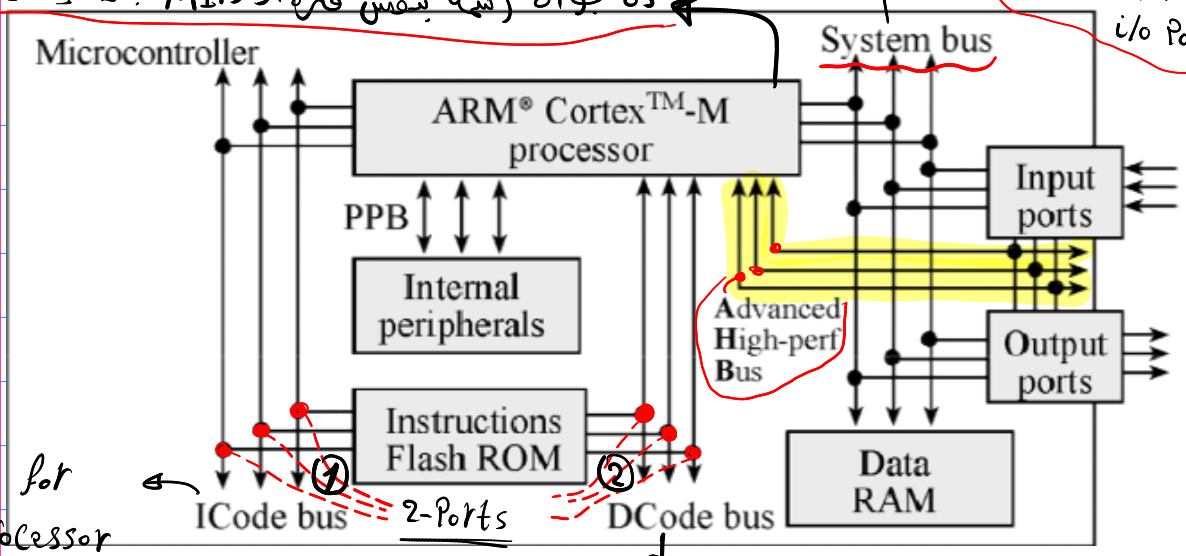
☹ حفظ

big endian & little endian



ده جواه رسمة بنفس فكرة الـ MIPS بحيث إنه بيفضل operations




is Connecting Processor With RAM and i/o Ports

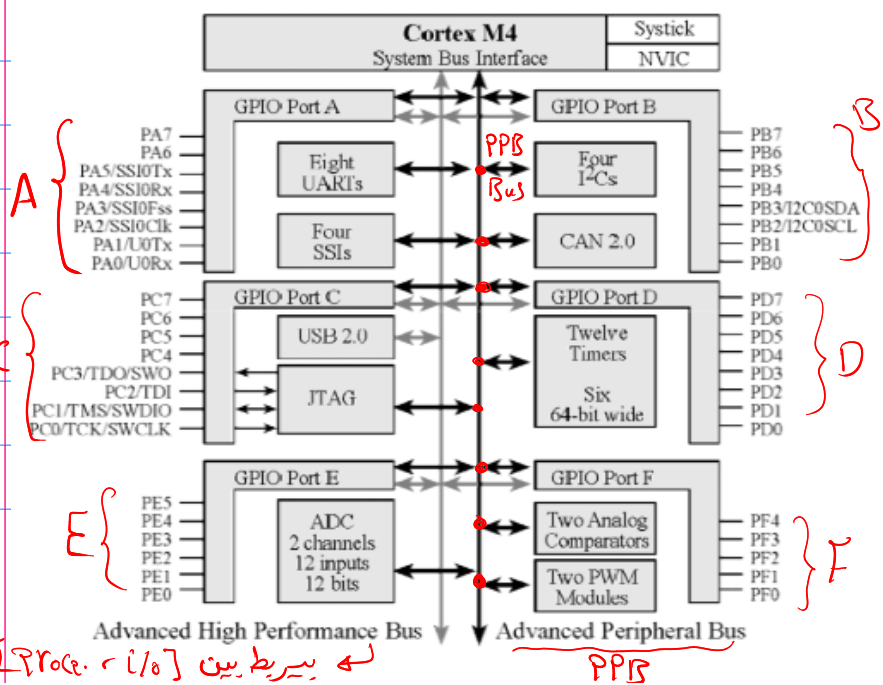
example
this used for telling Processor which operation will execute [OP-Code]

used to send constant data like immediate Part

① → Advanced High-Perf. Bus is Connecting i/o Ports With Processor
ex if you read from outer flash drive speed is Higher due to high Performance of this Bus.

② → Private Peripheral bus [PPB] : used to connect Processor with internal moduls like timer, PWM, ....

A, B, C, D, E, F → are [i/o Ports]




ARM Cortex-M4
+ 256K Flash
+ 32K RAM
+ JTAG
+ 43 Ports
+ SysTick
+ ADC
+ UART

[Proc. ↔ i/o] يربط بين