AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING
Credit Hours Engineering Programs - CHEP
Computer Engineering and Software Systems Program
Computer and Systems Engineering Department

Spring 2017 ***Examination Date : 6.06.2017*** ***Allowed Time: 3 Hours***

Real Time and Embedded Systems Design – CSE 345

Lecturer: Dr. Tamer Mostafa ***Total Marks: 40 Marks***

تعليمات هامة:

1) حيازة التليفون المحمول مفتوح / مغلق داخل لجنة الامتحان يعتبر حالة غش.

2) لا يسمح بدخول سماعة الأذن أو البلوتوث.

3) لا يسمح بدخول كتب أو ملازم أو أوراق داخل اللجنة والمخالفة لذلك تعتبر حالة غش.

==========

The exam consists of four questions in three pages. Answer all questions

Question 1: Mark each of the following statements either true (T) or false (F), and correct false statements. [10 Marks]

1 Hard real time means missing deadline results in degraded performance
2 The 8251 UART provides both serial and parallel communication
3 Pipelining increases throughput without reducing latency
4 Wait states are commonly used to connect fast, expensive memories to buses
5 Upon becoming bus master, the DMA controller has control of all bus signals including bus request and bus grant.
6 NOR flash memories are cheaper than NAND ones, have faster erase, and sequential access times
7 The time-out action of a Watchdog timer is to reset the processor
8 Using USB for transmitting data, 8 bits are transmitted at the same time.
9 In USB transmission, differential signaling is used to improve noise immunity
10 Many USB configurations can be active at the same time

Question 2: Answer the following questions [10 Marks]

A. **Writing embedded software (ARM Assembly):** **[5 marks]**
Convert the following C code into ARM assembly code. Assume a and b are two arrays of size 20, and z is a label in the program

```
for(i=0, z=0;i<20;i++)
    z = z + a[i]*b[i];
```

B. A video frame of 320x240 pixels/frame, where each pixel is represented in 3 bytes (Red, green, blue), is to be transferred at a rate of 30 frame/sec. What is the minimum bus transfer rate required in bytes/usec **[3 marks]**

C. Draw a block diagram showing the daisy chain priority interrupt with three devices connected to a CPU **[2 marks]**

Question 3 Memory management and Performance measurement [10 Marks]

Given the 16-bit memory address references below, as BYTE addresses in hex format:

0020, 0022, 00C8, 00C9, 0032, 0023, 004A, 0062, 0020, 0021

a) For each of these references, identify the binary address. **[1 Marks]**
b) Given a cache with a total of 16 words organized as 1 word/block, identify the tag, and the index for each reference using direct mapping. List if each reference is a hit or miss. How many bits in total does the cache has? **[2 Marks]**
c) Repeat (b), but with 2 words/block for a cache with a total of 16 words. **[2 Marks]**
d) Repeat (b) for a two-way set associative cache with 2 words/block, and a total size of 16 words. [**2 Marks]**
e) Repeat (b) for a fully associative cache with 1 word/block, and a total size of 16 words. **[2 Marks]**
f) Assume the given memory references are called in a loop of 100 times. Recalculate the number of hits and misses for all cases: (b), (c), (d) and (e). **[1 Marks]**

For set associative and fully associative caches, use Least Recently Used (LRU) replacement.

Question 5: Embedded system design [10 Marks]

A microprocessor-based system is designed to receive an input one-digit number (0-9) from a keypad, display it on a LCD and accordingly adjust a stepper motor to rotate a number of steps equal to the input number. The keypad, LCD, and the stepper motor are connected to the microprocessor through one 8255 chip. The keypad has a 8-bit data register connected to PA of the 8255. The LCD data pins are connected to PB, and the control pins: RS to PC4, R/W to PC5, and E to PC6. The stepper motor is connected to the lower part of PC (0-3). The ASCII code of "0" is 0x30, "1" is 0x31 and it continues with the same pattern until "9" (0x39). The table below shows the LCD pin assignment.

Pin	Symbol	I/O	Description
1	Vss		Ground
2	Vcc		+5V Power
3	Vee		Power to control Contrast
4	RS (Reg. Select)	I	RS = 0 -> Comm. Reg. RS = 1 -> Data Reg.
5	R/W	I	R/W = 0 -> Write R/W = 1 -> Read
6	E	I/O	Enable (falling edge)
7-14	DB0 – DB7	I/O	8-bit data bus

a) Draw a detailed block diagram showing the connections between the keypad, LCD, the 8255 PPI, a 4-phase stepper motor, and a CPU with a 16-bit address bus. Your design should follow the following specifications: - **(4 marks)**
    a. PA address is FAA0 H. Show the decoding circuitry.

b. Write down the control word.

b) Write assembly program to operate the system using the following steps: **(6 marks)**

1- Configure the 8255 by sending the proper control word to the control register,
2- Assume there is a flag Kin which is set to 1 when the keypad data register has a new input data. Keep polling the flag until its value is changed to 1.
3- If Kin==1, read the Keypad data register into PA, and disable the flag.
4- Display the input number on the LCD screen.
5- Convert the number from its ASCII form to its value.
6- Move the stepper motor number of steps equal to the input number.

Best wishes,

Examination Committee:

Dr. Tamer Mostafa