CSE 211: Introduction to Embedded Systems

Section 1

Contact Information

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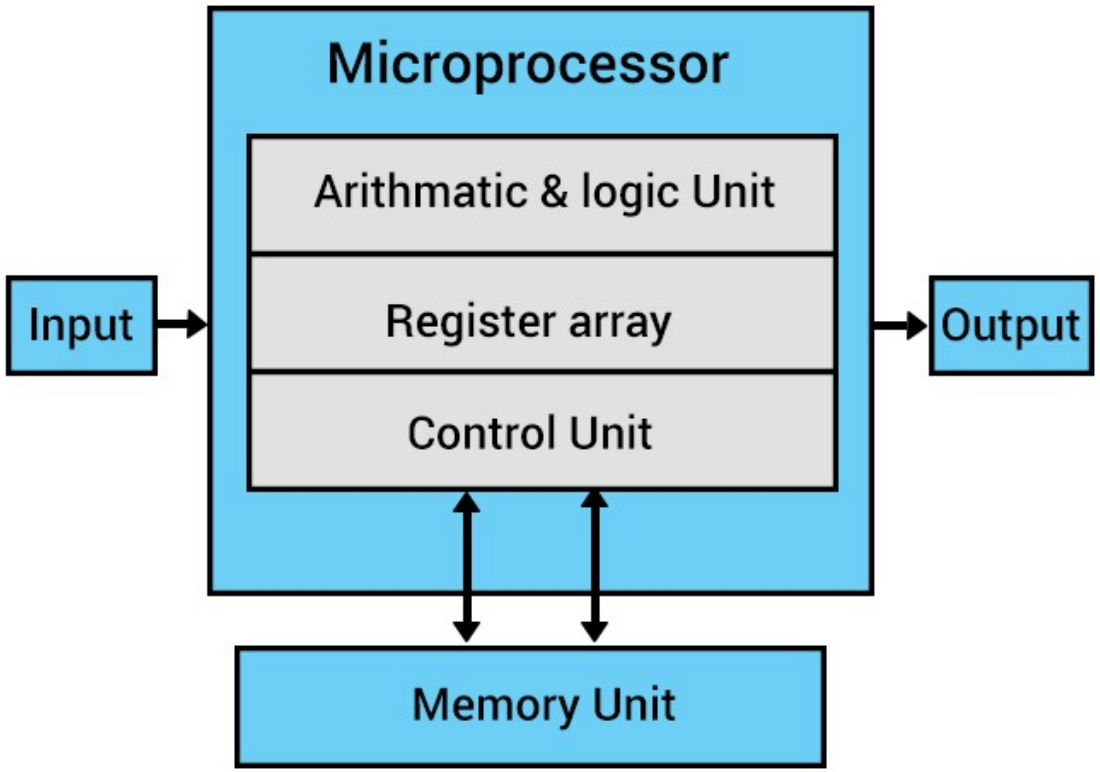
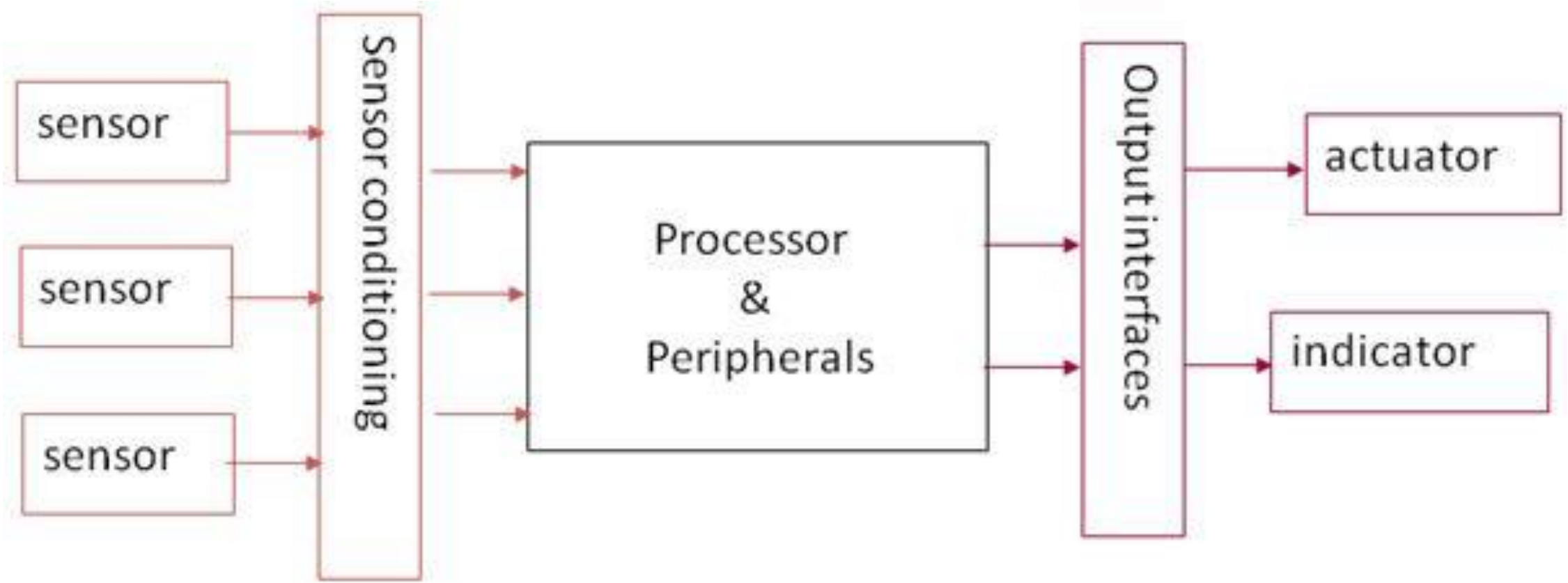
Coursework

Midterm	20 marks
Oral/Practical	10 marks
Student Activities	10 marks

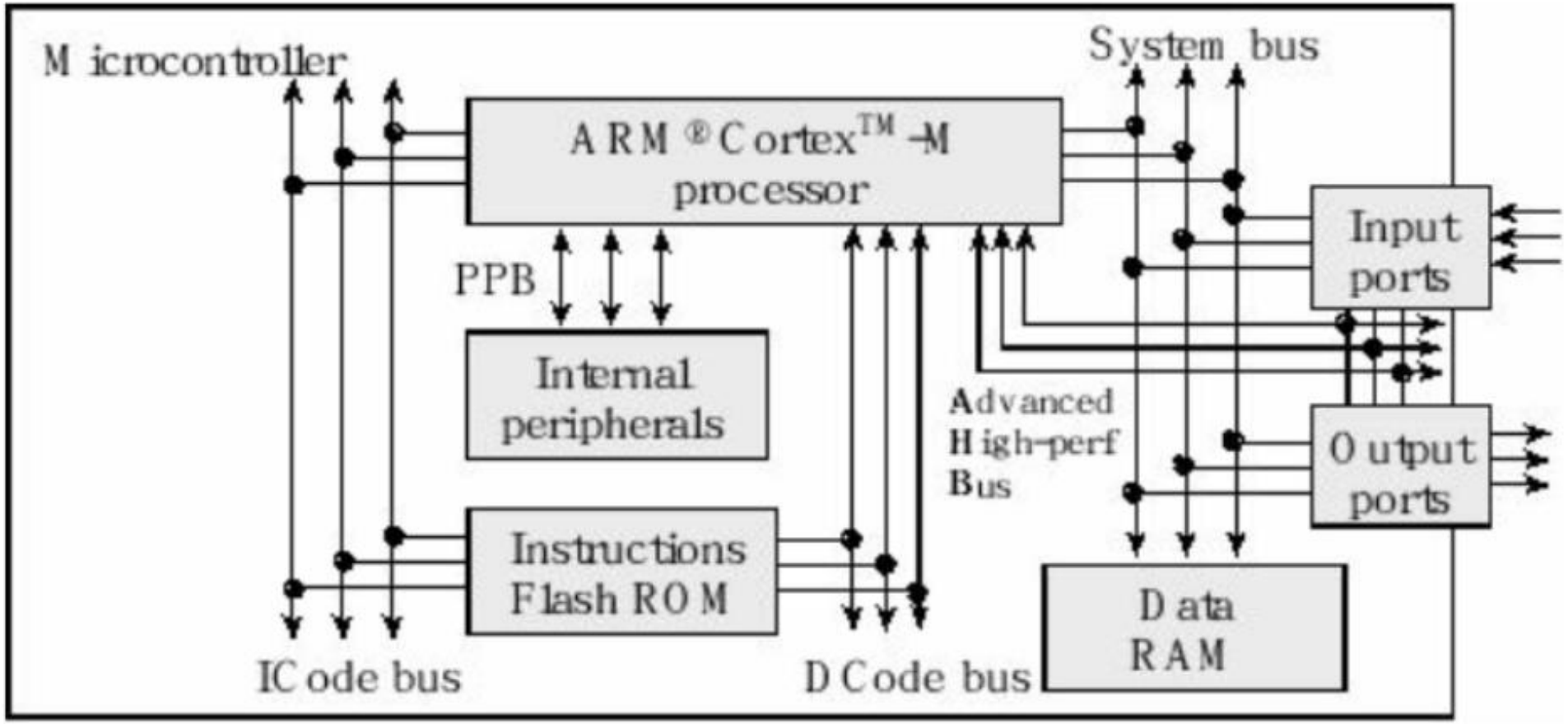
What is a microprocessor?



Embedded System



What is a microcontroller?



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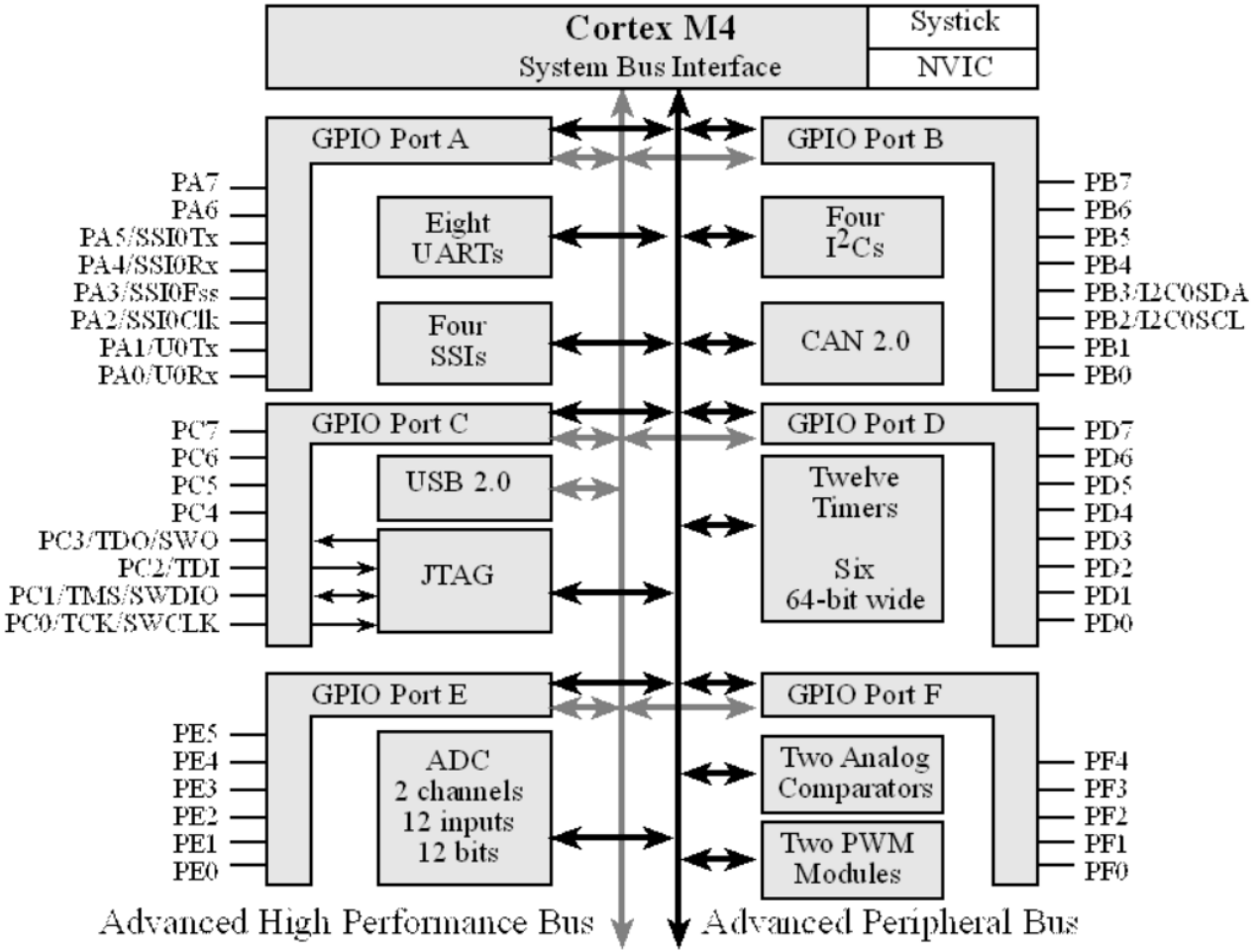
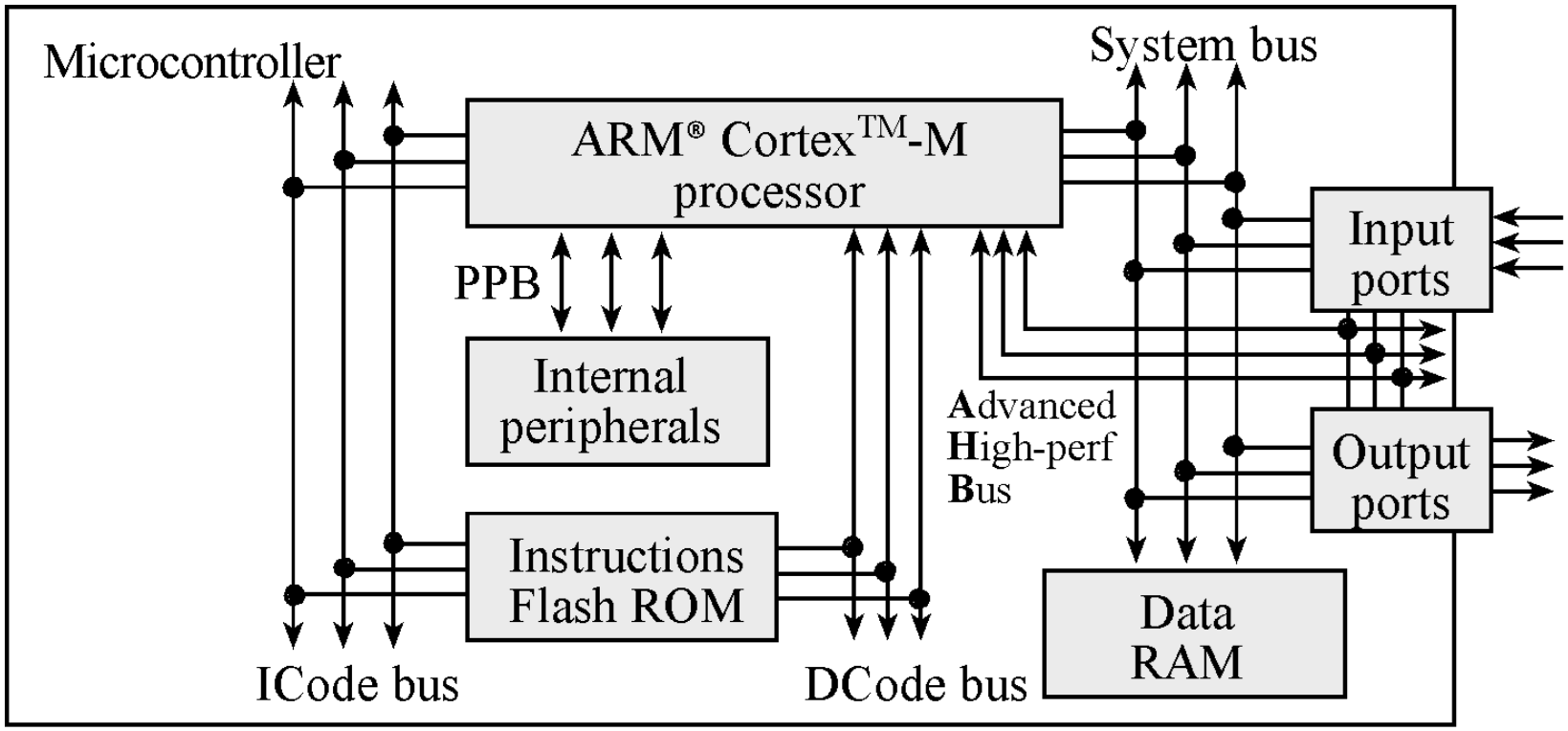


Sheet 1

- Draw the block diagram of ARM Cortex-M based Microcontroller. How many general-purpose registers does the ARM Cortex-M processor has?

Answer

- 13 Registers general purpose registers.
- From R0 to R12 are general purpose registers and contain either data or addresses.



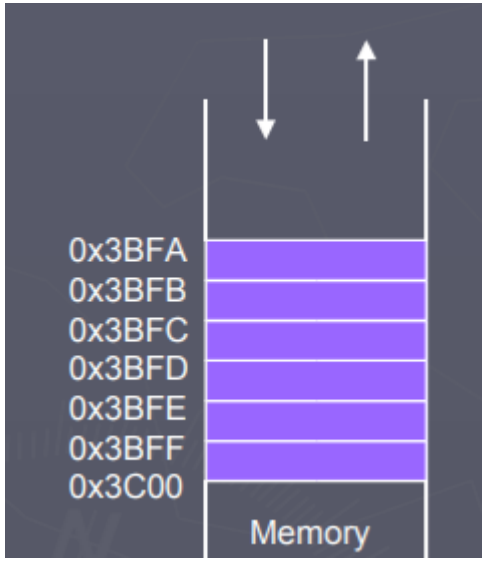
Sheet 1

- What is special about Register 13? Register 14? Register 15?

Answer

- Register R13 (also called the stack pointer, SP) points to the top element of the stack.
- Register R14 (also called the link register, LR) is used to store the return location for functions.
- Register R15 (also called the program counter, PC) points to the next instruction to be fetched from memory.

Stack (LIFO)



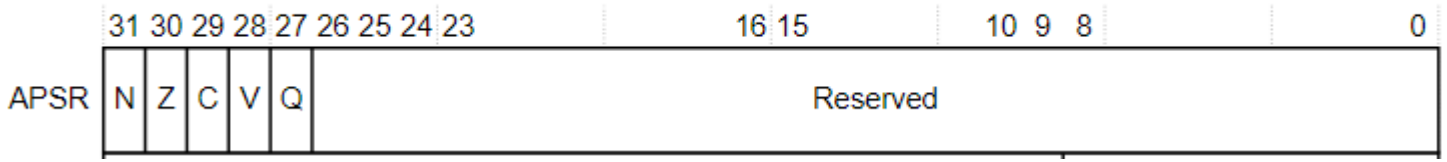
- A reserved area of memory used to keep track of a program's internal operation, including functions, return addresses, passed parameters, etc.
- The **Stack Pointer** (SP) register is used to indicate the location of the last item pu t item put onto the stack.
- When you PUT something ONTO the stack (**PUSH** onto the stack), the SP is decremented before the item is e item is placed on the stack.
- When you take something OFF of the stack (**PULL** from the stack), the SP is incremented after the item is e item is pulled from the stack.

Sheet 1

- What are the bits in the Program Status Register (PSR) of Cortex-M processor?

Answer

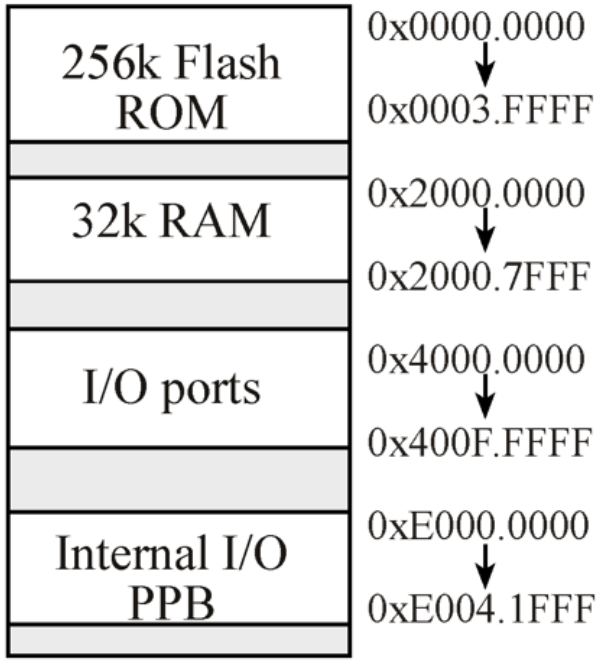
- The N, Z, V and C bits give information about the result of a previous ALU operation.
- N bit is set after an arithmetical or logical operation signifying whether the result is negative.
- Z bit is set if the result is zero.
- C bit means carry and is set on an unsigned overflow
- V bit signifies signed overflow



Sheet 1

- Draw the memory map of TM4C123? How much RAM and ROM are in TM4C123? What are the specific address ranges of these memory components?

Answer


256k Flash ROM
0x0000.0000
0x0003.FFFF
32k RAM
0x2000.0000
0x2000.7FFF
I/O ports
0x4000.0000
0x400F.FFFF
Internal I/O PPB
0xE000.0000
0xE004.1FFF

Sheet 1

- How do you specify where to begin execution after a reset?

Answer

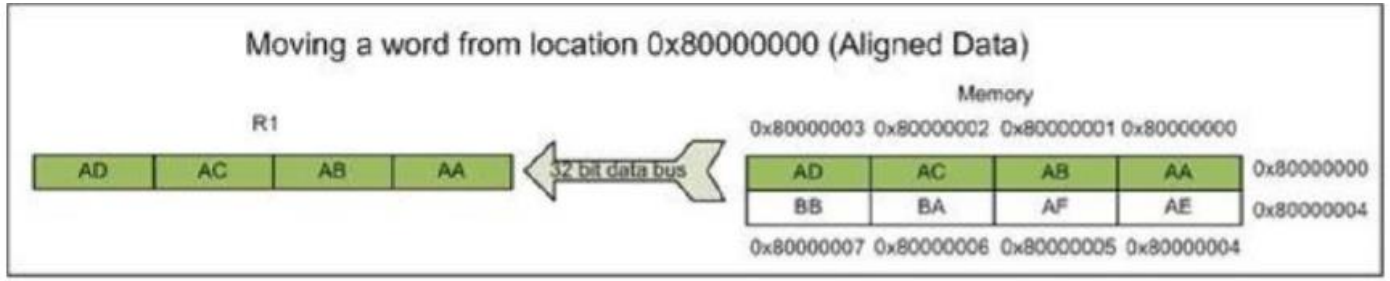
- After reset the 32-bit value stored at location 0 of flash ROM is loaded into the SP and the 32-bit value stored at location 4 of flash ROM is loaded into PC and LR register value is set to 0xFFFFFFFF

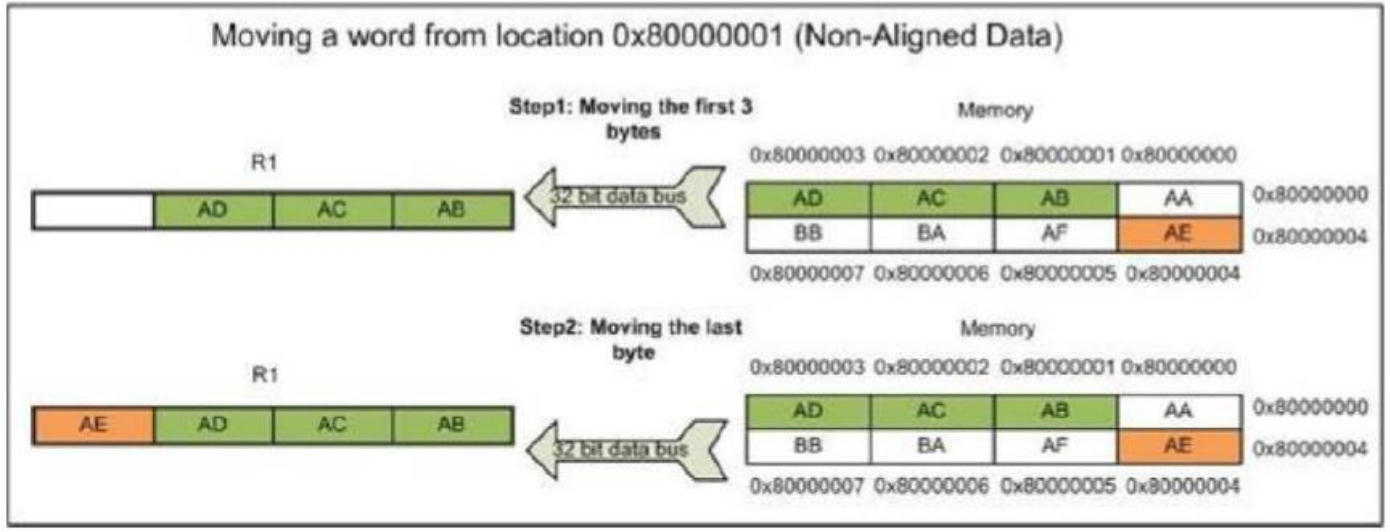
Sheet 1

- What does word-aligned and halfword-aligned mean?

Answer

- word-aligned : 32-bit word (each location in memory is 4 bytes) Address of words in memory must be multiples of 4 bytes.
- The least two significant bits of address must be zero





- Halfword-aligned : 16-bit word (each location in memory is 2 bytes). Address in memory must be multiples of 2 bytes.