AIN SHAMS UNIVERSITY
FACULTY OF ENGINEERING

April 5th, 2022 | **Course Code: CSE411** | *Time: 1 Hour*

Midterm – Real Time and Embedded Systems Design

The Exam Consists of 4 Questions in 4 Pages | *Total Marks: 20 Marks*

Question 1: (4 marks)

A. Having two tasks, each that executes its functionality within a while (1), what is/are the downgrade(s) of using the Program Counter (PC) to switch between the two tasks?
What is the Register that should be used instead of the Program Counter (PC)?

- Downgrades is that while Hooking PC the task executed From it's begining till time slice ends, so that the begining of code repeated and the context switch not recaled.

- The register used instead PC is SP stake Pointer of the task in(TCB). ↳ Task Frame

B. State the difference between **soft real-time requirements** and **hard real-time requirements**.

Question 2: (4 marks)

Choose the right answer.

Which of the following is NOT a part of the Exception frame?
a. Link register
b. Program counter
c. Stack pointer
d. PSR

0 1 2 3
12 LR PC PSR

Which of the following can periodically trigger the context switch?
a. Watchdog timer
(b.) SysTick timer
c. Peripheral
d. Memory

If you are doing context switching manually, which registers that you should manually save on the stack by yourself (other than those saved by the hardware)?
a. SP. PRIMASK, and FAULTMASK registers
b. PRIMASK and FAULTMASK registers
(c.) R11, R10, R9, R8, R7, R6, R5, and R4
d. PSR, PC, SP, LR, R12, R3, R2, R1, and RO

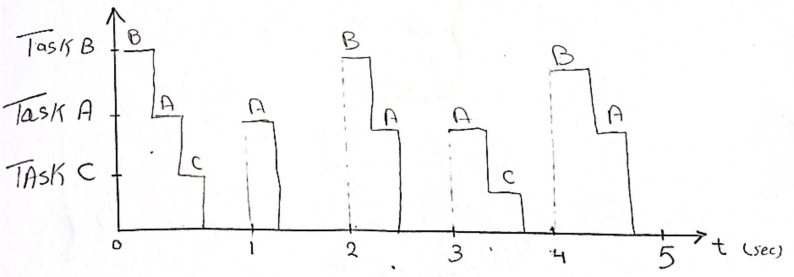
What is the CPU register that hold the address of the next instruction to be executed?
a. PSR
(b.) PC
c. Stack pointer
d. Link register

Question 3: (3 marks)

2 3 1

In a FreeRTOS project, three short periodic tasks were created (Task A, Task B and Task C). Task A, Task B, and Task C are having the periods 1 sec, 2 sec, and 3 sec respectively. Their priorities are 2, 3, and 1, respectively. Sketch tasks timing diagram for the first 5 Seconds. Vertical axe is the priority level while the horizontal axe is the time in seconds.

A 0, 1, 2, 3, 4
B 0, 2, 4
C 0, 3



Question 4: (9 marks)

Assume the following snippet of code/application that already had all necessary declarations, inclusions, and prototypes. **In the given table, order the first 9 break points to be hit, when GO is pressed.**

```
64  int main( void )
65  {
66    xTaskCreate( vTask1, NULL, 240, NULL, 2, &xTask1Handle );
67    xTaskCreate( vTask2, NULL, 240, NULL, 1, &xTask2Handle );
68    vTaskStartScheduler();
69    for( ;; );
70  }
71
72  void vTask1( void *pvParameters )
73  {
74    unsigned portBASE_TYPE uxPriority;
75    uxPriority = uxTaskPriorityGet( NULL );
76
77    for( ;; )
78    {
79      vTaskPrioritySet( xTask2Handle, ( uxPriority + 1 ) );
80      xTaskCreate( vTask3, NULL, 240, NULL, 3, NULL );
81      vTaskDelay(100000);
82    }
83  }
84
85  void vTask2( void *pvParameters )
86  {
87    unsigned portBASE_TYPE uxPriority;
88    uxPriority = uxTaskPriorityGet( NULL );
89
90    for( ;; )
91    {
92      vTaskPrioritySet( NULL, ( uxPriority - 2 ) );
93      vTaskDelay(100000);
94    }
95  }
96
97  void vTask3( void *pvParameters )
98  {
99    unsigned portBASE_TYPE uxPriority;
100   uxPriority = uxTaskPriorityGet( NULL );
101
102   for( ;; )
103   {
104     vTaskPrioritySet( xTask1Handle, ( uxPriority + 1 ) );
105     vTaskPrioritySet( NULL, ( uxPriority - 1 ) );
106     vTaskDelay(100000);
107   }
108 }
109
110 void vApplicationIdleHook( void )
111 {
112   ulIdleCycleCount++;
113 }
114
115
```

Task 2 Priority = 3

Task 2 Priority = 1

Task 1 Priority = 4

Task 3 Priority = 2

①	②	③	④	⑤	⑥	⑦
79	92	80	104	81	105	106

⑧	⑨
93	112

1st Break Point Hit	2nd Break Point Hit	3rd Break Point Hit	4th Break Point Hit	5th Break Point Hit
79	92	80	104	81

6th Break Point Hit	7th Break Point Hit	8th Break Point Hit	9th Break Point Hit
105	106	93	112