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VLSI Interview Questions and Answers

Q1). Explain how logical gates are controlled by Boolean logic?
Ans: In Boolean algebra, the **true state** is denoted by the number one, referred as logic one or logic high. While, the **false state** is represented by the number zero, called logic zero or logic low. And in the digital electronic, the logic high is denoted by the presence of a voltage potential.
Q2).Mention what are the different gates where Boolean logic are applicable?
Ans:

- **NOT Gate:**It has one out input and one output. For example, if the value of A= 0 then the Value of B=1 and vice versa
- **AND Gate:**It has one output due to the combination of two output. For example, if the value of A and B= 1 then value of Q should be 1
- **OR Gate:**Either of the value will show the same output. For example, if the value of A is 1 or B is 0 then value of Q is 1

These are the basic three types of gates where Boolean logic work, apart from these, other gates that are functional works with the combination of these three basic gates, they are XNOR gate, NAND gate, Nor gate and XOR gate.
Q3).Explain how binary number can give a signal or convert into a digital signal?
Ans: Binary number consists of either 0 or 1, in simple words number 1 represents the ON state and number 0 represents OFF state. These binary numbers can combine billion of machines into one machines or circuit and operate those machines by performing arithmetic calculations and sorting operations.
Q4).Mention what is the difference between the TTL chips and CMOS chips?
Ans:

TTL Chips	CMOS Chips
· TTL chips for transistor transistor logic. It uses two Bi-polar Junction Transistors in the design of each logic gate · TTL chips can consist of a substantial number of parts like resistors · TTLS chip consumes lot more power especially at rest. A single gate in TTL chip consumes about mW of power · TTL chips can be used in computers	· CMOS stands for Complementary Metal Oxide Semi-conductor. It is also an integrated chip but used field effect transistors in the design · CMOS has greater density for logic gates. In a CMOS chip, single logic gate can comprise of as little as two FETs · CMOS chips consume less power. A single CMOS chip consume about 10nW of power · CMOS chip is used in Mobile phones

Q5). Explain what is a sequential circuit?
Ans: A sequential circuit is a circuit which is created by logic gates such that the required logic at the output depends not only on the current input logic conditions, but also on the sequences past inputs and outputs.

Q6).Explain how Verilog is different to normal programming language?
Ans: Verilog can be different to normal programming language in following aspects

- Simulation time concept
- Multiple threads
- Basic circuit concepts like primitive gates and network connections

Q7). Explain what is Verilog?
Ans: Verilog is an HDL (Hardware Description Language) for describing electronic circuits and systems. In Verilog, circuit components are prepared inside a Module. It contains both behavioral and structural statements. Structural statements signify circuit components like logic gates, counters and micro-processors. Behavioral statements represent programming aspects like loops, if-then statements and stimulus vectors.
Q8). In Verilog code what does "timescale 1 ns/ 1 ps" signifies?
Q9). Mention what are the two types of procedural blocks in Verilog?
Ans: The two types of procedural blocks in Verilog are

- **Initial:** Initial blocks runs only once at time zero
- **Always:** This block loop to execute over and again and executes always, as the name suggests

Q10). Explain why present VLSI circuits use MOSFETs instead of BJTs?
Ans: In comparison to BJT, MOSFETS can be made very compact as they occupy very small silicon area on IC chip and also in term of manufacturing they are relatively simple. Moreover, digital and memory ICs can be employed with circuits that use only MOSFETs, i.e., diodes, resistors, etc.

Q11).Mention what are three regions of operation of MOSFET and how are they used?
Ans: MOSFET has three regions of operations

- Cut-off region
- Triode region
- Saturation region

The triode and cut-off region are used to function as a switch, while, saturation region is used to operate as an amplifier.

Q12).Explain what is the depletion region?
Ans: When positive voltage is transmitted across Gate, it causes the free holes (positive charge) to be pushed back or repelled from the region of the substrate under the Gate. When these holes are pushed down the substrate, they leave behind a carrier depletion region.
Q13).Explain why is the number of gate inputs to CMOS gates usually limited to four?
Ans: Higher the number of stacks, slower the gate will be. In NOR and NAND gates the number of gates present in the stack is usually alike as the number of inputs plus one. So input are restricted to four.
Q14).Explain what is multiplexer?
Ans: A multiplexer is a combination circuit which selects one of the many input signals and direct to the only output.
Q15). Explain what is SCR (Silicon Controlled Rectifier)?
Ans: SCR is a 4 layered solid state device which controls current flow. It is a type of rectifier that is controlled by a logical gate signal. It is a 4 layered, 3-terminal device.
Q16).Explain what is Slack?
Ans: Slack is referred as a time delay difference from the expected delay to the actual delay in a particular path. Slack can be negative or positive.
Q17).Explain what is the use of defpararm?
Ans: With the keyword defparam, parameter values can be configured in any module instance in the design.
Q18).What are the steps required to solve setup and Hold violations in VLSI?
Ans: There are few steps that has to be performed to solved the setup and hold violations in VLSI. The steps are as follows:
– The optimization and restructuring of the logic between the flops are carried way. This way the logics are combined and it helps in solving this problem.
– There is way to modify the flip-flops that offer lesser setup delay and provide faster services to setup a device.
Modifying the launch-flop to have a better hold on the clock pin, which provides CK->Q that

makes the launch-flop to be fast and helps in fixing the setup violations.
– The network of the clock can be modified to reduce the delay or slowing down of the clock that captures the action of the flip-flop.
– There can be added delay/buffer that allows less delay to the function that is used.

Q19).What are the different ways in which antenna violation can be prevented?

Ans: Antenna violation occurs during the process of plasma etching in which the charges generating from one metal strip to another gets accumlated at a single place. The longer the strip the more the charges gets accumulated. The prevention can be done by following method:
– Creating a jogging the metal line, that consists of atleast one metal above the protected layer.
– There is a requirement to jog the metal that is above the metal getting the etching effect. This is due to the fact that if a metal gets the etching then the other metal gets disconnected if the prevention measures are not taken.
– There is a way to prevent it by adding the reverse Diodes at the gates that are used in the circuits.

Q20).What is the function of tie-high and tie-low cells?

Ans: Tie-high and tie-low are used to connect the transistors of the gate by using either the power or the ground. The gates are connected using the power or ground then it can be turned off and on due to the power bounce from the ground. The cells are used to stop the bouncing and easy from of the current from one cell to another. These cells are required Vdd that connects to the tie-high cell as there is a power supply that is high and tie-low gets connected to Vss. This connection gets established and the transistors function properly without the need of any ground bounce occurring in any cell.

Q21).What is the main function of metastability in VSDL?

Ans: Metastability is an unknown state that is given as neither one or zero. It is used in designing the system that violates the setup or hole time requirements. The setup time requirement need the data to be stable before the clock-edge and the hold time requires the data to be stable after the clock edge has passed. There are potential violation that can lead to setup and hold violations as well. The data that is produced in this is totally asynchronous and clocked synchronous. This provide a way to setup the state through which it can be known that the violations that are occuring in the system and a proper design can be provided by the use of several other functions.

Q22).What are the steps involved in preventing the metastability?

Ans: Metastability is the unknown state and it prevents the violations using the following steps:
1. proper synchronizers are used that can be two stage or three stage whenever the data comes from the asynchronous domain. This helps in recovering the metastable state event.
2. The synchronizers are used in between cross-clocking domains. This reduces the metastability by removing the delay that is caused by the data element that are coming and taking time to get removed from the surface of metal.
3. Use of faster flip-flops that allow the transaction to be more faster and it removes the delay time between the one component to another component. It uses a narrower metastable window that makes the delay happen but faster flip-flops help in making the process faster and reduce the time delay as well.

Q23).What are the different design constraints occur in the Synthesis phase?

Ans: The steps that are involved in which the design constraint occurs are:
1. first the creation of the clock with the frequency and the duty cycle gets created. This clock helps in maintaining the flow and synchronizing various devices that are used.
2. Define the transition time according the requirement on the input ports.
3. The load values are specified for the output ports that are mapped with the input ports.
4. Setting of the delay values for both the input and output ports. The delay includes the input and output delay.
5. Specify the case-settings to report the correct time that are matched with the specific

paths.
6. The clock uncertainty values are setup and hold to show the violations that are occurring.

Q24).What are the different types of skews used in VLSI?

Ans: There are three types of skew that are used in VLSI. The skew are used in clock to reduce the delay or to understand the process accordingly. The skew are as follows:

Local skew:

This contain the difference between the launching flip-flop and the destination flip-flop. This defines a time path between the two.

Global skew:

Defines the difference between the earliest component reaching the flip flow and the the latest arriving at the flip flow with the same clock domain. In this delays are not measured and the clock is provided the same.

Useful skew:

Defines the delay in capturing a flip flop paths that helps in setting up the environment with specific requirement for the launch and capture of the timing path. The hold requirement in this case has to be met for the design purpose.

Q25).What are the changes that are provided to meet design power targets?

Ans: To meet the design power target there should be a process to design with Multi-VDD designs, this area requires high performance, and also the high VDD that requires low-performance. This is used to create the voltage group that allow the appropriate level-shifter to shift and placed in cross-voltage domains. There is a design with the multiple threshold voltages that require high performance when the Vt becomes low. This have lots of current leakage that makes the Vt cell to lower the performance. The reduction can be performed in the leakage power as the clock in this consume more power, so placing of an optimal clock controls the module and allow it to be given more power. Clock tree allow the switching to take place when the clock buffers are used by the clock gating cells and reduce the switching by the power reduction.

Q26).What are the different measures that are required to achieve the design for better yield?

Ans: To achieve better yeild then there should be reduction in maufacturability flaws. The circuit perfomance has to be high that reduces the parametric yield. This reduction is due to process variations The measures that can be taken are:

– Creation of powerful runset files that consists of spacing and shorting rules. This also consists of all the permissions that has to be given to the user.
– Check the areas where the design is having lithographic issues, that consists of sharp cuts.
– Use of redundant vias to reduce the breakage of the current and the barrier.
– Optimal placing of the de-coupling capacitances can be done so that there is a reduction in power-surges.

Q27).What is the difference between the mealy and moore state machine?

Ans:

– Moore model consists of the machine that have an entry action and the output depends only on the state of the machine, whereas mealy model only uses Input Actions and the output depends on the state and also on the previous inputs that are provided during the program.
– Moore models are used to design the hardware systems, whereas both hardware and software systems can be designed using the mealy model.
– Mealy machine's output depend on the state and input, whereas the output of the moore machine depends only on the state as the program is written in the state only.
– Mealy machine is having the output by the combination of both input and the state and the change the state of state variables also have some delay when the change in the signal takes place, whereas in Moore machine doesn't have glitches and its ouput is dependent only on states not on the input signal level.

Q28).What is the difference between Synchronous and Asynchronous reset?

Ans:

– Synchronous reset is the logic that will synthesize to smaller flip-flops. In this the clock works as a filter providing the small reset glitches but the glitches occur on the active clock

edge, whereas the asynchronous reset is also known as reset release or reset removal. The designer is responsible of added the reset to the data paths.
– The synchronous reset is used for all the types of design that are used to filter the logic glitches provided between the clocks. Whereas, the circuit can be reset with or without the clock present.
– Synchronous reset doesn't allow the synthesis tool to be used easily and it distinguishes the reset signal from other data signal. The release of the reset can occur only when the clock is having its initial period. If the release happens near the clock edge then the flip-flops can be metastable.

Q29).What are the different design techniques required to create a Layout for Digital Circuits?
Ans: The different design techniques to create the Layout for digital circuits are as follows:
– Digital design consists of the standard cells and represent the height that is required for the layout. The layout depends on the size of the transistor. It also consists of the specification for Vdd and GND metal paths that has to be maintained uniformly.
– Use of metal in one direction only to apply the metal directly. The metal can be used and displayed in any direction.
– Placing of the substrate that place where it shows all the empty spaces of the layout where there is resistances.
– Use of fingered transistors allows the design to be more easy and it is easy to maintain a symmetry as well.

Q30).Write a program to explain the comparator?
Ans: To make a comparator there is a requirement to use multiplexer that is having one input and many outputs. This allows the choosing of the maximum numbers that are required to design the comparator. The implementation of the 2 bit comparator can be done using the law of tigotomy that states that A > B, A < B, A = B (Law of trigotomy). The comparator can be implemented using:
combinational logic circuits or multiplexers that uses the HDL language to write the schematic at RTL and gate level.
Behavioral model of comparator represented like:

```
module comp0 (y1,y2,y3,a,b);
input [1:0] a,b;
output y1,y2,y3;
wire y1,y2,y3;
assign y1= (a >b)? 1:0;
assign y2= (b >a)? 1:0;
assign y3= (a==b)? 1:0;
endmodule
```

Q31).What is the function of chain reordering?
Ans: The optimization technique that is used makes it difficult for the chain ordering system to route due to the congestion caused by the placement of the cells. There are tool available that automate the reordering of the chain to reduce the congestion that is produced at the first stage. It increases the problem of the chain system and this also allow the overcoming of the buffers that have to be inserted into the scan path. The increase of the hold time in the chain reordering can cause great amount of delay. Chain reordering allows the cell to be come in the ordered format while using the different clock domains. It is used to reduce the time delay caused by random generation of the element and the placement of it.

Q32).What are the steps involved in designing an optimal pad ring?
Ans:
– To make the design for an optimal pad ring there is a requirement for the corner-pads that comes across all the corners of the pad-ring. It is used to give power continuity and keep the resistance low.
– It requires the pad ring that is to fulfil the power domains that is common for all the ground across all the domains.
– It requires the pad ring to contain simultaneous switching noise system that place the transfer cell pads in cross power domains for different pad length.

– Drive strength is been seen to check the current requirements and the timings to make the power pads.
– Choose a no-connection pad that is used to fill the pad-frame when there is no requirement for the inputs to be given. This consumes less power when there is no input given at a particular time.
– Checking of the oscillators pads take place that uses the synchronous circuits to make the clock data synchronize with the existing one.

Q33).What is the function of enhancement mode transistor?

Ans: The enhancement mode transistors are also called as field effect transistors as they rely on the electric filed to control the shape and conductivity of the channel. This consists of one type of charge carrier in a semiconductor material environment. This also uses the unipolar transistors to differentiate themselves with the single-carrier type operation transistors that consists of the bipolar junction transistor. The uses of field effect transistor is to physical implementation of the semiconductor materials that is compared with the bipolar transistors. It provides with the majority of the charge carrier devices. The devices that consists of active channels to make the charge carriers pass through. It consists of the concept of drain and the source.

Q34).What is the purpose of having Depletion mode Device?

Ans: Depletion modes are used in MOSFET it is a device that remains ON at zero gate-source voltage. This device consists of load resistors that are used in the logic circuits. This types are used in N-type depletion-load devices that allow the threshold voltages to be taken and use of -3 V to +3V is done. The drain is more positive in this comparison of PMOS where the polarities gets reversed. The mode is usually determined by the sign of threshold voltage for N-type channel. Depletion mode is the positive one and used in many technologies to represent the actual logic circuit. It defines the logic family that is dependent on the silicon VLSI. This consists of pull-down switches and loads for pull-ups.

Q35).What is the difference between NMOS and PMOS technologies?

Ans:

– PMOS consists of metal oxide semiconductor that is made on the n-type substrates and consists of active careers named as holes. These holes are used for migration purpose of the charges between the p-type and the drain. Whereas, NMOS consists of the metal oxide semiconductor and they are made on p-type substrates. It consists of electrons as their carriers and migration happens between the n-type source and drain.
– On applying the high voltage on the logic gates NMOS will be conducted and will get activated, whereas PMOS require low voltage to be activated.
– NMOS are faster than PMOS as the carriers that NMOS uses are electrons that travels faster than holes. The speed is twice as fast as holes.
– PMOS are more immune to noice than NMOS.

Q36).What is the difference between CMOS and Bipolar technologies?

Ans:

– CMOS technology allows the power dissipation to be low and it gives more power output, whereas bipolar takes lots of power to run the system and the ciricutary require lots of power to get activated.
– CMOS technology provides high input impedance that is low drive current that allow more current to be flown in the cirucit and keep the circuit in a good position, whereas it provides high drive current means more input impedance.
– CMOS technology provides scalable threshold voltage more in comparison to the Bipolar technology that provides low threshold voltage.
– CMOS technology provides high noise margin, packing density whereas Bipolory technology allows to have low noise margin so that to reduce the high volues and give low packing density of the components.

Q37).What are the different classification of the timing control?

Ans: There are different classification in which the timing control data is divided and they are:
1. Delay based timing control: this is based on timing control that allows to manage the component such that the delay can be notified and wherever it is required it can be given. The delays that are based on this are as:

– Regular delay control: that controls the delay on the regular basis.
– Intra-assignment delay control: that controls the internal delays.
– Zero delay control
2. Events based timing control: this is based on the events that are performed when an event happens or a trigger is set on an event that takes place. It includes
– Regular event control
– Named event control
– Event OR control
3. Level sensitive timing control: this is based on the levels that are given like 0 level or 1 level that is being given or shown and the data is being modified according the levels that are being set. When a level changes the timing control also changes.