

VLSI Project

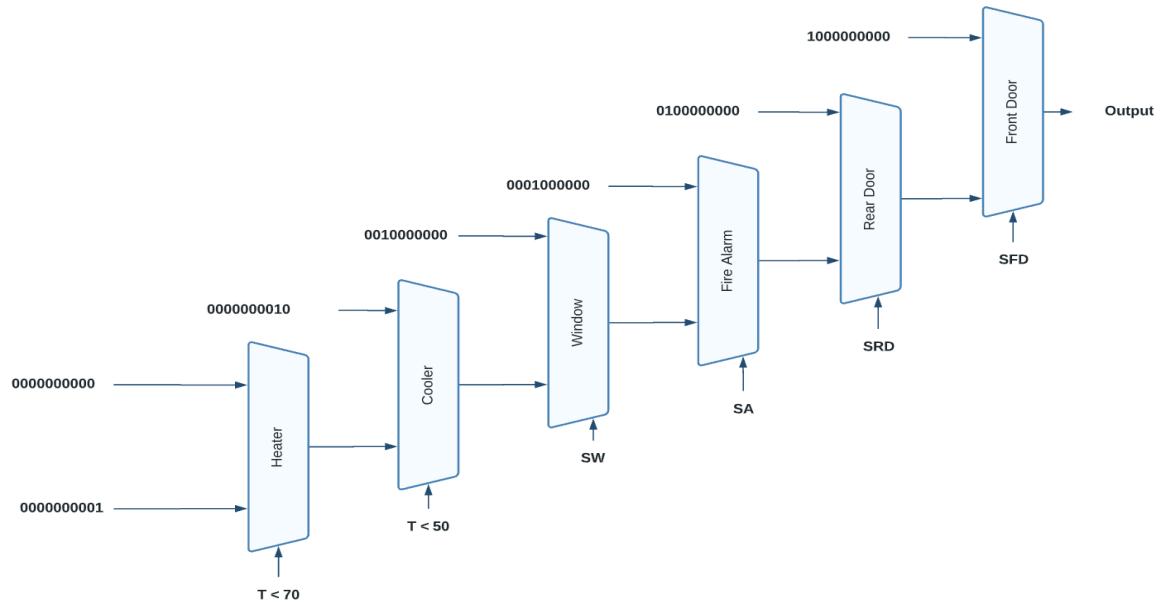
HOME SECURITY SYSTEM

Names	Section	Bench No.
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Ahmed Waleed	1	14
Essam Wisam	2	1
Mohamed Salama	2	15

Supervised by
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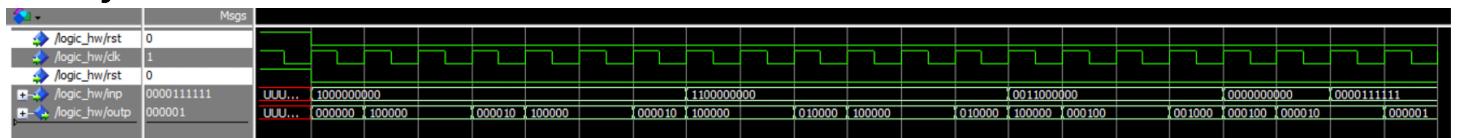
Primary Design Schematic



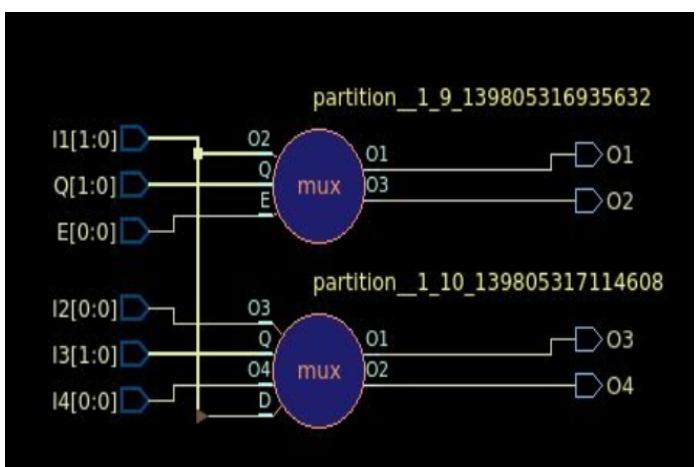
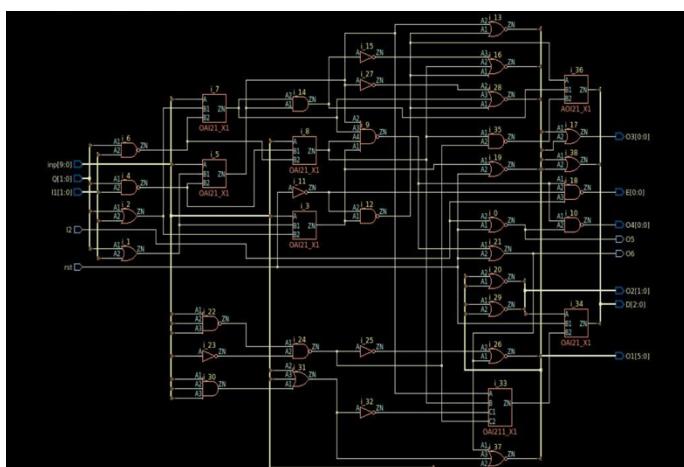
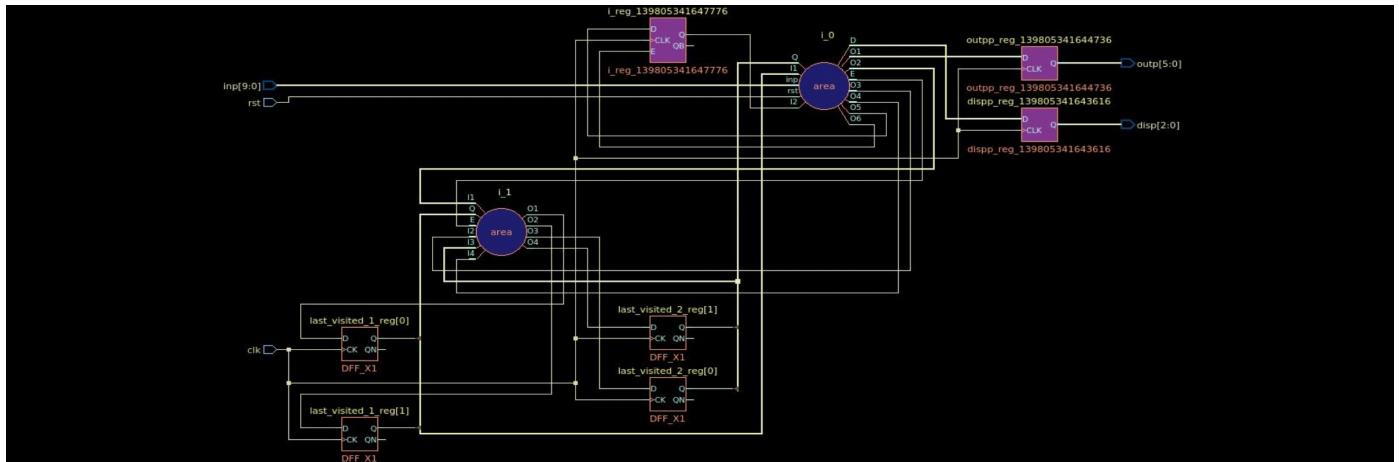
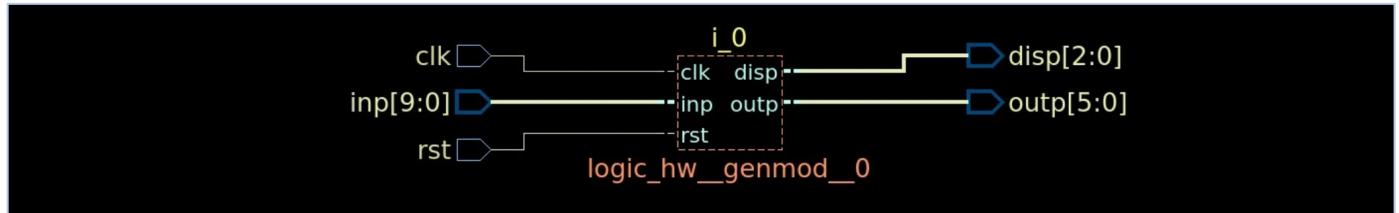
Code Snapshot

```
-- back door
elsif inp(8)='1' and not ((last_visited_1="01") and (last_visited_2="01")) then
    outpp <= (4 => '1', others =>'0');
    dispp <= "010";
    if(i = '0') then
        last_visited_1 <= "01";
        i <='1';
    else
        last_visited_2 <= "01";
        i <='0';
    end if;
-- For starvation
```

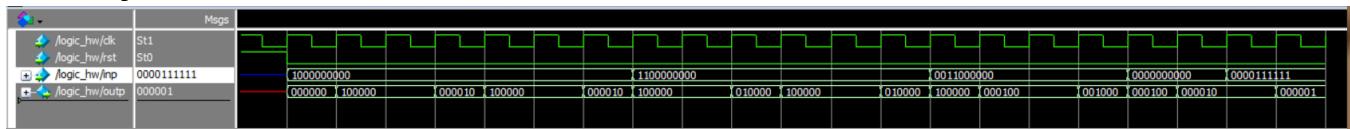
Pre-synthesis Simulation Results



Schematics of the Design After Synthesis

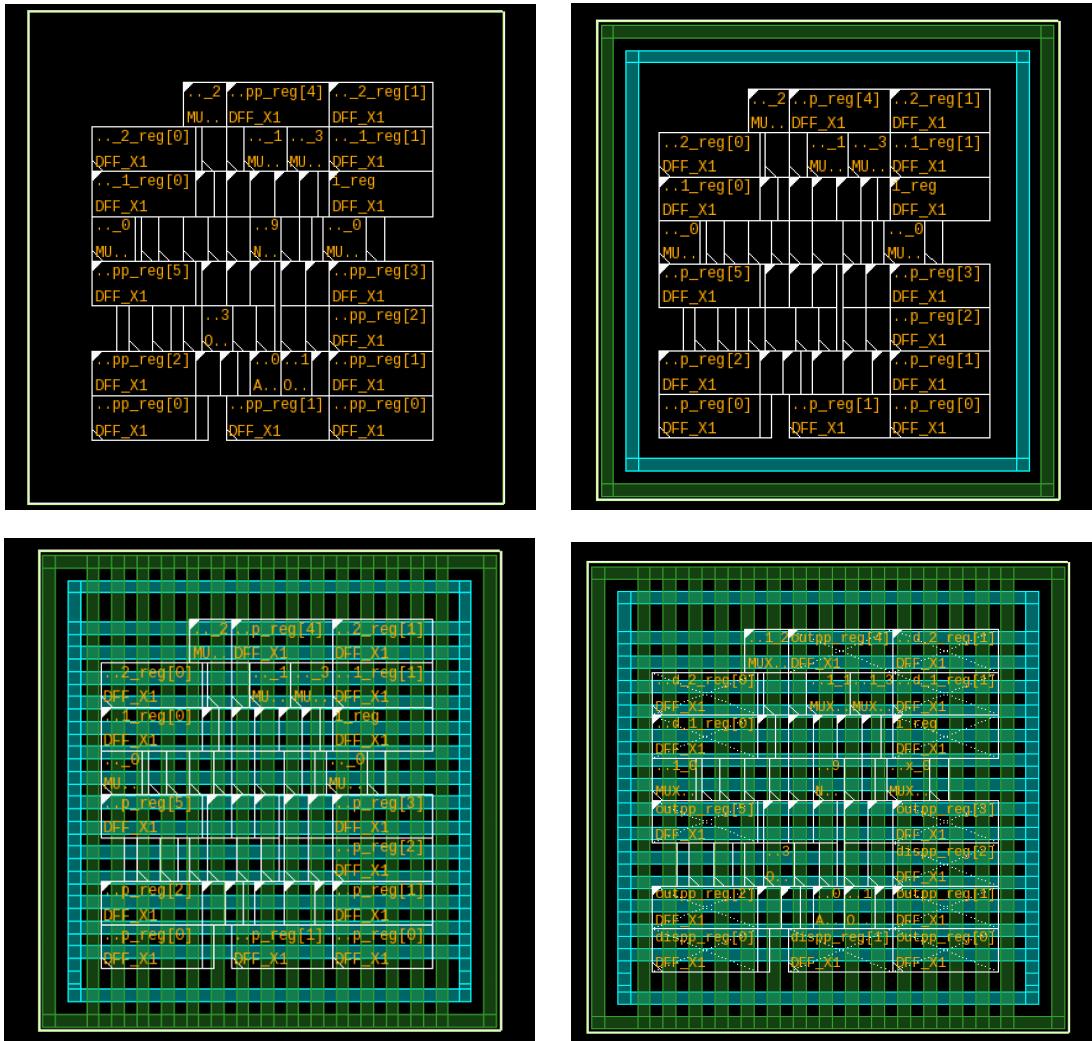


Post-synthesis Simulation Results

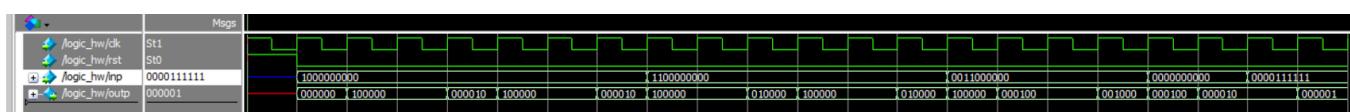


Post-synthesis Library Used: Nangate

Schematic of the Chip After Floorplanning, Placement & Routing



Post-routing Simulation Results



Synthesis Report (@1 GHz)

Report Physical info:

		Area (squm)	Leakage (uW)
Design Name	logic_hw		
Total Instances		58	109
Macros		0	0.000
Pads		0	0.000
Phys		0	0.000
Blackboxes		0	0.000
Cells		58	109
Buffers		0	0.000
Inverters		6	0.086
Clock-Gates		0	0.000
Combinational		38	42
Latches		0	0.000
FlipFlops		14	63
Single-Bit FF		14	1.108
Multi-Bit FF		0	0.000
Clock-Gated		0	0.000
Bits		14	63
Load-Enabled		0	0.000
Clock-Gated		0	0.000
Tristate Pin Count	Placed	0	
Physical Info			
Chip Size (mm x mm)	0.073 x 0.073	5399	
Fixed Cell Area		0	
Phys Only		0	
Placeable Area		168	
Movable Cell Area		109	
Utilization (%)	64		
Chip Utilization (%)	64		
Total Wire Length (mm)	0.776		
Longest Wire (mm)	0.037		
Average Wire (mm)	0.037		

Report Path Groups:

	Path Group	Weight	Critical Range(ps)	Worst Slack(ps)
1	default	1.000	0.0	593.4
2	I2R	1.000	0.0	16.3
3	I2O	1.000	0.0	<ill>
4	R2O	1.000	0.0	585.3

Worst Slack

Moveable Cell Area

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*dispp_reg[2]	0.644961	0.676065	0.079112	1.400139
2	*dispp_reg[1]	2.861119	2.997936	0.079112	5.938168
3	*dispp_reg[0]	3.889457	4.078257	0.079112	8.046825
4	*outpp_reg[5]	3.062198	3.217613	0.079112	6.358924
5	*outpp_reg[4]	1.860221	1.953875	0.079112	3.893208
6	*outpp_reg[3]	0.578602	0.608150	0.079112	1.265864
7	*outpp_reg[2]	1.054124	1.107195	0.079112	2.240431
8	*outpp_reg[1]	0.074011	0.077790	0.079112	0.230914
9	*outpp_reg[0]	0.373714	0.391500	0.079112	0.844326
10	*last_visited_1_reg[0]	3.782250	2.532695	0.079112	6.394057
11	*last_visited_1_reg[1]	3.955647	2.648806	0.079112	6.683566
12	*last_visited_2_reg[0]	3.050415	2.002007	0.079112	5.131534
13	*last_visited_2_reg[1]	3.955047	2.595724	0.079112	6.629883
14	*i_reg	3.275370	2.779124	0.079112	6.133606
15	*i_reg_enable_mux_0	1.939277	0.424889	0.035928	2.400094
16	*i_0_0_0	0.641428	1.848564	0.021200	2.511192
17	*i_0_0_1	0.622478	1.335967	0.022695	1.981140
18	*i_0_0_2	1.013769	2.171300	0.022695	3.207764
...					
56	*i_0_1_1	2.484963	0.503837	0.035928	3.024729
57	*i_0_1_2	1.724440	0.324646	0.035928	2.085014
58	*i_0_1_3	2.650426	0.507039	0.035928	3.193393
59					
60	*TOTAL	105.394875	119.476997	2.092153	226.964035

Total Power

Optimization Degree:

$$0.5(MCA) + 0.3(CLK - Worst Slack) + 0.2 (Total Power)$$

=

395.692

Brief Justification & Comparison:

The current design focuses on **optimizing area**, sustaining moderate **power** in sacrifice of some **speed**. Due to how simple it is, it was easily synthesizable and extending it with starvation was an easy process.

Prior to considering starvation, we considered two more designs (up to simulation and synthesis.) The first, *HomeSystem_Tree.vhd* aimed at shortening the critical path by dividing the whole design into two parts that would work in parallel each cycle (one responsible for temperature and another responsible for the doors, window and alarm). A simple MUX and an OR would do the job of deciding which output should propagate.

The second, *HomeSystem_Parallel.vhd* aimed at implementing a fully parallel design. Each bit in the output and display would be set independently using logic circuits that we derived for each bit.

After synthesis of each of the three designs (no starvation yet) at 1 *GHz* our results were:

	Area	Worst Slack	Power
Parallel	62	63	74.64
Regular	63	34	74.3
Tree	78	139	149

Clearly, the parallelized design seems to be slightly better than the regular one and the tree design has the best critical path in sacrifice of some power. However, whenever we started considering starvation for each of the designs the regular design did best in terms of the amount of extra hardware needed. Each logic circuit in the parallel design would be a function of four more input bits and our multiplexing logic in the tree design would ratchet up in complexity far more than normal. Thus, we stucked with the regular design.

Our approach to starvation is very straightforward; no sensor would be served more than two times consecutively if another also seeks to be served. For this we needed a small counter and four bits to record which two of the highest four priority sensors were served in the last two cycles.

We were also able to think about another slightly-more-complex solution to starvation that could be implemented in the regular design *HomeSystem_Dynamic.vhd* but after synthesis and comparing to our other solution to starvation we decided to stick with original one especially that its approach to starvation was somewhat less extreme.

Design Assumptions

1. The temperature sensor reading is 6-bits, which covers the range from 6 celsius to 41 celsius.
2. The system initially starts with a reset.

Thank you.