Universidad Nacional Autónoma de México
Facultad de Ingeniería
Diseño Digital VLSI

Descripción de *hardware*

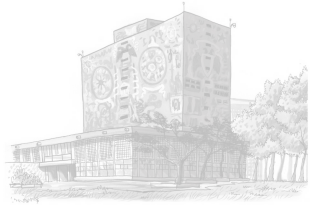
VHDL para circuitos secuenciales

M.I. Bryan Emmanuel Alvarez Serna

“Nadie puede hacerte sentir inferior sin tu consentimiento.”

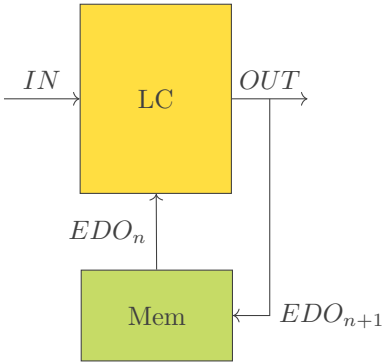
Eleanor Roosevelt

Contenido

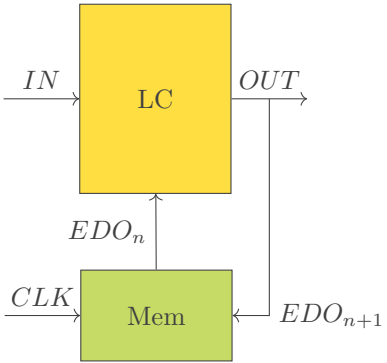


Circuitos secuenciales

Asíncrono

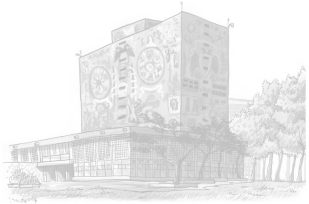


Síncrono

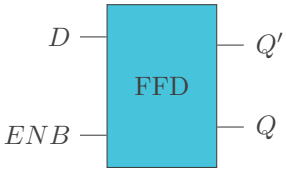


Contenido

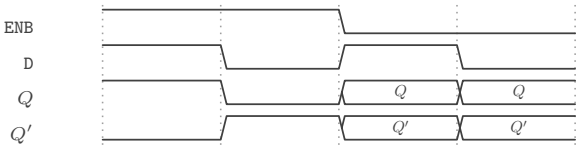
- Introducción
- **Asíncronos**
- Síncronos



FFD

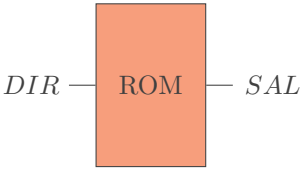


ENB	D	Q	Q'
1	1	1	0
1	0	0	1
0	1	Q	Q'
0	0	Q	Q'




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY ffd IS
        PORT(ENB, D: IN STD_LOGIC;
             Q, QN: BUFFER STD_LOGIC);
END ENTITY;

ARCHITECTURE BEAS OF ffd IS
BEGIN

     PROCESS(ENB)
     BEGIN
        IF ENB = '1' THEN
           Q <= D; QN <= NOT(Q);
        ELSE
           Q <= Q; QN <= QN;
        END IF;
     END PROCESS;

END ARCHITECTURE;
```

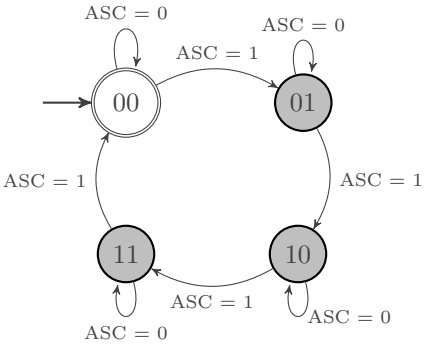
ROM




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY rom IS
PORT(DIR: IN INTEGER RANGE 0 TO 3;
     SAL: OUT STD_LOGIC_VECTOR(0 TO 7));
END ENTITY;

ARCHITECTURE BEAS OF rom IS
TYPE MEM IS ARRAY (0 TO 3) OF STD_LOGIC_VECTOR(0 TO 7);
CONSTANT ROM: MEM:=( X"F1", X"A8", X"9E", X"17");
BEGIN
  SALIDA <=ROM(DIR);
END BEAS;
```

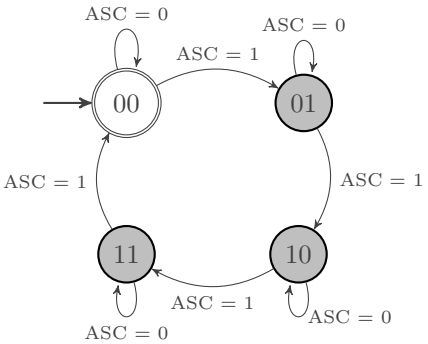
Contador asíncrono

Ejemplo: Contador asíncrono ascendente de 2 bits.



Contador asíncrono

Ejemplo: Contador asíncrono ascendente de 2 bits.



Contador asíncrono

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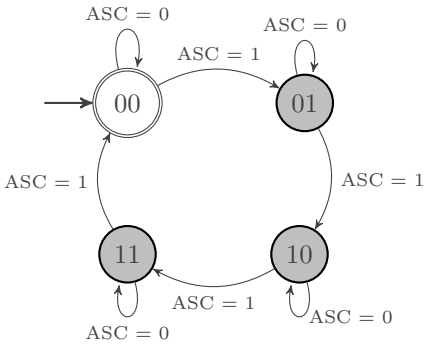
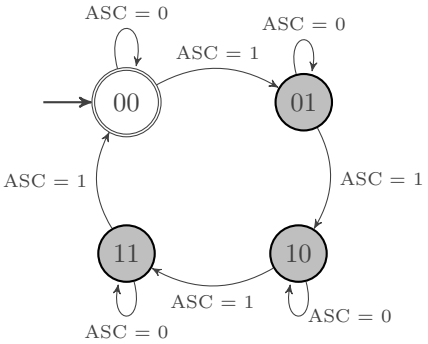


¿Funciona?

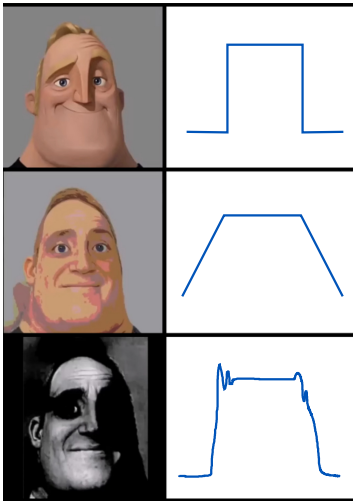
Contador asíncrono

Ejemplo: Contador asíncrono ascendente de 2 bits.



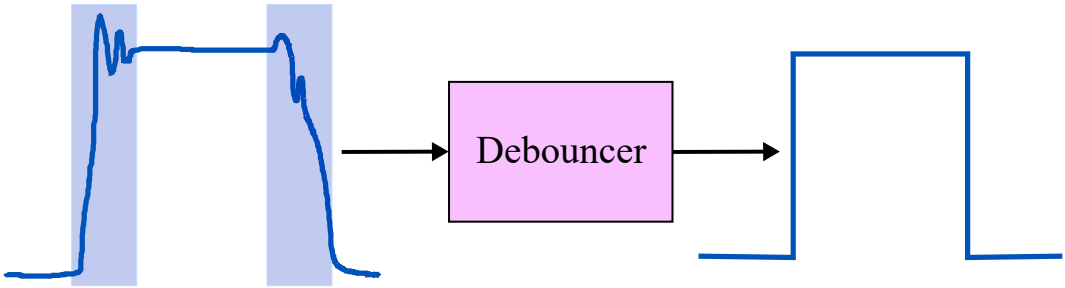
¿Funciona?
No siempre...

Rebote

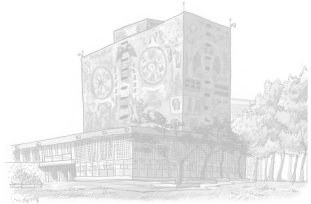


Rebote

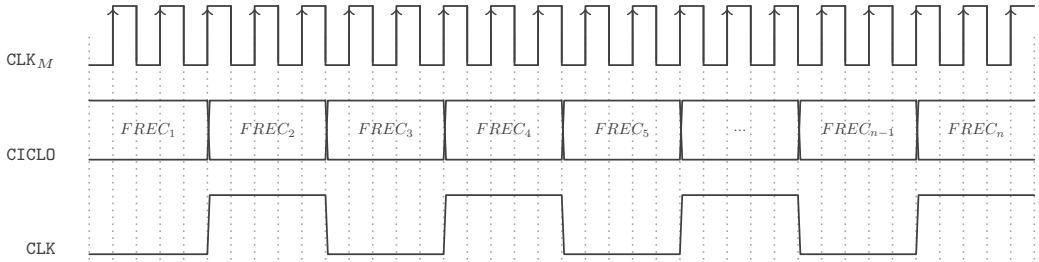
¿Cómo se soluciona?



Contenido



Divisor de frecuencia



$$FREC = \frac{CLK_M}{2f_x} - 1$$

Divisor de frecuencia


```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY divisor IS
   GENERIC(FREC: INTEGER := 24999999); -- FREC = (50 MHz/2*Fdeseada) - 1
        -- 24999     >> 1 kHz
        -- 249999    >> 100 Hz
        -- 24999999 >> 1 Hz
   PORT(CLK_MST: IN STD_LOGIC; -- RELOJ PRINCIPAL
                              CLK: BUFFER STD_LOGIC);
END ENTITY;

ARCHITECTURE BEAS OF divisor IS
SIGNAL AUX: INTEGER RANGE 0 TO FREC;
BEGIN

    PROCESS(CLK_MST)
    BEGIN
        IF RISING_EDGE (CLK_MST) THEN
           IF AUX = 0 THEN
              CLK <= NOT CLK;
              AUX <= FREC;
           ELSE
              AUX <= AUX - 1;
           END IF;
        END IF;
    END PROCESS;

END BEAS;
```

Contador síncrono

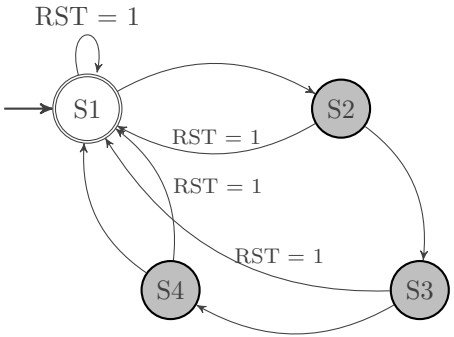
Ejemplo: Contador síncrono de anillo de n bits.

Contador síncrono

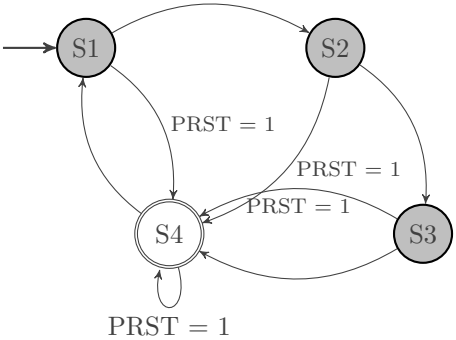
Ejemplo: Contador síncrono de anillo de n bits con RST o PRST.

RST y PRST

RST: Reiniciar.



PRST: Preestablecer.



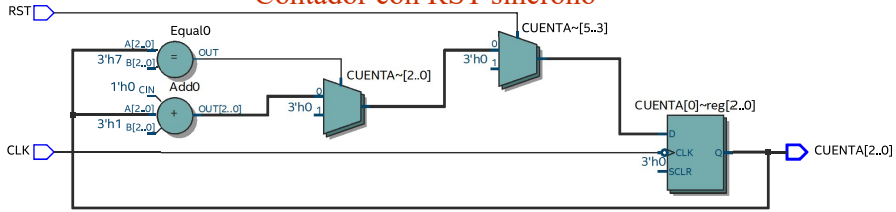
Contador con RST

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY conta IS
PORT(CLK, RST: IN STD_LOGIC;
     CUENTA: BUFFER INTEGER RANGE 0 TO 7);
END ENTITY;

ARCHITECTURE BEAS OF conta IS
BEGIN
  PROCESS(CLK, RST)
  BEGIN
     IF RST = '1' THEN
        CUENTA <= 0;
     ELSIF FALLING_EDGE(CLK) THEN
        IF CUENTA = 7 THEN
           CUENTA <= 0;
        ELSE
           CUENTA <= CUENTA + 1;
        END IF;
     END IF;
END PROCESS;
END BEAS;
```

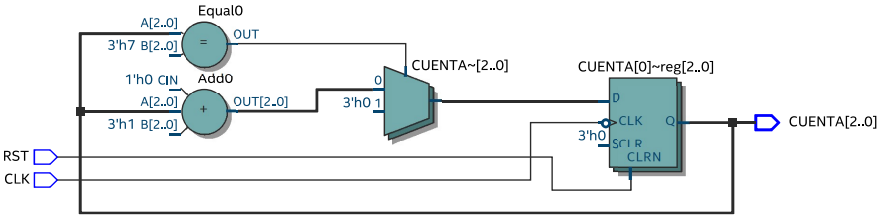
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY conta IS
PORT(CLK, RST: IN STD_LOGIC;
     CUENTA: BUFFER INTEGER RANGE 0 TO 7);
END ENTITY;

ARCHITECTURE BEAS OF conta IS
BEGIN
  PROCESS(CLK, RST)
  BEGIN
     IF FALLING_EDGE(CLK) THEN
        IF RST = '1' THEN
           CUENTA <= 0;
        ELSIF CUENTA = 7 THEN
           CUENTA <= 0;
        ELSE
           CUENTA <= CUENTA + 1;
        END IF;
     END IF;
  END PROCESS;
END BEAS;
```

Contador con RST

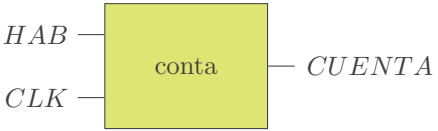
Contador con RST síncrono



Contador con RST asíncrono

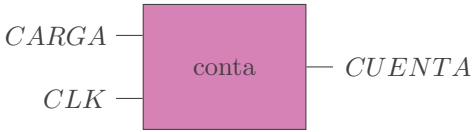


Contador con HAB



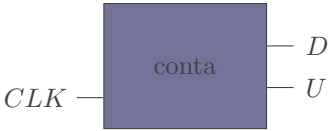

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY conta IS
PORT(CLK, HAB: IN STD_LOGIC;
     CUENTA: BUFFER INTEGER RANGE 0 TO 7);
END ENTITY;

ARCHITECTURE BEAS OF conta IS
BEGIN
  PROCESS(CLK, HAB)
  BEGIN
     IF FALLING_EDGE(CLK) THEN
        IF HAB = '1' THEN
           CUENTA <= CUENTA;
        ELSIF CUENTA = 7 THEN
           CUENTA <= 0;
        ELSE
           CUENTA <= CUENTA + 1;
        END IF;
     END IF;
  END PROCESS;
END BEAS;
```

Contador con carga paralela




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY conta IS
PORT(CLK, HAB: IN STD_LOGIC;
       CARGA: IN INTEGER RANGE 0 TO 7;
      CUENTA: BUFFER INTEGER RANGE 0 TO 7);
END ENTITY;

ARCHITECTURE BEAS OF conta IS
BEGIN
  PROCESS(CLK, HAB)
  BEGIN
     IF FALLING_EDGE(CLK) THEN
        IF CUENTA = CARGA THEN
           CUENTA <= 0;
        ELSE
           CUENTA <= CUENTA + 1;
        END IF;
     END IF;
  END PROCESS;
END BEAS;
```

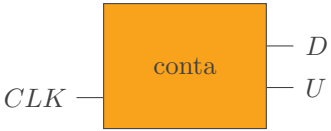
Contador por década



0	1	2	3	4	5	6	7	8	9
1									

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY contadec IS
        PORT(CLK: IN STD_LOGIC;
             D, U: BUFFER INTEGER RANGE 0 TO 9);
END ENTITY;

ARCHITECTURE BEAS OF contadec IS
BEGIN

    PROCESS(CLK)
    BEGIN
        IF FALLING_EDGE (CLK) THEN
           IF U = 9 THEN
              U <= 0;
              IF D = 9 THEN
                 D <= 0;
              ELSE
                 D <= D + 1;
              END IF;
           ELSE
              U <= U + 1;
           END IF;
        END IF;
    END PROCESS;

END BEAS;
```

Contador con MOD



Ejemplo:

$25/20 = 2$ y sobran 5

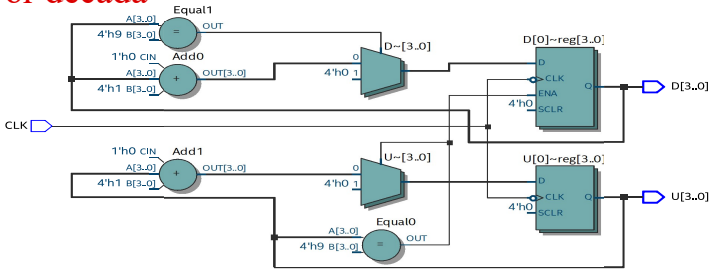
$\therefore 25 \text{ MOD } 10 = 5$

$(25/10) \text{ MOD } 10 = 2.5$

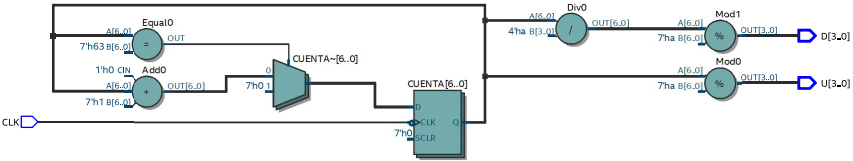
```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY contamod IS
    PORT(CLK: IN STD_LOGIC;
         D, U: OUT INTEGER RANGE 0 TO 9);
END ENTITY;

ARCHITECTURE BEAS OF contamod IS
SIGNAL CUENTA: INTEGER RANGE 0 TO 99;
BEGIN

    PROCESS(CLK)
    BEGIN
       IF FALLING_EDGE (CLK) THEN
          IF CUENTA = 99 THEN
             CUENTA <= 0;
          ELSE
             CUENTA <= CUENTA + 1;
          END IF;
       END IF;
    END PROCESS;

    PROCESS(CUENTA)
    BEGIN
       U <= CUENTA MOD 10;
       D <= (CUENTA/10) MOD 10;
    END PROCESS;
```

Comparación de hardware

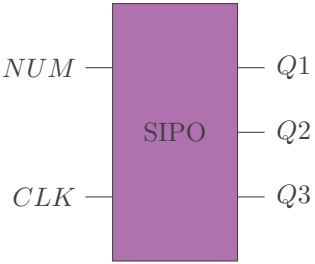
Por década

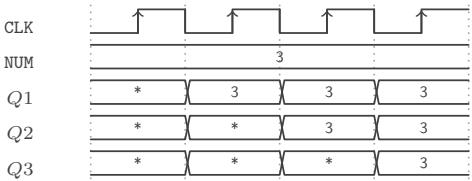


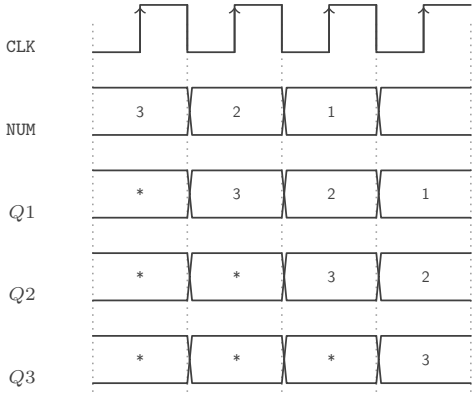
Con MOD



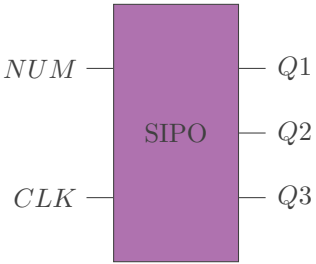
Registro SIPO





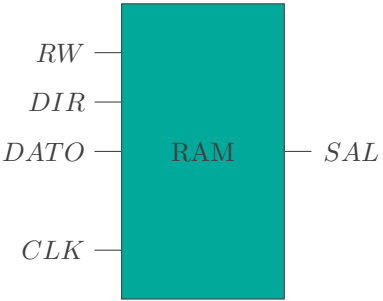


Registro SIPO




```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY reg_d IS
PORT(NUM: IN INTEGER RANGE 0 TO 9;
     CLK: IN STD_LOGIC;
     Q1,Q2,Q3: BUFFER INTEGER RANGE 0 TO 9);
END ENTITY;

ARCHITECTURE BEAS OF reg_d IS
BEGIN

        PROCESS(CLK)
        BEGIN
           IF RISING_EDGE(CLK) THEN
              Q1 <= NUM;
              Q2 <= Q1;
              Q3 <= Q2;
           END IF;
        END PROCESS;

END BEAS;
```

Memoria RAM




```
ENTITY ram IS
  PORT(CLK,RW:STD_LOGIC;
           DIR: IN INTEGER RANGE 0 TO 7;
           SAL: OUT INTEGER RANGE 0 TO 255;
          DATO: IN INTEGER RANGE 0 TO 255);
END ENTITY;

ARCHITECTURE BEAS OF ram IS
TYPE MEMORIA IS ARRAY (0 TO 7) OF INTEGER RANGE 0 TO 255;
SIGNAL RAM: MEMORIA;
BEGIN
     PROCESS(CLK)
     BEGIN
        IF RISING_EDGE (CLK) THEN
           IF RW='1' THEN
              RAM(DIR) <= DATO;
           ELSE
              SAL <= RAM(DIR);
           END IF;
        END IF;
     END PROCESS;
END BEAS;
```