Esteban José Garzón Córdova

Post-Doctoral Research Fellow

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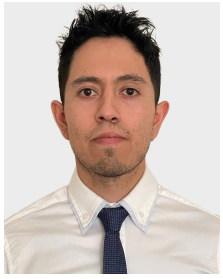

Biref Biography

Esteban Garzón received the B.Sc. Degree (cum laude) in Electronics Engineering from the Universidad San Francisco de Quito (USFQ), Ecuador, in 2016, the dual M.Sc. degree (GPA: 4.0/4.0) in Nanoelectronics and Electronics from USFQ and University of Calabria (UNICAL), Italy, in 2018, and the Ph.D. degree in Electronics Engineering from UNICAL, in 2022. The same year, he won a highly competitive research fellowship funded by the Italian Ministry for Universities and Research (MUR), under the call "Horizon Europe 2021-2027 Programme". He is currently a research fellow with the Department of Computer Engineering, Modeling, Electronics, and Systems Engineering (DIMES), UNICAL.
In 2019-2020 he was a visiting Ph.D student at EnICS laboratories, BIU, Israel. In Jul-Sep 2022 and Jul-Aug 2023, he was a visiting researcher at EnICS labs.
E. Garzón was IEEE graduate student member from 2016, and became IEEE member from 2022. He has authored/coauthored more than 40 scientific papers in international peer-reviewed journals and conferences, and has participated in several IC tapeouts. His research interests include domain-specific hardware accelerators, electronics/spintronics, cryogenic memories, and standard and emerging technologies for logic & memory, and low-power applications. He has received several awards, research grants, and funding. E. Garzón has been part of several IEEE conference committees, journal boards (review editor of Frontiers in Electronics and Frontiers in Aerospace Engineering), and has been an active reviewer of several journals (IEEE and Elsevier) and conferences (only IEEE).

Professional Experience

01/06/2022–present **Postdoctoral Research Fellow (Current position)**, *Department of Computer Engineering, Modeling, Electronics and Systems (DIMES), University of Calabria,*, Rende, Italy.
Main research activities and responsibilities: spin electronics/spintronics | cryogenic electronics | emerging technologies for logic & memory, and low-power applications | hardware design for probabilistic computing | Content-addressable memories | Digital-on-top IC design (Cadence tools).

09/07/2023–28/08/2023 **Visiting Researcher**, *Emerging NanoScaled Integrated Circuits & Systems Labs, Faculty of Engineering, Bar-Ilan University*, Ramat-Gan, Israel.
Main activities and responsibilities: (a) Design of a hardware accelerator for Vision Transformer. (b) Exploiting associative (content-addressable) memories for detection and identification of Pathogens. (c) Development of a setup and measurements of an associative memory built in 65 nm process. (d) Research on multi-ported memories using standard-cell memory approach.

05/07/2022–04/09/2022 **Visiting Researcher**, *Emerging NanoScaled Integrated Circuits & Systems Labs, Faculty of Engineering, Bar-Ilan University*, Ramat-Gan, Israel.
Main activities and responsibilities: (a) Design of associate processor using standard (CMOS) and emerging memory technologies (resistive memories); (b) Design of programmable address decoder for a fully associative cache. (c) Design of an associative memory (i.e., CAM) prototype in 65 nm process.

29/09/2019–20/09/2020 **Visiting Ph.D. Student**, *EnICS Labs, Faculty of Engineering, Bar-Ilan University*, Ramat-Gan, Israel.
Main research activities and responsibilities: design and evaluation of emerging embedded memories operating at cryogenic temperatures (77 K) and full Backend design of a novel System-on-Chip (SoC).

10/06/2016–21/12/2016 **Semiconductor Wafer Test Engineer**, *Institute of Micro and Nanoelectronics, Universidad San Francisco de Quito*, Quito, Ecuador.
Main activities and responsibilities: Testing, measuring, and characterizing radio frequency devices on a silicon wafer by a Cascade probe station.

Education

01/11/2018–31/05/2022 **Ph.D. in Electronics Engineering**, *Department of Computer Engineering, Modeling, Electronics and Systems (DIMES), University of Calabria.*, Rende, Italy, Final grade: Highest regard.
- Advisor: Prof. Marco Lanuzza
- Co-Advisor: Prof. Adam Teman
- Ph.D Thesis:"Spin-Transfer Torque Magnetic RAM (STT-MRAM) For Embedded Memory Applications"
- Main subject / occupational skills covered: VLSI Circuits, Systems, and Applications; Spin Electronics/Spintronics; Emerging memory technologies (In particular, MRAMs); Device-to-System Level Assessments; Cryogenic memories; Approximate high-performance memories.

22/08/2016–19/09/2018 **M.Sc. in Electronics Engineering (Degree 2 of a Double Degree Program)**, *University of Calabria*, Rende, Italy, Final grade (GPA): 110/110.
- Thesis:"Assessment of Write and Read Operations in Nanoscaled STTMRAM Technologies"
- Main subject / occupational skills covered: FinFET-28nm; STT-MRAM; Bitcell memory design; Magnetic tunnel junction (MTJ); Single- Barrier MTJ (SMTJ); Double-Barrier MTJ (DMTJ); technology scaling; Synopsys & Cadence Tools.

22/08/2016–19/09/2018 **M.Sc. in Nanoelectronics (Degree 1 of a Double Degree Program)**, *Universidad San Francisco de Quito*, Quito, Ecuador, Final grade (GPA): 3.9/4.0.
- Thesis:"Assessment of Write and Read Operations in Nanoscaled STT-MRAM Technologies"
- Main subject / occupational skills covered: FinFET-28nm; STT-MRAM; Bitcell memory design; Magnetic tunnel junction (MTJ); Single- Barrier MTJ (SMTJ); Double-Barrier MTJ (DMTJ); technology scaling; Synopsys & Cadence tools.

22/08/2011–09/06/2016 **B.Sc. in Electronics Engineering**, *Universidad San Francisco de Quito*, Quito, Ecuador, Final Grade: Cum Laude.
Thesis activities include silicon wafer measurements, setup development for RFCV measurements, and use of ultra-scaled transistors/RF devices.

Training: Courses, Webinars, Workshops, Events

28/11/2023 **Webinar**, *"Low power cryo-CMOS design for quantum computing applications"*, ACRC Webinar, Virtual.

28/11/2023 **Event**, *"From Chips to Chiplets in the Generative AI Era"*, IBM/IEEE AI Compute Symposium. This hybrid event focuses on AI/ML computing research, Virtual.

21/11/2023, 12/11/2023 **Webinar**, *"Fondi europei 2021-2027, tecniche di progettazione e budget"*, Obiettivo Europa Group, Online.

09/11/2023, 13/11/2023 **Workshop**, *"Non-Traditional Computing Paradigms with Emerging Technologies for Energy Efficiency"*, IEEE SSCS, Online.

18/10/2023 **Webinar**, *"The Synergy of AI and Video Compression in the Era of Internet of Video Things"*, Online.

27/09/2023 **Webinar**, *"Challenges and Directions in State of the Art Nanoelectronics"*, Online.

26/04/2023 **Webinar**, *"Advancing Magnetic Memory Technology with Atomistic Modeling of Novel Materials & Concepts"*, Synopsys Webinars, Online.

24/05/2023 **Webinar**, *"Advancing MRAM Technology with Atomistic Spin Dynamics Simulations"*, Synopsys Webinars, Online.

22/03/2023 **Webinar**, *"On-chip communication: from architectures to circuits"*, IEEE SSCS and IEEE Israel CASS Chapters, Online.

22/03/2023 **Webinar**, *"On-chip communication: from architectures to circuits"*, IEEE SSCS and IEEE Israel CASS Chapters, Online.

13/12/2022–16/12/2022 **Course**, *"Spintronics: Fundamentals and applications"*, IEEE Magnetics Society Italy Chapter, In Person.

01/11/2022–07/11/2022 **Course**, *"2022 Intelligence in Chip"*, IEEE CASS Seasonal School, Online.

04/10/2022–13/10/2022 **Webinar**, *"OPEN SCIENCE IN HORIZON EUROPE"*, APRE, Online, October 04, 05, and 13.

20/07/2022 **Event**, *"Intel 2022 Academic Day"*, Intel, Virtual.

23/05/2022–26/05/2022 **Course**, *"Hardware for Deep Learning"*, DIMES, University of Calabria, In-Person.

23/02/2021–26/02/2021 **Course**, *"Spintronics for Beyond-CMOS Computing"*, DIMES, University of Calabria, In-Person.

08/02/2021–12/02/2021 **Course**, *"Implementation of Tensilica ASSP Core: RTL, synthesis, and physical implementation using Cadence tools (Genus, Innovus, and Tempus)"*, Europractice, Online.

03/02/2021 **Seminar**, *"Circuits and Architectures with Ultra-Wide Power-Performance Adaptation – Going way beyond voltage scaling"*, Department of Electrical Engineering, Technion-Israel Institute of Technology, Online.

16/11/2020–17/11/2020 **Course**, *"PhD3.0 - Valorizzazione della ricerca e Creazione d'impresa"*, DIMES, University of Calabria, Online.

17/08/2020 **Seminar**, *"Mixed-Signal Computing for Deep Neural Network Inference"*, Department of Electrical Engineering, Technion-Israel Institute of Technology, Online.

09/08/2020 **Seminar**, *"Evolution of Cellular RFICs (2G to 5G)"*, Department of Electrical Engineering, Technion-Israel Institute of Technology, Online.

02/06/2020 **Seminar**, *"Agile Hardware Design with a Generator-Based Methodology"*, Department of Electrical Engineering, Technion-Israel Institute of Technology, Online.

14/05/2020 **Seminar**, *"Quantum Computer on a CMOS Chip"*, Department of Electrical Engineering, Technion-Israel Institute of Technology, In Person.

20/02/2020 **Seminar**, *"Bio-Inspired Micro & Nano Electronic Systems for Robotics and Biomedical Applications"*, Faulty of Engineering, Bar-Ilan University, In Person.

01/13/2020–15/08/2020 **Course**, *"Advanced Digital VLSI Design II – Lecture Series on Hardware for Deep Learning"*, Faulty of Engineering, Bar-Ilan University, Online.

14/10/2019 **Training**, *"The PULP Training - Speeding up the knowledge of the coolest microcontroller"*, Faulty of Engineering, Bar-Ilan University, In Person.

17/09/2019 **Course**, *"Universal hashing, perfect hashing and bloom filters"*, DIMES, University of Calabria, In Person.

08/07/2019–12/07/2019 **Course**, *"Approximation Fixpoint Theory and its Applications"*, DIMES, University of Calabria, In Person.

10/04/2019–12/04/2019 **Course**, *"Microwave Imaging"*, DIMES, University of Calabria, In Person.

08/04/2019–10/04/2019 **Course**, *"Design of Experiments Classical results and recent advances"*, DIMES, University of Calabria, In Person.

26/03/2019–29/03/2019 **Course**, *"Ensemble Learning for Big Data and cybersecurity"*, DIMES, University of Calabria, In Person.

11/02/2019–15/02/2019 **Course**, *"From Modeling to Implementation of IoT Systems"*, DIMES, University of Calabria, In Person.

04/02/2019–09/02/2019 **Course**, *"Emergent novel technologies for the design of planar devices"*, DIMES, University of Calabria, In Person.

12/12/2018–13/12/2018 **Course**, *"EBio-Inspired Algorithms and Parallel Comp in Emerging App Domain"*, DIMES, University of Calabria, In Person.

12/12/2018–13/12/2018 **Workshop**, *"Workshop of Digital Integrated Circuits Design with Synopsys tools"*, Synopsys, In Person.

Language Skills

Mother Tongue: **Spanish**.

Other languages: **English**.
Listening: C2 | Reading: C2 | Writing: C2 | Spoken Production: C2 | Spoken Interaction: C2

Italian.
Listening: C2 | Reading: C2 | Writing: C1 Spoken Production: C1 | Spoken Interaction: C1

French.
Listening: A1 | Reading: A1 | Writing: A1 Spoken Production: A1 | Spoken Interaction: A1

Hard Skills

Digital Skills: Microsoft Office: proficient user | Visio | Slack | Trello | Slack | Zoom | Operating Systems (Windows, Linux) | Inkscape | Gimp

Programming/Scripting: Python | GIT & Github | TCL Scripting | Verilog | LaTeX | VerilogA | bash-script | C++ | MATLAB | VHDL | SKIL L

CAD/EDA Tools: Cadence tools: Virtuoso, Genus, Innovus, Xcelium | Synopsys Tools: Sentaurus, CDesigner, IC compiler.

Teaching Experience

Spring 2021–Present **Graduate Course**, *Analog Systems Design Lab*, Department of Computer Engineering, Modeling, Electronics and Systems, University of Calabria (UNICAL), Rende, Italy.
Graduate course: Electronics Graduate Degree at UNICAL
Academic years: Spring 2021, Spring 2022, Spring 2023
CFU: 1.3 | Hours: 16

14/06/2023–15/06/2023 **PhD Course**, *Spintronic Technology For Energy-Efficient hybrid CMOS/MTJ Memory Applications*, University of Calabria, Rende, Italy.
CFU: 1 | Hours: 4

15/05/2023–16/05/2023 **PhD Course**, *Hybrid CMOS/MTJ Circuit Design*, Politecnico di Bar, Bari, Italy.
CFU: 1.5 | Hours: 5

13/02/2023–24/02/2023 **Invited Course**, *Digital CMOS Technology*, Institue of Micro and Nano Electronics, Universidad San Francisco de Quito (USFQ), Quito, Ecuador.
Graduate-level course: Nanoelectronics Graduate Degree at USFQ
CFU: 3 | Hours: 24

13/06/2022–24/06/2022 **Invited Course**, *Digital CMOS Technology*, Institue of Micro and Nano Electronics, Universidad San Francisco de Quito (USFQ), Quito, Ecuador.
Graduate-level course: Nanoelectronics Graduate Degree at USFQ
CFU: 3 | Hours: 24

Research Activity

Assessment of Spin-Transfer Torque Magnetic RAM (STT-MRAM) For Embedded Energy-Effcient Memory Applications and Beyond.

Non-volatile spintronic memories represent a promising knob to deal with the increased leakage power resulting from the scaling down of CMOS technology towards the end of Moore's law. In particular, spin-transfer torque magnetic random access memories (STT- MRAMs) based on perpendicular magnetic tunnel junctions (pMTJs) are already on the market with potential improvements targeting low-power and high-speed operation, high density, high endurance, long data retention time, low fabrication cost, and easy integration with CMOS processes. Thanks to the above properties, STT-MRAMs are actually considered premier candidates for replacing conventional semiconductor-based cache memories at more scaled technology nodes. However, one of the main challenges for a wider spread of STT-MRAMs is the reduction of their writing currents for both energy and area savings.

My research activity is focused on non-volatile cache memories implemented by STT-MRAMs based on state-of-the-art pMTJs, along with low-power devices like FinFETs or TFETs.

The main research topics cover:

- Technology and voltage scaling by considering STT-MRAMs based on single-barrier MTJs (SMTJs) and double-barrier MTJs (DMTJs).
- STT-MRAMs for ultralow-power/ultralow-energy application domains by considering very scaled DMTJs along with tunnel FET (TFET) technology.
- SMTJ-based and DMTJ-based STT-MRAMs operating at the liquid nitrogen temperature, which is considered an interesting alternative to deal with the power/ memory wall of classical room-temperature computing. Other memory technologies include embedded DRAM and SRAM.
- In-memory-computing with emerging memory technologies.

Hardware accelerators based on associative memories (a.k.a. Content-Addressable Memories) for Emerging Data-Intensive Applications.

Content-addressable memories (CAMs) offer outstanding performance in applications where high-speed searching is a crucial feature. In addition to conventional applications, such as network routers, digital signal processing, analytics, and reconfigurable computing. CAMs can be used for a variety of compare-intensive big data workloads, as well as for genome analysis. In particular, genome analysis is a growing research field and the basis for different kinds of applications, such as monitoring environmental ecosystems, sustainable agriculture, Earth's environment, and medicine. For medical applications, genome analysis, along with the real-time polymerase chain reaction (PCR) method, is widely used for the diagnosis of viral diseases. However, PCR diagnostic tests for virus detection in living organisms are not always available and are often limited by performance and reliability. This limits the possibility of safe and quick detection of the emergence of pathogenic viruses.

Within the above context, the research consists of the design of a novel approximate CAM for DNA pattern search, which can be exploited for viral DNA detection. Results obtained from electrical simulations are used to test the novel memory system in real genome-sequenced examples by considering real SARS-CoV-2 viral data samples from the National Center for Biotechnology Information (NCBI) online data sets. Sequenced SARSCoV-2 data can be used as a readout and can be fed to the system as the reference pattern to be able to compare it with different SARS-CoV-2 samples. In this way it is expected outstanding sensitivity for virus detection, proving that approximate CAMs can be a noteworthy solution for DNA pattern detection. This research activity is carried out in joint cooperation with EnICS Laboratories, Bar-Ilan University, Israel.

Research Grants & Funding

09/2022–Present **Funded Project**, *Design and implementation of novel computation systems based on spintronic devices*, The Italian factory of micromagnetic modeling and spintronics (IT-SPIN), 2020LWPKH7.

- Role: Researcher
- Budget: 796k€ (160k€ net amount of the local unit or department

12/2022–11/2024 **Research Grant**, *Develop scientific ideas and competitive project proposals within the Horizon Europe program*, Italian Ministry for Universities and Research (MUR), H25F21001420001.

- Role: Main Investigator/Workforce
- Budget: 77k€

12/2022–11/2024 **Research Grant**, *Training programs for the presentation of research projects within the context of the calls of the European Research Council (ERC)*, Italian Ministry for Universities and Research (MUR), under the call "Horizon Europe 2021-2027 programme – H25F21001420001".
- Role: Main Investigator/Workforce
- Budget: 15k€

Scientific Collaborations

National.

1. Department of Computer Engineering, Modeling, Electronics and Systems, University of Calabria, Rende, Italy.
   Referent: Prof. Marco Lanuzza | Prof. Felice Crupi | Prof. Raffaele De Rose | Dr. Ramiro Taco
2. Department of Information Engineering, University of Pisa, Pisa, Italy.
   Referent: Prof. Giuseppe Iannaccone | Prof. Sebastiano Strangio
3. Department of Electrical and Information Engineering, Politecnico di Bari, Bari, Italy
   Referent: Prof. Mario Carpentieri | Dr. Adrea Meo
4. Department of Mathematical and Computer Sciences, Physical Sciences and Earth Sciences, University of Messina, Messina, Italy
   Referent: Prof. Giovanni Finocchio

International.

1. EnICS Labs, Faculty of Engineering, Bar-Ilan University, Raman-Gan, Israel.
   Referent: Prof. Adam Teman | Dr. Leonid Yavits | Prof. Alexander Fish
2. Institut supérieur d'électronique de Paris, Paris, France
   Referent: Prof. Giuseppe Iannaccone | Prof. Lionel Trojman
3. L'Institut National des Sciences Appliquées, Toulouse, France
   Referent: Prof. Etienne Sicard
4. University of California, Berkeley, California, USA.
   Referent: Prof. Andrei Vladimirescu
5. Institute of Micro and Nano Electronics, Faculty of Engineering, Quito, Ecuador.
   Referent: Prof. Luis-Miguel Procel

Bibliometric Indicators

Total number of publications (peer-reviewed): 43

International Journals: 27

Conferences: 15

Book Chapter: 1

Total number of citations: 228 (Scopus Database; updated: 28/11/2023)

H-index: 10 (Scopus Database; updated: 28/11/2023)

i10-index: 11 (Scopus Database; updated: 28/11/2023)

Prizes, Honours, Awards

08/2023 **Featured Article**.
- Journal: Applied Physics Letters
- Paper: A. Meo, **E. Garzón**, R. De Rose, G. Finocchio, M. Lanuzza, M. Carpentieri, "Voltage-controlled magnetic anisotropy based physical unclonable function," in Applied Physics Letters, 2023. DOI: 10.1063/5.0166164.

02/2023 **Best Paper Award**.
- Conference: LASCAS 2023
- Paper: T. Moposita, **E. Garzón**, F. Crupi, L. Trojman, A. Vladimirescu, and M. Lanuzza, "Efficiency of Double-barrier Magnetic Tunnel Junction-based Digital eNVM Array for Neuro-Inspired Computing," (invited to be published in IEEE Transactions On Circuits and Systems II (TCAS-II), 2023), DOI: 10.1109/TCSII.2023.3240474.

02/2023 **Invited Article**.

- Conference: LASCAS 2023
- Paper: **E. Garzón**, L. Yavits, A. Teman, and M. Lanuzza, "STT-MRAM Technology For Energy-Efficient Cryogenic Memory Applications," in Proc. of IEEE Latin American Symposium on Circuits and Systems (LASCAS), Quito, Ecuador, Feb. 2023. DOI: 10.1109/LASCAS56464.2023.10108316.

01/2023 **Awarded an "Honorary Mention" in IEEE Micro Top Picks 2022**.

- Selected paper: R. Hanhan, **E. Garzón**, Z. Jahshan, M. Lanuzza, A. Teman, and L. Yavits, "EDAM: Edit Distance tolerant Approximate Matching content addressable memory," in Proc. of IEEE/ACM International Symposium on Computer Architecture (ISCA), New York, USA, Jun. 2022. DOI: 10.1109/MM.2023.3278069

02/2022 **Awarded IEEE Circuits and Systems Society Grant**.

- Awarding institution: IEEE Circuits and Systems Society
- Winner of the award (Here) 2021 IEEE Circuits and Systems Pre-Doctoral Grant. Mobility grant for PhD students researching Circuits and Systems.

12/2021 **Selected top ranked paper**.

- Selected paper: **E. Garzón**, R. De Rose, F. Crupi, L. Trojman, G. Finocchio, M. Carpentieri, M. Lanuzza, "Relaxing Non-Volatility for Energy-Efficient DMTJ Based Cryogenic STT- MRAM," Solid-State Electronics, p. 108090, 2021. DOI: 10.1016/j.sse.2021.108090
- An extended version of the paper has been invited to "Solid-State Electronics Journal": **E. Garzón**, R. De Rose, F. Crupi, L. Trojman, G. Finocchio, M. Carpentieri, M. Lanuzza, "Adjusting Thermal Stability in Double-Barrier MTJ for Energy Improvement in Cryogenic STT-MRAMs," Solid-State Electronics, p.108315, 2022. DOI: 10.1016/j.sse.2022.108315

10/2021 **Semifinalist Awarding – Student Research Competition (SRC)** .

- Awarding institution: 54th International Symposium on Microarchitecture
- Related work: R. Hanhan, L. Yavits, Z. Jahshan, E. Garzón, M. Lanuzza, A. Teman, and R. Ginosar, "EDCAM: Edit Distance Tolerant Content-Addressable Memory"

11/2019 **Invited Article**.

- "Evaluating the Energy Efficiency of STT-MRAMs Based on Perpendicular MTJs with Double Reference Layers", 13th IEEE International Conference on ASIC (ASICON 2019), Chongqing, China, Oct. 29-Nov.1, 2019. DOI: 10.1109/ASICON47005.2019.8983643

09/2019 **Awarded Ph.D. Sandwich Program**.

- Awarding institution: Israel Council for Higher Education
- Sandwich Program attracts high-achieving doctoral scholars from universities around the world to do a one-year (Oct. 2019 - Sept. 2020) research fellowship as part of their Ph.D. studies at Bar-Ilan University, Israel.

07/2019 **Selected top-ranked paper**.

- Selected paper: **E. Garzón**, R. De Rose, F. Crupi, L. Trojman, G. Finocchio, M. Carpentieri, M. Lanuzza, "Exploiting Double-Barrier MTJs for Energy-Efficient Nanoscaled STT-MRAMs," 2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lausanne, Switzerland, 15-18 July 2019. DOI: 10.1109/SMACD.2019.8795223
- An extended version of the paper has been invited to "Integration The VLSI Journal": **E. Garzón**, R. De Rose, F. Crupi, L.Trojman, G. Finocchio, M. Carpentieri, M. Lanuzza " Assessment of STT-MRAMs based on double-barrier MTJs for cache applications by means of a device-to-system level simulation framework", Integration The VLSI Journal, Vol. 71, pp. 56-69, March 2020. DOI: 10.1016/j.vlsi.2020.01.002

07/2019 **Awarded a M.Sc. Scholarship**.

- Awarding institution: Universidad San Francisco de Quito (USFQ)
- Awarded an excellence scholarship by the Master program of the Institute of Micro and Nanoelectronics, University San Francisco de Quito, Ecuador.

Networks & Memberships

01/06/2022–Present **IEEE Member (ID Number: 92927687). Student IEEE Member from 01/06/2015 – 31/05/2022**.

01/02/2019–Present **IEEE Circuits and Systems Society Member**.

16/06/2022–Present **Società Italiana Elettronica (SIE) – Socio Ordinario**.

30/07/2021–31/07/2022 **Association for Computing Machinery (ACM) Student Member**.

Peer Review Activities

Frontiers in Electronics.
IEEE NANO Technology Magazine.
Journal of Circuits, Systems, and Computers.
Cybernetics and Systems.
IEEE International Symposium on Circuits and Systems (ISCAS).
IEEE Access.
Sensors Journal.
IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I).
IEEE Transactions on Nanotechnology (TNANO).
IEEE Micro Magazine.
IEEE International Conference on Nanotechnology (NANO).
IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II).
IEEE Latin American Symposium on Circuits and Systems (LASCAS).
Elsevier Microelectronics Journal (MEJ).
Elsevier Journal of Magnetism and Magnetic Materials.
IEEE Ecuadorian Technical Chapters meeting (ETCM).

Conference Commitees

2024 **IEEE Latin American Symposium on Circuits and Systems (LASCAS)**, *Technical Program Committee Member*.

2024 **IBERCHIP Workshop**, *Technical Program Committee Member*.

2023 **IBERCHIP Workshop**, *Chair of IBERCHIP-LA*.

2023 **IEEE Latin American Symposium on Circuits and Systems (LASCAS)**, *Nanoelectronics Track Chair*.

2021–2023 **IEEE Ecuadorian Technical Chapters Meeting (ETCM) Conference**, *Technical Program Committee Member*.

2021 **IBERCHIP Workshop**, *Technical Program Committee Member*.

Journal Boards

01/11/2023–Present **Elsevier | Memories - Materials, Devices, Circuits and System**, *Executive Guest Editor of the Special Issue "Memory Technologies for Energy-Efficient Computing and Emerging Data-Intensive Applications"*.

09/12/2022–Present **Frontiers in Aerospace Engineering**, *Review Editor of the Intelligent Aerospace Systems*.

01/03/2022–Present **Frontiers in Electronics**, *Review Editor of the Integrated Systems and VLSI*.

Publications

Book Chapters

B1 [2022] **Esteban, Garzón**, Leonid Yavits, Marco Lanuzza, and Adam Teman. Emerging Memory Structures for VLSI Circuits. ***Wiley Encyclopedia of Electrical and Electronics Engineering***, pages 1–28. Wiley Online Library, 2022. DOI: 10.1002/047134608X.W8438.

Journal Articles (Impact factor (IF) and Quartile is related to the year of publication. If the year of publication information is not available online (WoS or SJR), the reported data (IF and Quartile) is referred to the previous year)

J1 [2023] Ariana Musello, **Esteban, Garzón**, Marco Lanuzza, Luis Miguel Prócel, and Ramiro Taco. XNOR-bitcount operation exploiting computing-in-memory with STT-MRAMs. ***IEEE Transactions on Circuits and Systems II: Express Briefs***, volume 70, pages 1259–1263. IEEE, 2023. DOI: 10.1109/TCSII.2023.3241163. **(Impact Factor: 4.4, Quartile: Q1)**.

J2 [2023] Tatiana Moposita, **Esteban, Garzón**, Felice Crupi, Lionel Trojman, Andrei Vladimirescu, and Marco Lanuzza. Efficiency of Double-Barrier Magnetic Tunnel Junction-Based Digital eNVM Array for Neuro-Inspired Computing. ***IEEE Transactions on Circuits and Systems II: Express Briefs***, volume 70, pages 1254–1258. IEEE, 2023. DOI: 10.1109/TCSII.2023.3240474. **(Impact Factor: 4.4, Quartile: Q1)**.

J3 [2023] Itay Merlin, **Esteban, Garzón**, Alex Fish, and Leonid Yavits. DIPER: Detection and Identification of Pathogens using Edit distance-tolerant Resistive CAM. ***IEEE Transactions on Computers***. IEEE, 2023. DOI: 10.1109/TC.2023.3315829. **(Impact Factor: 3.2, Quartile: Q1)**.

J4 [2023] Andrea Meo, **Esteban, Garzón**, Raffaele De Rose, Giovanni Finocchio, Marco Lanuzza, and Mario Carpentieri. Voltage-controlled magnetic anisotropy based physical unclonable function. ***Applied Physics Letters***, volume 123. AIP Publishing, 2023. DOI: 10.1063/5.0166164. **(Impact Factor: 4.0, Quartile: Q1)**.

J5 [2023] Hanan Marinberg, **Esteban, Garzón**, Tzachi Noy, Marco Lanuzza, and Adam Teman. Efficient Implementation of Many-Ported Memories by Using Standard-Cell Memory Approach. ***IEEE Access***, volume 11, pages 94885–94897, 2023. DOI: 10.1109/ACCESS.2023.3310940. **(Impact Factor: 4.4, Quartile: Q1)**.

J6 [2023] **Esteban, Garzón**, Leonid Yavits, Adam Teman, and Marco Lanuzza. Approximate content-addressable memories: a review. ***Chips***, volume 2, pages 70–82. MDPI, 2023. DOI: 10.3390/chips2020005.

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Personal Talks

T1 [2023] STT-MRAM Technology For Energy-Efficient Cryogenic Memory Applications. *IEEE Latin American Symposium on Circuits and Systems (LASCAS), Quito, Ecuador, 02 Mar.*, 2023.

T2 [2023] Spintronic Technology For Energy-Efficient hybrid CMOS/MTJ Memory Applications. *University of Calabria, Rende, Italy, 14-15 Jun.*, 2023.

T3 [2023] MRAM Based Associative Memory For In-Memory Computing. *IEEE Trends in Magnetism Conference (TMAG2023), Rome, Italy, 04-08 Sep.*, 2023.

T4 [2023] Hybrid CMOS/MTJ Circuit Design. *Politecnico di Bari, Bari, Italy, 15-16 May*, 2023.

T5 [2023] A Low-Complexity Sensing Scheme for Approximate Matching Content-Addressable Memory. *IEEE International Symposium on Integrated Circuits and Systems (ISICAS), Jeju, South Korea, 24-25 Oct.*, 2023.

T6 [2022] Voltage and Technology Scaling of DMTJ-based STT-MRAMs for Energy-Efficient Embedded Memories. *IEEE Latin American Symposium on Circuits and Systems (LASCAS), Puerto Varas, Chile, 08 Mar.*, 2022.

T7 [2022] Spin-Transfer Torque Magnetic RAM For Embedded Memory Applications. *IEEE CAS Ecuador Chapter, Quito, Ecuador, 10 Jun.*, 2022.

T8 [2022] Content-Addressable Memory for Approximate Matching Applications in Genome Analysis. *53rd Annual Meeting of the Associazione Società Italiana di Elettronica (SIE), Pizzo (VV), Italy, 09 Sep.*, 2022.

T9 [2022] A RISC-V-based Research Platform for Rapid Design Cycle. *IEEE International Symposium on Circuits and Systems (ISCAS), Austin Texas, USA, 28 May*, 2022.

T10 [2021] STT-MRAMs for Cryogenic Non-Volatile Cache Applications. *Microelectronic Week: IEEE EDS-CAS Ecuador Joint Chapter, Quito, Ecuador, 10 Oct.*, 2021.

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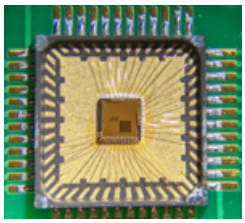
T14 [2019] Device-to-System Level Simulation Framework for STT-DMTJ Based Cache Memory. *IEEE International Conference on Electronics Circuits and Systems (ICECS), Genova, Italy, 28 Nov.*, 2019.

Research Tapeouts (Fabricated Test Chips & Prototypes)

2021 – 2022 **HD-CAM Memory Macro in 65** nm.

- Full design at EnICS Labs, Ramat Gan, Israel
- Chip Name: LEO-II
- Memory Macro Name: HD-CAM
- Technology: TSMC 65 nm
- Role: Support in the design and experimental measurements of an Hamming Distance tolerant content-addressable memory (CAM)
- Description: A novel Hamming distance tolerant CAM (HD-CAM) for energy-efficient in-memory approximate matching applications

2022 **Fully-Integrated Temperature Sensor**.



- Design at Department of Computer Engineering, Modeling, Electronics and Systems, University of Calabria, Rende, Italy
- Technology: TSMC 180 nm
- Role: Support in layout design and experimental measurements of the test chip. Main design done by the Ph.D. candidate Benjamin Zambrano
- Description: Fully-integrated, ultralow-power, ring oscillator based CMOS temperature sensor for energy-constrained, low-cost applications (e.g., Internet-of-Things).

2020 **LEO-I Research Platform in 65 nm**.

- Joint design with EnICS Laboratories, Bar-Ilan University, Israel
- Chip Name: LEO-I
- Technology: TSMC 65 nm
- Role: backend designer (entire SoC integration)
- Description: A novel platform for bringing a project from the concept to the tapeout stage in a short amount of time. An open-source and extendable RISC-V architecture is exploited to build a small area footprint core. This leads the research platform to be flexible in terms of design integration, while also allowing fast design cycles of research chips