# Spintronic Technology For Energy-Efficient In Memory Computing

## Part 1 – Introduction and Motivation


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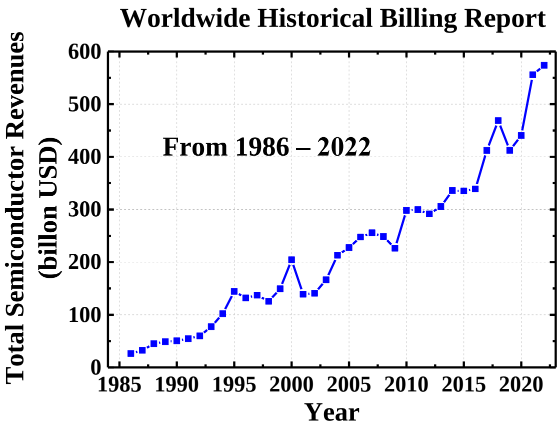
# Lecture Outline

1. Semiconductor Industry
2. From Transistors to Integrated Circuits (IC)
3. Moore's Law and Scaling
4. IC Design Challenges and Limitations
5. Miniaturization, Diversification, and Beyond CMOS

# Semiconductor Revenues Worldwide




*Source: Figure done from data available from the "World Semiconductor Trade Statistics" (WSTS) by Esteban Garzón*

- **An ever-growing industry**
  - Emerging technologies have to be compatible with current semiconductor industry.
- In about 35 years ($\sim$1987 to $\sim$2021), Asia Pacific region went from a few billon USD to more than 300 billon USD $\rightarrow$ this is about 2 $\times$ more than the rest of the regions combined.

- The integrated circuit design is not an easy task...
- There is always a **trade-off** between:

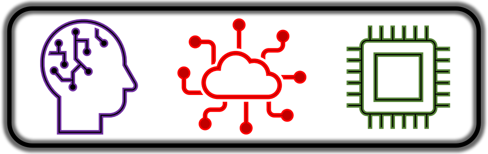
**Performance:** Referred to the speed, frequency, throughput.

**Cost:** Strongly related to the area (the smaller the chip, the lower its cost will be). Silicon is the most expensive real state in the world.

**Reliability:** From the chips we make, how many will work?... what about aging?

**Power:** Two examples: (1) Less power = better battery life. (2) More power = more heat = more money to dissipate such heat.

- The advent of new technologies including, artificial intelligence (AI), internet of things (IoT), advanced microprocessors, and quantum computing, have skyrocketed the design complexity.
- These technologies are **creating a need for semiconductors that are smaller, lighter, and more powerful.**



# Transistor Evolution

- **1947**: First transistor invented by William Shockley, Walter Brattain, and John Bardeen at Bell Labs. It was a point-contact transistor based on germanium material Go to 1947
- **1948**: The first Bipolar transistor introduced by Shockley Go to 1948
- **1954-1955**: Fabrication of the first silicon transistor (Bell Labs), and commercialization of silicon transistors (Texas Instruments) Go to 1954-1955
- **1956**: First bipolar digital logic gate by Harris Semiconductor
- **1958**: First demonstration of an IC by Jack Kilby at Texas Instruments Go to 1958
- **1960**: First commercial IC logic gates by Fairchild Semiconductors Go to 1960
- **1964**: First commercial metal-oxide-semiconductor (MOS) IC Go to 1964

# Transistor Evolution (Cont.)

- 1974: General purpose microcontroller family announced. These power a wide spectrum of electronic devices.
- 1980's: CMOS process exploiting MOSFET technology because of power benefits
- 1998: Start of the 180 $\mathrm{nm}$ commercial IC process
- 2003-2004: Start of the 90 $\mathrm{nm}$ commercial IC process
- 2014: Start of the 16 $\mathrm{nm}$ commercial IC process
- 2020: Start of the 5 $\mathrm{nm}$ commercial IC process
- **Today: Industry working on 3nm and 2nm CMOS, new materials and structures for improved performance and power efficiency.**

# Milestones in Computer Technology

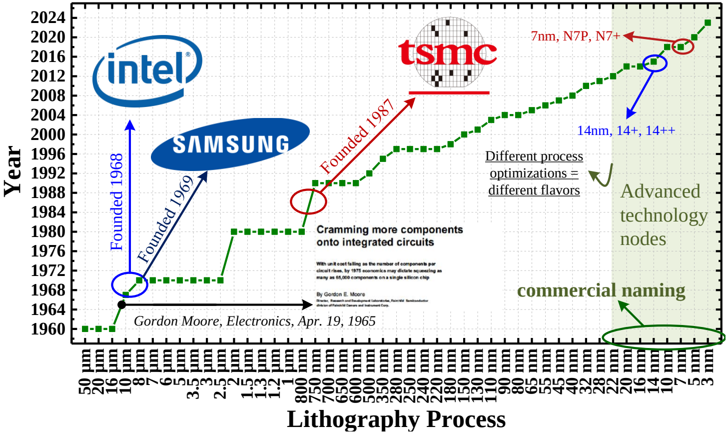
**1946**: ENIAC – First Electronic Computer Go to ENIAC

**1947**: First Transistor Go to first transistor

**1958**: First Integrated Circuit Go to first IC

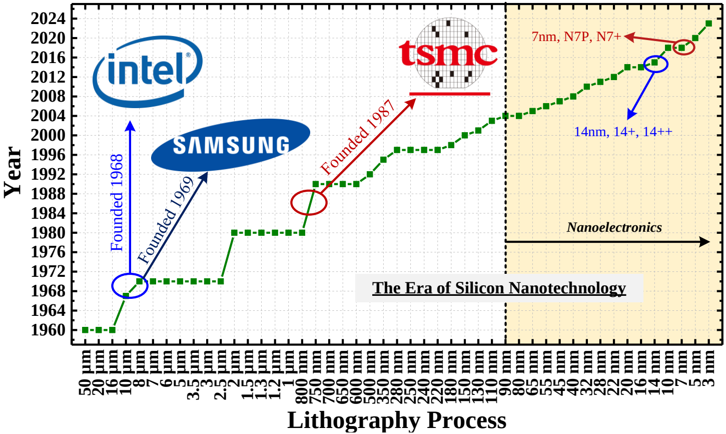
**1959**: First MOSFET Go to first MOSFET

**1971**: First Microprocessor Go to first Microprocessor



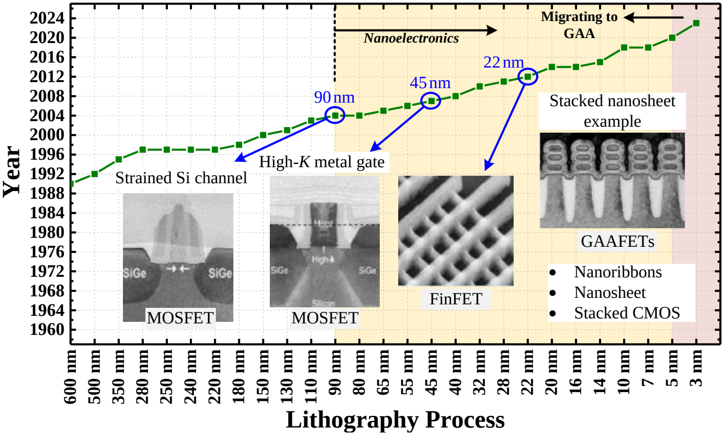

*Source: Figure done from data available from "WikiChip" by Esteban Garzón*

- Most data is referred to the Microprocessing Unit (MPU)
- For the memory systems, the years may differ
- 1965 Moore's paper became the basis for his *Moore's Law*
- For advanced technology nodes (around 22 nm and beyond), the 'label' in nm does not represent any geometry of the transistor. It is a commercial naming.




*Source: Figure done from data available from "WikiChip" by Esteban Garzón*

- Silicon nanotechnology/nanoelectronics started with the introduction of the 90 nm node.
- The big three (Intel, Samsung, and TSMC) keep up with the technology scaling down to extreme processes.

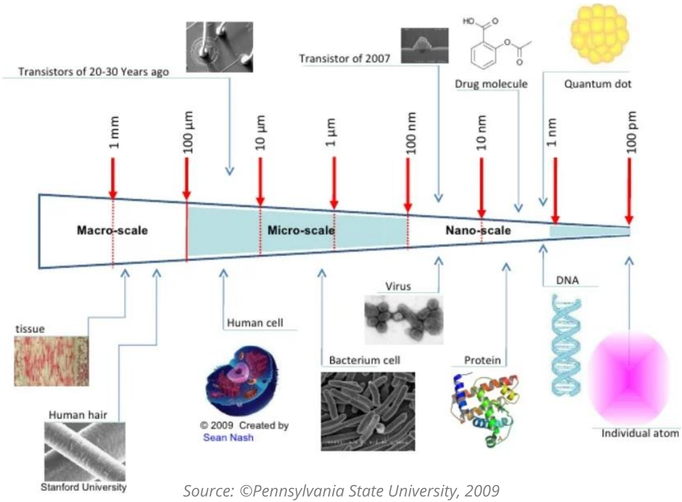



*Source: Figure done from data available from "WikiChip" by Esteban Garzón. Other lithography process photos from application note Here*

- **Billons of transistors integrated in a single chip!**
- Transistors innovation! From planar MOSFETs to FinFETs. Now migrating to Gate-All-Around (GAA), e.g., GAAFETs.
- GAA is expected to be introduced in the 5 nm/3 nm process nodes.

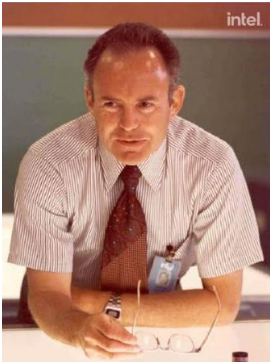
# Nanometer scale

## Man-made structures versus living organisms




*Source: ©Pennsylvania State University, 2009*

# Moore’s Law





*Source: ©Intel, 2023*

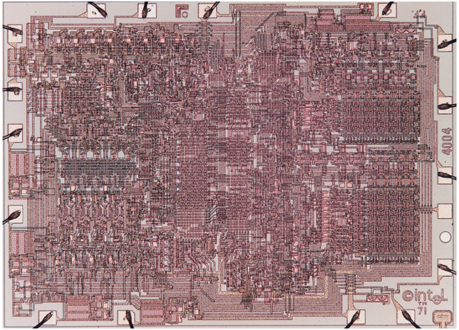
- “Moore, who set the course for the future of the semiconductor industry...” (Intel Newsroom, March 24, 2023)

# Moore's Law

- In 1965, Gordon Moore observed that the number of **transistors** on a single chip would **double every 18 to 24 months.**
- Moore forecasted that the technology of semiconductors would double in effectiveness every 18 months, resulting in exponential growth over time.
- This prediction proved to be incredibly accurate, as the milestone of one million transistors on a chip was achieved in the 1980s.
  - Intel 4004, 1971 – 2300 transistors, 0.1 $\mathrm{MHz}$ clock
  - Intel P4, 2001 – 42 millon, 1.5 $\mathrm{GHz}$ clock

# Intel Microprocessors

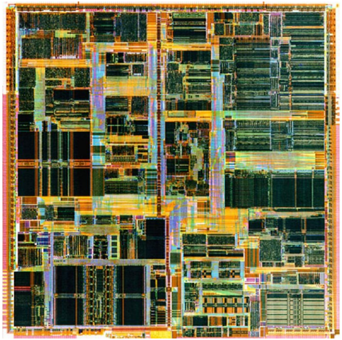
## Intel 4004 Microprocessor (1972)




*Source: ©WikiChip*

- Num. of transistors: 2 300 million
- Process node: 10 $\mu m$
- Area: 0.3 $mm \times$ 0.4 $mm$
- Clock: 0.108 $MHz$

## Intel Pentium IV Microprocessor (2000)

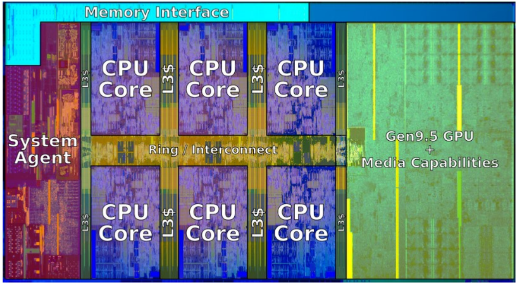


*Source: ©WikiChip*

- Num. of transistors: 42 000 000
- Process node: 180 $nm$
- Area: 20 $mm^2$
- Clock: 1.5 $GHz$

# Intel Microprocessors

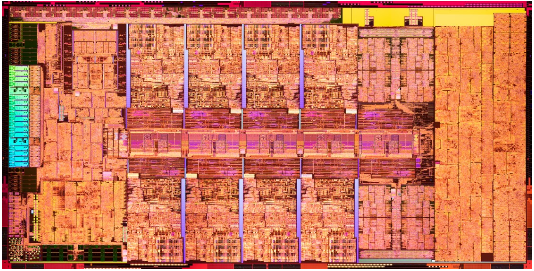
## Intel Cofee Lake Hexa-Core (2017)




*Source: ©WikiChip*

- Num. of transistors: 1 900 million
- Process node: 14 nm (14 nm ++)
- Area: 149.6 $\mathrm{mm}^2$
- Clock (Depends on the class): 2.7 GHz

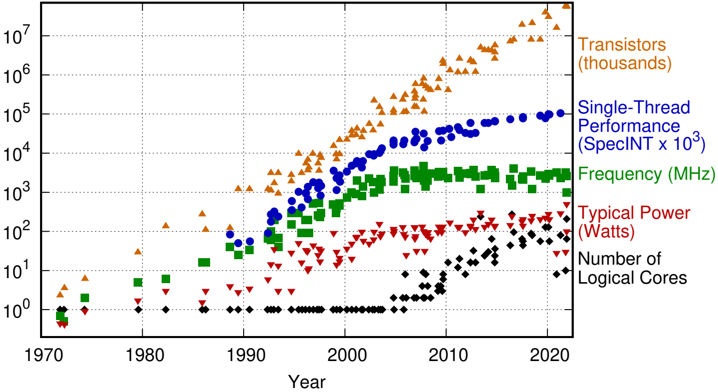
## Intel Alder Lake (2021)



*Source: ©WikiChip*

- Num. of transistors: 10 200 million
- Process node: 7 nm
- Area: 10.5 mm $\times$ 20.5 mm
- Clock (Depends on the class): 3.8 GHz

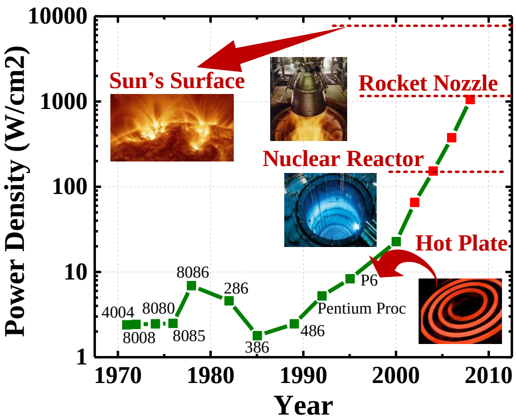
# Microprocessor Trend Data – 50 Years of Microprocessor Trend Data




Source: Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten. New plot and data collected for 2010-2021 by K. Rupp

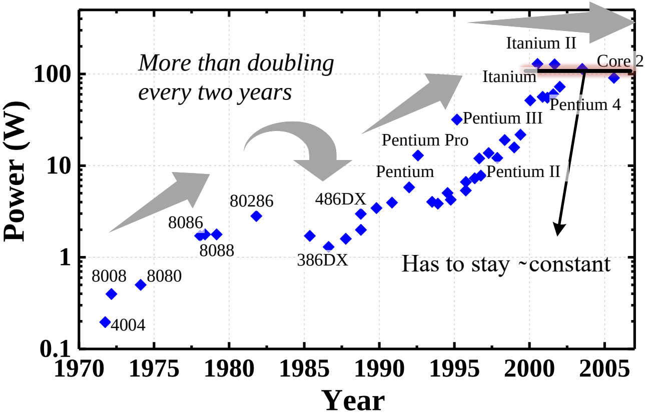
- Number of transistors per die: Transistors on lead microprocessors double every 2 years
- Frequency: $2 \times$ every two years at the beginning. After 2000, it remains around $3.8\,\mathrm{GHz}$.
- Power density: Too high to keep junctions at low temperatures

- Increasing power consumption of microprocessors.
- This is due to the continued trend towards miniaturization and increased functionality of microprocessors.
- As the power density of microprocessors increases, it becomes more difficult to dissipate the heat they generate.




*Source: Adapted from the original by R. Chau, Intel Corporation*

- Since the introduction of microprocessors, the power has been *more* doubling every two years up to around 2005.
- Power has to stay ∼constant




*Source: Adapted from original. Intel, John Urbanic (Pittsburgh Supercomputing Center).*

# Why Scaling?

- The technology shrinks by approximately 0.7 times per generation.
- With each new generation, it is possible to integrate twice as many transistors on a chip, while the cost of the chip remains relatively stable.
- The cost decreases.
- However, how to design chips with more and more functions? Chip designs become increasingly complex...
- Technology Scaling Models
  - Voltage scaling – 1970s-1990s
  - Dennard scaling – 1990s-2005
  - General scaling

# Main Design Challenges

**Microscopic issues:**

- Physical limits
- ultra high speeds
- power dissipation
- chip interconnections
- noise, crosstalk
- reliability, manufacturability, aging
- clock distribution

**Macroscopic issues:**

- time-to-market
- design complexity (millions of gates)
- high levels of abstractions
- reuse and IP, portability
- systems-on-chip (SoC)
- tool interoperability

# The Future of Technology Evolution

**The semiconductor industry faces challenges extending integrated circuit technology, which fall into five categories:**

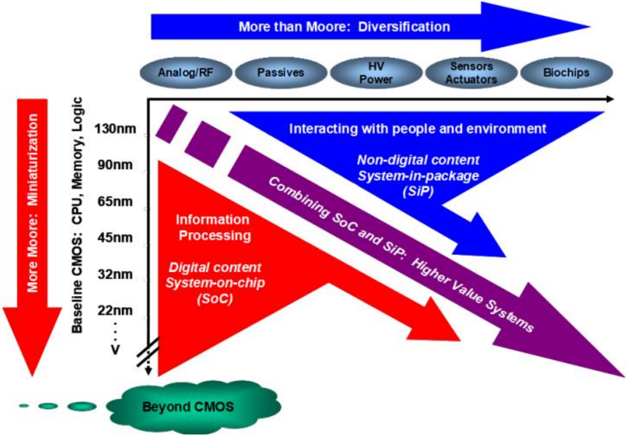
1. Extend **CMOS scaling** with alternative channel materials.
2. Invent a **new information processing platform technology** that substantially surpasses CMOS capabilities (new devices, interconnections,architectures, etc.).
3. Extend ultimately **scaled CMOS** into **new domains** of functionalities and applications.
4. **Bridge the gap** between **novel devices** and **unconventional architectures** and computing paradigms.
5. Integrate a new high-speed, high-density, and low-power memory technology onto the CMOS platform. **Pushing CMOS beyond its ultimate density and functionality.**

**There is a need for more efficient design methods, and more...**

- **More Moore**: Miniaturization – mainly CMOS: CPU, memory, logic
- **More than Moore**: Diversification – systems integration, biochips, etc.
- **Beyond CMOS**...

- The IEEE International Roadmap for Devices and Systems (IRDS) builds a comprehensive, end-to-end view of the computing ecosystem (from devices to systems)
- It is an annual report (annual conference) produced by a team of semiconductor industry and academy experts
- It was first called ITRS (International Technology Roadmap for Semiconductors)
- It serves as reference to the academics, consortia, industry researchers to stimulate innovation in various areas of technology.

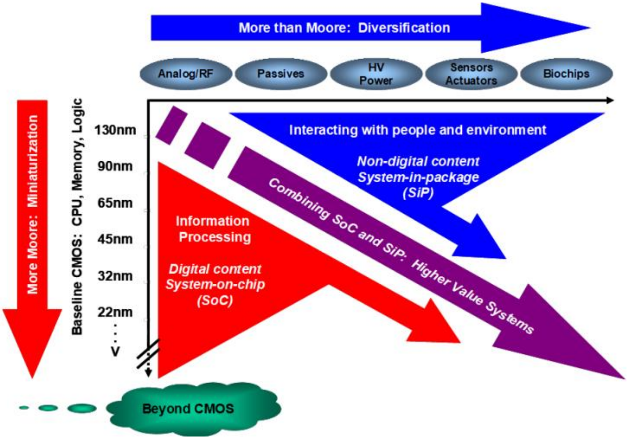
# More Moore, More than Moore, and Beyond CMOS




*Source: ©IEEE IRDS*

- **More Moore: Miniaturization**
  - System scaling enabled by Moore's Law.
  - This is mainly referred to the nano-fabrication of logic technologies of the digital realm.
  - The More Moore roadmap aims to **enable the scaling of MOSFETs to maintain the historical trend** of improved device performance at lower power and cost while producing high volumes, which is crucial for the continued scaling of digital logic devices.

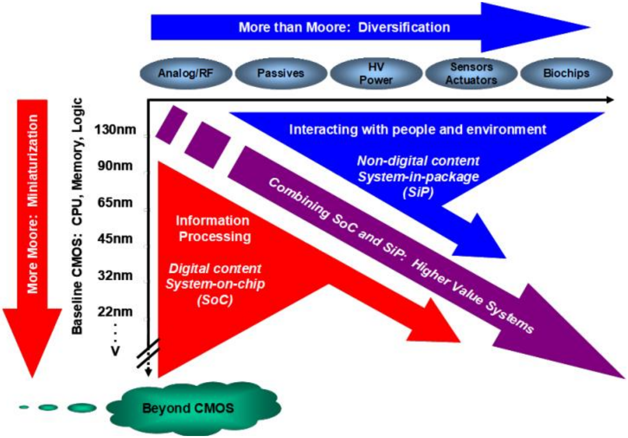
# More Moore, More than Moore, and Beyond CMOS




Source: ©IEEE IRDS

- **More Moore (Challenges)**
  - A significant amount of semiconductor device production is dedicated to digital logic.
  - Speed, power, density, cost, capacity, and time-to-market are crucial considerations for this technology platform. $\Rightarrow$ **Difficult challenges to continue scaling.**
  - Some Near-Term and Long-term challenges:
    - Power scaling
    - Parasitics scaling
    - Cost reduction
    - Integration enablement for SRAM-cache applications, ...

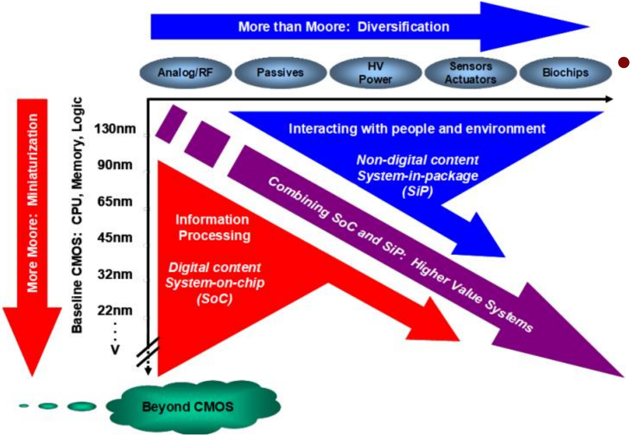
# More Moore, More than Moore, and Beyond CMOS




Source: ©IEEE IRDS

- **More than Moore: Diversification**
  - It adds value through non-scaling functionalities
  - Non-digital functions (e.g., RF, sensors, etc.) move from system board to chip (System-on-Chip and System-in-Package) $\Rightarrow$ might impact performance scaling
  - Goal is to use silicon technology for new, non-digital functions
  - **Main goal is to expand the possibilities of silicon-based technology beyond the traditional digital functionalities, to create more value and enhance performance of compact systems and system-of-systems.**

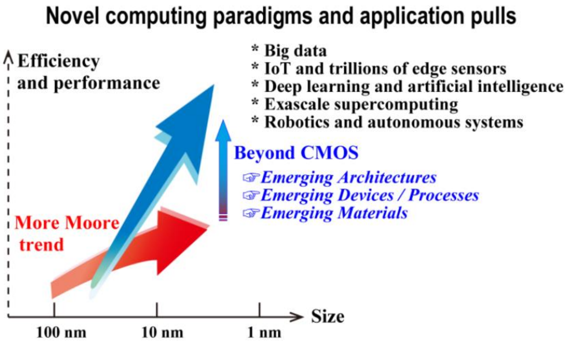
# More Moore, More than Moore, and Beyond CMOS




Source: ©IEEE IRDS

- **More than Moore: Challenges**
  - It faces a challenge in creating technology platforms (Hardware and Software) for building blocks of various applications.
  - Target applications include:
    - smart sensors
    - smart energy
    - energy harvesting, and
    - flexible/wearable electronics.

# More Moore & Beyond CMOS

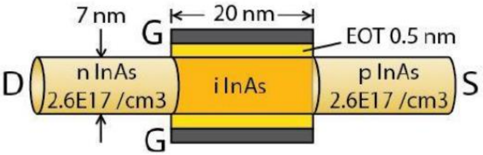



*Source: ©IEEE IRDS (Courtesy of Japan beyond-CMOS Group)*

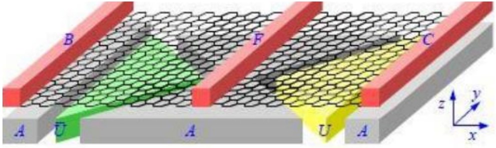
- Motivation: extend the functionality of CMOS platform and stimulate invention of new information processing paradigms.
- This is achieved through two domains:
  - **"More Moore"** by integrating new technologies, and
  - **"Beyond CMOS"** by exploring new information processing paradigms.
- New and emerging computing applications and requirements need better performance and efficiency $\rightarrow$ **challenging for "More Moore" technologies to achieve**
- **Beyond-CMOS technologies could potentially offer suitable devices, processes, and architectures to meet the demands of the new computing era.**

# Beyond CMOS

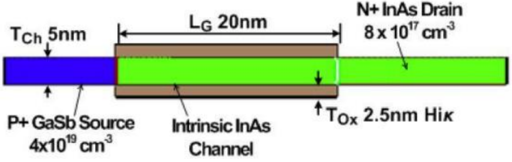
## Example Electronic Devices



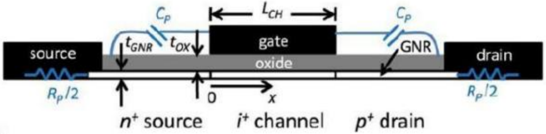

Homojunction Tunneling FET




Graphene pn Junction




Heterojunction Tunneling FET

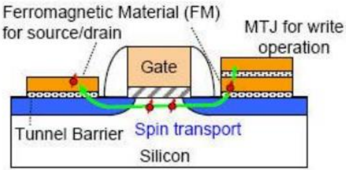



Graphene Nanoribbon Tunneling FET

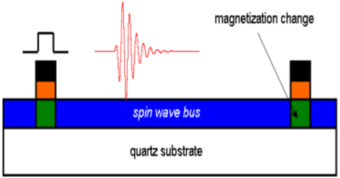
*Source: ©Nikonov, NCN Summer School, 2014. Intel Corporation*

# Beyond CMOS

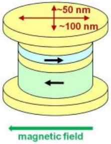
## Example Spintronic Devices



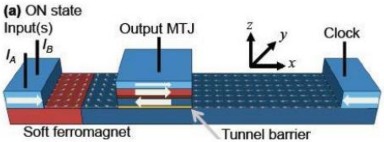

SpinFET



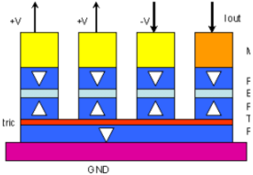

Spin Wave Device



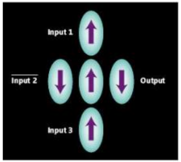

Spin Torque Oscillator




Domain Wall Logic



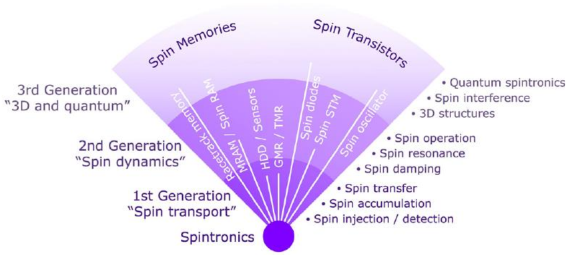

Spintronic Majority



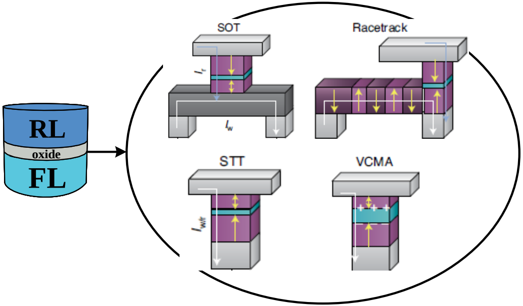

Nano Magnet Logic

*Source: ©Nikonov, NCN Summer School, 2014. Intel Corporation*

- Spintronics to meet the demands of the new computing era.
- In particular, we can exploit spintronics non-volatile memory technology for:
  - Energy-efficient memories, and
  - Beyond-CMOS computing




*Source: Hirohata, A., et al. (2014), Future perspectives for spintronic devices. J. of Physics D: Applied Physics*



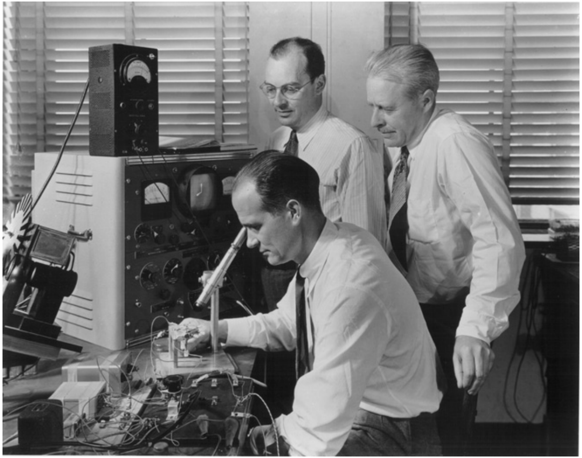

*Source: Dieny, B., et al. (2020), Opportunities and challenges for spintronics in the microelectronics industry. Nature Elect.*

# Key Takeaways

- The advent of new technologies have skyrocketed the design complexity.
- Moore’s Law: the number of transistors (on a single chip) double every two years
- Billons of transistors integrated in a single chip!
- Beyond-CMOS technologies could potentially offer suitable devices, processes, and architectures to meet the demands of the new computing era
- Spintronics technology is considered as a promising alternative for Beyond CMOS

# 1947 – Bardeen, Brattain, Shockley at Bell Labs

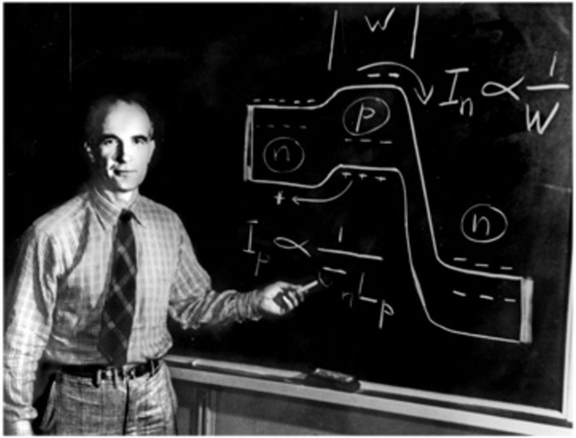
Transistor Evolution



*Source: ©WIRED*

# 1948 – William Shockley explaining the junction transistor theory

Transistor Evolution




*Source: ©2006-2007 Alcatel-Lucent. All rights reserved.*

# 1954-1955 – Bell Labs (left) and Texas Instruments (right)

Transistor Evolution

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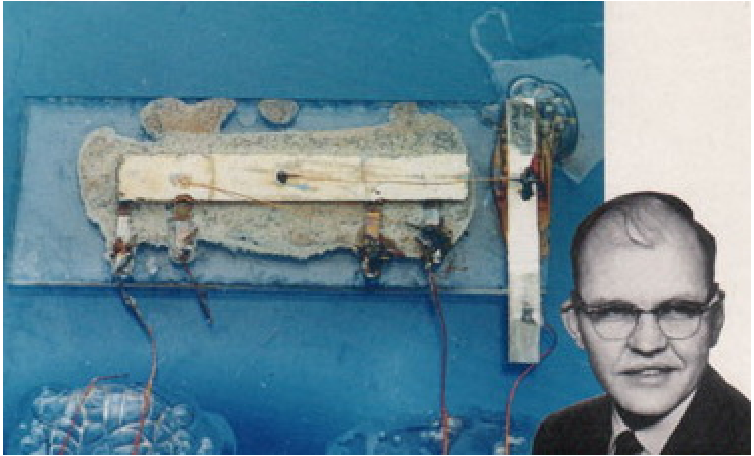
*Source: ©Texas Instruments.*

# 1958 – First monolithic IC by Jack Kilby

Transistor Evolution

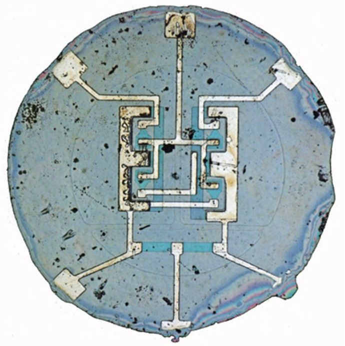


*Source: ©Texas Instruments.*

# 1960 – IC by Fairchild Semiconductor (Left: Gordon Moore at the background. Right: Type-F Flip-Flop)

Transistor Evolution

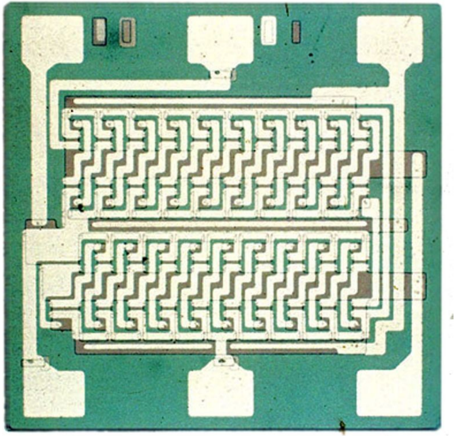
*Source: ©Fairchild Semiconductor.*



*Source: ©Fairchild Semiconductor.*

# 1964 – 20-bit Shift Register by General Microelectronics

Transistor Evolution

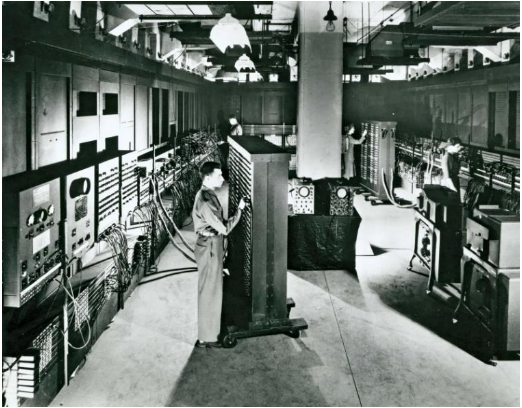


*Source: ©Texas Instruments.*

# ENIAC – First Electronic Computer (1945)

Back to Milestones

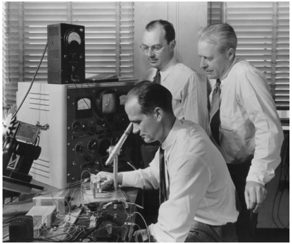
- **ENIAC** stands for **E**lectronic **N**umerical **I**ntegrator **A**nd **C**omputer)
- The first general purpose electronic computer capable of being reprogrammed to solve a wide range of numerical problems.
- 18 000 vacuum tubes to perform calculations
- Use cases include:
  - Military applications: artillery firing tables (Ballistic Research Laboratory, USA)
  - Research: thermonuclear weapon

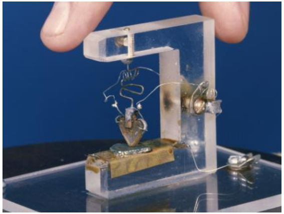


*Source: Courtesy of the Moore School of Electrical Engineering, University of Pennsylvania.*

Back to Milestones

- **The single invention that changed our way of life**
- The transistor (**TRAN**sfer re**SISTOR**) is a ”simple” device, but is the foundation of our modern technology.
- In 1947, the first working transistor by John Bardeen, Walter Brattain and William Shockley at the Bell Laboratories.
- It was a point-contact germanium transistor.
- John Bardeen, Walter Brattain and William Shockley won the 1956 Nobel Prize in Physics



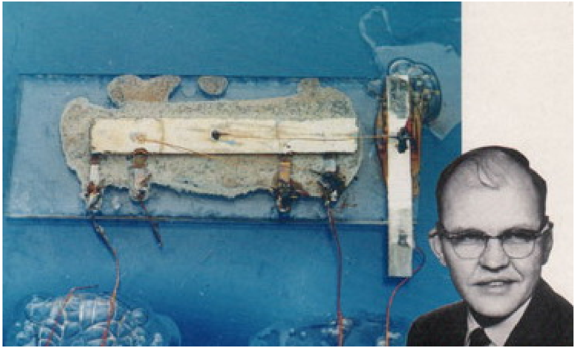


*Source: WIRED, European Digital Museum for Science & Technology*

# First Integrated Circuit (1958)

◂ Back to Milestones

- In 1958, Jack Kilby created a microcircuit (chip or integrated circuit, IC) using germanium-based p-n-p transistors
- The circuit contained both active and passive elements made from semiconductor material.
- After this achievement, the amplifier was demonstrated by Jack Kilby. About 7-months later, Texas Instruments introduced its first commercial device.



*Source: ©Texas Instruments.*

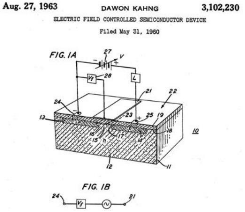
# First MOSFET (1959)

◂ Back to Milestones

- **International cast of engineers and scientists make the MOSFET device possible.**
- Lilienfeld (Canada) in 1925 and by Heil (England) in 1934m and Shockley's early experiments contribute to the development of the MOSFET.
- Dawon Kahng (Korean electrical engineer) and Martin Atalla demonstrated the field-effect transistor (FET) at Bell Labs.
- This FET was made up of a sandwich of metal (M – gate), oxide (O – insulation), and silicon (S – semiconductor) layers. It is commonly referred to as MOSFET or MOS.
- Today's IC technology is referred to the CMOS process/technology (uses both n-type and p-type transistors)

Martin M. Atalla (1924 – 2009)

Dawon Kahng (1931 – 1992)

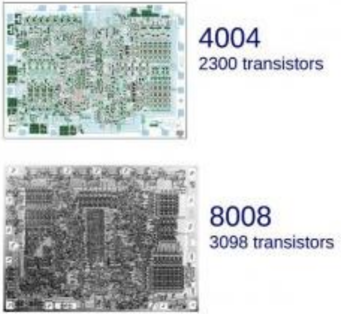



*Source: ©Computer History Museum*

# First Microprocessor (1971)

Back to Milestones

- This microprocessor was led by Intel design team of logic architects and silicon engineers: ederico Faggin, Marcian (Ted) Hoff, Stanley Mazor, and Masatoshi Shima.
- Faggin and Shima were able to fit 2,300 transistors onto the 4004 CPU device.
- This was one of the densest chips fabricated at that time.




*Source: ©Computer History Museum*