Lösung 2 Logikgatter in VHDL und FPGAs

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1 Einfache Gatter

VHDL_main:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity main is
    Port ( sw0 : in STD_LOGIC;
           sw1 : in STD_LOGIC;
           sw2 : in STD_LOGIC;
           sw3 : in STD_LOGIC;
           sw4 : in STD_LOGIC;
           sw5 : in STD_LOGIC;
           sw6 : in STD_LOGIC;
           sw7 : in STD_LOGIC;
           sw8 : in STD_LOGIC;
           sw9 : in STD_LOGIC;
           sw10 : in STD_LOGIC;
           sw11 : in STD_LOGIC;
           sw12 : in STD_LOGIC;
           sw13 : in STD_LOGIC;
           sw14 : in STD_LOGIC;
           ld0 : out STD_LOGIC;
           ld2 : out STD_LOGIC;
           ld4 : out STD_LOGIC;
           ld6 : out STD_LOGIC;
           ld8 : out STD_LOGIC;
           ld10 : out STD_LOGIC;
           ld12 : out STD_LOGIC;
           ld14 : out STD_LOGIC);
end main;

architecture Behavioral of main is
begin

ld0 <= sw0 and sw1;
ld2 <= sw2 or sw3;
ld4 <= sw4 nand sw5;
ld6 <= sw6 nor sw7;
```

```
ld8 <= sw8 xor sw9;
ld10 <= sw10 xnor sw11;
ld12 <= not sw12;

end Behavioral;
```

Constraints:

```
set_property -dict { PACKAGE_PIN V17   IOSTANDARD LVCMOS33 } [get_ports { sw0}];
set_property -dict { PACKAGE_PIN V16   IOSTANDARD LVCMOS33 } [get_ports { sw1}];
set_property -dict { PACKAGE_PIN w16   IOSTANDARD LVCMOS33 } [get_ports { sw2}];
set_property -dict { PACKAGE_PIN w17   IOSTANDARD LVCMOS33 } [get_ports { sw3}];
set_property -dict { PACKAGE_PIN w15   IOSTANDARD LVCMOS33 } [get_ports { sw4}];
set_property -dict { PACKAGE_PIN v15   IOSTANDARD LVCMOS33 } [get_ports { sw5}];
set_property -dict { PACKAGE_PIN w14   IOSTANDARD LVCMOS33 } [get_ports { sw6}];
set_property -dict { PACKAGE_PIN w13   IOSTANDARD LVCMOS33 } [get_ports { sw7}];
set_property -dict { PACKAGE_PIN v2   IOSTANDARD LVCMOS33 } [get_ports { sw8}];
set_property -dict { PACKAGE_PIN t3   IOSTANDARD LVCMOS33 } [get_ports { sw9}];
set_property -dict { PACKAGE_PIN t2   IOSTANDARD LVCMOS33 } [get_ports { sw10}];
set_property -dict { PACKAGE_PIN r3   IOSTANDARD LVCMOS33 } [get_ports { sw11}];
set_property -dict { PACKAGE_PIN w2   IOSTANDARD LVCMOS33 } [get_ports { sw12}];

set_property -dict { PACKAGE_PIN U16   IOSTANDARD LVCMOS33 } [get_ports { ld0}];
set_property -dict { PACKAGE_PIN u19   IOSTANDARD LVCMOS33 } [get_ports { ld2}];
set_property -dict { PACKAGE_PIN w18   IOSTANDARD LVCMOS33 } [get_ports { ld4}];
set_property -dict { PACKAGE_PIN u14   IOSTANDARD LVCMOS33 } [get_ports { ld6}];
set_property -dict { PACKAGE_PIN v13   IOSTANDARD LVCMOS33 } [get_ports { ld8}];
set_property -dict { PACKAGE_PIN w3   IOSTANDARD LVCMOS33 } [get_ports { ld10}];
set_property -dict { PACKAGE_PIN p3   IOSTANDARD LVCMOS33 } [get_ports { ld12}];
```

4.:
Jedes Logikgatter wird in eine LUT übersetzt. Das FPGA hat intern keine Logikgatter fest verbaut.

2 Look Up Table

1.: Wahrheitstabellen der Logikgatter.
2.: Einer der beiden Eingänge muss mit "not" invertiert werden. Ein nichtsymmetrisches LUT mit zwei Eingängen kann immer in ein Nicht-Gatter übersetzt werden.
3.: Es schaltet zwei CLBs in Reihe.