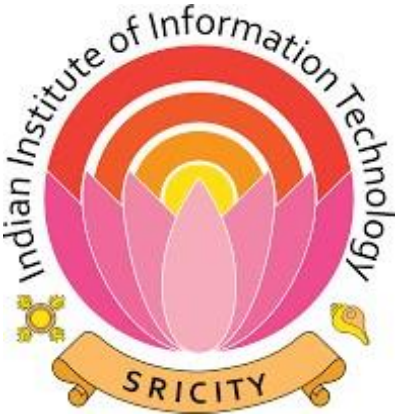


Electronics and Communication Engineering

Academic Year 2020 - 2024

AVLSI

Project Report

Group-20

Members:

- Geeta Sai Eswar Adapa – S20200020241
- Sayee Sreenivas G B – S20200020259

Objective :

To Design the Schematic and Layout for **BCD to EXCESS 3**

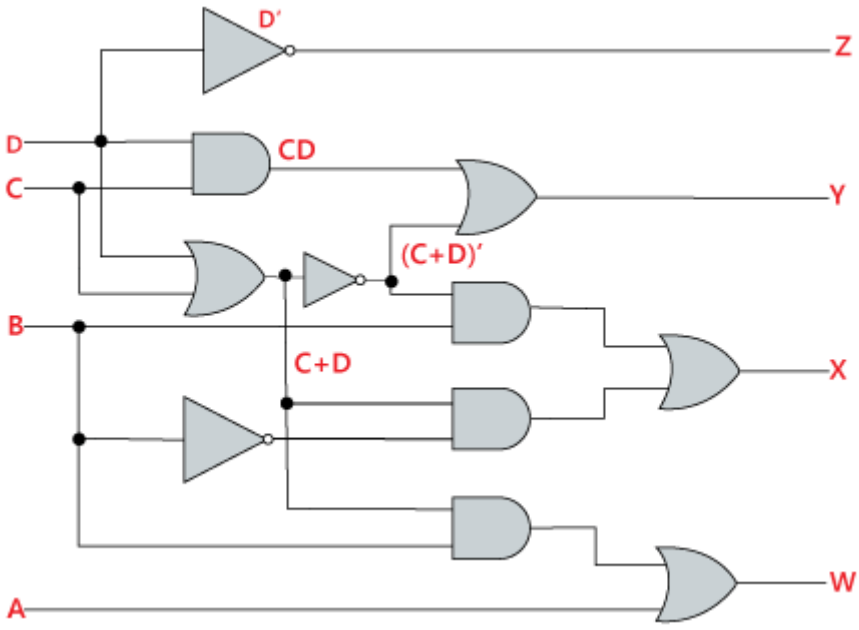
Software Used :

Electric and LT Spice.

Theory :

The word BCD describes how to express the 10 decimal digits in binary forms, using four bits for each digit. A non-weighted coding called Excess-3 is used to represent decimal integers. Another significant binary code, it solves the problems with the 8421 BCD code when adding two decimal digits whose sum is greater than nine. This makes it particularly vital for arithmetic operations. Excess-3 just adds 3 to each number to change the appearance of the codes. Excess-3 code to BCD system is created by subtracting 0011 from each Excess-3 value, whereas the BCD to Excess-3 system is created by adding 0011 to each BCD value.

Circuit Diagram :



Explanation :

A BCD digit can be converted to its corresponding Excess-3 code by simply adding 3 to it . Here A,B,C,D represents the binary numbers , where D is the LSB and A is the MSB . W,X,Y,Z represents the gray code of the binary numbers where Z is the LSB and W is the LSB .

$$w = A + BC + BD$$
$$x = B'C + B'D + BC'D'$$
$$y = CD + C'D'$$
$$z = D'$$

BASIC GATES TO IMPLEMENT ABOVE SCHEMATIC :

- **Components required for building of the circuit:**
- **AND** gate(2 input)
- **OR** gate(2 input)
- **NOT** gate
- **W/l Ratio = 2**
- **Area =** 422400 sq.µm

Steps followed are:

1. **Make the schematic first**: A schematic is a diagram that demonstrates the connections between the parts of a circuit. Create a quick sketch of the circuit to start. Label every component and wire carefully. All gates' schematics are being built using electrical software.
2. **Design the layout**: Once you have a schematic, you can design the physical layout of the circuit. Determine the size and shape of the circuit board.
3. **Testing circuit:** Once the circuit is assembled, test it to make sure it works as expected.
    - Design rule check (DRC)

- Electrical rule check (ERC)
- Network Consistency Checking (NCC)

4. **Ltspice:**Checking the working flow of the circuit using LTspice.by placing spice code in schematic we can check outputs.
5. **Make adjustments**: If the circuit isn't working correctly, make adjustments as needed.Check for any wiring mistakes, component failures. Make adjustments to the layout or component selection as shown in DRC check.
6. **Finalize the design**: After checking DRC, NCC and ERC of all circuit components we get the outputs in LTspice.

Parameters taken under Consideration :

1.We have taken 180nm technology node and Minimum spacing of (3 µm) is maintained and the layout area is as optimized as possible.

2. In the layout spacing between actives & polysilicon 3 µm is given.
3. Zero DRC and ERC errors is there and PMOS W/L is 2.5 times W/L of NMOS.

Simulate the file :

1.Go to Preference, then categories, then general, then set the memory as 512 megabytes.

2.Go to the tools, then NCC, and enable the check transistor size.

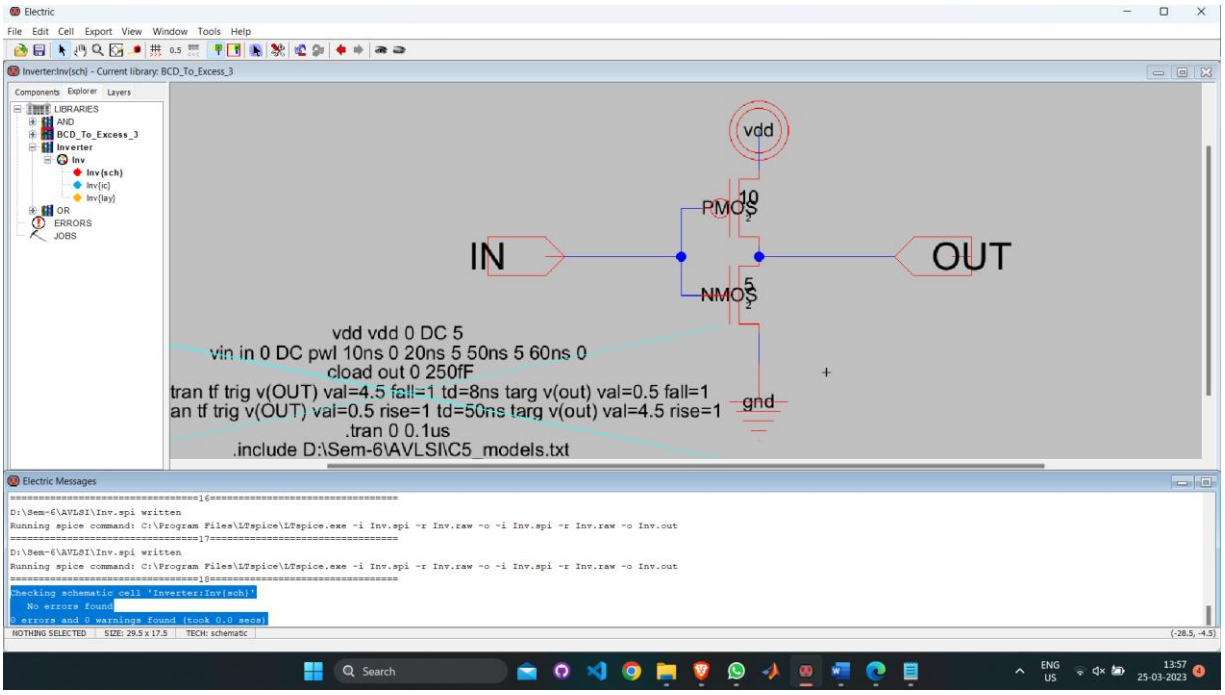
3.Go to the tools, then SPICE/CDL, then spice engine, then choose **spice 3** and **level 3.** In the run program, set the path of the LT SPICE. In my case: "C:\Program Files\LTspice\LTspice.exe", also add with args as “-i ${FILENAME} -r ${FILENAME_NO_EXT}.raw -o ${FILENAME_NO_EXT}.out”.

4. Set the technology node as 180nm.

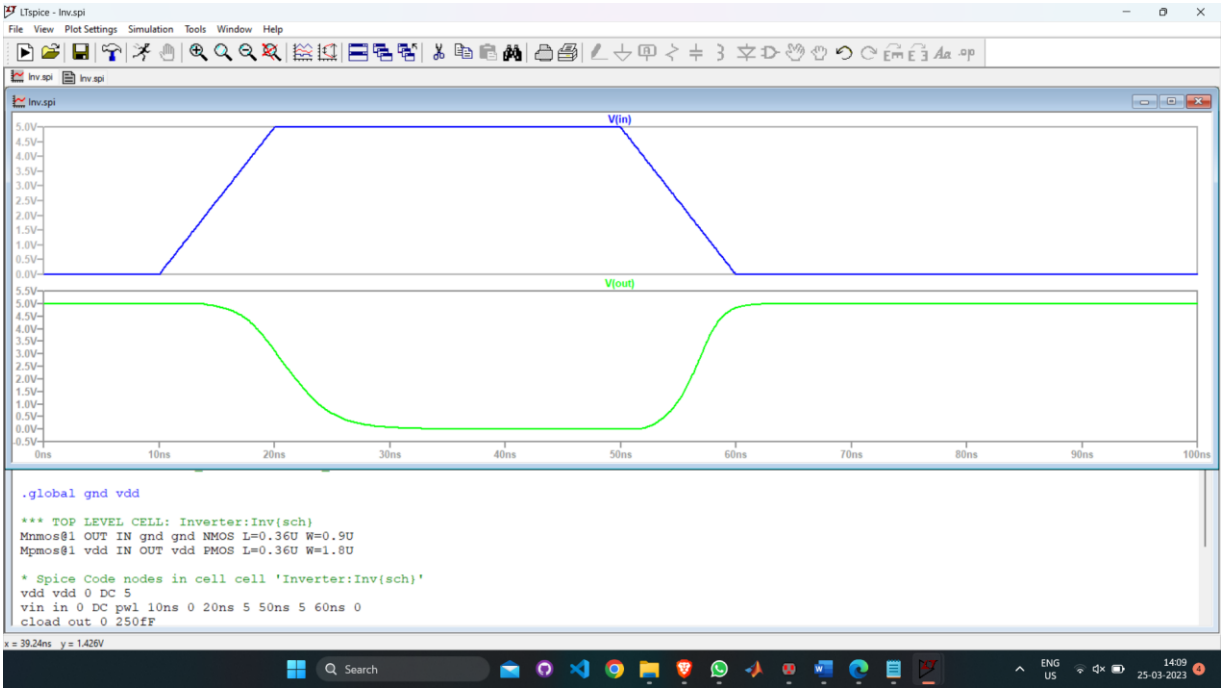
5. In the zip folder uploaded, run the **electricBinary-9.07.jar,** then open library, and then choose **BCD_To_Excess_3.jelib,** in this you will find the CMOS inverter schematic and its layout and BCD to Excess 3 and its layout. Run the DRC, ERC and NCC to for the confirmation of 0 error and 0 warning.

Results:

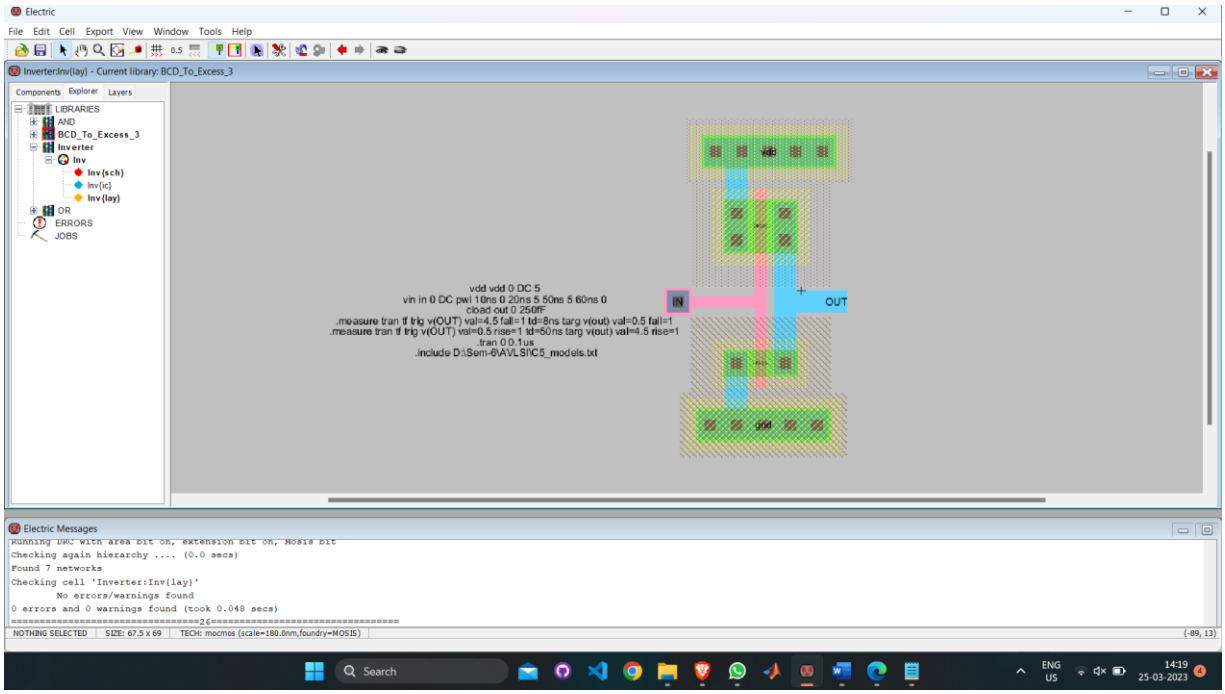
CMOS Inverter Schematic:



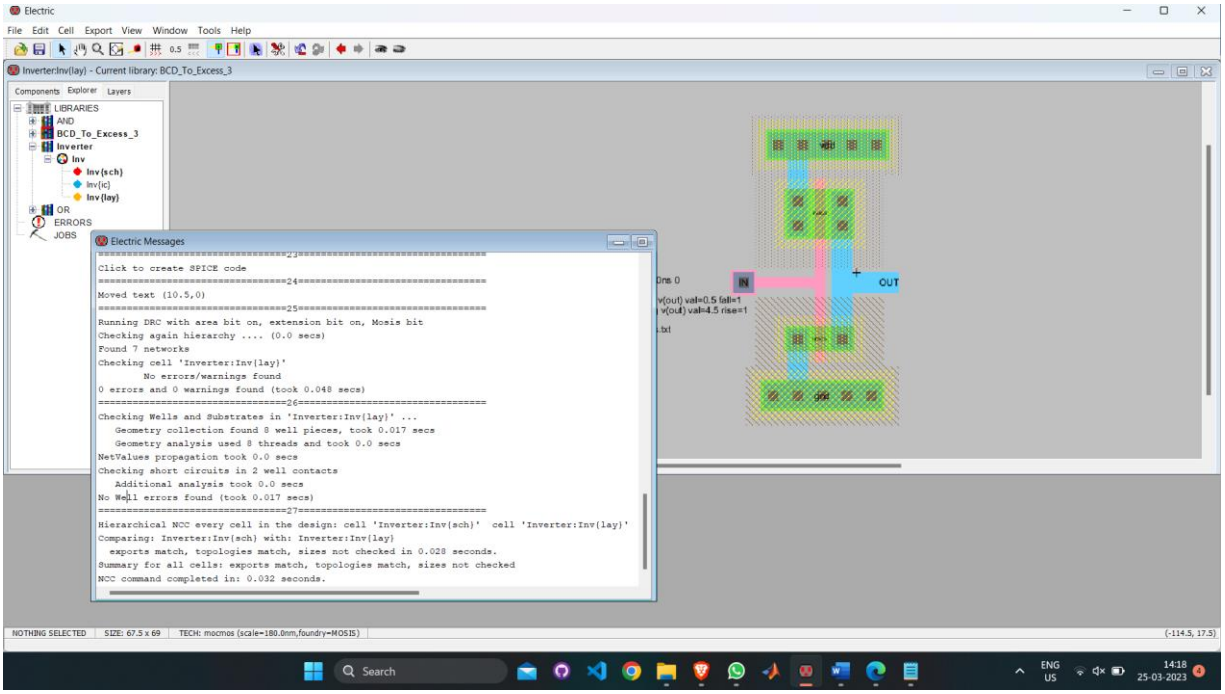
Output Graph of CMOS Inverter -



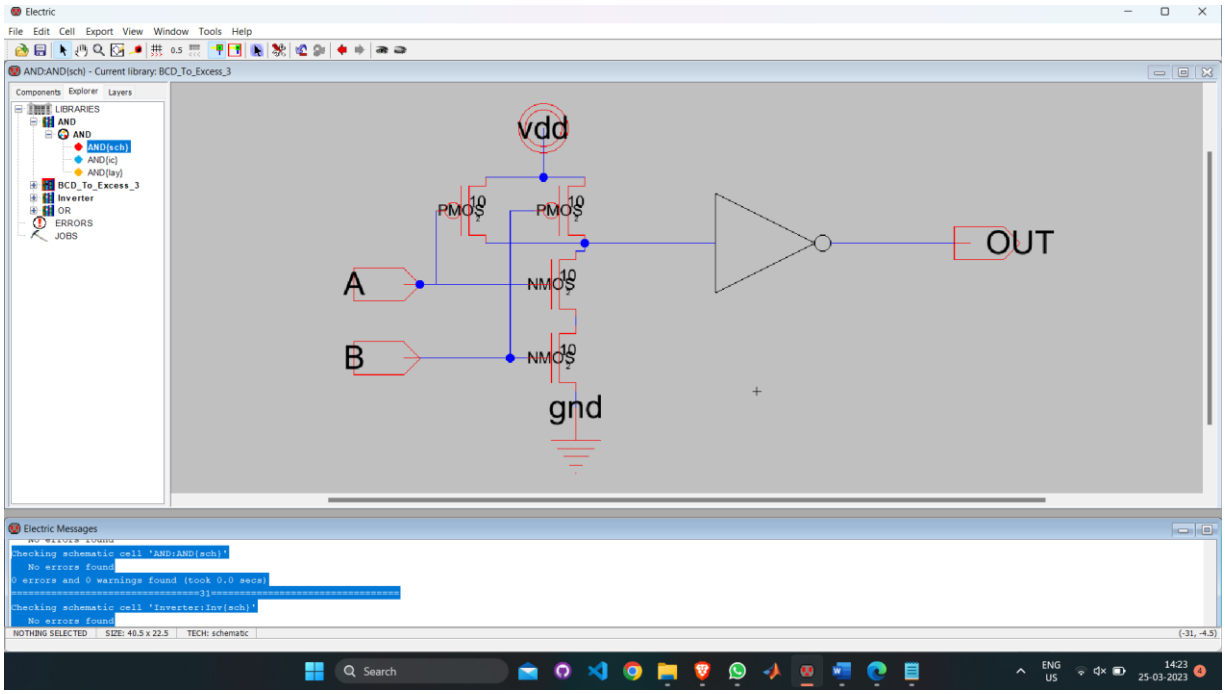
CMOS Inverter Layout:



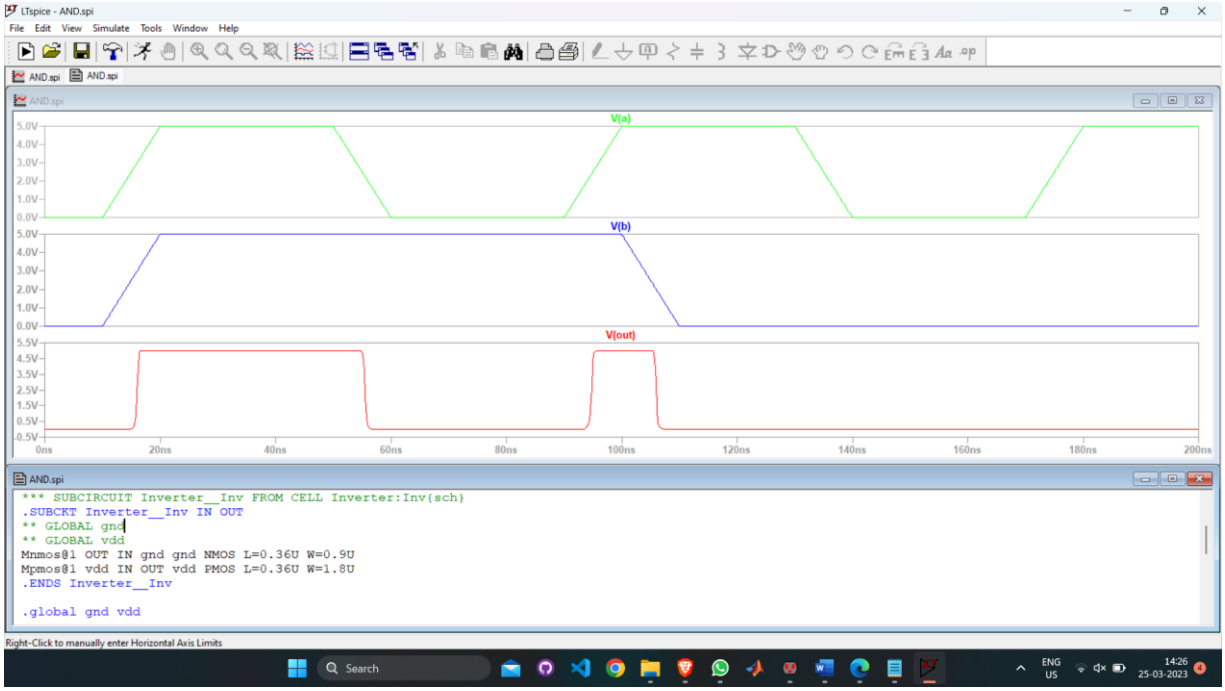
0 DRC, 0 ERC, 0 NCC Errors and 0 warnings –



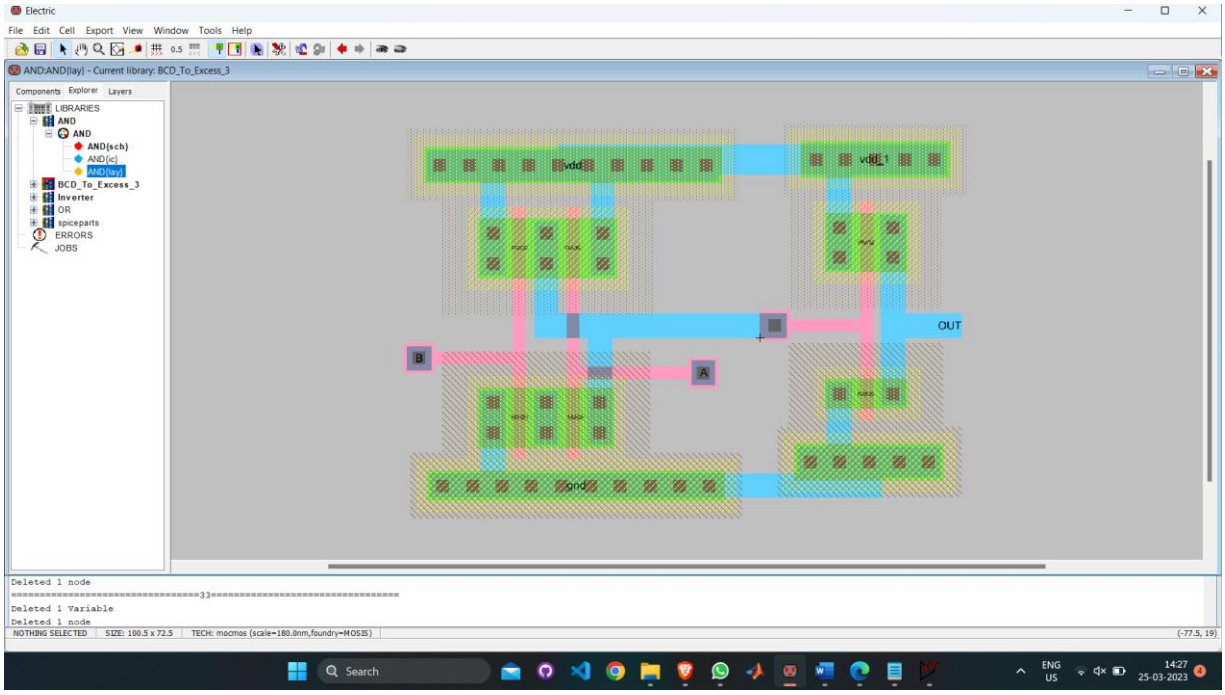
AND Gate Schematic :



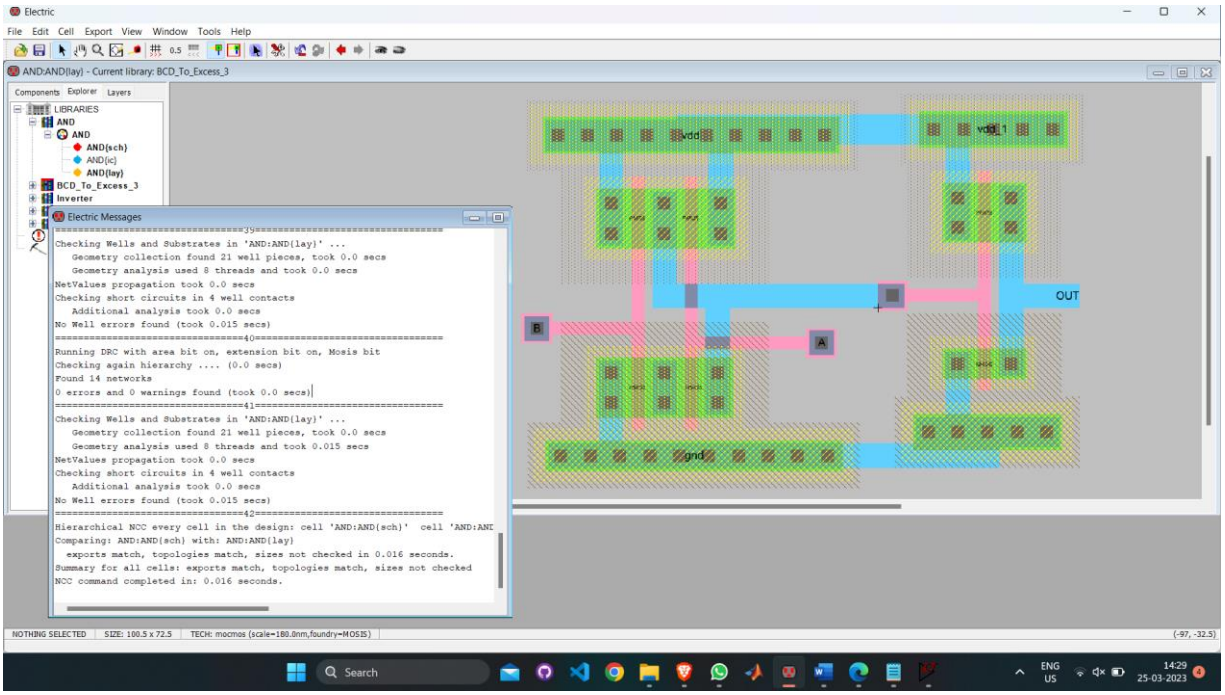
AND Gate Schematic Output:



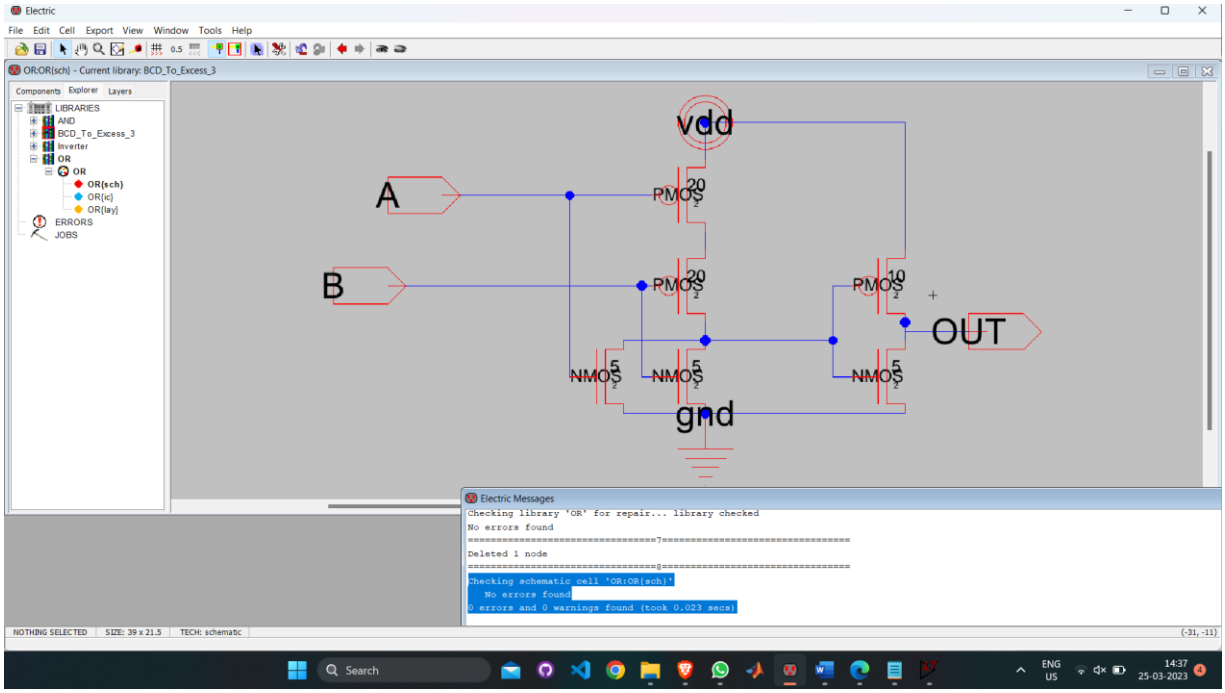
AND Gate Layout :



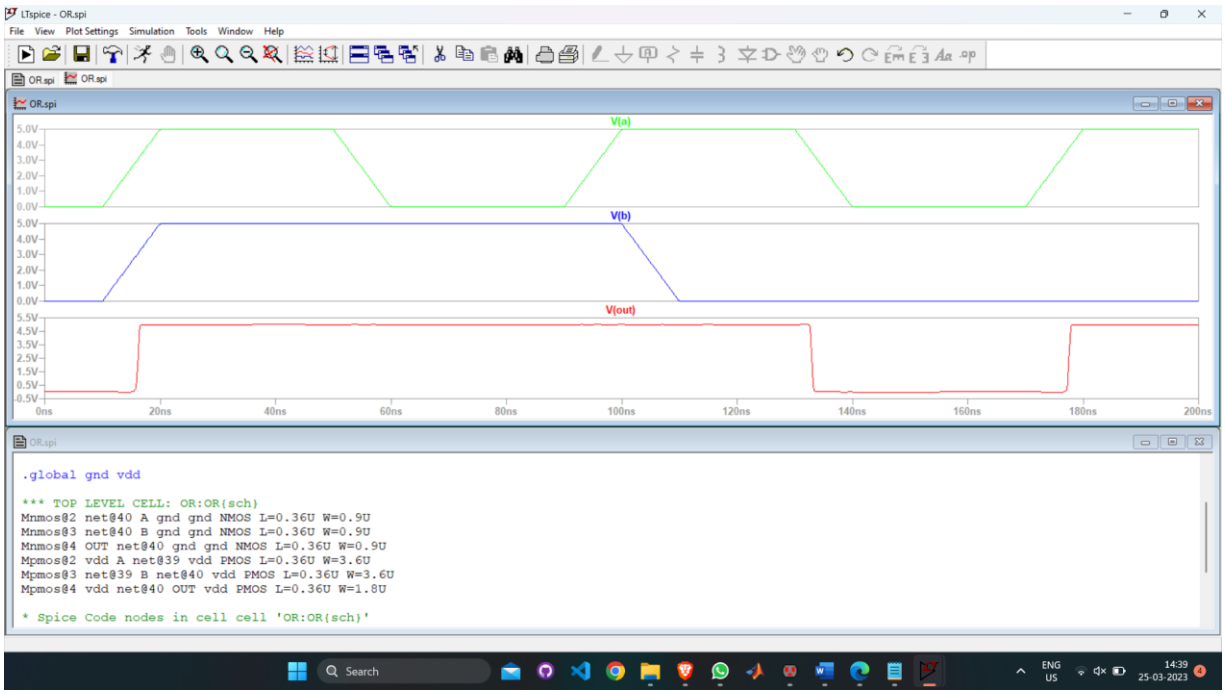
0 DRC, 0 ERC, 0 NCC Errors and 0 warnings –



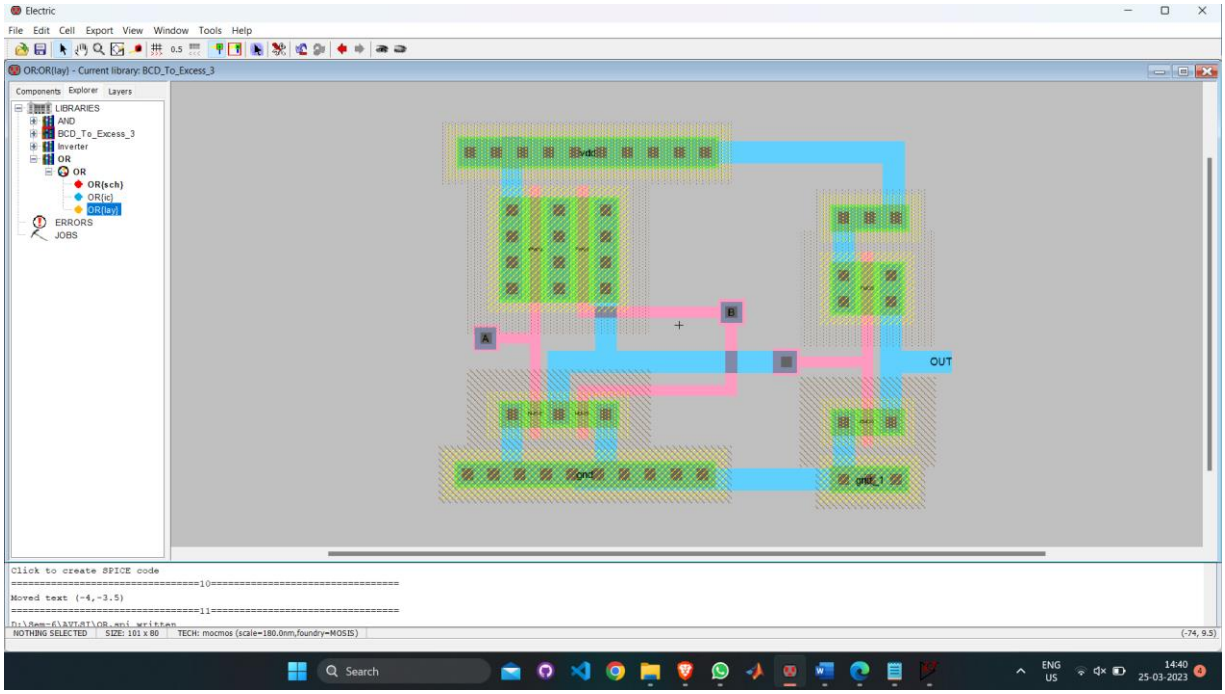
OR Gate Schematic :



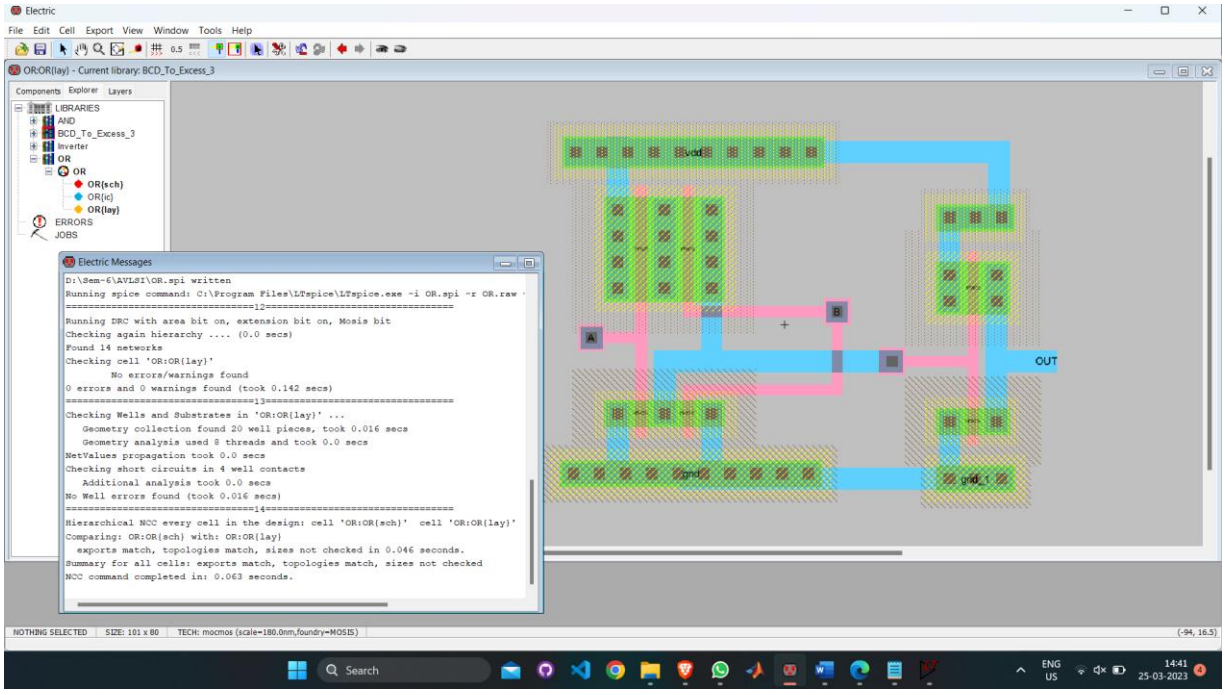
OR Gate Schematic Output –



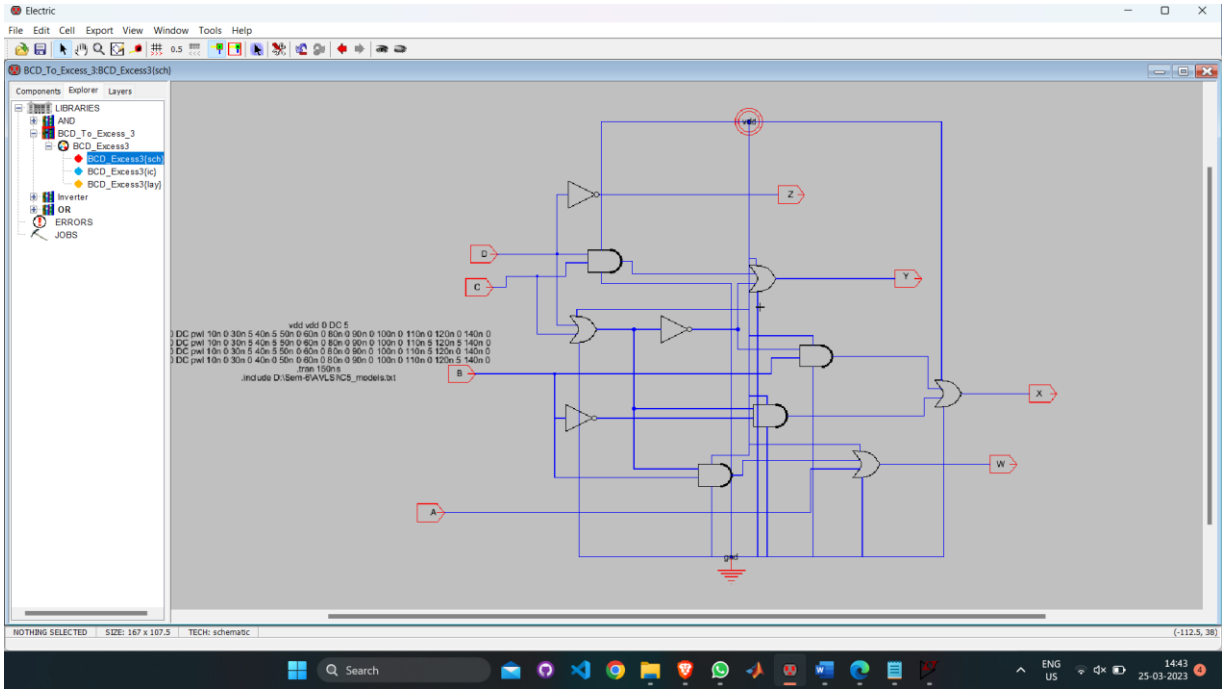
OR Gate Layout:



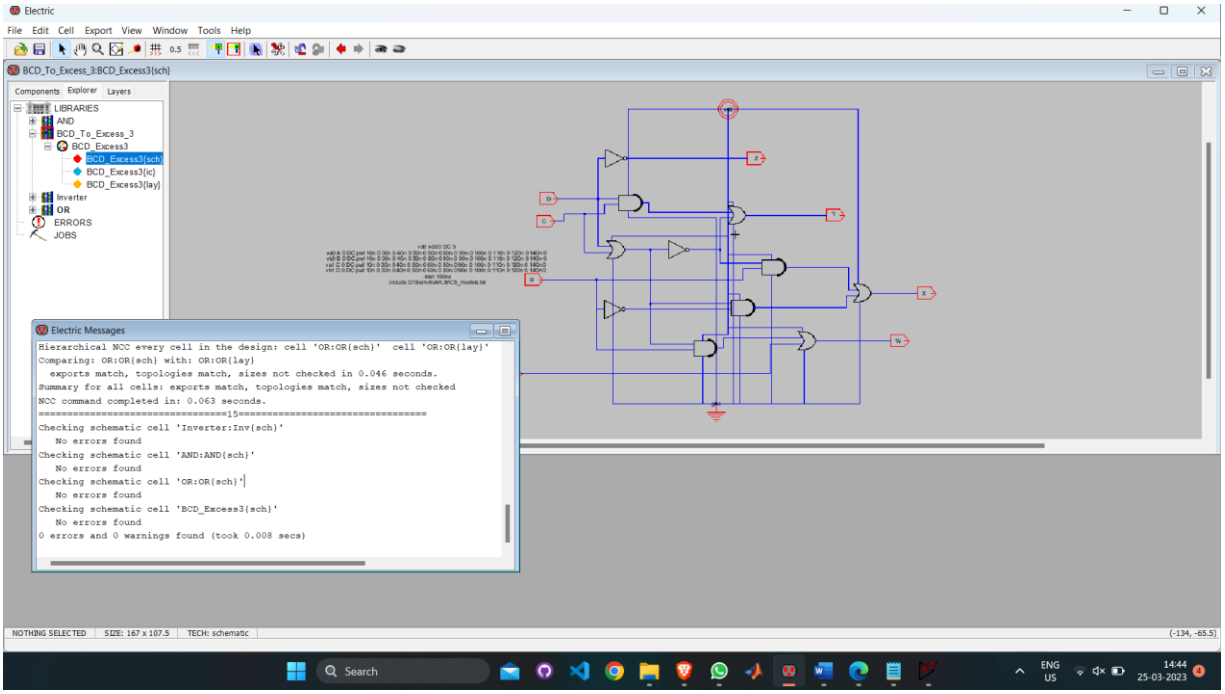
0 DRC, 0 ERC, 0 NCC Errors and 0 warnings!



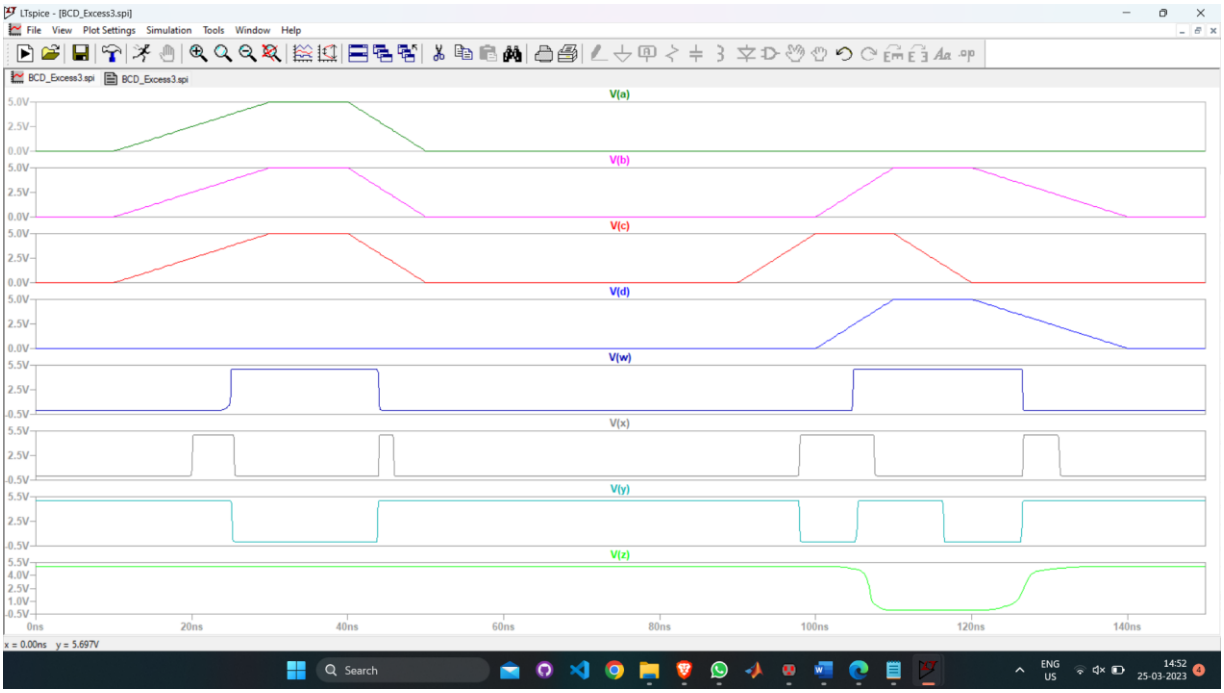
BCD to Excess-3 Schematic :



0 DRC Errors and 0 warnings –



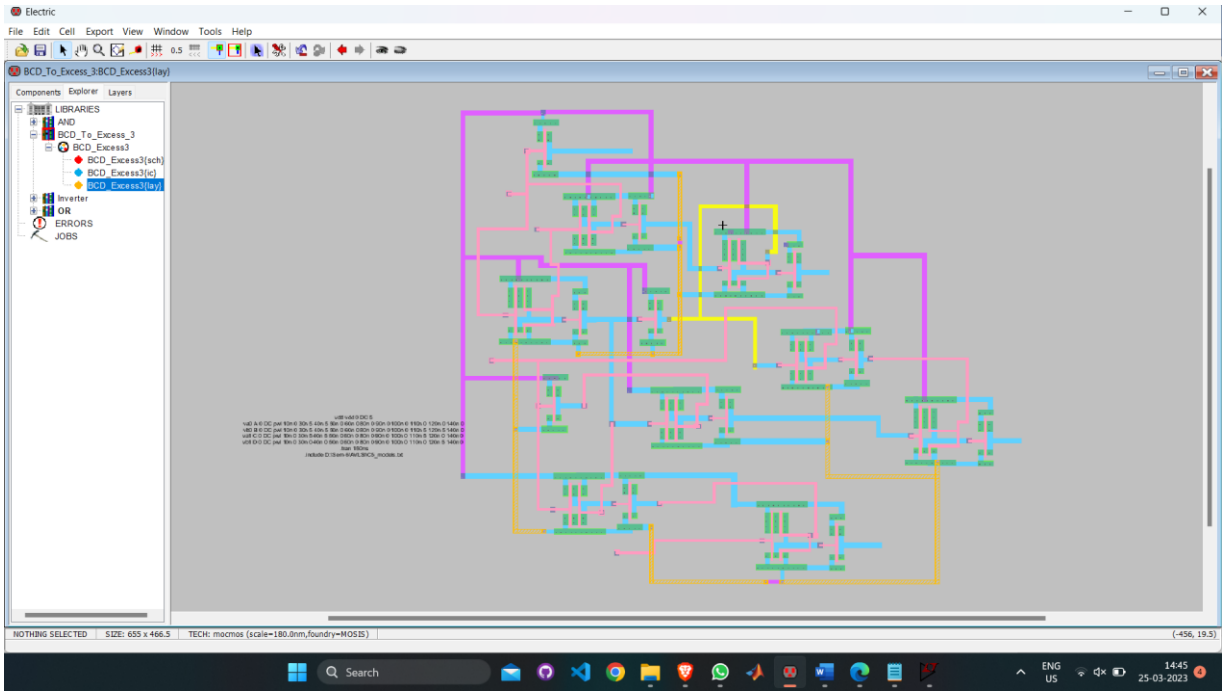
BCD to Excess-3 Schematic Output –



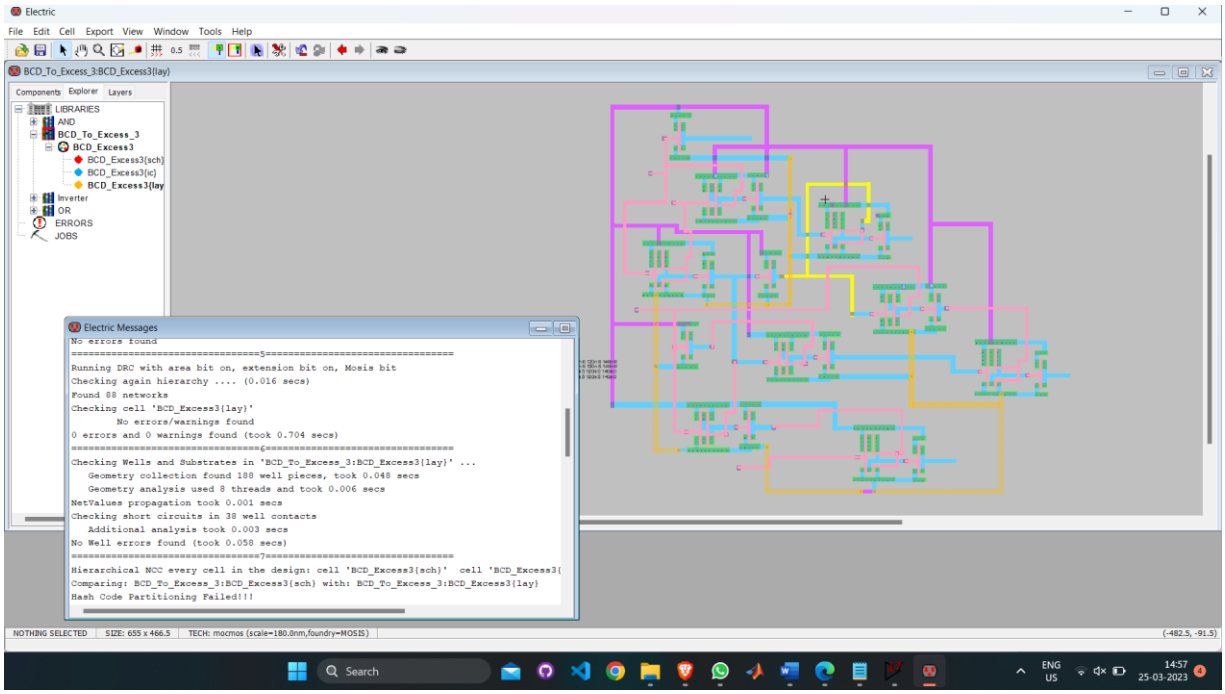
BCD to Excess-3 Truth Table :

BCD(8421)				Excess-3			
A	B	C	D	w	x	y	z
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	X	X	X	X
1	0	1	1	X	X	X	X
1	1	0	0	X	X	X	X
1	1	0	1	X	X	X	X
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

BCD to Excess-3 Layout -



0 DRC, 0 ERC, 0 NCC Errors and 0 warnings -



Contribution of each team member:

1. Eswar – Done BCD to Excess-3 and OR gate Layout and Schematic and its analysis.

2.Sayee Sreenivas– Done Inverter, And gate Layout and Schematic and its analysis.

Conclusion:

We have tried to implement the layout and schematic of BCD to Excess-3. And tried to analyze all the circuits and their behaviors and tried to make the layout and schematic as optimized as possible with 180 nm technology node and a minimum spacing of 3um . Zero DRC and ERC errors is there and PMOS W/L is 2.5 times W/L of NMOS .