CSE BUBBLE Processor Report

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PDS1 :

We will be using 16 32-bit registers.

The roles of the registers are:

S.No	Register	Purpose
1	$t0-t7	Temporary registers to hold immediate values
2	PC	Used to keep count of the next instruction to be executed
3	a,b	Used to transfer data to the alu
4	c	Used to receive data from alu
5	Instruction	Used to store machine code of Instruction

The remaining space is used for decoding and implementing the instruction i.e, opcode,func,rs,rd,rt,shamt,addr_const,jump_inst

PDS2 :

We will be using 32 Registers in the VEDA memory. 16 Registers are used for Instructions and 16 Registers are used for Data . 0-15 registers are used for storing Instructions and 16-31 Registers are used for storing data

PDS3 :

Instruction	OP code	Type of instruction
add	0	R
sub	1	R
addu	2	R
subu	3	R
addi	4	I
addiu	5	I
and	6	R
or	7	R
andi	8	I
ori	9	I
sll	10	R
srl	11	R
lw	12	I
sw	13	I
beq	14	I
bne	15	I
bgt	16	I
bgte	17	I
ble	18	I
bleq	19	I
j	20	J
jr	21	R
jal	22	J
slt	23	R
slti	24	I

All the Instructions have op : Opcode at the first 6 bits.

I-format Instructions :

- Have 2 registers and a constant value immediately present in the instruction.
- rs: source register (5 bits)
- rt: destination register (5 bits)
- immediate value (16 bits)

J-format Instructions :

- Have an address (part of one, actually) in the instruction.

R-format Instructions :

- Have func `0`. (all of them!)
- rs: 1st register operand (register source) (5 bits)
- rt: 2nd register operand (5 bits)
- rd: register destination (5 bits)
- shamt: shift amount (0 when not applicable) (5 bits)
- funct: function code (identifies the specific R-format instruction) (6 bits)

We have added another instruction with opcode 63 to print all elements of a array