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8 BIT MAGNITUDE COMPARATOR

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ABSTRACT

Comparators are a basic design module and element in modern digital VLSI design, digital signal processors and data processing application-specific integrated circuits.

In many applications there is a growing demand for the development of low voltage and low power circuits and systems.

Low power consumption is of great interest because it increases the battery lifetime.

One of the main building blocks in many applications is the analogue-to-digital converter (ADC) which serves as an interface between the analogue world and the digital processing unit.

In all these designs the comparator of the ADC, which is one the most power-hungry blocks, is always on.

In order to reduce the power consumption of the ADC it is possible to turn the comparator off when the decision is made, and the comparator is not needed until the next clock cycle.

Especially, this work focuses on the reduction of the power dissipation, which is showing an ever-increasing growth with the scaling down of the technologies.

Various techniques at the different levels of the design process have been implemented to reduce the power dissipation at the circuit, architectural and system level.

INTRODUCTION

A Digital Comparator is a combinational logic circuit that is used for comparison of two binary values. Basically, it generates the desired signal (either low or high) at the output when compares two digital values provided at its in.

There are two types of digital comparators

(1) Identity comparator
(2) Magnitude comparator.

IDENTITY COMPARATOR: is a digital comparator that has only one output. It goes high when A = B, either both 1s (High) or both 0s (Low). This comparator can be implemented by a combination of logic gates (XNOR and AND gates) as shown in Figure 1. With 8-bit numbers, the comparator compares each bit of the number with an XNOR gate. Two 8-bit numbers are only equal if each bit is identical. Inputs: The bits of two numbers which need to be compared (A, B), 8 bits for each number. Outputs: one output terminal, it goes High if A = B.

MAGNITUDE COMPARATOR: Comparators with three output terminals and checks for three conditions i.e. greater than or less than or equal to is magnitude comparator.

These are also available in IC form with different bit comparing configurations such as 1-bit,2-bit,4-bit, 8-bit, etc.

METHODLGY

An 8-bit comparator compares the two 8-bit numbers by cascading of two 4-bit comparators.

4-Bit Comparator:

It can be used to compare two four-bit words. The two 4-bit numbers are A = A3 A2 A1 A0 and B3 B2 B1 B0 where A3 and B3 are the most significant bits.

It compares each of these bits in one number with bits in that of other number and produces one of the following outputs as A = B, A < B and A>B. The output logic statements of this converter are

If A3 = 1 and B3 = 0, then A is greater than B (A>B). Or

If A3 and B3 are equal, and if A2 = 1 and B2 = 0, then A > B. Or

If A3 and B3 are equal & A2 and B2 are equal, and if A1 = 1, and B1 = 0, then A>B. Or

If A3 and B3 are equal, A2 and B2 are equal and A1 and B1 are equal, and if A0 = 1 and B0 = 0, then A > B.

The logical expression for A>B output can be written as

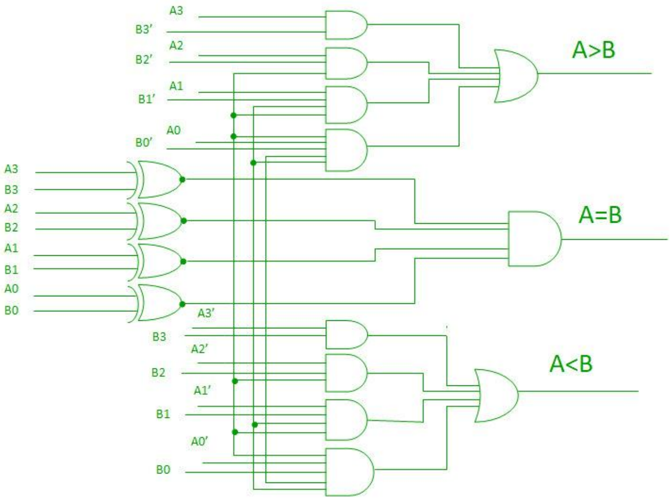
A > B : $A\ \overline{B3}$ + (A3 EX-NOR B3)A2$\overline{B2}$ + (A3 EX-NOR B3) (A2 EX-NOR B2) A1$\overline{B1}$ + (A3 EX-NOR B3)(A2 EX-NOR B2)(A1 EX-NOR B1)A0$\overline{B0}$

The logical expression for A<B output can be written as:

A < B : $\overline{A3}B3$ + (A3 EX-NOR B3)$\overline{A2}B2$ + (A3 EX-NOR B3) (A2 EX-NOR B2) $\overline{A1}B1$ + (A3 EX-NOR B3)(A2 EX-NOR B2)(A1 EX-NOR B1)$\overline{A0}B0$

The logical expression for A=B output can be written as

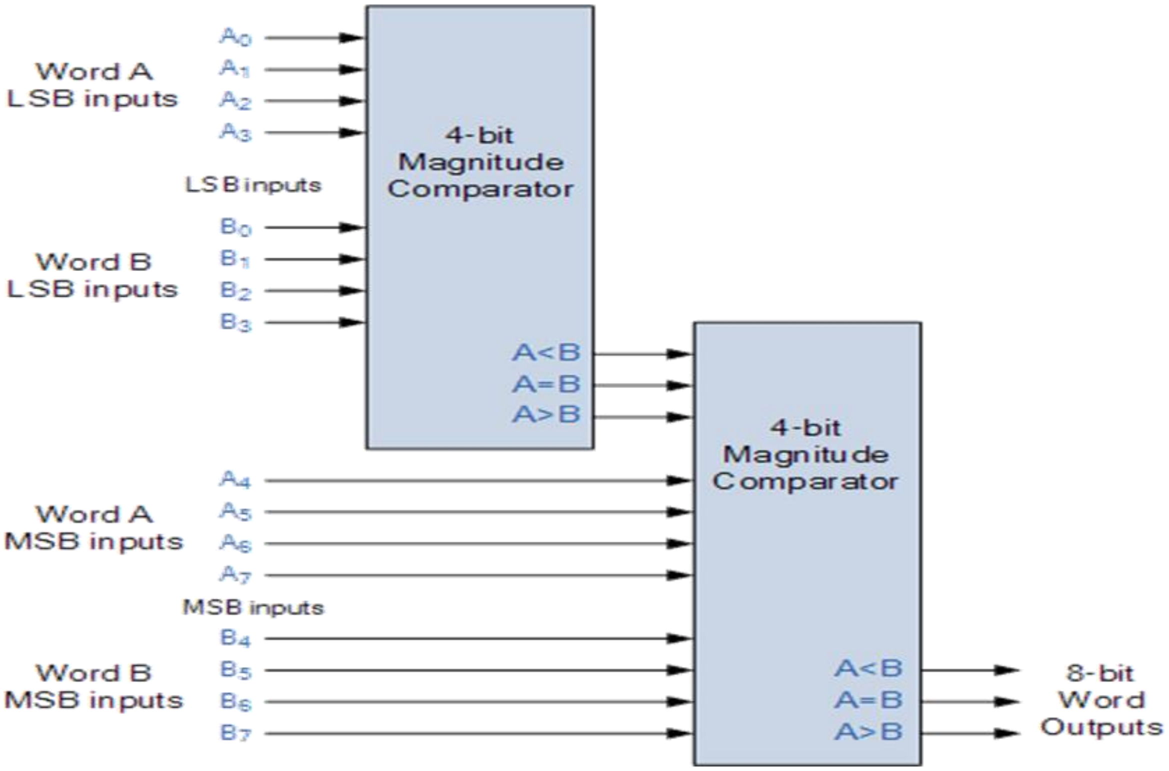
E = (A3 Ex-NOR B3) (A2 Ex-NOR B2) (A1 Ex-NOR B1) (A0 Ex-NOR B0)



8-Bit Comparator:

An 8-bit comparator compares the two 8-bit numbers by cascading of two 4-bit comparators. The circuit connection of this comparator is shown below in which the lower order comparator A<B, A=B and A>B outputs are connected to the respective cascade inputs of the higher order comparator.

For the lower order comparator, the A=B cascade input must be connected High, while the other two cascading inputs A, B must be connected to LOW. The outputs of the higher order comparator become the outputs of this eight-bit comparator.



IMPLEMENTATION/Code

4 Bit comparator as component Code:

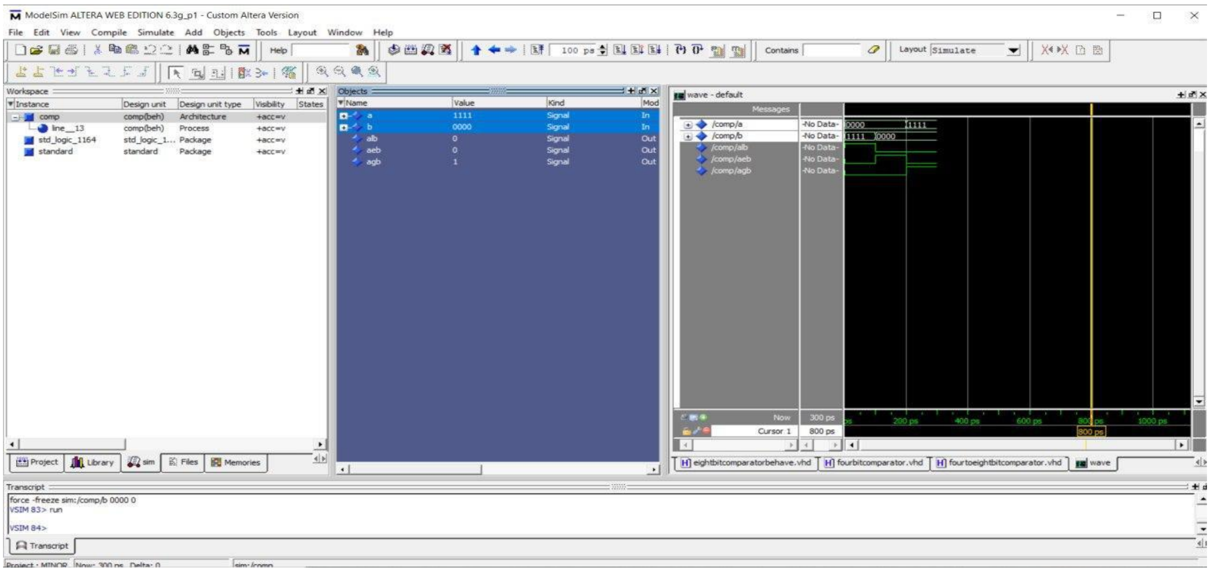
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity comp is
   Port ( a,b : in  STD_LOGIC_VECTOR (3 downto 0);
          alb,aeb,agb : out  STD_LOGIC);
end comp;
architecture Beh of comp is
begin
process( a,b)
begin
if ( a < b) then              -----a greater than b ?
agb<='0';
alb<='1';
aeb<='0';
elsif ( a > b) then            -----a less than than b ?
agb<='1';
alb<='0';
aeb<='0';
else                           --- a equal to b
agb<='0';
alb<='0';
aeb<='1';
end if;
end process;
end beh;
```

<u>8 Bit comparator using two 4 bit comparator Code:</u>

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL.
entity comp8_bit is
    Port ( a,b : in  STD_LOGIC_VECTOR (7 downto 0);
           aeb,alb,agb : out  STD_LOGIC);
end comp8_bit;
architecture Behavioral of comp8_bit is
component comp is
port( a,b:in std_logic_vector(3 downto 0);
 alb,aeb,agb : out  STD_LOGIC:='0');
 end component;
 signal g,l,e,g1,l1,e1:std_logic;
begin
x1:comp port map(a(7 downto 4),b(7 downto 4),l,e,g);
x2:comp port map(a(3 downto 0),b(3 downto 0),l1,e1,g1);
process(g1,l1,e1,g,l,e) is
begin
if(g='1') then agb<='1';alb<='0';aeb<='0';
elsif(l='1') then agb<='0';alb<='1';aeb<='0';
else--if(e='1') then
if(g1='1')then agb<='1';alb<='0';aeb<='0';
elsif(l1='1') then agb<='0';alb<='1';aeb<='0';
else aeb<='1'; alb<='0';agb<='0';
end if;
end if;
end process;
end behavioral;
```

RESULTS:

4-bit Magnitude Comparator Output:



Instance	Design unit	Design unit type	Visibility	States
comp	comp(beh)	Architecture	+acc=v	
line__13	comp(beh)	Process	+acc=v	
std_logic_1164	std_logic_1...	Package	+acc=v	
standard	standard	Package	+acc=v	

Name	Value	Kind	Mod
a	1111	Signal	In
b	0000	Signal	In
alb	0	Signal	Out
aeb	0	Signal	Out
agb	1	Signal	Out

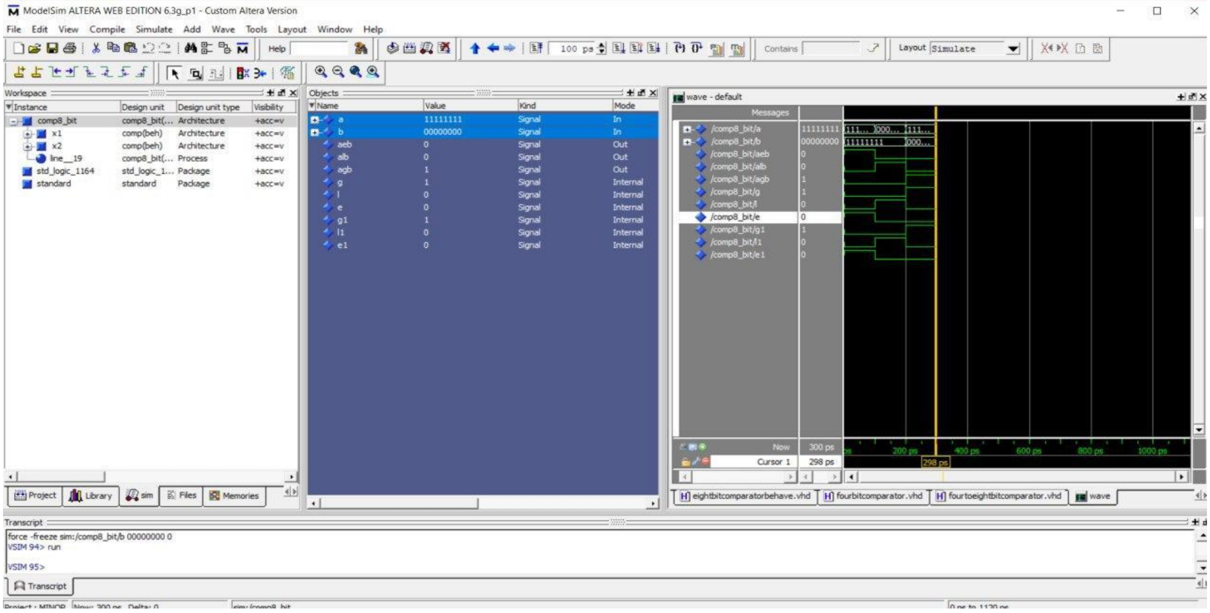
Messages	
/comp/a	-No Data-
/comp/b	-No Data-
/comp/alb	-No Data-
/comp/aeb	-No Data-
/comp/agb	-No Data-

```
force -freeze sim:/comp/b 0000 0
VSIM 83> run

VSIM 84>
```

Project : MINOR Now: 300 ps Delta: 0 sim:/comp

8-bit Magnitude Comparator Output:



Instance	Design unit	Design unit type	Visibility
comp8_bit	comp8_bit(...	Architecture	+acc=v
x1	comp(beh)	Architecture	+acc=v
x2	comp(beh)	Architecture	+acc=v
line__19	comp8_bit(...	Process	+acc=v
std_logic_1164	std_logic_1...	Package	+acc=v
standard	standard	Package	+acc=v

Name	Value	Kind	Mode
a	11111111	Signal	In
b	00000000	Signal	In
aeb	0	Signal	Out
alb	0	Signal	Out
agb	1	Signal	Out
g	1	Signal	Internal
l	0	Signal	Internal
e	0	Signal	Internal
g1	1	Signal	Internal
l1	0	Signal	Internal
e1	0	Signal	Internal

Messages	
/comp8_bit/a	11111111
/comp8_bit/b	00000000
/comp8_bit/aeb	0
/comp8_bit/alb	0
/comp8_bit/agb	1
/comp8_bit/g	1
/comp8_bit/l	0
/comp8_bit/e	0
/comp8_bit/g1	1
/comp8_bit/l1	0
/comp8_bit/e1	0

```
force -freeze sim:/comp8_bit/b 00000000 0
VSIM 94> run

VSIM 95>
```

Project : MINOR Now: 300 ps Delta: 0 sim:/comp8_bit

Applications of Comparators –

1. Comparators are used in central processing units (CPUs) and microcontrollers (MCUs).
2. These are used in control applications in which the binary numbers representing physical variables such as temperature, position, etc. are compared with a reference value.
3. Comparators are also used as process controllers and for Servo motor control.
4. Used in password verification and biometric applications.

Advantage: The main advantage of this cascading ability and this work is that it requires a smaller number of gates compared to the conventional structure of magnitude comparator.

Disadvantage: The main disadvantage in the serial bit stream data comparator is it takes much time to perform the comparison.

CONCLUSION: From this project, I have learned the design of a 8-bit digital comparator circuit of Magnitude from 4-bit digital comparator circuit of Magnitude using VHDL in ModelSim.

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