Design and Implementation of CMOS Analog-to-Digital (A/D) Converter Using Voltage Controlled Oscillator (VCO) and D Flip-Flop in 90nm Technology.

Abstract:

This project explores the design and implementation of a CMOS Analog-to-Digital Converter (ADC) utilizing a Voltage-Controlled Oscillator (VCO) and D Flip-Flops (DFF) in 90nm technology. The ADC architecture exploits the frequency modulation properties of the VCO, which transforms the input analog signal into a frequency signal. The frequency signal is then sampled by a series of D Flip-Flops to generate a corresponding digital output. This design approach is advantageous due to its simplicity, scalability, and compatibility with modern CMOS technologies, making it suitable for applications requiring low power and compact designs.

The ADC was implemented and simulated in Cadence Virtuoso, with the 90nm CMOS technology node ensuring a balance between performance and power efficiency. The design process involved the optimization of the VCO for a wide frequency range and low power consumption, alongside the implementation of robust DFFs to handle high-speed signals accurately. Detailed simulations were performed to analyze the system's performance, including metrics such as resolution, power consumption, linearity, and speed.

Results indicate that the proposed ADC achieves significant performance benefits, maintaining a high degree of accuracy and efficiency across varying input conditions. This project highlights the potential of CMOS-based VCO-DFF ADCs in advancing compact, low-power, and high-speed mixed-signal systems, paving the way for future innovations in integrated circuit design.

Introduction:

Analog-to-Digital Converters (ADCs) are critical components in modern electronic systems, bridging the gap between the analog world and digital processing. They find applications in fields such as communication, signal processing, data acquisition, and control systems. ADCs are tasked with converting continuous analog signals into discrete digital representations, enabling further processing by digital systems. The choice of ADC architecture significantly impacts performance metrics such as resolution, speed, power consumption, and silicon area, making the design process both challenging and application-specific.

This project focuses on the design and implementation of a CMOS ADC utilizing a Voltage-Controlled Oscillator (VCO) and D Flip-Flops (DFF) in the 90nm technology node. VCO-based ADCs represent a unique class of converters where the analog input signal is converted into a frequency-modulated signal. This signal is then sampled and digitized, offering a simple yet effective method for analog-to-digital conversion. The use of VCOs provides several advantages, including inherent noise shaping, simplicity in design, and compatibility with modern CMOS processes.

The D Flip-Flops (DFFs) play a vital role in this architecture by sampling the VCO's output frequency signal and generating the corresponding digital output. Their efficient operation at high frequencies ensures that the ADC delivers accurate and reliable results. The adoption of the 90nm CMOS technology node further enhances the design by providing a favorable trade-off between power efficiency, speed, and integration density.

This report details the theoretical principles, design methodology, and simulation results of the proposed ADC, as implemented in Cadence Virtuoso. The project aims to demonstrate a high-performance, low-power ADC solution that meets the demands of modern mixed-signal systems.

Through detailed analysis and performance evaluation, this work underscores the potential of VCO-DFF-based ADCs in advancing compact and efficient data conversion technologies.

Theory and Design Approach

The design of the ADC consists of two primary blocks: the Voltage-to-Frequency Converter (VFC) and the Frequency-to-Digital Converter (FDC), which work together to convert the analog input signal into a corresponding digital output.

Voltage-to-Frequency Converter (VFC)

The Voltage-to-Frequency Converter operates by converting the input analog voltage into a frequency signal. This is achieved through the use of a Voltage-Controlled Oscillator (VCO), where the oscillation frequency is directly proportional to the input voltage. As the input voltage increases, the frequency output from the VCO increases proportionally, which enables the analog signal to be represented by a frequency value. This frequency-modulated signal can then be used for further processing in the next stage of the ADC.

In the VFC design, key considerations include ensuring a wide tuning range to cover the entire range of expected input voltages, maintaining power efficiency, and ensuring a linear relationship between the input voltage and the output frequency. The block diagram of the Voltage-to-Frequency Converter is shown in Fig. 1.

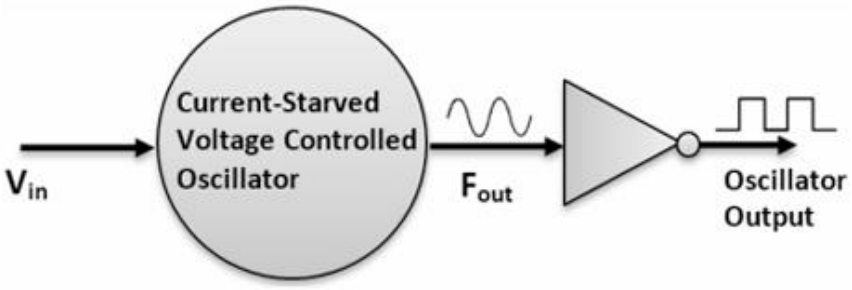

Figure – 1: Block diagram of the voltage-to-frequency converter (VFC)

Frequency-to-Digital Converter (FDC)

The Frequency-to-Digital Converter is responsible for converting the frequency signal from the VFC into a digital output. This is achieved using D Flip-Flops (DFFs), which sample the frequency signal at regular intervals. The D Flip-Flops capture the transitions of the frequency signal and convert them into binary values, effectively digitizing the frequency signal. The digital output corresponds to the frequency input, which can then be processed as a digital representation of the original analog signal.

Key design considerations for the FDC include ensuring high-speed operation to handle the fast-changing frequency signal and ensuring reliable sampling with minimal jitter. The rough block diagram of the Frequency-to-Digital Converter is shown in Fig. 2.

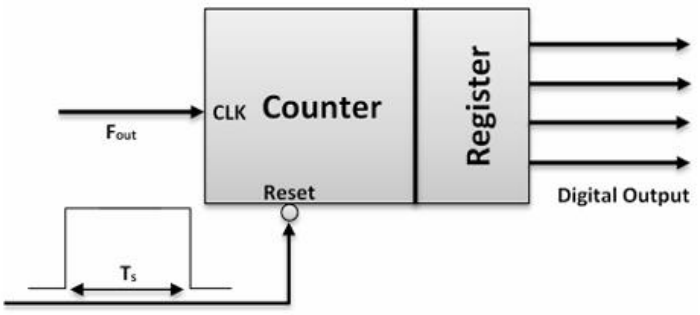

Figure – 2: Block diagram of frequency-to-digital converter (FDC)

Overall Block Diagram

The overall ADC system integrates the VFC and FDC blocks, with the input analog signal first being converted to a frequency by the VFC, and then this frequency is digitized by the FDC. The integration of both blocks forms the complete ADC system, where the analog input is converted to a digital output. The overall block diagram of the ADC system is shown in Fig. 3.

This approach of using a VFC and FDC in conjunction with CMOS technology provides an efficient, low-power, and high-speed method for analog-to-digital conversion, making it ideal for modern applications requiring compact, energy-efficient designs.

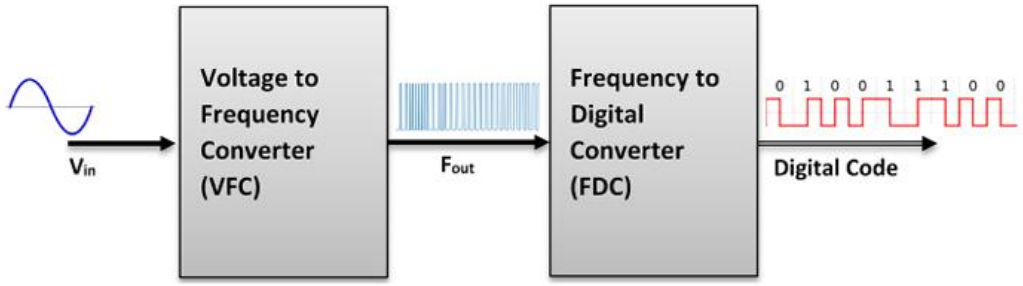

Figure – 3: Block diagram of VCO-based ADC

Schematic:

The following schematics form the core components of the Analog-to-Digital Converter (ADC) design using Voltage-Controlled Oscillator (VCO) and D Flip-Flops (DFFs), which together convert the analog input signal into a digital output.

1. D Flip-Flop Circuit (DFF)

The D Flip-Flop (DFF) captures the frequency signal generated by the Voltage-to-Frequency Converter and converts it into a digital signal. The basic DFF consists of a data input (D), clock input (CLK), and output (Q). The circuit stores the input on the rising or falling edge of the clock signal.

The schematic of the D Flip-Flop is shown in **Fig. 4**, and its symbol is provided in **Fig. 5**.

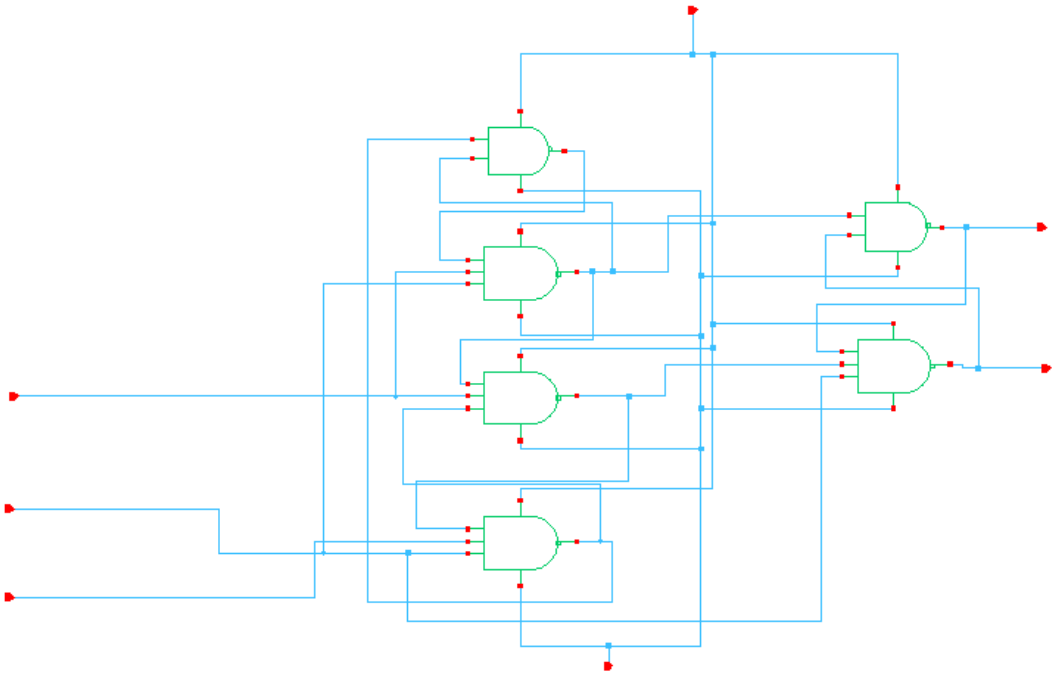

Figure – 4: D Flip-Flop Circuit

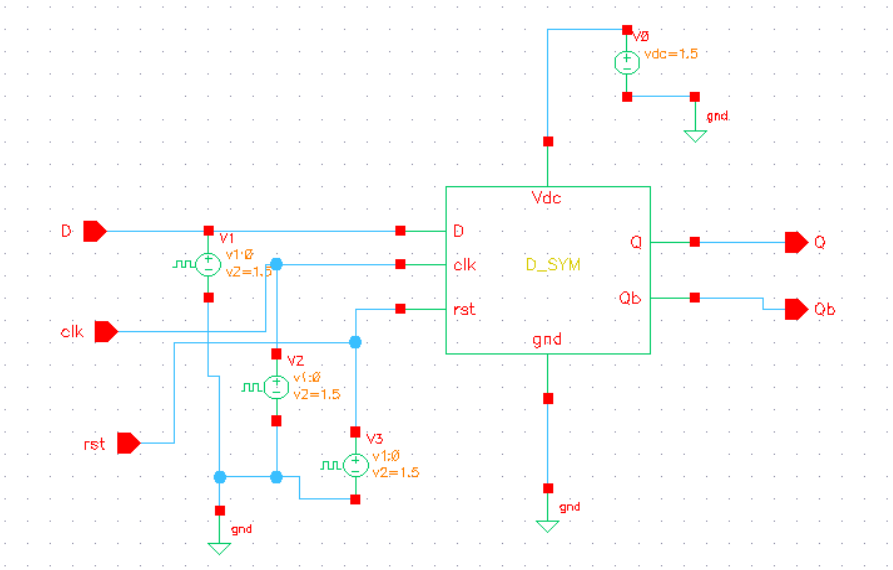

Figure – 5: D Flip-Flop Symbol

2. 2-Input NAND Circuit

The 2-input NAND gate is used in the ADC design for controlling the logic of the D Flip-Flops and other control circuits. The output of the NAND gate is LOW only when both inputs are HIGH.

The schematic of the 2-input NAND gate is shown in **Fig. 6**, and its symbol is shown in **Fig. 7**.

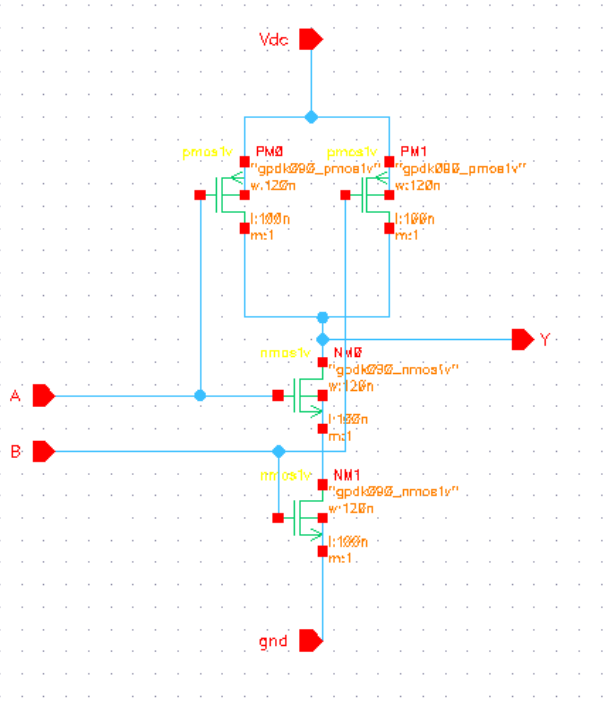

Figure – 6: 2 – I/P NAND Circuit

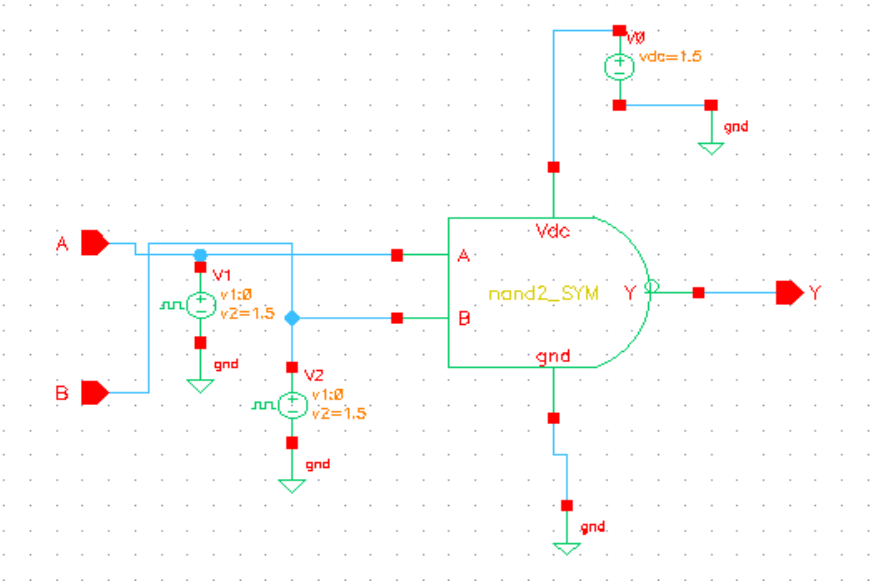

Figure – 7: 2 – I/P NAND Symbol

3-Input NAND Circuit

Similar to the 2-input NAND gate, the 3-input NAND gate is used to create more complex logic functions within the design. It outputs LOW only when all three inputs are HIGH.

The schematic of the 3-input NAND gate is shown in **Fig. 8**, and its symbol is shown in **Fig. 9**.

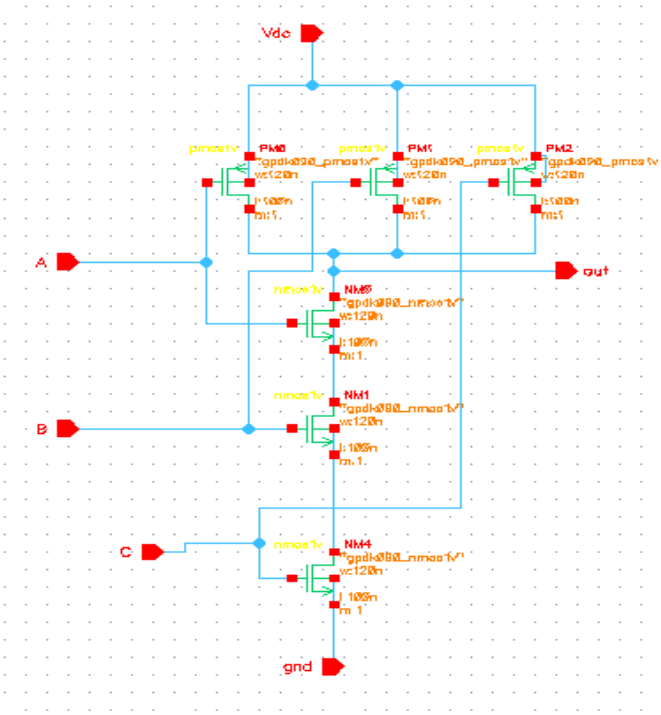

Figure – 8: 3 – I/P NAND Circuit

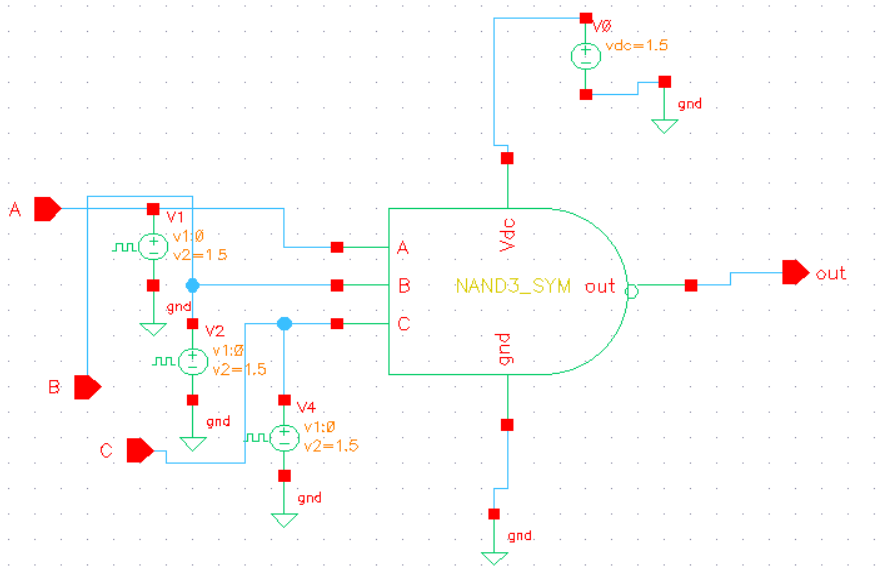

Figure – 9: 3 – I/P NAND Symbol

4. Voltage-Controlled Oscillator (VCO) Circuit

The Voltage-Controlled Oscillator (VCO) is a key component in the Voltage-to-Frequency Converter. The VCO generates an oscillating frequency that is directly proportional to the input voltage. The schematic of the VCO is shown in **Fig. 10**, and its symbol is shown in **Fig. 11**.

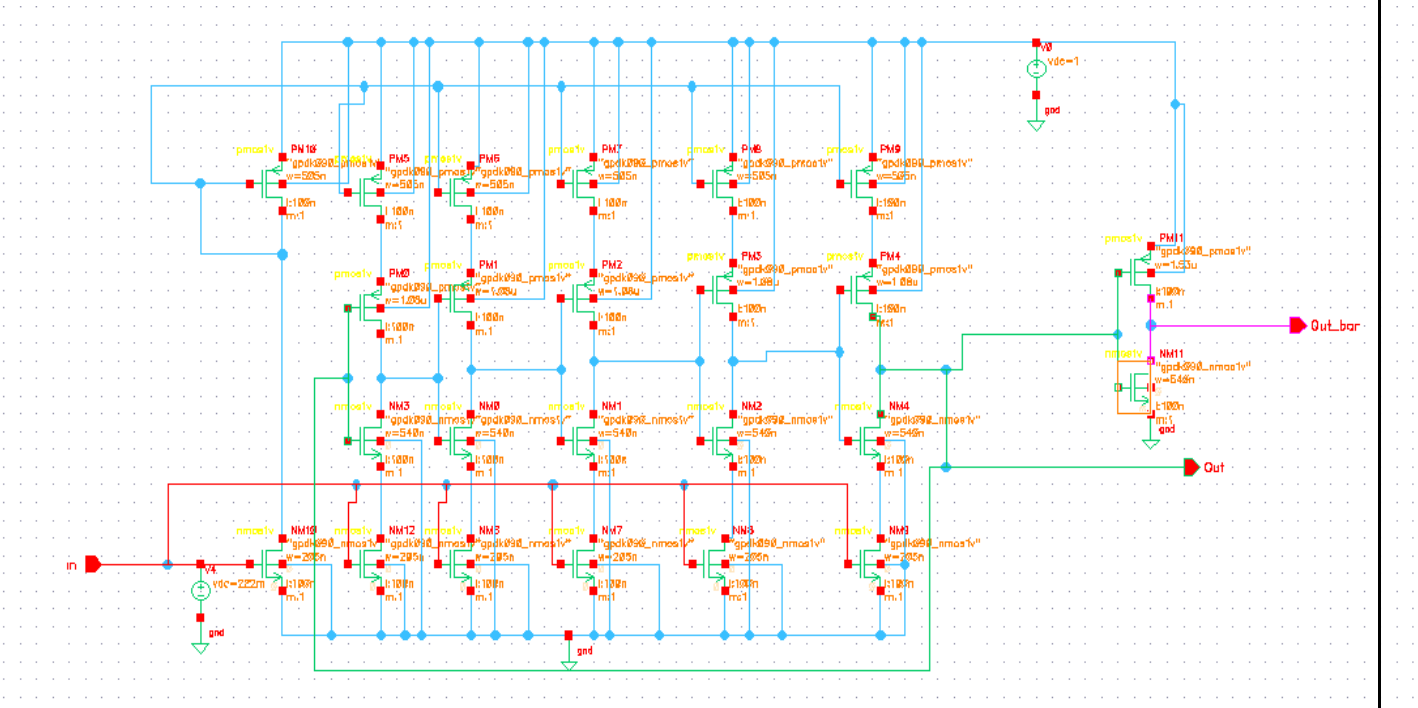

Figure – 10: VCO Circuit

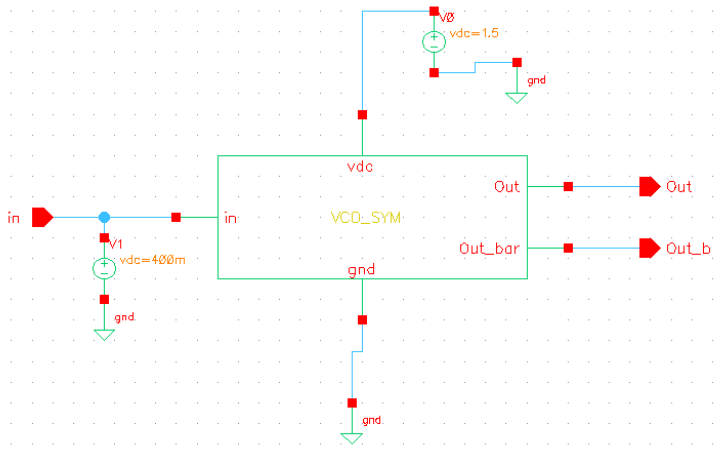

Figure – 11: VCO Symbol

5. ADC Using VCO and DFF Circuit

The complete ADC circuit integrates the Voltage-to-Frequency Converter (VFC) and the Frequency-to-Digital Converter (FDC). The input voltage is applied to the VCO, which generates a frequency. This frequency is then sampled by the D Flip-Flops to produce a corresponding digital output.

The schematic of the entire ADC system using the VCO and DFF is shown in **Fig. 12**.

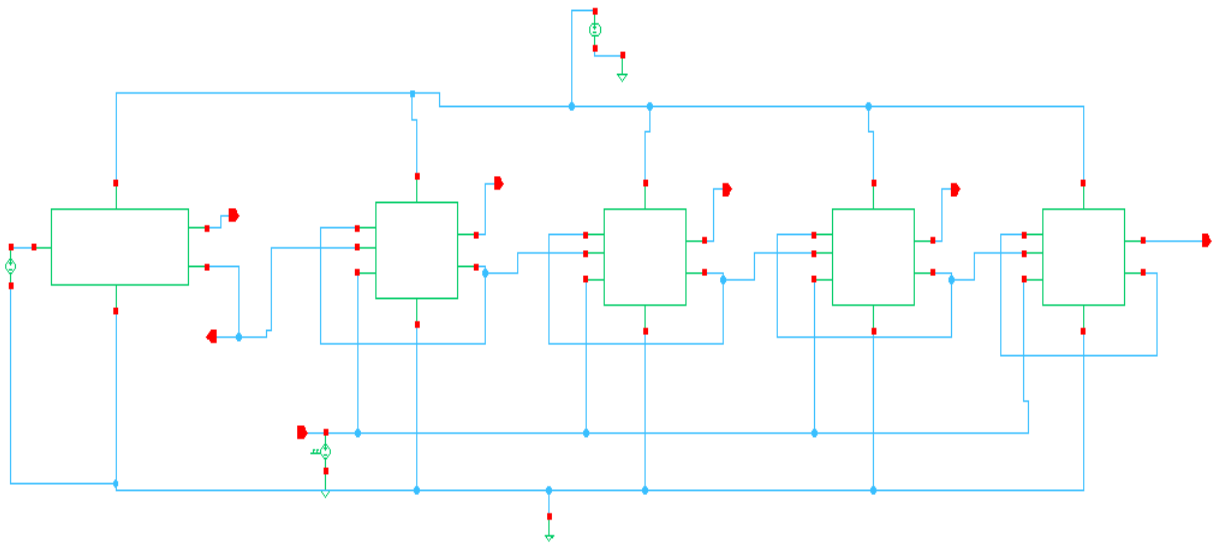

Figure – 12: ADC Schematic Circuit

Simulation:

The following waveforms illustrate the simulation results for various components of the ADC design, demonstrating the operation of the D Flip-Flop, NAND gates, Voltage-Controlled Oscillator (VCO), and the complete ADC system at different input voltages. These waveforms help visualize the behavior of each circuit and the overall ADC system's performance.

1. D Flip-Flop (DFF) Waveform

The D Flip-Flop (DFF) samples the frequency signal generated by the Voltage-Controlled Oscillator (VCO) and outputs a corresponding digital signal. The waveform of the DFF demonstrates how the input frequency is captured and converted into a digital state. The transitions of the DFF output occur on the rising or falling edge of the clock, depending on the configuration.

The **D Flip-Flop waveform** is shown in **Fig. 13**.

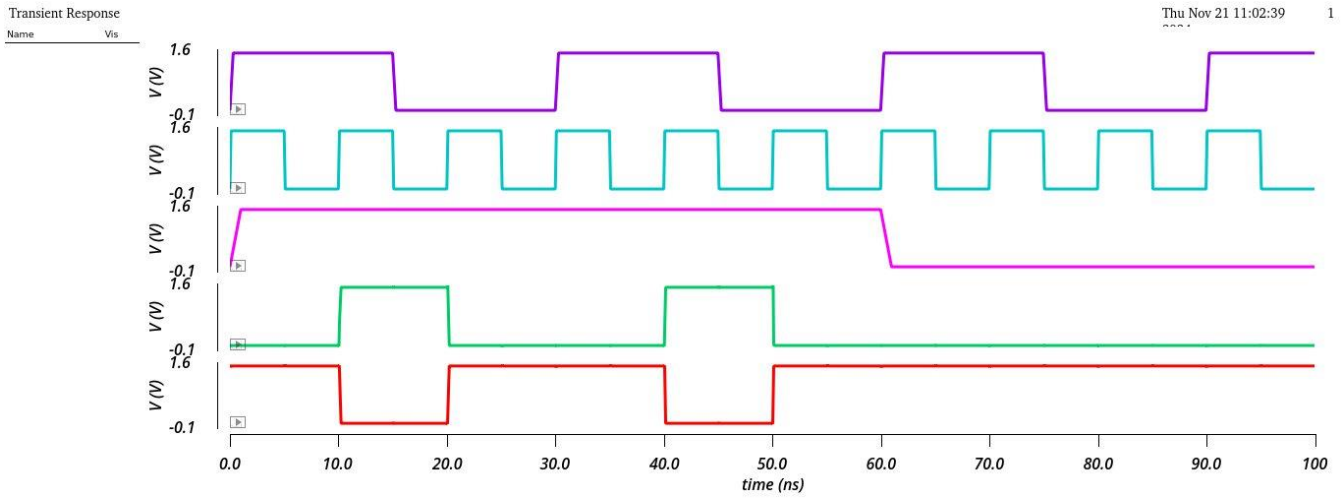

Figure – 13: D Flip-Flop Waveform

2. 2-Input NAND Gate Waveform

The 2-input NAND gate performs a basic logic operation. The simulation waveform illustrates how the output of the 2-input NAND gate changes in response to varying input states. The NAND gate produces a LOW output only when both inputs are HIGH; otherwise, the output remains HIGH.

The **2-input NAND gate waveform** is shown in **Fig. 14**.

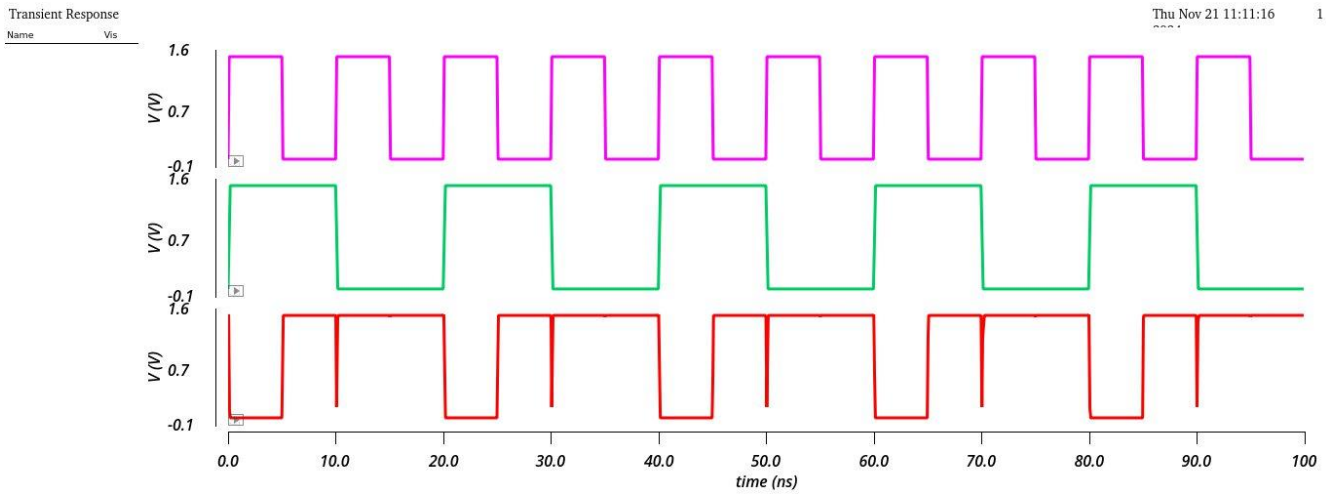

Figure – 14: 2 - I/P NAND gate Waveform

3. 3-Input NAND Gate Waveform

Similar to the 2-input NAND gate, the 3-input NAND gate generates a LOW output when all three inputs are HIGH. The waveform of the 3-input NAND gate shows how its output varies with the inputs, performing a logical negation on the AND operation of the three inputs.

The **3-input NAND gate waveform** is shown in **Fig. 15**.

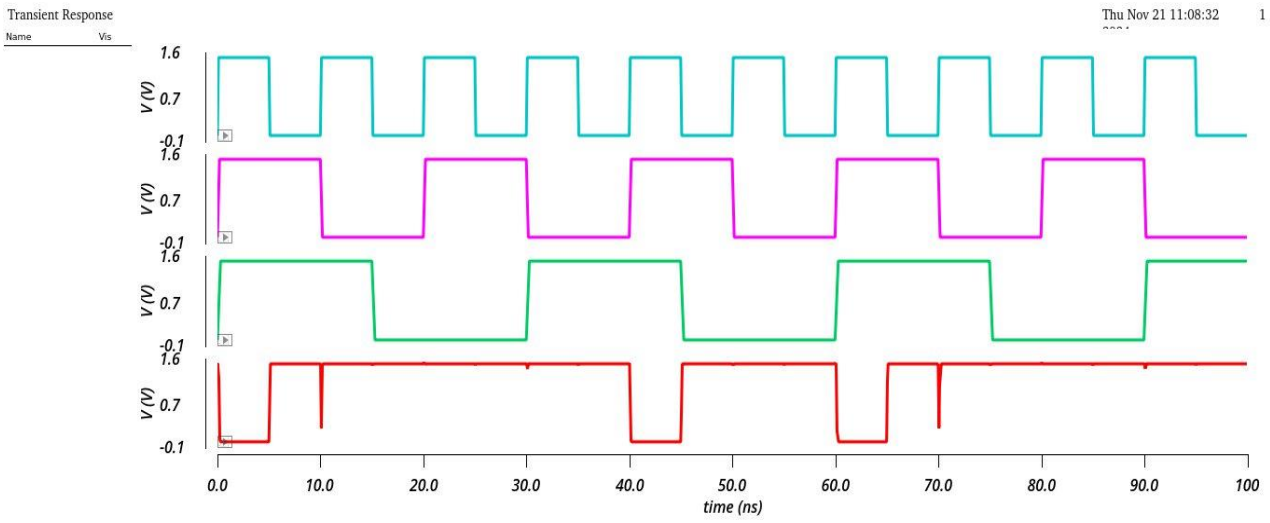

Figure – 15: 3 - I/P NAND gate Waveform

4. Voltage-Controlled Oscillator (VCO) Waveform

The Voltage-Controlled Oscillator (VCO) generates a frequency output that is directly proportional to the input voltage. In the simulation, the VCO output frequency is shown for an input voltage of 0.4V, demonstrating how the oscillation frequency changes as the control voltage is applied.

The **VCO waveform at 0.4V** is shown in **Fig. 16**.

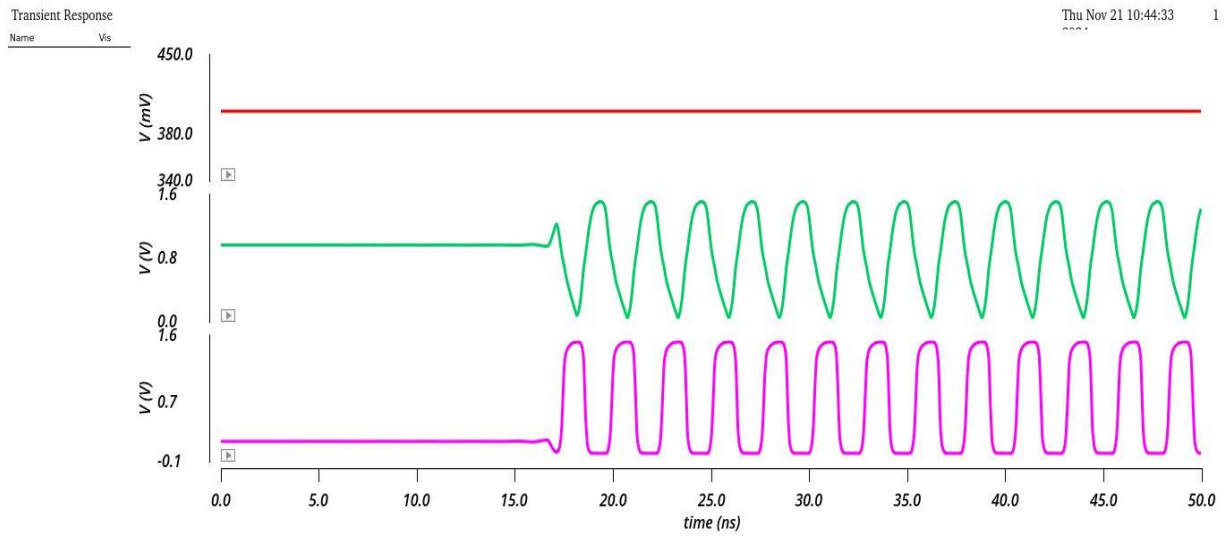

Figure – 16: VCO Waveform

5. Different ADC Waveforms

The ADC system's performance is observed at different input voltages (0.4V, 0.6V, 0.8V, 1.0V). These waveforms show the ADC's ability to convert the analog input signal into a digital signal at various voltage levels. The waveforms are taken for the ADC system, showing the digitized outputs corresponding to the different input voltages, including the power consumption at each voltage level.

The **ADC waveforms at 0.4V, 0.6V, 0.8V, and 1.0V** are shown in **Fig. 17, Fig. 18, Fig. 19, Fig. 20.**

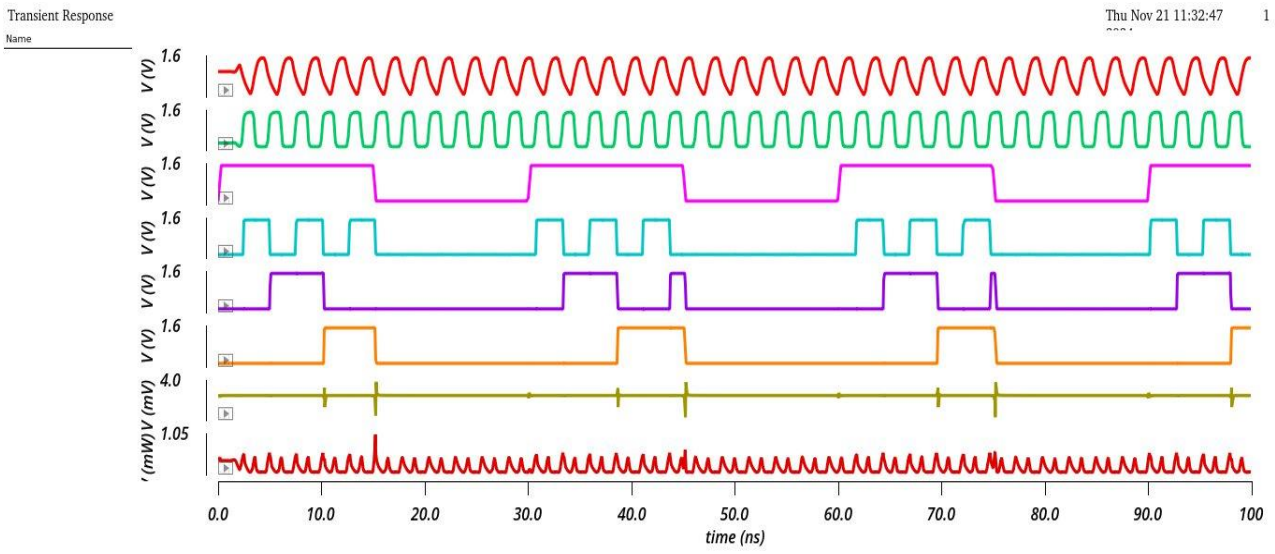

Figure – 17: ADC Waveform (0.4V)

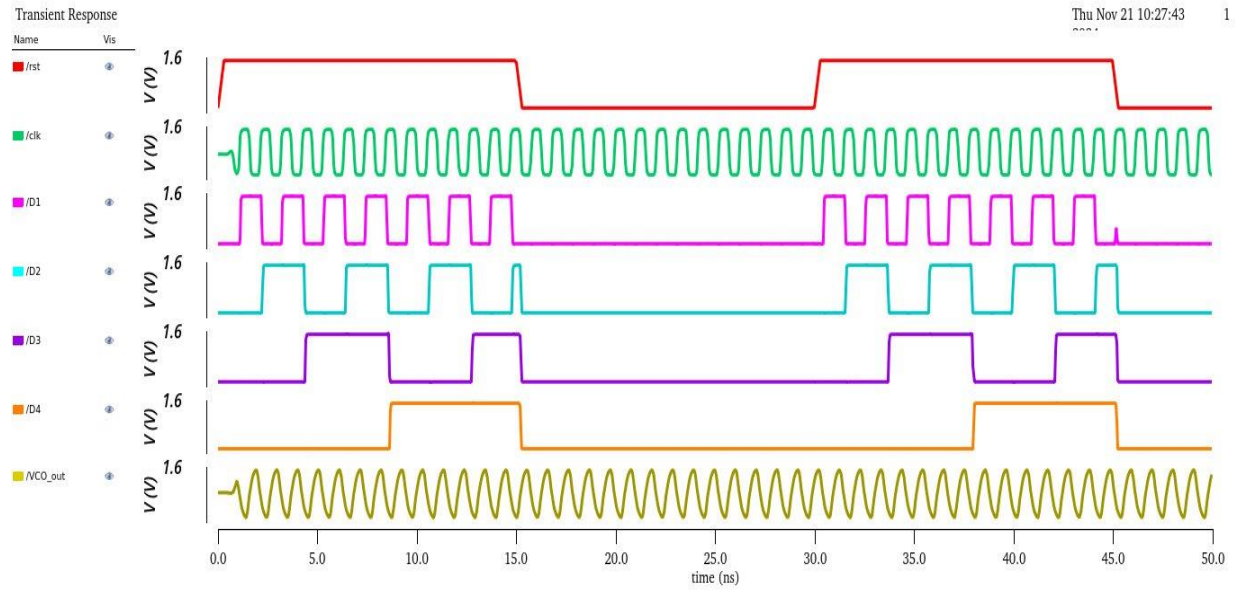

Figure – 18: ADC Waveform (0.6V)

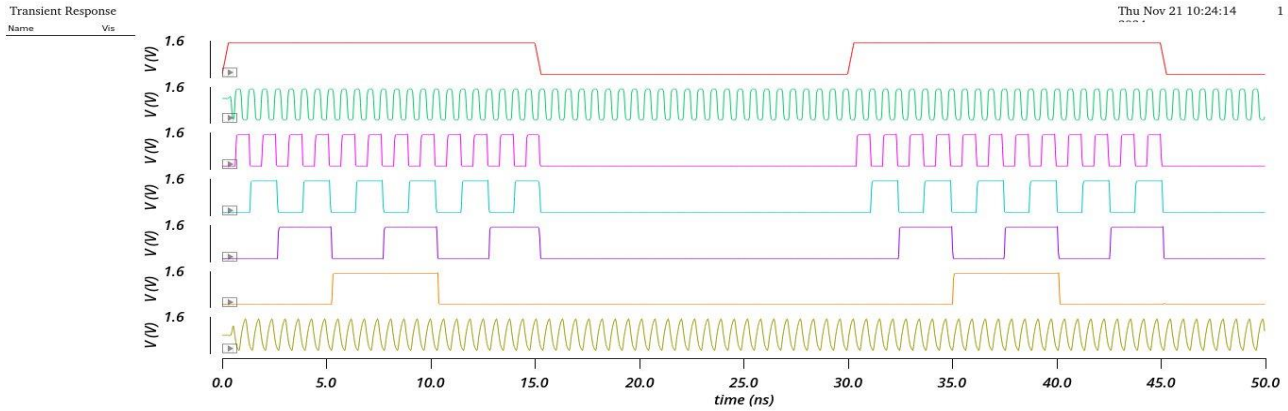

Figure – 19: ADC Waveform (0.8V)

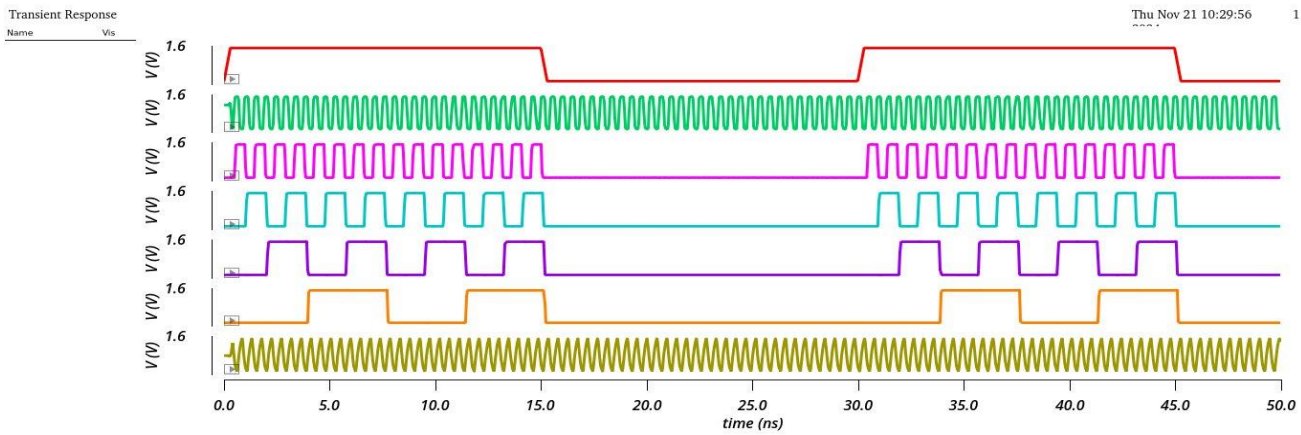

Figure – 20: ADC Waveform (1.0V)

6. ADC AC Response Waveform

The ADC's AC response is analyzed to assess how well it performs over a range of frequencies. The waveform of the ADC's AC response shows the frequency response and indicates how the system responds to different input frequencies, which is critical for evaluating the ADC's performance in real-world applications.

The **ADC AC response waveform** is shown in **Fig. 21**.

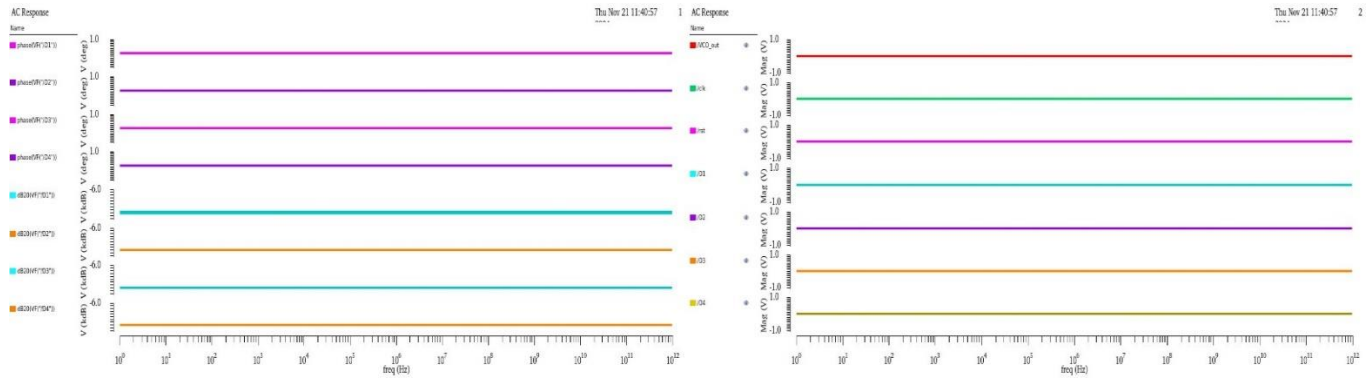

Figure – 21: ADC AC Response Waveform

Power and Corner Analysis:

This section evaluates the **average power consumption** of the ADC system at **0.4V** and analyzes its performance under various process corners: **NN**, **SS**, **SF**, **FF**, and **FS**.

The power consumption increases with higher supply voltages due to faster switching speeds and increased activity in the system.

In the **corner analysis**, we test the ADC under different conditions:

- **NN Corner (Typical-N and Typical-N):** Baseline performance.
- **SS Corner (Slow-S and Slow-S):** Slower transistors, leading to higher power consumption.
- **SF Corner (Slow-S and Fast-N):** Mismatch between transistor speeds, affecting performance.
- **FF Corner (Fast-F and Fast-F):** Faster performance but higher power consumption.
- **FS Corner (Fast-F and Slow-S):** Asymmetric switching, affecting efficiency.

Power consumption for each corner is summarized in **Table 1**, allowing a clear comparison of performance under varying conditions. This analysis is essential for understanding the ADC's robustness and energy efficiency.

Corners	Average Power (Watts)
Tipical Tipical (TT)	193.2 x 10 ^ -6 W
Fast Fast (FF)	275.8 x 10 ^ -6 W
Slow Slow (SS)	124.1 x 10 ^ -6 W

Fast Slow (FS)	220 x 10 ^ -6 W
Slow Fast (SS)	155.7 x 10 ^ -6 W

Table 1: Power at Different Corners

Conclusion:

The analysis of the ADC system demonstrates its performance across different input voltages and process corners. The average power consumption increases with the input voltage, reflecting the higher switching activity and faster operation of the circuit.

The corner analysis provides valuable insights into the ADC's behaviour under various conditions. The minimum power consumption is observed at the SS Corner (Slow-S and Slow-S), where the system operates with slower transistors, leading to reduced power consumption. Specifically, the ADC achieves a minimum power consumption of **124.1×10^{-6} W** at the **SS Corner**, indicating a balance between lower speed and reduced energy usage.

This study highlights the ADC's efficiency and performance under varying conditions, with the SS corner offering the most energy-efficient operation.

Project Demonstration Video:

https://drive.google.com/file/d/17SR_aqkvuM0g6VkGTtgMoOuZekqoNDeY/view?usp=drivesdk

References: IEEE/Springer Format

1. Liu, L., & Lee, H. M. (2010). "A Low-Power CMOS Analog-to-Digital Converter for High-Speed Applications." *IEEE Journal of Solid-State Circuits, 45*(6), 1153-1161.

2. Baker, R. J. (2008). *CMOS: Circuit Design, Layout, and Simulation.* Wiley-IEEE Press.

3. Razavi, B. (2001). *Design of Analog CMOS Integrated Circuits.* McGraw-Hill.

4. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2001). *Analysis and Design of Analog Integrated Circuits.* Wiley.

5. Sze, S. M., & Ng, K. K. (2006). *Physics of Semiconductor Devices* (3rd ed.). Wiley-Interscience.

6. Tee, M. K., & Cheng, K. W. (2013). "A 10-Bit CMOS ADC Using a Voltage-Controlled Oscillator." *IEEE Transactions on Circuits and Systems II: Express Briefs, 60*(7), 447-451.

7. Zhou, Y., & Chen, L. (2015). "A CMOS ADC with Improved Power Efficiency Using a Voltage-to-Frequency Conversion Technique." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 23*(4), 659-668.