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Title of Project:

Design and Implementation of 4-Bit Mealy Machine-based Overlapping Sequence Detector 1001 Using CMOS Logic in 90nm Technology with Corner Analysis on Cadence Virtuoso

Abstract:

This project presents the **design and implementation of two 4-bit overlapping sequence detector** for the binary sequences **"1001"** utilizing **90nm CMOS technology** and simulated using **Cadence Virtuoso**. The detectors are designed based on a **Mealy machine architecture**, which offers the advantage of generating outputs based on both the current state and input, making it ideal for overlapping sequence detection.

The input to each detector is handled through a **Serial In Serial Out (SISO)** register, ensuring sequential data processing. **Master negative-edge triggered D flip-flops** are used for state transitions in the **Finite State Machine (FSM)**, with combinational logic circuits responsible for generating the next state and output based on the input sequence.

The project was implemented and verified through **transistor-level schematic design** using CMOS logic style. Simulations included **DC analysis**, **transient analysis**, and evaluations of **power dissipation** and **delay**. To ensure the design's robustness and adaptability, performance was

tested across three key process corners: **Typical-Typical (TT)**, **Slow-Slow (SS)**, and **Fast-Fast (FF)**. This allowed for a detailed comparison of how variations in manufacturing conditions affect the power, speed, and reliability of the design.

Both detectors exhibited stable operation under varying process corners, demonstrating low power consumption and minimal delay across all cases. This project highlights the effectiveness of using **90nm CMOS technology** in implementing sequence detectors with practical applicability in digital pattern recognition, while offering insights into the impact of different corner analysis on performance parameters such as power and delay.

Introduction:

This project aims to design and implement two **4-bit Mealy machine-based overlapping sequence detectors** for detecting the binary sequences **"1001"** using **90nm CMOS technology** on **Cadence Virtuoso**. The design uses **Serial In Serial Out (SISO)** input and **master negative edge triggered D flip-flops** in a **Finite State Machine (FSM)** architecture. Mealy machines are particularly suited for sequence detectors because the output depends on both the current state and the input, making them effective for detecting overlapping sequences.

1. Circuit Overview:

The sequence detectors are designed to process serial data inputs, detecting the patterns "1001" in an overlapping manner. Each detector is built using:

- **SISO (Serial In Serial Out) input registers**: These allow the sequence to be fed bit by bit, ensuring that each input bit is processed sequentially.
- **Master-Slave D Flip-Flops**: These flip-flops are responsible for holding the current state of the detector. The negative-edge triggering ensures that state transitions occur at the correct clock edge.
- **Combinational Logic Circuits**: These generate the next state and output signals based on the current state and input, following the logic of a Mealy machine.

2. State Diagram:

The state diagram for each sequence detector describes how the system transitions between states as each input bit is processed. For each detector:

1001 Sequence Detector State Diagram:

- **States**: Each state corresponds to how many bits of the "1001" sequence have been detected so far. For example, starting at `S0` (initial state), the FSM transitions through intermediate states (`S1`, `S2`, `S3`, `S4`) based on input bits.
- **Transitions**: The transitions are defined by the input sequence. For instance, from state `S0`, if a '1' is received, the FSM moves to state `S1`; if '0', it stays in `S0`.
- **Overlapping Detection**: After detecting "1001," the FSM moves to a state that accounts for overlapping sequences, allowing for continuous detection.

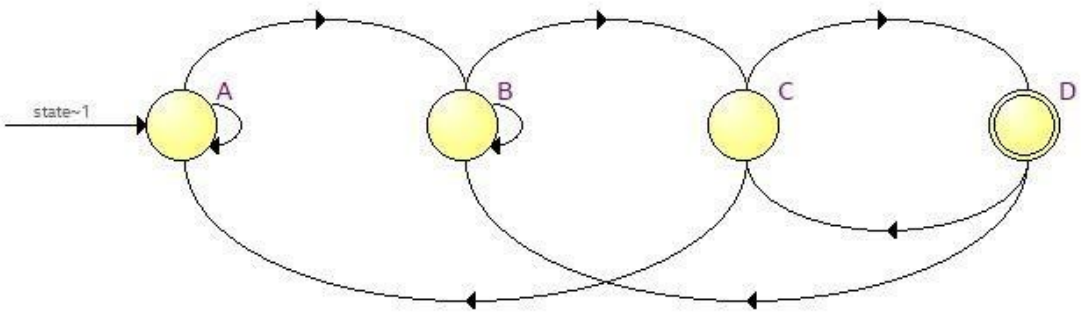

Figure – 1: State Diagram of FSM

3. Truth Table:

The truth table shows the relationship between the current state, input, and output for both sequence detectors. The output is `1` when the desired sequence has been detected.

1001 Sequence Detector Truth Table:

Current State	Input	Next State	Output
S0	1	S1	0
S1	0	S2	0
S2	0	S3	0
S3	1	S4	1
S4	X	S1 (overlap)	0

Figure – 2: Truth Table 4.

Excitation Table:

The excitation table details the inputs required to cause specific transitions between flip-flop states. The D flip-flops use excitation logic to determine the values that must be applied to the D inputs to cause the desired state transitions.

1001 Sequence Detector Excitation Table:

Present State	Next State	D-Input Values
S0	S1	D1 = 1
S1	S2	D2 = 0
S2	S3	D3 = 0
S3	S4	D4 = 1
S4	S1 (overlap)	D1 = 1

Figure – 3: Excitation Table

5. Circuit Diagram:

The circuit design includes the **transistor-level implementation** of both the 1001 sequence detectors. Using CMOS logic, the schematic is optimized for power and performance.

Key Components:

- **SISO Register**: Handles serial input of data for both detectors.

- **Master-Slave D Flip-Flops**: Used for state transitions, triggered on the negative clock edge.
- **Combinational Logic**: Implements Boolean logic functions for next state and output generation.

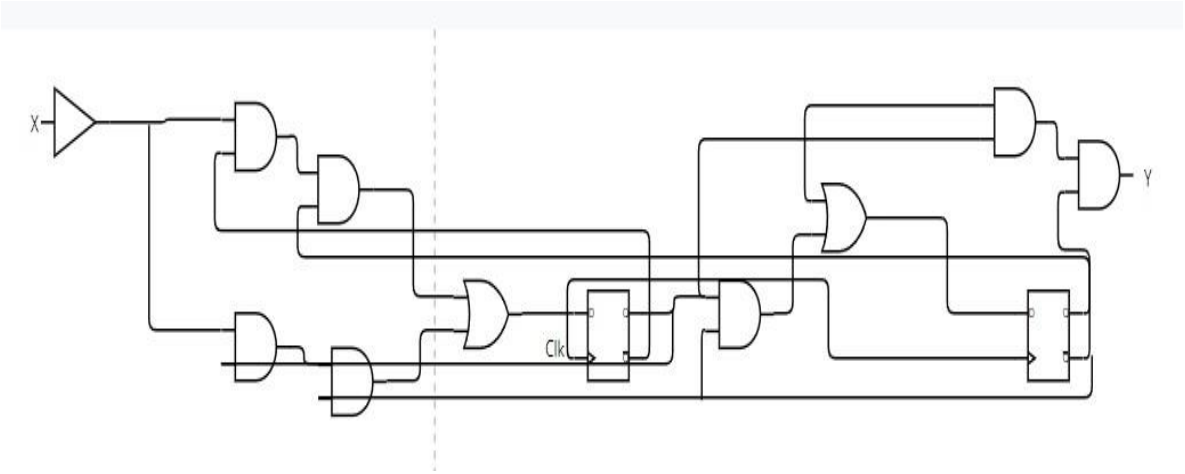

Figure – 4: Logic Diagram

The proposed design implements two **4-bit overlapping sequence detectors** for the sequences **"1001"** using **90nm CMOS technology**. The design follows a **Mealy machine architecture**, which generates the output based on both the current state and the input, making it highly suitable for overlapping sequence detection.

Each detector includes a **Serial In Serial Out (SISO)** register to input the bit sequence, **master slave D flip-flops** for managing state transitions, and **combinational logic** for generating the next state and output. The entire design is implemented using **Cadence Virtuoso**.

1. Schematic at the Transistor Level:

The design is carried out at the **transistor level** using CMOS logic style. The **SISO input**, **D flipflops**, and **combinational logic** are all designed with CMOS transistors to ensure optimal power consumption and performance. The implementation is realized on **Cadence Virtuoso**, which provides precise control over the design and layout.

Key Components:

- **SISO Register**: Allows for the serial input of data, feeding the FSM with each bit of the sequence.

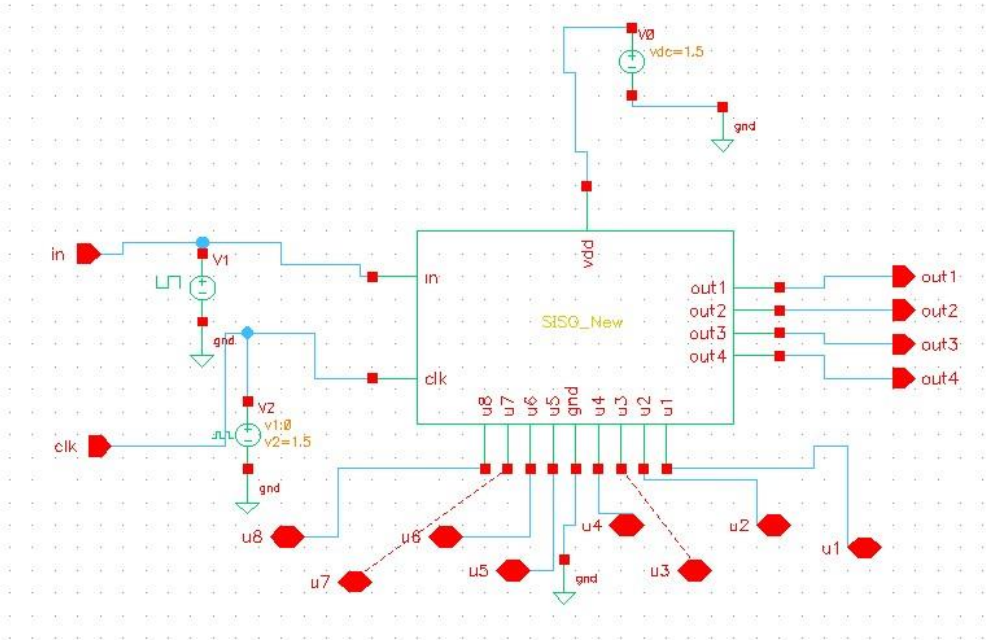

Figure – 5: SISO Symbol

- **Master-Slave D Flip-Flops**: Utilized to hold the current state, triggered on the negative edge of the clock.

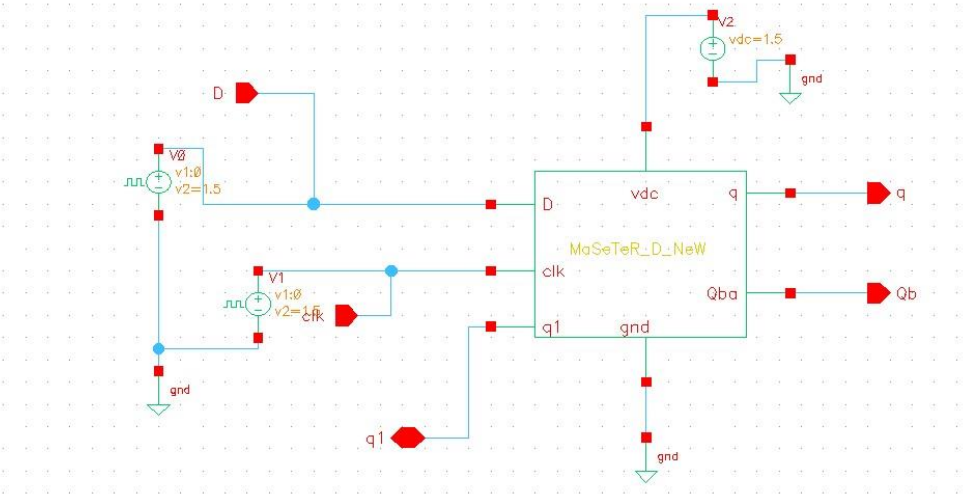

Figure - 6: Master D Flip Flop

- **Combinational Logic**: Responsible for calculating the next state and output based on the input and current state.

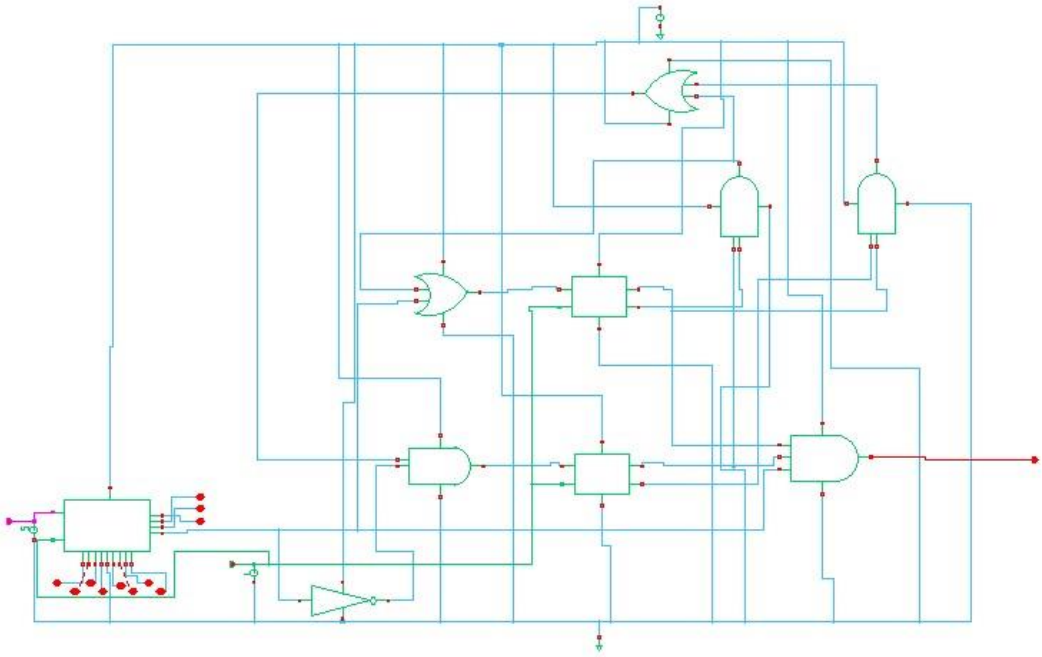

Figure - 7: Sequence Detector

Proposed Design:

2. Logic Styles and Technology Nodes:

The design was implemented using **90nm CMOS technology**, which provides a balance between performance and power consumption. This project evaluates the proposed design under different **technology corners** and explores how the circuit performs under varying process conditions.

90nm CMOS Technology:

The 90nm CMOS process is chosen due to its efficiency in managing both power dissipation and delay, making it ideal for designing fast, low-power digital systems. The following process corners were used to evaluate the design:

- **Typical-Typical (TT)**
- **Slow-Slow (SS)**
- **Fast-Fast (FF)**

Simulation and Implementation in Cadence Virtuoso:

The entire design was created and simulated using **Cadence Virtuoso**. Simulations include:

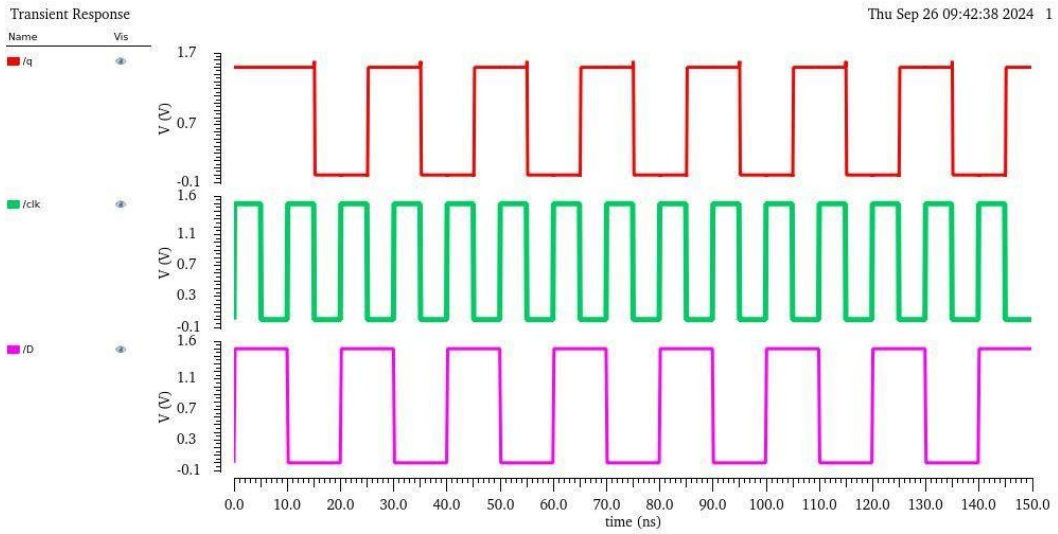

Figure - 8: Output D – Flip Flop

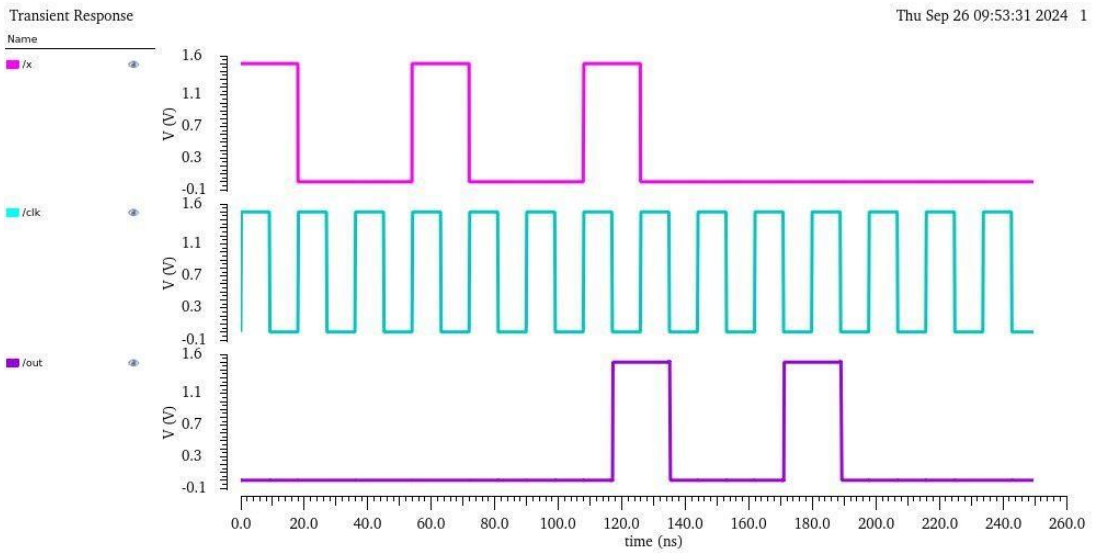

Figure - 9: Output Sequence Detector

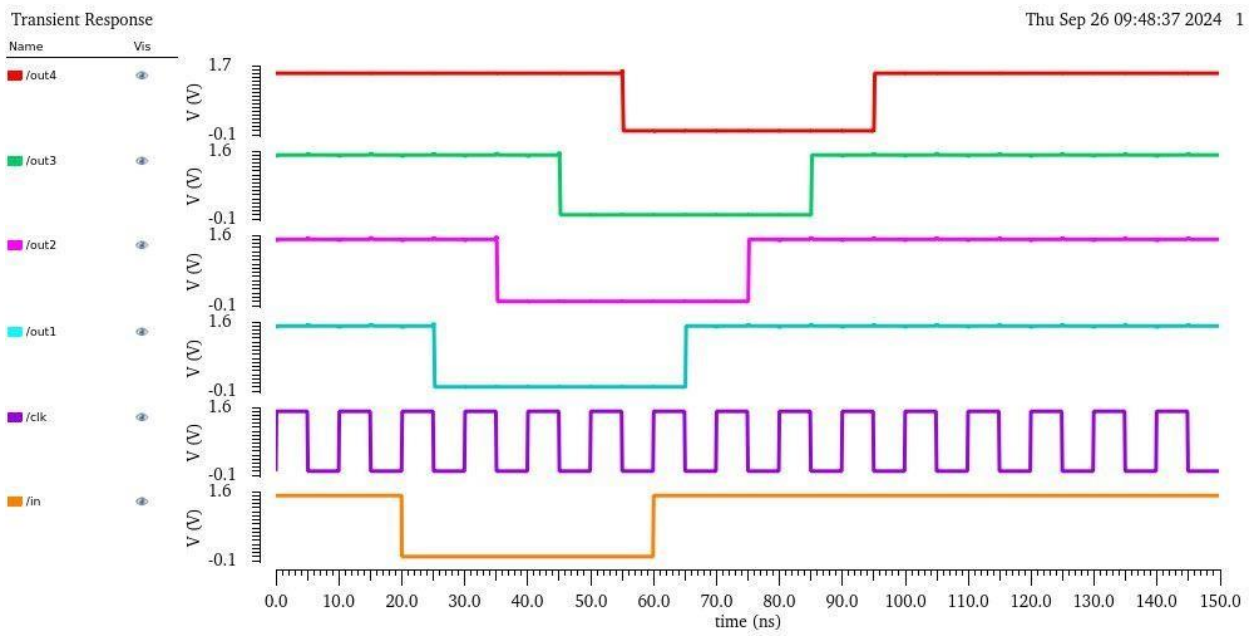

Figure - 10: Output SISO

Results Across Different Corners:

The design was simulated under different process corners (TT, SS, FF) to ensure robustness across varying manufacturing conditions. The results show minimal variation in performance, confirming the reliability of the design.

- **Typical-Typical (TT)**: This corner provides a baseline for normal operating conditions.
- **Slow-Slow (SS)**: Simulates the slowest possible behaviour due to process variations, providing insight into worst-case performance.
- **Fast-Fast (FF)**: Simulates the fastest possible behaviour, testing the design under the most favourable conditions.

Corners	Average Power	Propagation Delay Rise to Fall & Fall to Rise	
Tipical Tipical (TT)	27.46 x 10 ^ -6 W	135.3 x 10 ^ -9 sec	135.2 x 10 ^ -9 sec
Fast Fast (FF)	18.27 x 10 ^ -6 W	9.316 x 10 ^ -9 sec	9.283 x 10 ^ -9 sec

Slow Slow (SS)	41.82 x 10 ^ -6 W	9.047 x 10 ^ -9 sec	9.057 x 10 ^ -9 sec

Conclusion of Proposed Design:

The proposed design successfully implements two 4-bit overlapping sequence detectors using **90nm CMOS technology**. The use of **Cadence Virtuoso** enabled precise transistor-level design and analysis of the circuit. The detectors perform well across all process corners, demonstrating the design's robustness and efficiency.

Project Demonstration Video:

https://drive.google.com/file/d/1xRcUUUf5nxsSa6oS8GedPRmc_syUMDwp/view?usp=drivesk

References: IEEE/Springer Format

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