

	1	2	3	4	5	6						
A	<div>Sheet: UpperPCB</div> <div>Obere Platine: CPU, Terminals, Eingangsverarbeitung Interfaces ADC EEPROM</div> <div>File: OP.sch</div>					A						
B						B						
C	<div>Sheet: LowerPCB</div> <div>Untere Platine Spannungsversorgung Ausgangsverarbeitung DAC</div> <div>File: UP.sch</div>					C						
D	<div>Modifications: M37 Experimental study OP (Upper) and UP (Lower) Board CC BY-NC-SA 2023 C.Niesen, Koenigswinter, Germany</div> <div>Sheet: / File: HomeTeensy40.sch</div> <div>Title: myT40-PLC (PLC with Teensy 4.0)</div> <table><tr><td>Size: A4</td><td>Date: 2023-11-23</td><td>Rev: V2.6 (PFS)</td></tr><tr><td colspan="2">KiCad E.D.A. kicad (5.1.7)-1</td><td>Id: 1/3</td></tr></table>					Size: A4	Date: 2023-11-23	Rev: V2.6 (PFS)	KiCad E.D.A. kicad (5.1.7)-1		Id: 1/3	D
Size: A4	Date: 2023-11-23	Rev: V2.6 (PFS)										
KiCad E.D.A. kicad (5.1.7)-1		Id: 1/3										
	1	2	3	4	5	6						



