

	1	2	3	4	5	6
A	<div>Sheet: UpperPCB</div> <div>Obere Platine: CPU, Terminals, Eingangsverarbeitung Interfaces ADC EEPROM</div> <div>File: OP.sch</div>					A
B						B
C	<div>Sheet: LowerPCB</div> <div>Untere Platine Spannungsversorgung Ausgangsverarbeitung DAC</div> <div>File: UP.sch</div>					C
D	<div>Modifications: M41 Experimental study OP (Upper) and UP (Lower) Board CC BY-NC-SA 2024 <b>C.Niesen, Koenigswinter, Germany</b></div> <div>Sheet: / File: HomeTeensy40.sch</div> <div><b>Title: myT40-PLC (PLC with Teensy 4.0)</b></div> <div><div>Size: A4</div><div>Date: 2024-06-09</div><div>Rev: V2.9 (PFS)</div></div> <div><div>KiCad E.D.A. kicad (5.1.7)-1</div><div>Id: 1/3</div></div>					D
	1	2	3	4	5	6



