1. PROCESSOR

1) clock period: 320ps

time to execute an instruction: 320+275+310+305+250 = 1460ps

2) (1) $6: ID $8:ID (2) $6:MEM $8:EX

2. PIPELINE

1) F级阻塞 stall用N或S表示都对

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
I1: ADDI	F	D	X	M	W																				
I2: ADD		F	D	X	M	W																			
I3: LW			F	D	X	M	W																		
I4: ADD				F	**S**	**S**	D	X	M	W															
I5: LW							F	D	X	M	W														
I6: SUB								F	**S**	**S**	D	X	M	W											
I7:ADDI											F	D	X	M	W										
I8:ADDI												F	D	X	M	W									
I9:ADDI													F	D	X	M	W								
I10:BNE														F	**S**	**S**	D								
I3: LW																	F	**F**	D	X	M	W			
I4: ADD																			F	**S**	**S**	D	X	M	W

D级阻塞 stall用N或S表示都对

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
I1: ADDI	F	D	X	M	W																				
I2: ADD		F	D	X	M	W																			
I3: LW			F	D	X	M	W																		
I4: ADD				F	D	**S**	**S**	X	M	W															
I5: LW					F	**S**	**S**	D	X	M	W														
I6: SUB								F	D	**S**	**S**	X	M	W											
I7:ADDI									F	**S**	**S**	D	X	M	W										
I8:ADDI												F	D	X	M	W									
I9:ADDI													F	D	X	M	W								
I10:BNE														F	D	**S**	**S**								
I3: LW															F	**S**	**S**	**F**	D	X	M	W			
I4: ADD																			F	D	**S**	**S**	X	M	W

2) 2(可忽略)+100*15 = 1502 cycles (1500也对)

CPI = 1502/(2+8*100)=1.873 (若忽略开始2条指令，CPI=1500/800=1.875)

3. CACHE

Address	Split Address			Result	Set 0			Set 1		
	Tag	Index	Offset		Way 0	Way 1	LRU	Way 0	Way 1	LRU
FF	F	1	7	O			0	F		1
F7	F	0	7	O	F		1	F		1
0B	0	1	3	O	F		1	F	0	0
24	2	0	4	O	F	2	0	F	0	0
FB	F	1	3	H	F	2	0	F	0	1
CA	C	1	2	O	F	2	0	F	C	0
08	0	1	0	F/P	F	2	0	0	C	1
F8	F	1	0	F/P	F	2	0	0	F	0
35	3	0	5	O	3	2	1	0	F	0
F7	F	0	7	F/P	3	F	0	0	F	0
32	3	0	2	H	3	F	0	0	F	0

F或P均对，但上下应一致（都为F或都为P）

4. Virtual memory

1) Physical page number：

$$2^{31}/2^{11} = 20$$

2) Tag:

$$2^{32}/2^{11}/2^{4} = 17$$

3) The number of bits required in each entry of a TLB:

1+20+17 = 38

5. Choice

1~5 : C B C D D

6~10 : A D A C A

11~15 : A A D B C

16~20 : D B C D C

6. CACHE DESIGN (10 points) (Additional Questions)

A:

Component	Total (ns)
Decoder	2.4
Memory Array	4
N-to-1 MUX	2
Buffer driver	2
Data output driver	2
Critical Path Dealy	10.4

B:

Read Addresss	Set0		Set1		Set2		Set3		Cache Hit?	Way-Prediction	
	Way0	Way1	Way0	Way1	Way0	Way1	Way0	Way1		Prediction	Correct?
	0	-*	9	-*	A*	6	7	B*			
04									Y	0	Y
68									Y	1	Y
2C					2				N	1	-
B4									Y	0	N
54				5					N	0	-
3C							3		N	0	-
94									Y	1	N
28									Y	0	Y
64									Y	0	N
80		8							N	0	-
64									Y	1	Y
B4									Y	1	Y