浙江大学 2015－2016 学年秋冬学期

《计算机组成与设计》课程期末考试试卷

课程号：67190020，开课学院：信息与电子工程学院

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式：√闭、开卷（请在选定项上打√），

允许带 1 张 A4 大小的手写资料和计算器入场

考试日期：2016 年 1 月 22 日，考试时间：120 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____学号：_____所属院系（专业）：_____

题序	一	二	三	四	五	总 分
得分						
评卷人						

一． **CHOICE** (60 points): (note: only **one** is correct)

1. What is the range of exponent of IEEE 745 single precision? (____)

   A 1~254　　B -128~126　　C -126~127　　D -127~+128

2. You want to maximize the performance of an application with the following characteristics: large number of data structures, low spatial locality, high temporal locality including frequent loads and stores to the same variable, 50% of the memory accesses are stores. Assuming a fixed total cache size, which set of choices below would most likely lead to increased performance. (____)

   A Small block size, High associativity, LRU replacement, Write back, Write allocate

   B Large block size, Low associativity, LRU replacement, Write back, Write allocate

   C Small block size, High associativity, MRU replacement, Write through, No write allocate

   D Large block size, Low associativity, LRU replacement, Write through, Write allocate

3. In a one level cache-memory system, assume that hit rate is 95%, and penalty to access the cache and main memory to be 5ns and 100ns, respectively. We can infer that the average memory access time is (____) ns.

   A (5＋100)/2

   B 100×5%＋5×95%

   C 105×5%＋5×95%

   D 100×95%＋5×5%

4. There are some cell processors following the table. Please choose the combination to get 4.8GHz performance. Make sure it is the smallest number of Watts.(____)

Frequency	2GHz	2.2GHz	2.4GHz	2.6GHz	2.8GHz	4.8GHz
Watts	1W	1W	1W	2W	2W	10W

A 2GHz and 2.8GHz
B 2.2GHz and 2.6GHz
C 2.4GHz and 2.4GHz
D 4.8GHz

5. What is the MIPS assembly code for the binary? ( )
100011 01010 01000 0000010010110000
A lw $t0, 300($t2) B lw $t0, 200($t2)
C lw $t2, 300($t0) D lw $t2, 1200($t0)

6. Use always-taken predictor to predict the ***beq*** instructions. Assume that branch outcomes are determined in the **MEM** stage, there are no data hazards, and that no delay slots are used. The always-taken predictor's accuracy is 60%. The percentage of ***beq*** is 10%. So what is the extra CPI (Cycle per Instructions) due to mispredicted braches. (____)
A 0.04 B 0.08 C 0.12 D 0.16

7. Assume that the following MIPS code is executed on a pipelined processor with a five-stage pipeline, full forwarding, and a predict-taken branch predictor:

```
        add $1, $5, $3

Label1: sw $1, 0($2)

        add $2, $2, $3

        beq $2, $4, label1;  (Not taken)

        add $5, $5, $1

        sw $1, 0($2)
```

If the delay slots are used. In the given code, the instruction that follows the branch is now the delay slot instruction for that branch. Calculate the cycle if we run the whole program. Branches execute in the EX stage. (____)
A 12 B 10 C 11 D 9

8. For a 32-bit cache-memory system, a 32KB, 4-way set-associative cache has 2 words cache line size, how many bits are there in such cache's tag? (____)
A 19 B 21 C 23 D 25

9. Suppose we have made the following measurements ,

Frequency of Instruction A= 25%
Average CPI of Instruction A= 4.0
Average CPI of other instructions = 1.2
Frequency of Instruction B= 2%
Average CPI of Instruction B= 20
If we decrease the CPI of Instruction B to 2, calculate the total CPI. (_____)
A 1.64 B 1.54 C 1.36 D 1.27

10. Given the following MIPS assembly code (and assuming all registers start at 0):

```
        addi $1, $0, 10

        add $2, $1, $1

repeat: addi $2, $2, -4

        add $3, $2, $2

        addi $1, $1, -2

        bne $0, $1, repeat
```

What is the final value of $3? (____)
A 0 B -8 C 8 D 4

11. Assume the current PC is 0x10000010, what's next value of PC after execution of "j 254"? (___)
A 0x00000FE B 0x10000FE C 0x00003F8 D 0x100003F8

12. The following commands were used to store the contents of registers $s0 and $s1 onto the stack:

```
addi $sp, $sp, -8

sw $s0, 0($sp)

sw $s1, 4($sp)

# insert various unrelated instructions here
```

Assuming that neither the stack pointer nor the stack has been changed during the "various unrelated instructions" part, which of the following would allow you to recover the contents of $s0 and $s1 while returning $sp to its original (pre-decremented) value? (____)
A addi $sp, $sp, 8; lw $s0, 4($sp); lw $s1, 0($sp)
B addi $sp, $sp, 8; lw $s0, 0($sp); lw $s1, 4($sp)
C lw $s0, 4($sp); lw $s1, 0($sp); addi $sp, $sp, 8
D lw $s0, 0($sp); lw $s1, 4($sp); addi $sp, $sp, 8

13. Which of the following instructions could this single-cycle datapath description be referring to? (___)

    Description : Two source registers (ReadReg) and one destination register (WriteReg) are selected, and the values are read from the source registers and sent as input to the ALU. The ALU operation is performed, the result is written to the destination register, and the PC is updated.

    A add B ori C li D sll

14. Consider a workload with 30% branches and a 66.66% branch prediction accuracy (33.33% misprediction rate). You may ignore memory operations. For a simple five-stage pipeline, what is the CPI of this workload assuming a three-cycle misprediction penalty and a single-cycle latency for all other instructions? Calculate under what condition a much deeper pipeline with double the core clock frequency will outperform the shallower pipeline? (____)

    A 10 B 13 C 16 D 30

15. For the following memory access pattern: 1, 5, 1, 6, 3, what's the content of a 4-entry, direct-mapped cache, assuming cache is vacant at the beginning. (____)

A

	1	6	3

B

1	6	3	5

C

5	6	3	

D

	6	3	

16. Increasing associativity can reduce (____).

    A Compulsory misses (cold-start misses)

    B Capacity misses

    C Conflict misses (collision misses)

    D All three misses

17. Which of the following is generally true about a design with two levels of caches? (____)

    A First-level caches are more concerned about hit time, and second-level caches are more concerned about miss rate.

    B First-level caches are more concerned about miss rate, and second-level caches are more concerned about hit time.

    C Second-level caches often use lower associativity than first-level caches given the focus of reducing miss rates.

    D Second-level caches are as fast as first-level caches.

18. Consider a virtual memory system with 32-bit virtual byte address, 4KB/page, 32 bits each entry. The physical memory is 512MB. Then, the total size of page table needs (____).

A 1MB B about 3MB C 4MB D 8MB

19. Here is a series of address references given as word addresses:
2, 3, 11, 16, 21, 13, 64, 48, 19, 11, 3, 22, 4, 27, 6, 11.
Determine how many misses will happen in this condition: A two-way set-associative cache with four-word blocks and a total size of 16 words. Use LRU replacement. (____)
A 7 B 8 C 13 D 15

20. A certain government agency simultaneously monitors 100 cellular phone conversations and multiplexes the data onto a network with a bandwidth of 1 MB/sec and an overhead latency of 350 micro-sec per 1-KB message. Calculate the transmission time per message. Assume that the phone conversation data consists of 2 bytes sampled at a rate of 4 KHz. (____)
A 0.8s B 1.35s C 1s D 1.08s

二. **TRUE (T) OR FALSE (F)** (10 points)

1. All other things equal, direct mapped caches have a lower tag overhead than fully associative caches. [ ]
2. On every store instruction, a write back cache will write to main memory.[ ]
3. Superscalar processors can reduce CPI below 1.0 by employing multiple pipelines.[ ]
4. Bigger cache blocks always lead to a higher hit rate.[ ]
5. Pipeline designs improve CPI over multi-cycle designs by overlapping the execution of multiple instructions. [ ]

三. **PIPELINE** (9 points)

Problems refer to the following instruction sequences:

```
I1   add $1 , $2, $3

I2   sw   $2, 0($1)

I3   lw   $1 , 4($2)

I4   add $2 , $2, $1
```

The basic pipeline is following the Figure.1. Please use it to solve the Q1 and Q2

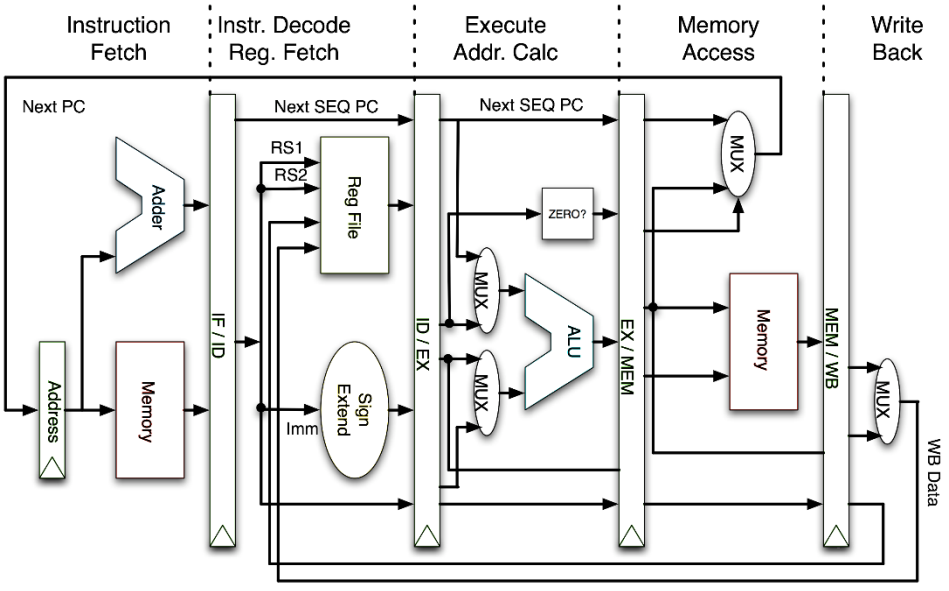

Figure.1 Basic Pipeline

Please use Figure.2 to solve the Q3.

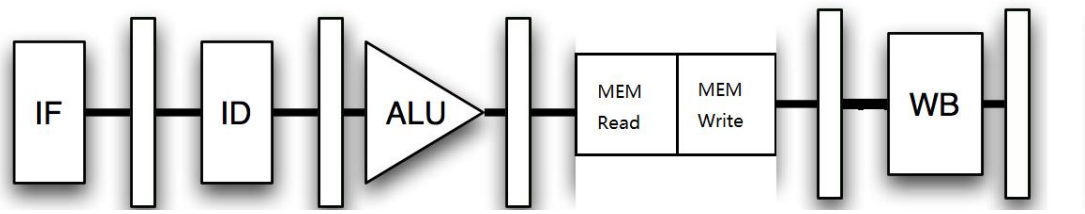

Figure.2 6-stage pipeline

1. Find all data dependences in this instruction sequence.

WAR	RAW	WAW
e.g. ($2) I1 to I4		

2. Find all hazards in this instruction sequence for a 5-stage pipeline without forwarding. Please specify the instructions, like ($2) I1 to I4.

Hazards

3. To reduce clock cycle time, we are considering a split of the MEM stage into two stages. Repeat Q.2 for this 6-stage pipeline. Please specify the instructions, like ($2) I1 to I4.

Hazards

The remaining two problems in this exercise assume that, before any of the above is executed, all values in data memory are zeroes and that registers R0 through R3 have the following initial values:

$0	$1	$2	$3
0	1	31	1000

4. Which value is the first one to be forwarded and what is the value it overrides?

First one to be forward	Overrides value

5. If we assume forwarding will be implemented when we design the hazard detection unit, but then we forget to actually implement forwarding, what are the final register values after this instruction sequence?

$0	$1	$2	$3

四. **CACHE** (12 points)

Consider a processor whose ISA uses 16-bit addresses and byte-granularity addressing (each address specifies a byte in memory). The processor has a direct-mapped 16KB cache with 16-byte cache blocks. The cache is initially empty (all blocks invalid). As a reminder, for such a cache the 16-bit address is divided into a 2-bit tag, a 10-bit index, and a 4-bit offset.

1. Consider a short (two-instruction) program that loads from the following two addresses. The cache starts empty, so the first load will always miss. However, will the second load hit or miss in the cache? (chose the correct answer)

   Load from address: 0010 1010 0111 1000 (miss)

   Load from address: 0010 1010 0101 1010 A hit B miss

2. Now assume the processor's cache has 4096-byte blocks (but the size of the cache is unchanged). Will the second load hit or miss in the cache? (chose the correct answer)

   Load from address: 0010 1010 0111 1000 (miss)

   Load from address: 0010 1010 0101 1010 A hit B miss

3. What program property is responsible for the decrease in miss rate?

4. Consider a different program that loads from the following three addresses. As before, the cache starts empty, so the first load will always miss. However, will the second and third loads hit or miss in the cache with 16-byte blocks? (chose the correct answer)

   Load from address: 0010 1010 0111 1000 (miss)

   Load from address: 1010 1100 0101 1110 A hit B miss

   Load from address: 0010 1010 0101 1010 A hit B miss

5. Now assume the processor's cache has 256-byte blocks, but the size of the cache is unchanged. (chose the correct answer)

   Load from address: 0010 1010 0111 1000 (miss)

   Load from address: 1010 1100 0101 1110 A hit B miss

   Load from address: 0010 1010 0101 1010 A hit B miss

6. What hardware phenomenon is responsible for the increase in miss rate?

7. Other than adjusting the block size, what is the most reasonable way to change the cache hardware to remedy this degradation in miss rate?

五．**VIRTUAL MEMORY** (9 points)

Suppose that a system has a 32-bit (4GB) virtual address space. It has 1GB of physical memory, and uses 1MB pages.

1. How many bits are there in the page offset?

2. How many virtual pages are there in the address space?

3. How many physical pages are there in the address space?

4. How many bits are there in the virtual page number?

5. How many bits are there in the physical page number?

Entry Number	Value
0	1F
1	3C
2	55
3	9C
4	DD
5	EE
6	99
…	…
20	2F
21	4C
22	65
23	AC
24	ED
25	FE
26	100
…	…
40	11F
41	13C
42	155
43	19C
44	1DD
45	1EE
46	199
…	…

6. Some entries of the page table are shown to the right (all values are in hex, and all entries shown are valid).Translate virtual address 0x410423 to a physical address, using the translations in this page table.