浙江大学 2018－2019 学年秋冬学期

《计算机组成与设计》课程期末考试试卷

课程号： 67190020 ，开课学院： 信息与电子工程学院

考试试卷： √A 卷、B 卷（请在选定项上打 √）

考试形式： √闭、开卷（请在选定项上打 √），

允许带 1 张 A4 大小的手写资料和计算器入场

考试日期： 2019 年 1 月 25 日，考试时间： 120 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：_____学号：_____所属院系（专业）：_____

题序	一	二	三	四	五	六	七	八	总 分
得分									
评卷人									

I. CHOICE (60 points)

1. Which number representation can be used to represents a negative number? (_____) D

A. Two's Complement

B. One's Complement

C. Signed Magnitude

D. All of above

2. Suppose we have made the following measurements ,

Frequency of Instruction A= 25%

Average CPI (clock cycles per instruction) of Instruction A= 4.0

Average CPI of other instructions = 1.2

Frequency of Instruction B= 2%

Average CPI of Instruction B= 20

If we decrease the CPI of Instruction B to 7, calculate the total CPI. (_____) A

A. 1.64

B. 1.54

C. 1.36

D. None of the above.

3. Two processors A and B have clock frequencies of 700 MHz and 900 MHz, respectively. Suppose A can execute an instruction with an average of three steps and B can execute with an average of five steps. For the execution of the same instruction which processor is faster? (_____) A

A. A

B. B

C. Both take the same time

D. Insufficient information

4. The MIPS addressing mode of "j 254" is (_____). B

A. Immediate addressing

B. Pseudodirect addressing

C. PC-relative addressing

D. None of the above.

5. The L1 cache on a high-end processor is most likely to use which technology? (_____) C

A. flash

B. magnetic disk

C. SRAM

D. DRAM

6. Pipelining a processor implementation probably won't do which of the following: (_____) A

A. decrease latency

B. increase throughput

C. allow a faster clock rate

D. all of the above probably will happen

7. What is an advantage of increasing the number of pipelines? (_____) C

A. Less complex circuit

B. Faster computation on a whole instruction

C. Faster clock speed

D. Increased clock period

8. The execution of the following two instructions may have the (_____) hazard. C

```
lw  R3,0(R2)
lw  R2,0(R1)
```

A. RAW (Read after Write)

B. WAW (Write after Write)

C. WAR (Write after Read)

D. No hazards

9. The main purpose of having memory hierarchy is to (_____). D

A. Reduce access time

B. Provide large capacity

C. Reduce propagation time

D. Reduce access time & provide large capacity

10. Suppose you have a cache with capacity of 2^{15} bytes, with 32-byte blocks. Assume 8 bits are used to select the set. What is the associativity of the cache? (_____) C

A. The cache is direct-mapped.

B. The cache is two-way set associative.

C. The cache is four-way set associative.

D. None of the above.

11. You have a cache with 8B blocks, and a total size of 64B. However, you forgot the associativity! Given this sequence of accesses on word-addressed memory (4B), what is the associativity? **(_____)** C

0 (MISS), 1 (HIT), 2 (MISS), 15 (MISS), 17 (MISS), 0 (HIT), 32 (MISS), 1 (MISS)

A. Fully associative (8-way)
B. 4-way
C. 2-way
D. Direct-mapped

12. You have two caches:

- Direct mapped (DM) cache: 2 tag bits, 1 index bit, 1 offset bit
- 2-way set associative (SA) cache: 3 tag bits, 0 index bits, 1 offset bit.

Assume MRU (most recently used) replacement policy. Calculate the miss rate on the following sequence of accesses: 0, 1, 2, 5, 3. (_____) A

A. DM: 0.6 SA: 0.8
B. DM: 1 SA: 0.6
C. DM: 0.4 SA: 0.4
D. DM: 0.6 SA: 1

13. For a 32-bit cache-memory system, a 16KB, 4-way set-associative cache has 4 words cache line size, how many bits are there in such cache's tag? **(_____)** A

A. 20
B. 21
C. 22
D. None of the above.

14. If a system is 64-bit machine, then the length of each word will be **(_____).** B

A. 4 bytes
B. 8 bytes
C. 16 bytes
D. 12 bytes

15. Increasing associativity can reduce **(_____).** C

A. Compulsory misses (cold-start misses)
B. Capacity misses
C. Conflict misses (collision misses)
D. All three misses

16. Which of the following situation will not happen? **(_____)** D

A. TLB (Translation-lookaside Buffer) miss, Cache hit, Page hit
B. TLB miss, Cache miss, Page hit
C. TLB miss, Cache miss, Page miss
D. TLB hit, Cache miss, Page miss

17. If we want to construct a PTE (Page Table Entry) where there are flags for Writable, Valid, and Dirty. And we have a total of 1 TB space in Main Memory. Each page also has the size of 8 KB, what is the minimum number of bits we need to fill up the PTE? **(_____)** B

A. 28 bits
B. 30 bits
C. 32 bits
D. 33 bits

18. What is the decimal of the binary real number 10.11×2^{-1}? **(_____)** D

A. 1.5
B. 2.75
C. 2.625
D. 1.375

19. Two's complement in 8 bits for -128 is **(_____)**. B

A. 0100 0000
B. 1000 0000
C. 0000 0000
D. Overflow

20. The unit which acts as an intermediate agent between memory and backing store to reduce process time is **(_____).** D

A. TLB's
B. Registers
C. Page tables
D. Cache

II. TRUE OR FALSE (10 points)

1. _ T _In 8-bit two's complement numbers, the negative of 10101101 (binary) is 01010011.
2. _ T _The physical memory is not as large as the address space spanned by the processor.
3. _ T _Both multithreading and multicore rely on parallelism to get more efficiency from a chip.
4. _ T _The directly mapped cache no replacement algorithm is required.
5. _ T _Multiple levels of page tables can also be used to reduce the total amount of page table storage.
6. _ F _To help the operating system estimate the LRU pages, some computers provide a dirty bit, which is set whenever a page is accessed.
7. _ F _In virtual memory, the number of entries of a page table is equals to the physical page number.
8. _ F _The starting address of the page table is stored in TLB.
9. _ F _Write-through: A scheme that handles writes by updating values only to the block in the cache, then writing the modified block to the lower level of the hierarchy when the block is replaced.
10. _ F _For L2 cache, reducing hit time is as important as reducing miss rate.

III. PIPELINE (10 points)

Consider the standard MIPS 5 stage pipeline. The bypass is allowed, including the bypass from MEM stage. The register write to the register file is executed in the first half of the clock cycle, and the register read from the register file is executed in the second half of the clock cycle. For your reference, refer to the figure in page 6. For this question, we will use the following code to evaluate the pipeline's performance:

```
1   add     $t2, $s1, $sp
2   lw      $t1, $t1, 0
3   addi    $t2, $t1, 7
4   add     $t1, $s2, $sp
5   lw      $t1, $t1, 0
6   addi    $t1, $t1, 9
7   sub     $t1, $t1, $t2
```

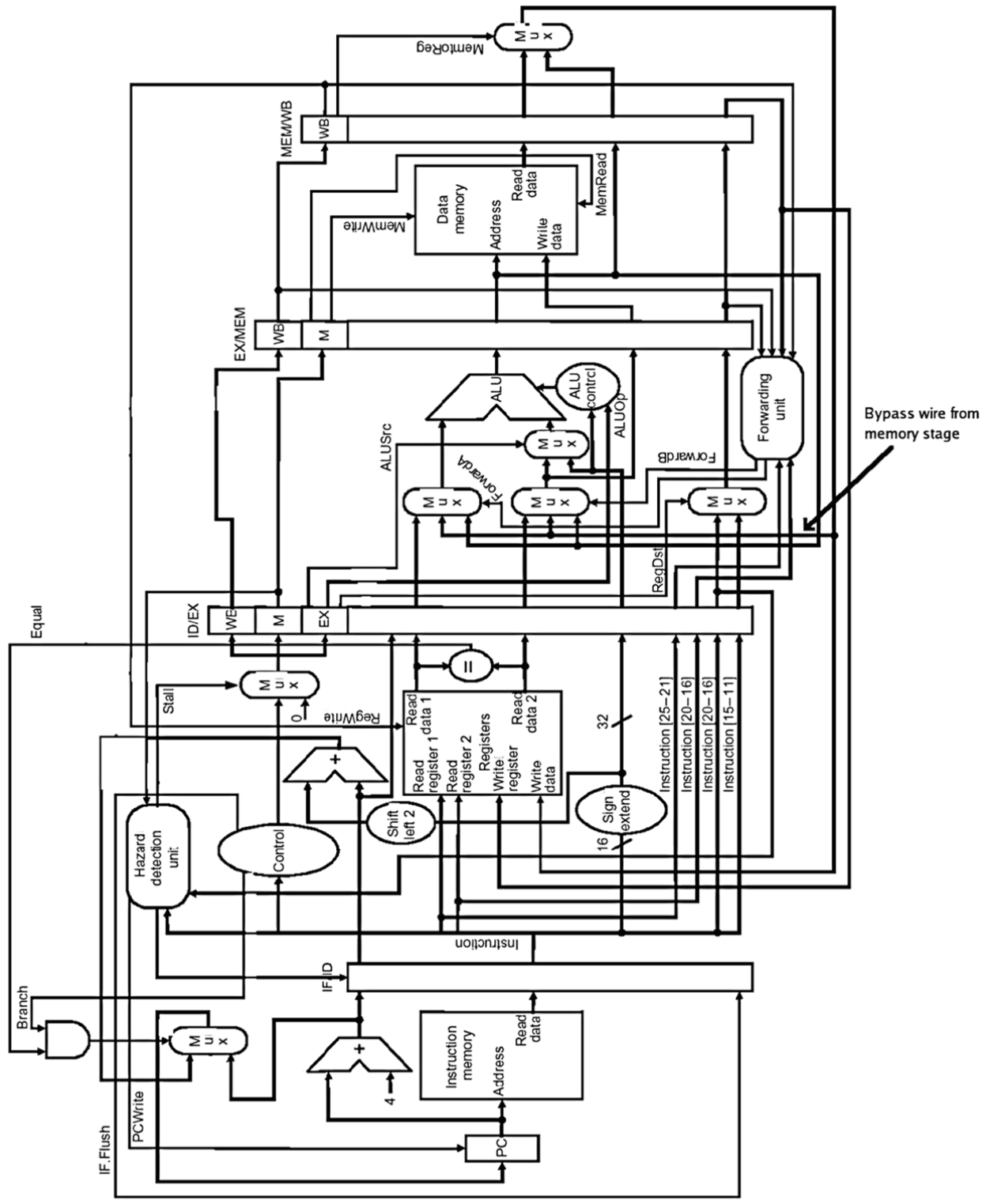
Using the standard MIPS pipeline, identify whether the value for each register operand is coming from the bypass or from the register file. For clarity, please write **REG or BYPASS** in each box.

Instruction	**Src Operand 1**	**Src Operand 2**
1		
2		**N/A**
3		**N/A**
4		
5		**N/A**
6		**N/A**
7		

Solution:

Instruction	Src Operand 1	Src Operand 2
1	Register File	Register File
2	Register File	N/A
3	Bypass	N/A
4	Register File	Register File
5	Bypass	N/A
6	Bypass	N/A
7	Bypass	Register File

(each blank 1 point)


MemtoReg
MEM/WB
WB
Data memory
Address
Read data
Write data
MemRead
MemWrite
EX/MEM
WB
M
ALU
ALU control
ALUOp
ALUSrc
Forward A
Forward B
Forwarding unit
Bypass wire from memory stage
RegDst
ID/EX
WB
M
EX
Equal
Stall
RegWrite
Registers
Read register 1
Read register 2
Write register
Read data 1
Read data 2
Write data
32
Instruction [25–21]
Instruction [20–16]
Instruction [20–16]
Instruction [15–11]
Sign extend
16
Shift left 2
Hazard detection unit
Control
Instruction
IF/ID
Branch
Instruction memory
Address
Read data
4
PCWrite
IF.Flush
PC

IV. CACHE (12 points)

Consider a computer with an 8-bit address space and a direct-mapped 64-byte data cache containing 16-byte cache blocks.

1. How many sets are in the cache?

2. The table below shows a trace of addresses accessed by the processor. Assume the cache is initially empty. For each access, please **indicate whether it hits or misses.**

Hex Address	Binary Address	Hit/Miss
00	00000000	
20	00100000	
0A	00001010	
86	10000110	
06	00000110	
F1	11110001	
33	00110011	
70	01110000	
01	00000001	
7A	01111010	

Solution:

1. 4 (2 points)

2.

Hex Address	Binary Address	Hit/Miss
00	00000000	M
20	00100000	M
0A	00001010	H
86	10000110	M
06	00000110	M
F1	11110001	M
33	00110011	M
70	01110000	M
01	00000001	H
7A	01111010	H

(each blank 1 point)

V. VIRTUAL MEMORY (8 points)

Assume a system that has:

- A two-way set associate TLB
- A TLB with 8 entries total
- 2^8-byte page size
- 2^{16} bytes of virtual memory

TLB

Index	Tag	Frame Number	Valid
0	0x27	0xC6	1
0	0x29	0x73	1
1	0x11	0xFF	0
1	0x0A	0xEC	1
2	0x29	0xCD	1
2	0x3A	0xAB	1
3	0x32	0xFB	0
3	0x23	0x46	0

According to the TLB to fill in the table. Strike out anything that you don't have enough information to fill in. If you don't have enough information to fill the blank, fill the blank with "/".

Virtual Address	Physical Address
0xA601	
0x8F0F	
0x2933	
0x2839	

Solution:

Virtual Address	Physical Address
0xA601	0xCD01
0x8F0F	/
0x2933	0xEC33
0x2839	/

(each blank 2 points)