浙江大学 2019－2020 学年秋冬学期

《计算机组成与设计》课程期末考试试卷

课程号： 67190020 ，开课学院： 信息与电子工程学院

考试试卷：√A 卷、B 卷（请在选定项上打√）

考试形式：√闭、开卷（请在选定项上打√），

允许带 1 张 A4 大小的手写资料和计算器入场

考试日期： 2020 年 1 月 12 日，考试时间： 120 分钟

诚信考试，沉着应考，杜绝违纪。

考生姓名：____________学号：____________所属院系（专业）：______________

题序	一	二	三	四	五	六	七	八	总 分
得分									
评卷人									

I. CHOICE (Only one correct answer, 60 points)

1. Compute the average CPI (Clock cycle Per Instruction) of the following instructions. (_______)

B

Instruction type	CPI	Frequency
ALU	1	50%
Branch	2	20%
Load	2	20%
Store	2	10%

A. 1.0

B. 1.5

C. 2.0

D. 2.5

2. What is the content of stack pointer (SP)? (_______) C

A. address of the current instruction

B. address of the next instruction

C. address of the top element of the stack

D. size of the stack

3. What is the function of the compiler? (_______) D

A. Translates assembly language into binary instructions.

B. Translates source code into intermediates and immediately executes it.

C. Combines independent programs and resolves labels into an executable file.

D. Translate a high-level language into assembly language.

4. The bit used to signify that the cache location is updated is **(________)**. A

A. Dirty bit

B. Update bit

C. Reference bit

D. Flag bit

5. Interrupts can be generated in response to **(________)**. D

A. detected program errors such as arithmetic overflow or division by zero

B. detected hardware faults

C. input/output activities

D. All of the above.

6. Write Through technique is used in which memory for updating the data? **(________)** D

A. Virtual memory

B. Main memory

C. Auxiliary memory

D. Cache memory

7. The execution of the following two instructions may have the **(________)**. A

```
lw   x5,0(x6)
lw   x7,0(x5)
```

A. RAW (Read after Write)

B. WAW (Write after Write)

C. WAR (Write after Read)

D. No data dependency.

8. Forwarding is a technique used in a pipeline to reduce the number of stall cycles caused by hazards. Each sequence of instructions shown below causes a hazard for the version of the RISC-V pipeline that we studied in class. The pipeline bubble that would be caused by some of these hazards can be avoided through the use of forwarding. Others cannot. Mark the sequences for which the bubble cannot be avoided through forwarding. **(________)** D

A. lw x5, 0(x6)
   sll x9, x10, x11
   add x7, x8, x5

B. add x7, x8, x9
   beq x7, x0, L2

C. sub x5, x6, x7
   add x8, x9, x5

D. lw x5, 0(x6)
   add x7, x8, x5

9. The RISC-V addressing mode of "jal x1, 100" is (_______). C

A. Immediate addressing
B. Base addressing
C. PC-relative addressing
D. None of the above.

10. Which type of parallel computing architecture is no longer commonly encountered in machines today? (_______) B

A. MIMD (Multiple Instruction/Multiple Data Stream)
B. MISD (Multiple Instruction/Single Data Stream)
C. SIMD (Single Instruction/Multiple Data Stream)
D. SISD (Single Instruction/Single Data Stream)

11. Calculate AMAT (Average Memory Access Time) for a machine with the following specs: L1 hits take 3 cycles, L1 local miss rate is 25%. L2 hits take 10 cycles, L2 local miss rate is 60%. L3 hits take 100 cycles, L3 global miss rate is 9%. Main memory accesses take 1000 cycles and all data is available in memory. (_______) B 3+0.25*(10+0.6*(100+0.6*1000))

A. 105.5 cycles
B. 110.5 cycles
C. 24.5 cycles
D. None of the above.

12. Suppose you have a cache with capacity of 2^{15} bytes, with 32-byte blocks. Assume the cache is two-way set associative. How many bits are used to select the set? (_______) A

A. 9 bits
B. 8 bits
C. 7 bits
D. None of the above.

13. You have a cache with 8B blocks, and a total size of 64B. The cache is two-way set associative. Use a least-recently used replacement policy. Given this sequence of accesses on word-addressed memory (4B), what is the hit rate? (_______) C

0 (MISS), 1 (HIT), 2 (MISS), 15 (MISS), 17 (MISS), 0 (HIT), 32 (MISS), 1 (HIT)

0, 1, 2, 15, 17, 0, 32, 1

A. 12.5%
B. 25.0%
C. 37.5%
D. None of the above.

14. For a computer with an 8-bit address space, a 64-byte, 2-way set-associative cache has 4B cache line size. How many bits are there in such cache's tag? (_______) B

A. 2
B. 3
C. 5

D. None of the above.

15. The drawback of building a large memory with DRAM (Dynamic Random Access Memory) is **(________).** C

A. The large cost factor

B. The inefficient memory organization

C. The Slow speed of operation

D. All of the mentioned

16. What is the decimal of the binary real number 10.01×2^{-1}? **(________)** A

A. 1.125

B. 2.75

C. 2.625

D. 1.375

17. What is the RISC-V assembly code for the binary? **(________)** A

00100100011000111010110000100011

A. sw t1, 600(t2)

B. sw t1, 1200(t2)

C. sw t2, 600(t1)

D. sw t2, 1200(t1)

18. The effectiveness of the cache memory is based on the property of **(________).** A

A. Locality of reference

B. Memory localization

C. Memory size

D. None of the mentioned

19. An L2 cache, out of 100 total accesses to the cache system, missed 20 times. If L1 cache had a miss rate of 50%, what is the local miss rate of L2 cache? **(________)** D

A. 20%

B. 30%

C. 35%

D. 40%

20. Virtual memory uses a page table to track the mapping of virtual addresses to physical addresses. Assume 4 KiB pages, 32-bit virtual address. A cache designer wants to design a virtually indexed, physically tagged cache. To make an 8 KiB cache, assuming 4 words per block. What is the associativity? **(________)** BC

A. The cache is direct-mapped.

B. The cache is two-way set associative.

C. The cache is four-way set associative.

D. None of the above.

II. TRUE OR FALSE (10 points)

1. _ F _Multiple levels of page tables will increase the total amount of page table storage.
2. _ T _Static RAM is typically used to implement Cache.
3. _ F _First-level caches are more concerned about miss rate, and second-level caches are more concerned about hit time.
4. _ T _Two's complement in 8 bits for -128 is 1000 0000.
5. _ T _When meeting cache misses, “no write allocate” means only writing to main memory.
6. _ T _Pipelining a processor implementation probably will increase throughput.
7. _ F _If hit rates are well below 0.9, then they’re called as speedy computers.
8. _ T _Assume two cache designs C_A and C_B have the same block size. C_A is a 32 KiB 2-way set associative cache and C_B is a 16 KiB direct-mapped cache. The length of the tag, measured in the number of bits, is the same in C_A and in C_B.
9. _ F _Each stage in pipelining should be completed within 5 cycles.
10. _ T _If a data cache does not contain a dirty bit, then it must be using a write-through policy.

III. CACHE (8 points)

The contents of an associative cache are shown below. This cache has four-byte blocks and 32-bit addresses. Tags and sets are shown in binary, and data values in hex. The “…” should be replaced by an appropriate number of 0’s.

Set	V	Tag	0	1	2	3	
0	1	11110…011110000	0x44	0x33	0x22	0x11	Line A
	1	10000…010110010	0xAA	0xBB	0xCC	0xDD	Line B
1	1	10000…011110000	0x01	0x02	0x03	0x04	Line C
	1	10000…010000000	0x12	0xAB	0x34	0xEF	Line D

What are the addresses that are cached in each block? Write the range in hexadecimal using all eight digits, e.g. 0x00000000-0x000000AC.

Line A: ____

Line B: ____

Line C: ____

Line D: ____

Solution:

Line A: 0xF0000780 0xF0000781 0xF0000782 0xF0000783

Line B: 0x80000590 0x80000591 0x80000592 0x80000593

Line C: 0x80000784 0x80000785 0x80000786 0x80000787

Line D: 0x80000404 0x80000405 0x80000406 0x80000407

(2 points for each line)

IV. PIPELINE (12 points)

Data hazards occur due to data dependencies among instructions. Forwarding (aka bypassing) can solve many data hazards. We assume that the write is in the first half of the clock cycle and the read is in the second half.

1. Given the RV32I code below, spot the data dependencies in the code below. (2 points)

Figure out how forwarding can resolve data hazards. (2 points)

Instruction	C0	C1	C2	C3	C4	C5	C6
addi t0, s0,-1	IF	ID	EX	MEM	WB		
and s2, t0, a0		IF	ID	EX	MEM	WB	
sw s0, 100(t0)			IF	ID	EX	MEM	WB

Solution:

The REG step for instructions 2 and 3 depend on data in the registers only available after the WB step of instruction 1. (2 points, 1 point for 1 pair of instructions having data dependency)

We can forward the ALU output of the first instruction to the EX stages of future instructions. (2 points, 1 point for 1 pair of instructions having data dependency)

2. Given the RV32I code below and a pipelined CPU with no forwarding, write out all hazards, using the following form: instruction 1-2. (4 points)

What types are each hazard (data hazard or control hazard)? (2 points)

How many stalls would there need to be in order to fix each data hazard(s)? (2 points)

	Instruction	C0	C1	C2	C3	C4	C5	C6	C7	C8
1	addi t0, s0,-1	IF	ID	EX	MEM	WB				
2	and s2, t0, a0		IF	ID	EX	MEM	WB			
3	sw s2, 100(t0)			IF	ID	EX	MEM	WB		
4	beq s0, s3, label				IF	ID	EX	MEM	WB	
5	addi t2, x0, x0					IF	ID	EX	MEM	WB

Solution:

hazards from 1-2, 1-3, 2-3, 4-5 (4 points, 1 point for 1 hazard)

4-5 is a control hazard, all others are data hazard. (2 points, 0.5 point for 1 hazard)

Assuming concurrent reads and writes to registers are possible, two stalls for instruction 2 are needed for register t0 between 1 and 2, two stalls are needed for the register s2 between 2 and 3.
(2 points, 1 point for 1 data hazard)

V. VIRTUAL MEMORY (10 points)

Given the information below:

- 1 MiB of virtual memory
- 256 KiB of physical memory
- 4 KiB page size
- TLB: 8 entries, 2-way set associative

1. How many bits are needed to represent the virtual address space, physical address space and page offset respectively? (3 points)

Solution: 20, 18, 12

2. How many bits are in the TLB index and TLB tag respectively? (2 points)

Solution: 2, 6

3. Translate virtual address 0x15213 to physical address, given the contents of the TLB and the first 32 entries of the page table below. (5 points)

TLB

Index	Tag (Hex)	Physical page number (Hex)	Valid
0	05	13	1
	3F	15	1
1	10	0F	1
	0F	1E	0
2	1F	01	1
	11	1F	0
3	03	2B	1
	1D	23	0

Page Table

VPN(Hex)	PPN(Hex)	Valid	VPN(Hex)	PPN(Hex)	Valid
00	17	1	10	26	0
01	28	1	11	17	0
02	14	1	12	0E	1
03	0B	0	13	10	1
04	26	0	14	13	1
05	13	0	15	18	1
06	0F	1	16	31	1
07	10	1	17	12	0
08	1C	0	18	23	1
09	25	1	19	04	0
0A	31	0	1A	0C	1
0B	16	1	1B	2B	0
0C	01	0	1C	1E	0
0D	15	0	1D	3E	1
0E	0C	0	1E	27	1
0F	2B	1	1F	15	1

VPN=________
TLB Tag=________, TLB miss or hit________
Page table miss or hit________
Physical Address=________ (If you don't have enough information to fill the blank, fill the blank with "/")

Solution: VPN=0x15, TLBI=1, TLBT=0x05, TLB miss
page table hit
Physical Address: 0x18213

Instruction encoding for a reducing RISC-V ISA

name	*format type*	*instruction format*					
beq	*B-type*	*imm[12|10:5]*	*rs2*	*rs1*	*000*	*imm[4:1|11]*	*1100011*
lw	*I-type*	*imm[11:0]*		*rs1*	*010*	*rd*	*0000011*
sw	*S-type*	*imm[11:5]*	*rs2*	*rs1*	*010*	*imm[4:0]*	*0100011*
addi	*I-type*	*imm[11:0]*		*rs1*	*000*	*rd*	*0010011*
add	*R-type*	*0000000*	*rs2*	*rs1*	*000*	*rd*	*0110011*
sub	*R-type*	*0100000*	*rs2*	*rs1*	*000*	*rd*	*0110011*
sll	*R-type*	*0000000*	*rs2*	*rs1*	*001*	*rd*	*0110011*
srl	*R-type*	*0000000*	*rs2*	*rs1*	*101*	*rd*	*0110011*
or	*R-type*	*0000000*	*rs2*	*rs1*	*110*	*rd*	*0110011*
and	*R-type*	*0000000*	*rs2*	*rs1*	*111*	*rd*	*0110011*
jal	*J-type*	*imm[20|10:1|11|19:12]*				*rd*	*1101111*