Introduction to Register Transfer Language

The symbolic notation used to describe the micro operation transfers among register is called register transfer language. It is one of the forms of hardware description language (HDL). The term 'register transfer' implies the availability of hardware logic circuits that can perform a stated instruction and transfer the data. It also transfers result of the operation to the same or another register. The term 'language' is borrowed from programmers, who apply this term to programming language.

RTL is the convenient tool for describing the internal organization of digital computers in concise and precise manner. It can also be used to facilitate the design process of digital systems such as microprocessors.

RTL is the systematic notation used to describe the main operation transfer among registers.

RTL for MOV A, B:

Machine cycle= 1 machine cycle = opcode fetch = 4 T states

Opcode Fetch Cycle:
T1: MAR ←PC
T2: MBR ← [MAR]
T3: IR ← MBR
T4: PC ← PC + 1

RTL for LXI H, 3000H

Machine cycle= 3 machine cycle = opcode fetch (4T), memory read (3T), memory read (3T) = 10 T states

Opcode Fetch Cycle:
T1: MAR ←PC
T2: MBR ← [MAR]
T3: IR ← MBR
T4: PC ← PC + 1

Execute Cycle

Memory read cycle

T5: MAR ←PC

T6: MBR ← [MAR]

T7: IR[Address of L]←MBR

PC ← PC + 1

Memory read cycle

T8: MAR ←PC

T9: MBR ← [MAR]

T10: IR[Address of H]←MBR

PC ← PC + 1

RTL for LDA 3000H

Machine cycle= 4 machine cycle = opcode fetch (4T), memory read (3T), memory read (3T), memory read (3T) = 13 T states

Opcode Fetch Cycle:
T1: MAR ←PC
T2: MBR ← [MAR]
T3: IR ← MBR
T4: PC ← PC + 1

Execute Cycle

Memory read cycle

T5: MAR ←PC

T6: MBR ← [MAR]

T7: IR[Address of Z]←MBR

PC ← PC + 1

Memory read cycle

T8: MAR ←PC

T9: MBR ← [MAR]

T10: IR[Address of W]←MBR

PC ← PC + 1

Memory read cycle

T11: MAR ←WZ

T12: MBR ← [MAR]

T13: IR[Address of A]←MBR

RTL for STA 3000H

Machine cycle= 4 machine cycle = opcode fetch (4T), memory read (3T), memory read (3T), memory write (3T) = 13 T states

Opcode Fetch Cycle:
T1: MAR ←PC
T2: MBR ← [MAR]

T3: IR ← MBR
T4: PC ← PC + 1

Execute Cycle

Memory read cycle

T5: MAR ←PC

T6: MBR ← [MAR]

T7: IR[Address of Z]←MBR

PC ← PC + 1

Memory read cycle

T8: MAR ←PC

T9: MBR ← [MAR]

T10: IR[Address of W]←MBR

PC ← PC + 1

Memory read cycle

T11: MAR ←WZ

T12: MBR ← IR[Address of A]

T13: [MAR]←MBR

HW: MVI, LHLD, SHLD, INR M