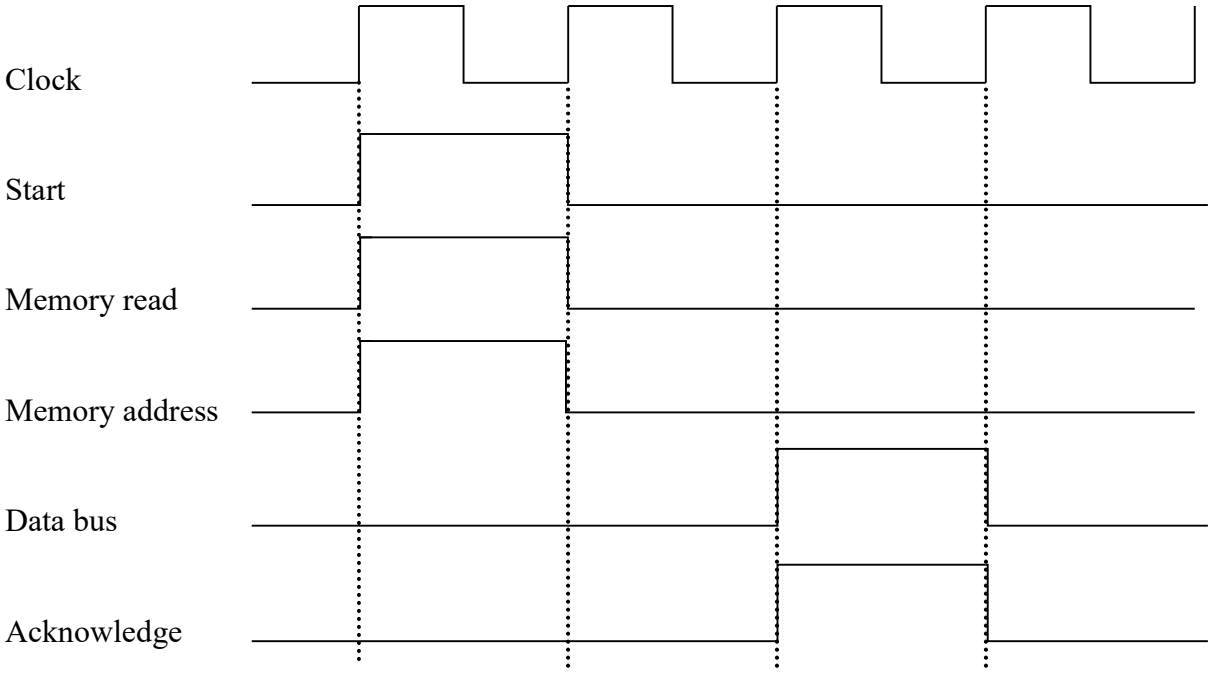
Types of Buses

1. Synchronous Bus

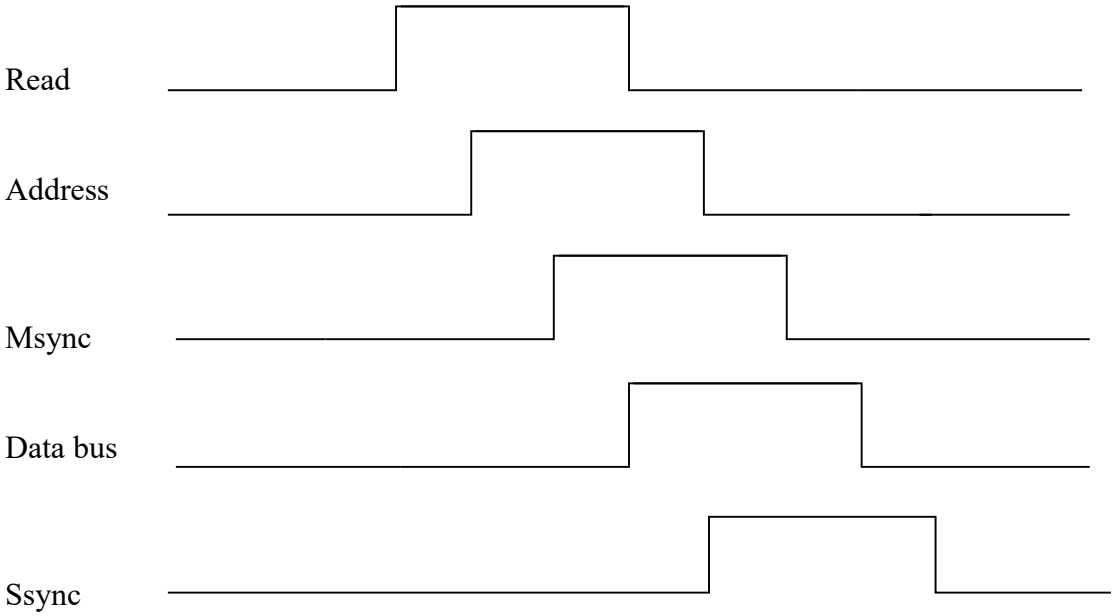
- Occurrence of each event in the bus is determined by the clock.
- A single 1-0 is called a clock cycle or bus cycle.
- All devices on the bus can read clock signal and all events start at the beginning of the clock cycle.
- All devices operate at a fixed rate.
- System cannot take advantage of device performance i.e. Speed is limited to the clock speed.
- Example:



- CPU issues Start signal to indicate the presence of address and control information in the bus.
- It then issues Memory read signal and places Memory address on the address bus.
- Memory gets the address after one clock delay and it places the data on the Data bus and Acknowledge signal to indicate the data has been sent.

2. Asynchronous Bus

- Occurrence of one event on the bus depends on the occurrence of previous event.
- System speed can be faster than the clock speed.
- Example:



- CPU issues Read signal and places address on the Address bus.
- After allowing these two signals to stabilize, it issues Msync signal to indicate valid address on bus.
- Addressed memory responds with valid data and Ssync signal.
- Msync= Master synchronous and Ssync= Slave synchronous.