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3.1 基准性能为38。每条指令需一个时钟周期，再加上额外的延迟周期。

| | | | |
|---|---|---|---|
| Loop: | fld | f2.0(Rx) | 1+3=4 |
| I0: | fmul.d | f2.f0.f2 | 1+4=5 |
| I1: | fdiv.d | f8.f2.f0 | 1+10=11 |
| I2: | fld | f4.0(Ry) | 1+3=4 |
| I3: | fadd.d | f4.f0.f4 | 1+2=3 |
| I4: | fadd.d | f10.f8.f2 | 1+2=3 |
| I5: | fsd | f4.0(Ry) | 1+1=2 |
| I6: | addi | Rx.Rx.8 | 1 |
| I7: | addi | Ry.Ry.8 | 1 |
| I8: | sub | x20.x4.Rx | 1 |
| I9: | bnz | x20.Loop | 1+1=2 |

4+5+11+4+3+3+2+1+1+1+2=37

分支延迟槽T=1

37+1=38

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3.2

```
Loop:  fld      f2, 0(Rx)                    1+3
       <stall due to LD latency>
       <stall due to LD latency>
       <stall due to LD latency>
I0:    fmul.d   f2, f0, f2                   1+4
       <stall due to fmul.d latency>
       <stall due to fmul.d latency>
       <stall due to fmul.d latency>
       <stall due to fmul.d latency>
I1:    fdiv.d   f8, f2, f0                   1+10
I2:    fld      f4, 0(R4)                    1+3
       <stall due to LD latency>
       <stall due to LD latency>
       <stall due to LD latency>
I3:    fadd.d   f4, f0, f4                   1+2
       <stall due to fdiv.d latency>
       <stall due to fdiv.d latency>
       <stall due to fdiv.d latency>
       <stall due to fdiv.d latency>
       <stall due to fdiv.d latency>
I4:    fadd.d   f10, f8, f2
I5:    fsd      f4, 0(Ry)                    1+2
I6:    addi     Rx, Rx, 8                    1+1
I7:    addi     Ry, Ry, 8                    1
I8:    sub      X20, X4, Rx                  1
I9:    bnz      X20, Loop                    1+1
       <stall due to branch delay slot>
```

总计：27个时钟周期